Few words on very front end electronics SPIROC/EASIROC based

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Round table on detectors for muon radiography

The SPIROC chip: a user perspective

- Highly integrated ASIC
- Up to 36 channels management (32 used in MuRay boards)
- Individual Vbias adjusting (0-4 V, 175 mV step)
- Fast discriminator response (ONLY for the logical OR of all channels)
- Low power consumption (25 μW/ch)

Issues: Designed for syncronous, triggered applications;
Learning curve; (SPIROC *is* user friendly:
it is just very selective on who his
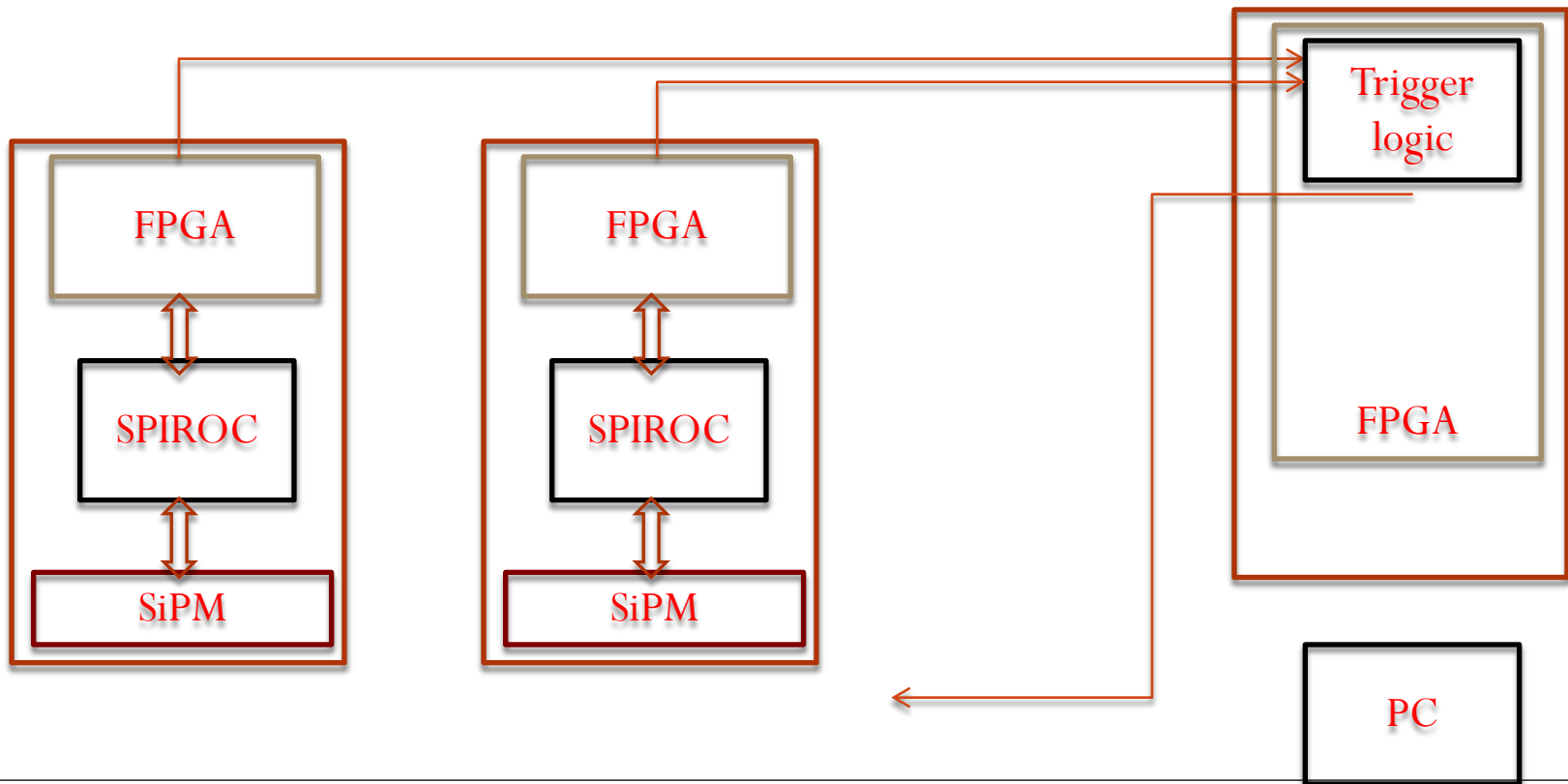friends are ;-))
Known features/limitations

MuRay DAQ strategy

SPIROC are host in boards controlled by FPGA (SLAVES)

One MASTER provides the trigger logic.

All the SLAVEs work in RUN mode, i.e. until a trigger is produced the FPGA clock is OFF and all the logic is combinatorial and power consumption is limited.

Power consumption about 1.5 W /slave board (3 W for the Master)

The (next) future: EASIROC

- Better adapted to asynchronous operation
- Greater granularity for a more versatile triggering
- Less components integrated on a die
  - Lower power consumption
  - More flexibility in deployment

Adapting existent VFE from SPIROC to EASIROC is «straightforward»

First tests in Florence VERY ENCOURAGING