IN2P3

Omega

Photon sensor system development platform & MPPC readout ASIC

FJPPL KEK/Orsay /Tohoku/Shinshu/Kyoto

S. Callier, N. Dinu, F. Dulucq, R. Kadono, C. de La Taille, G. Martin-Chassard, A. Koda, K. Miwa, I. Nakamura, T. Nakaya, K. Nishijima, V. Puill, N. Seguin-Moreau, M. Tanaka, T. Takeshita, T. Uchida, M. Yokoyama, K. Yoshimura

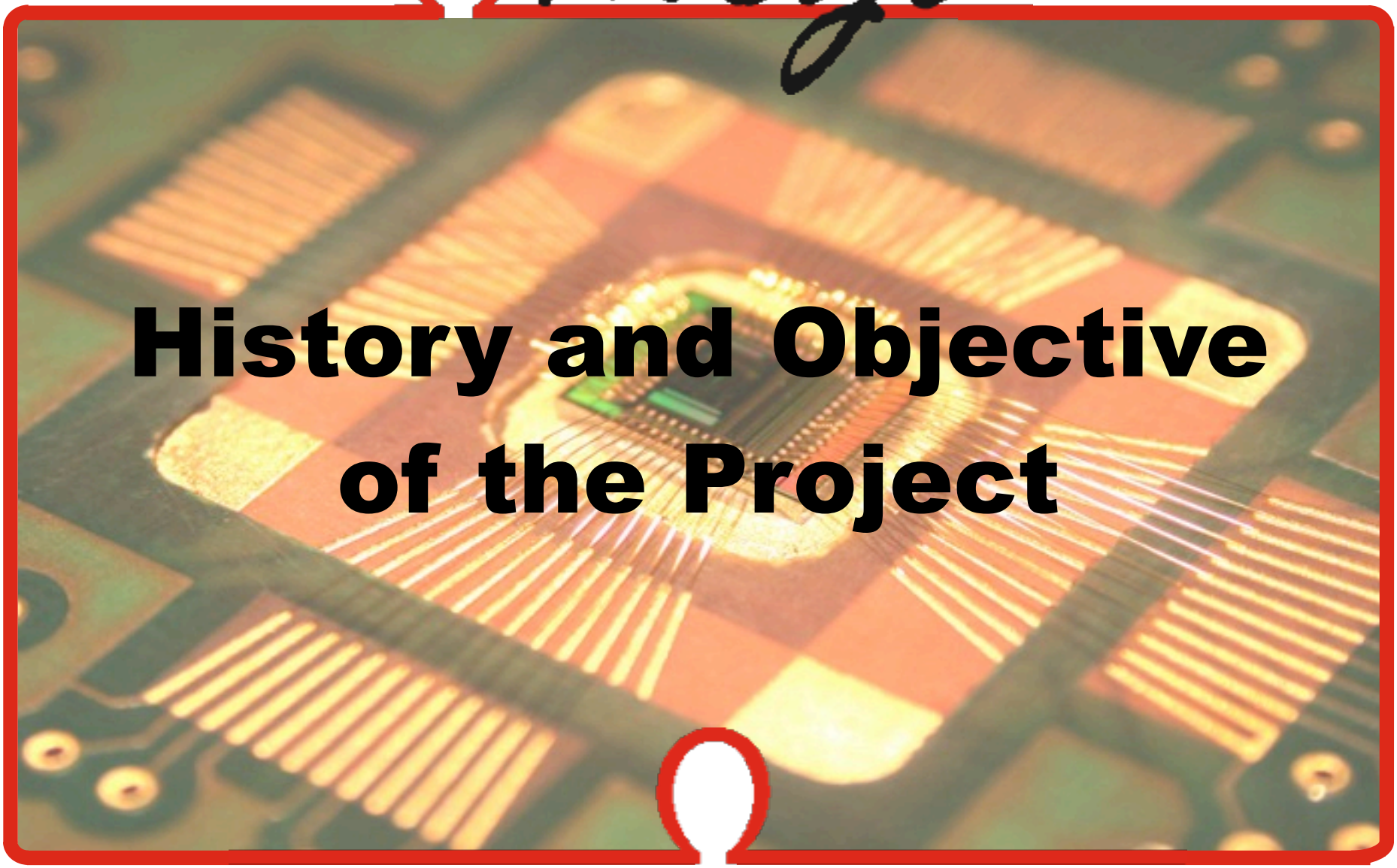
Orsay MicroElectronic Group Associated

Outline

- History and Objective of the project
- SPIROC chip and readout system
  - Read out for the specific (ILC) use.
- EASIROC chip and readout system
  - General applications.
- Summary
  - Report from the previous FY
  - Prospect of the coming FY

IN2P3

Omega

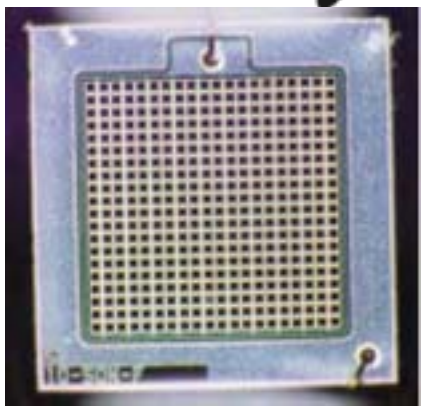


History and Objective of the Project

Orsay MicroElectronic Group Associated

SiPM/MPPC

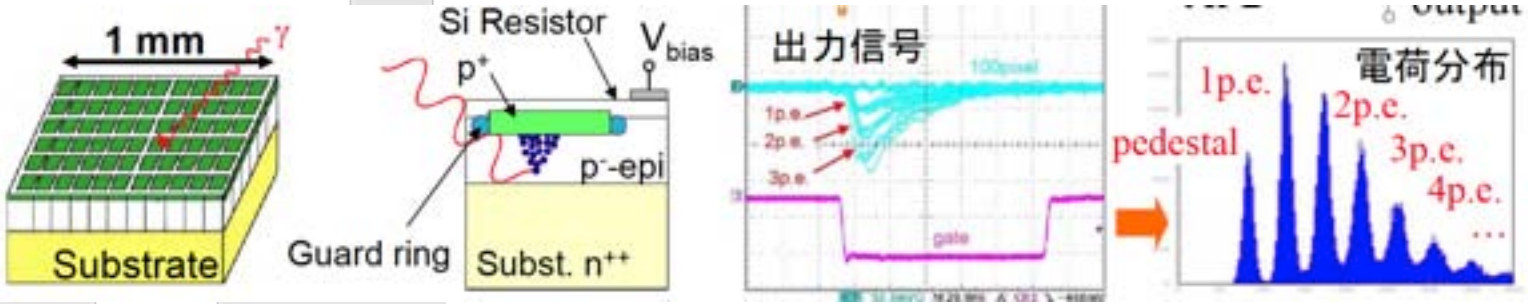
- PPD(Pixelated Photon Detector)
  - Array of Geiger-mode APDs
  - SiPM MEPhI/Pulsar, MPI, ITC-IRST
  - MPPC Hamamatsu
  - SMP SensL
  - G-APD JINR/Micron



- Features
  - Compact, High gain (10^5~10^6)
  - Magnetic field
  - Low cost but small
  - Low bias voltage 50~70V (need to be fine-adjusted)

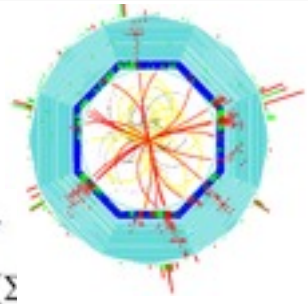
Many advantages over **conventional PD**

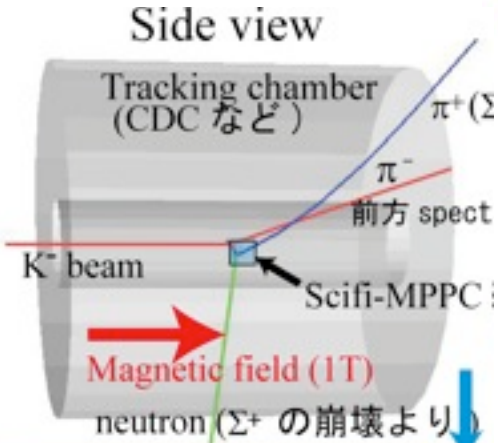
(PMT, APD etc.)

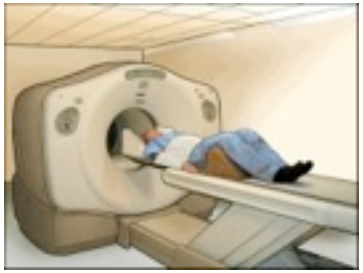


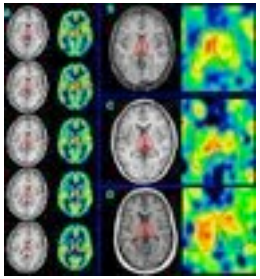
Rapid growth of SiPM/MPPC applications

- High Energy physics : calorimetry, PID…
- Nuclear Physics
- Astrophysics
- Medical : imaging, PET..





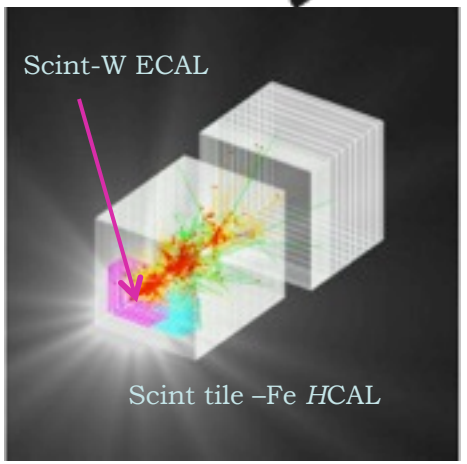


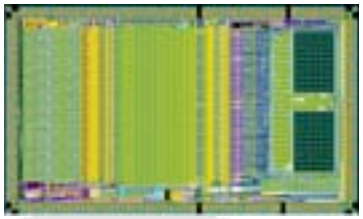


ROC for SiPM/MPPC application : CALICE

- "imaging calorimetry" at ILC
  - 8000 SiPM for tiles readout for AHCAL
  - >Million MPPC for Scintillator ECAL

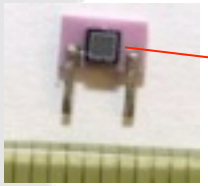
  => Need of highly integrated readout chip

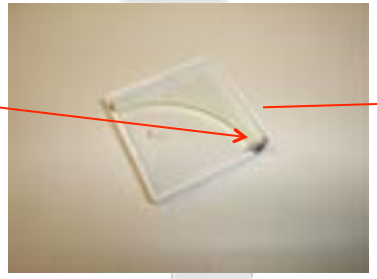




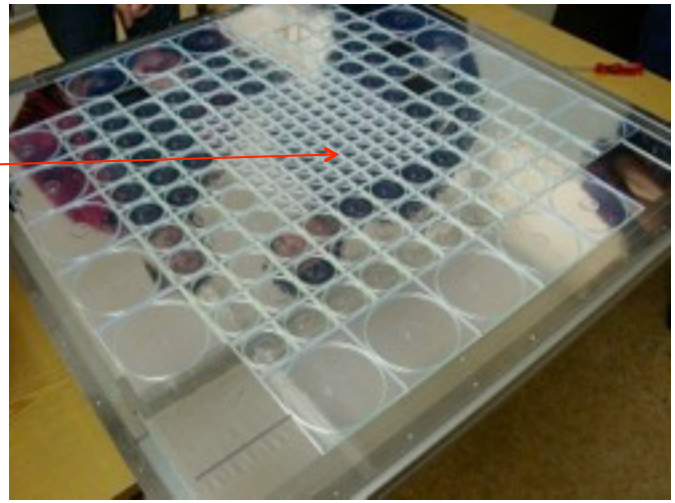
SPIROC2
Analog HCAL
36 ch. 30mm²

SiPM
1 mm²





Tuile plastique 3 x 3 cm²



CALICE
Calorimeter for ILC

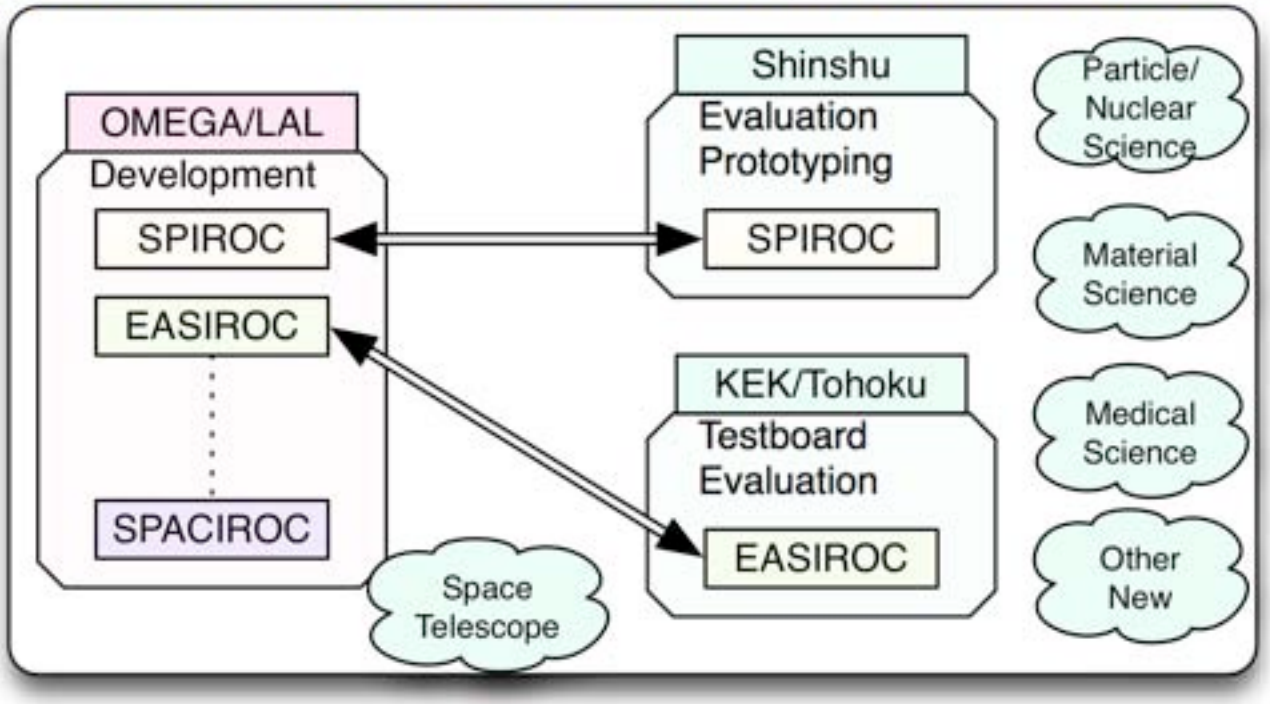
Demand of ROC for SiPM/MPPC

- SiPM/MPPC is now widely used in varieties of field.
- Readout Electronics is now urgent issue.
  - Small area (~mm2) → Multi channel (Typically >100 ch)
  - Sensitive to bias voltage → need to be controlled by 10mV.
  - Large temperature dependence
- Development of ASIC chip is essential!
  - Fine adjustment of bias voltage
  - Highly integrated
  - Low power
  - Various Trigger scheme

France Japan collaboration

- Objectives
  - ASIC chip development
    - SPIROC
    - EASIROC
  - Readout system for Photon sensors
  - Widen applications

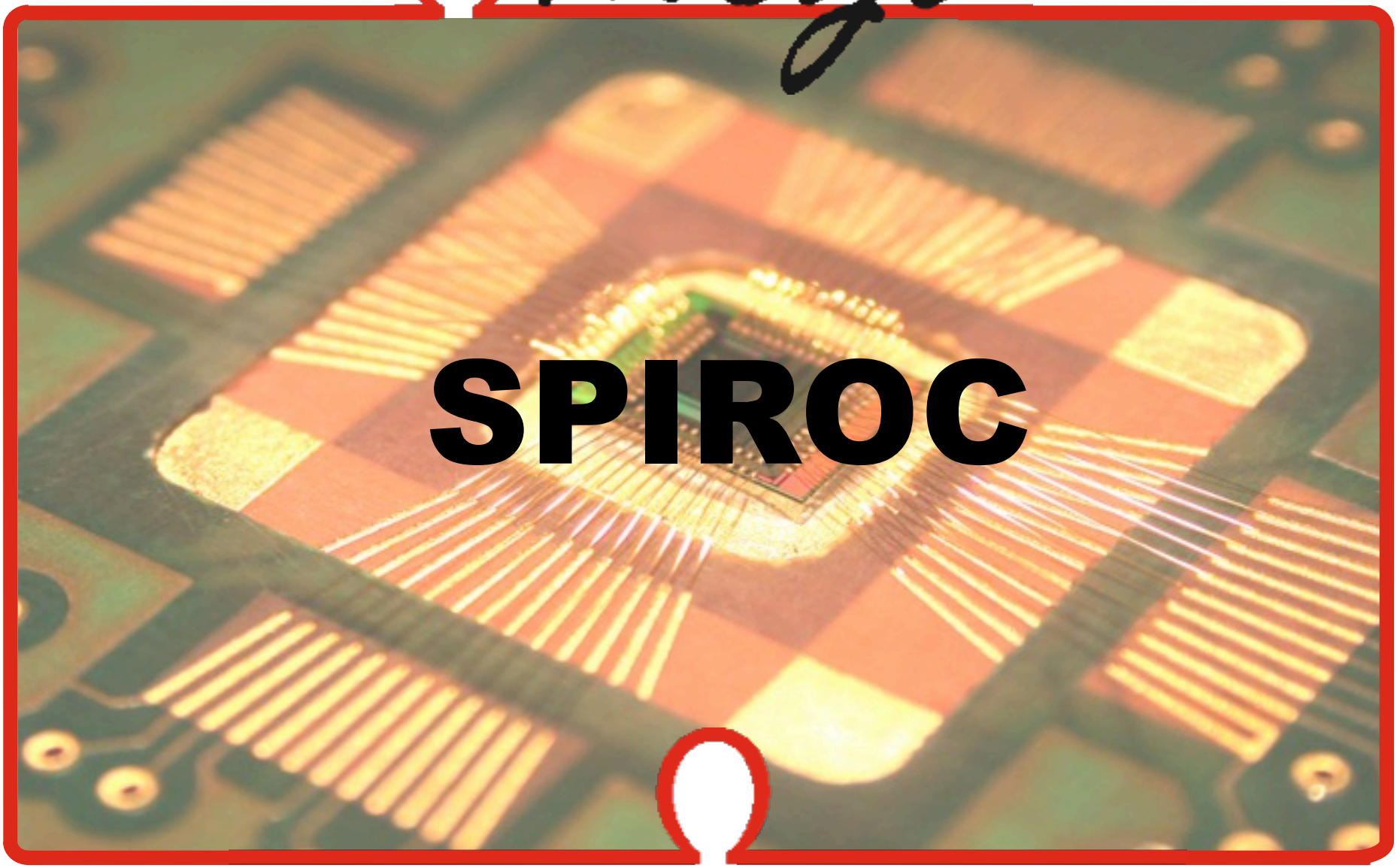
Photon sensor system development platform (FJPPL)



2008~

IN2P3

Omega

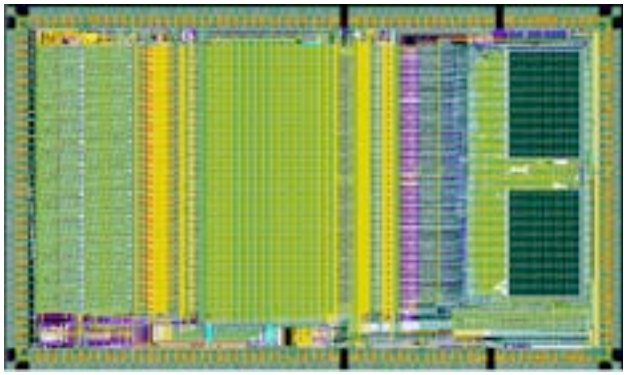


SPIROC

Orsay MicroElectronic Group Associated

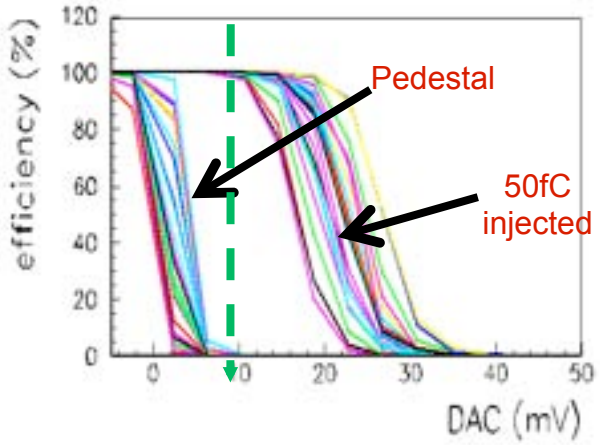
SPIROC main features

- **36-Channel ASIC**
- **Internal input 8-bit DAC** (0-5V) for individual SiPM gain adjustment
- **Energy measurement : 14 bits**
  - 2 gains (1-10) + 12 bit ADC : 1 pe → 2000 pe
  - Variable shaping time from 25 ns to 175 ns
  - pe/noise ratio : ~11
- **Auto-trigger on MIP or on single photo-electron**
  - pe/noise ratio on trigger channel : ~24
  - Fast shaper : ~10 ns
  - Auto-Trigger on 1/3 pe (50fC)
- **Time measurement :**
  - 12-bit Bunch Crossing ID (coarse time)
  - 12-bit step~1 ns TDC->TAC (fine time)
- **Other features:**
  - Analog memory for time and charge measurement : depth = 16
  - Low consumption : ~25 µW per channel (in power pulsing mode)
  - Individually addressable calibration injection capacitance
  - Embedded features (bandgap, 10-bit DAC, etc.)
  - Multiplexed analog output for physics prototype DAQ
  - 4kbytes internal memory and daisy chain readout

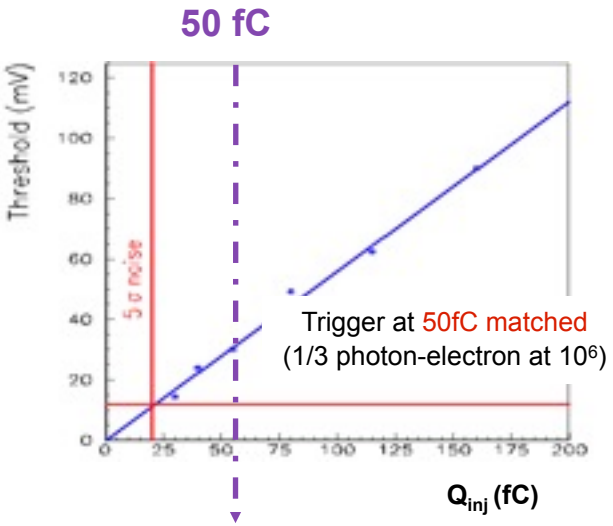


SPIROC: trigger efficiency measurements

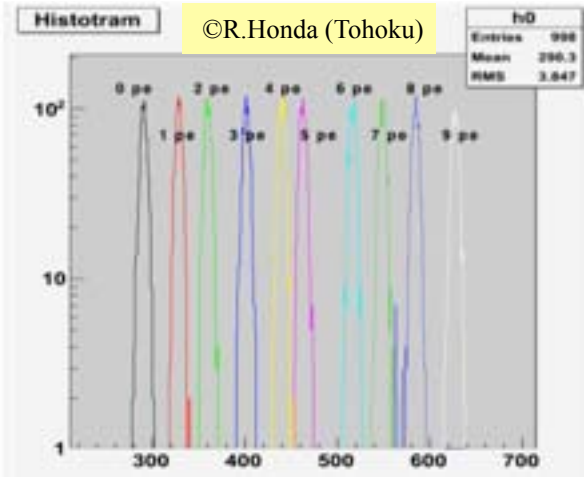
36-channel S-curves: trigger efficiency versus threshold (1 LSB = 2 mV)



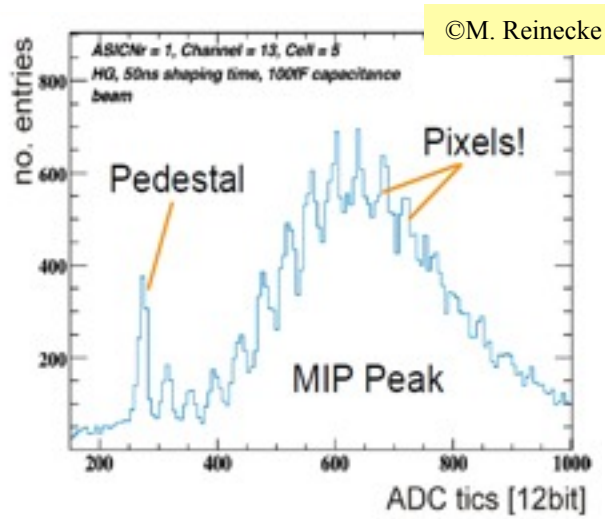
50 % Trigger efficiency point vs Q_{inj}

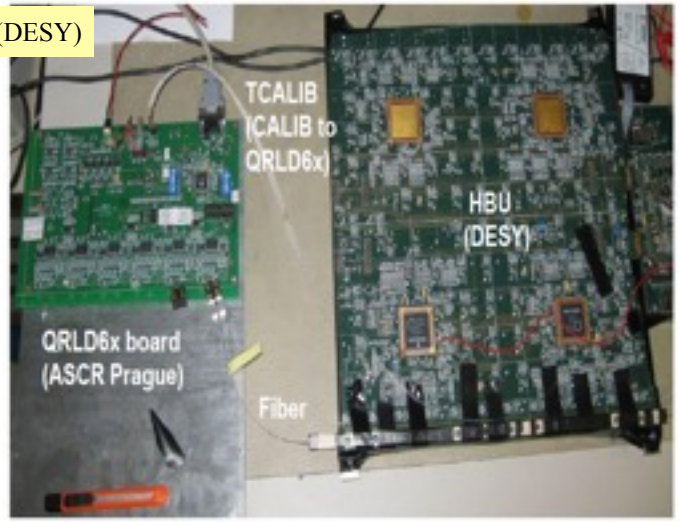


Response with different injected charge

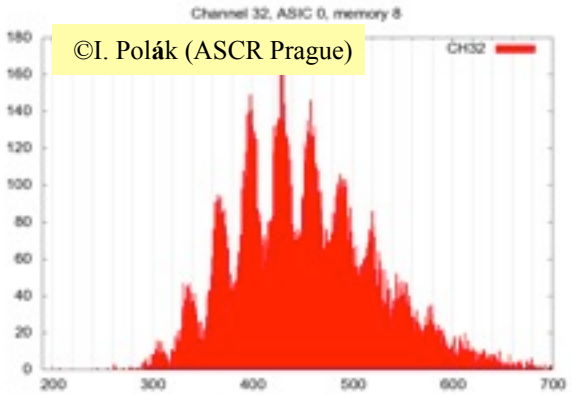


MIP response in DESY 6 GeV electron testbeam



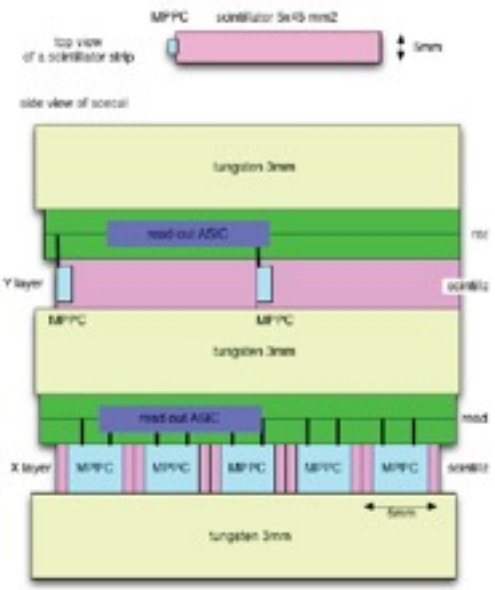


Spectrum obtained with the LED calibration system



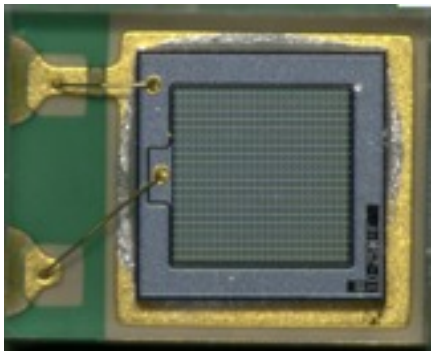
SPIROC for Sc ECAL(CALICE)

- Granular ECAL using Pixelated Photodetector (PPDs) and scintillator strips with orthogonal directions for fine segmentation (5 mmx 5 mm lateral granularity)
- Tungsten absorbers
- Physics prototypes tested in testbeam
  - 30 layers, 72 strips per layer



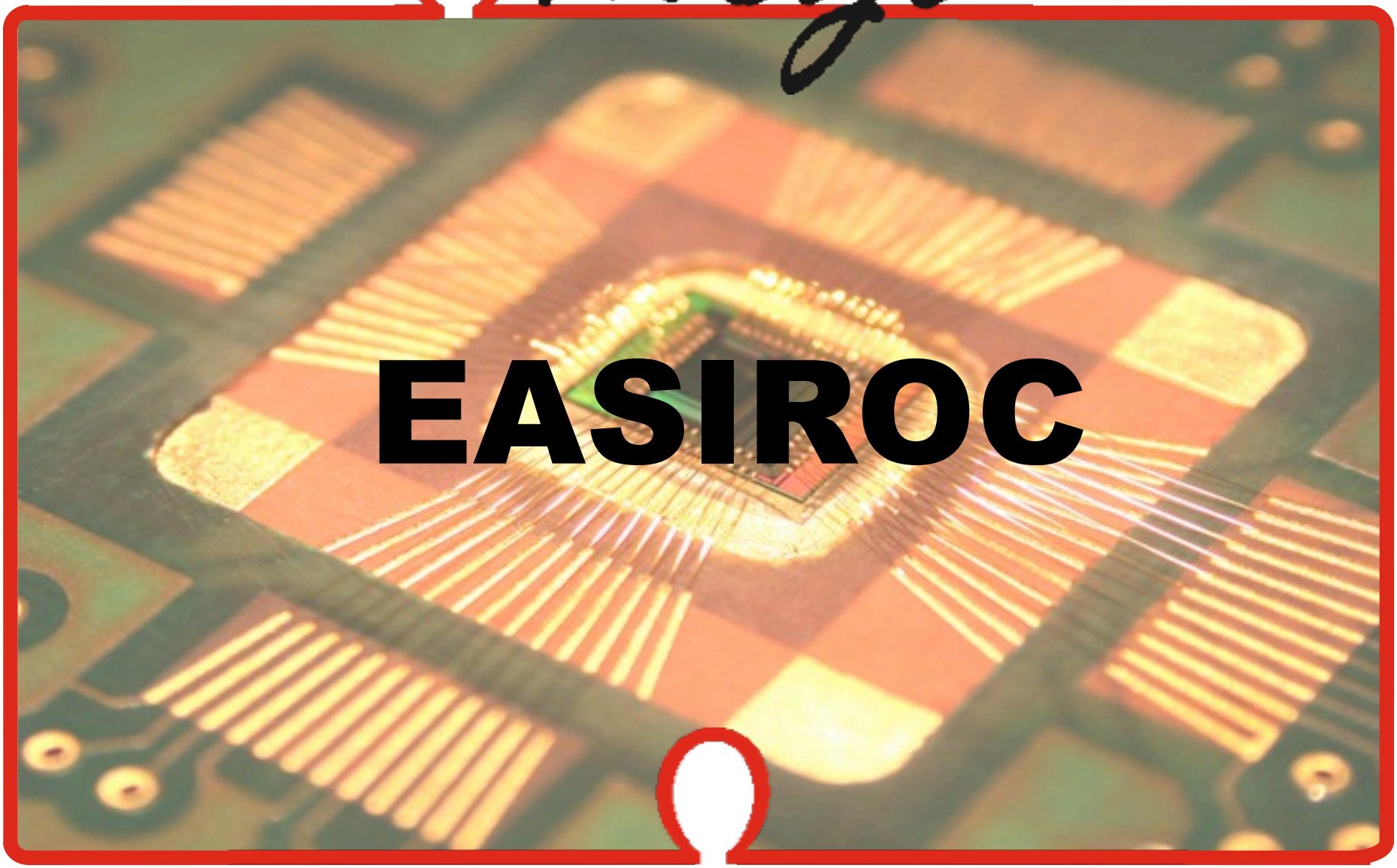
- Current development for finer granularity:
  - Sensor layer on printed circuit board (EBU boards):
  - 4 rows of 18 scintillator strips
  - 1 SPIROC2b for 1 row
  - Beam test: Fall 2012

@K. Kotera, T. Takeshita



IN2P3

Omega

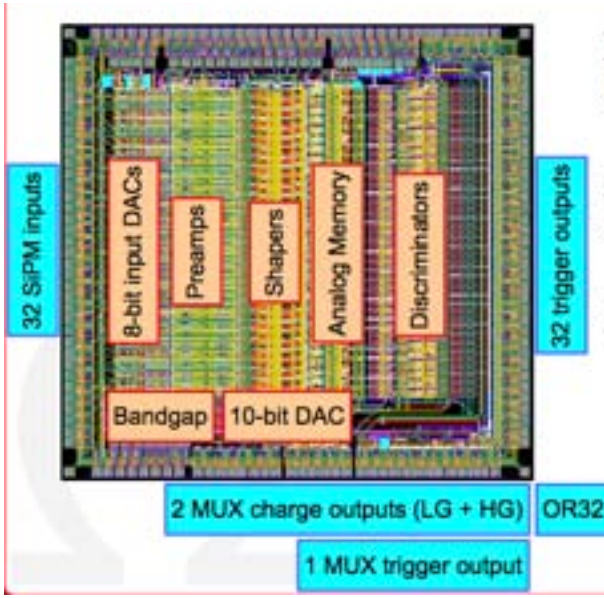


EASIROC

Orsay MicroElectronic Group Associated

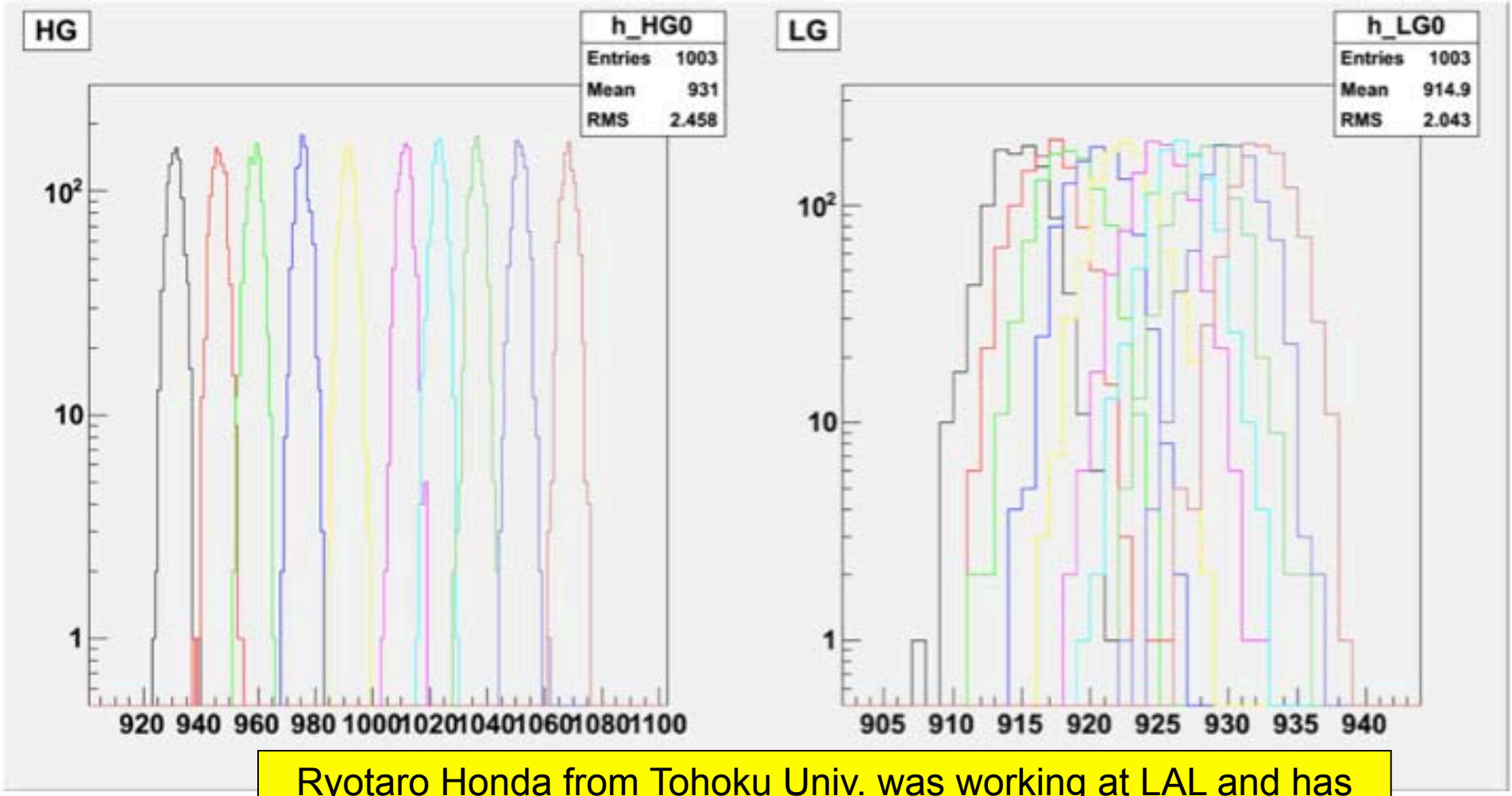
EASIROC: SIMPLEST VERSION OF SPIROC CHIP

- 32-channel front-end readout (analogue part of SPIROC)
- Individual 8-bit DAC for SiPM Gain adjustment
- Energy measurement from 160fC to 320pC (1pe to 2000pe @ SiPM gain = 10^6)
  - 1 pe/noise ratio ~11
  - Variable gain preamplifier
  - Variable time constant CRRC² shaper (25 to 175ns)
  - Common 10-bit DAC for threshold adjustment
  - 2 multiplexed analog outputs
    - (high gain, low gain) [tri state outputs]
- Trigger output
  - 1 pe/noise ratio ~24
  - Trigger on 1/3 pe (50fC)
  - 32 Trigger outputs
  - OR32 output
  - Trigger multiplexed output (latch included) [Tri state output]
- Individually addressable calibration capacitance
- Low power : 4.84mW/channel, 155mW/chip
  - Unused feature can be disabled to reduce power consumption
  - Power pulsing facility (idle mode with external signal)



ANALOG OUTPUT

- Histogram for 1 to 10 pe- on both gains



Ryotaro Honda from Tohoku Univ. was working at LAL and has contributed in the initial test of the EASIROC chip.

Test Circuit Board with EASIROC

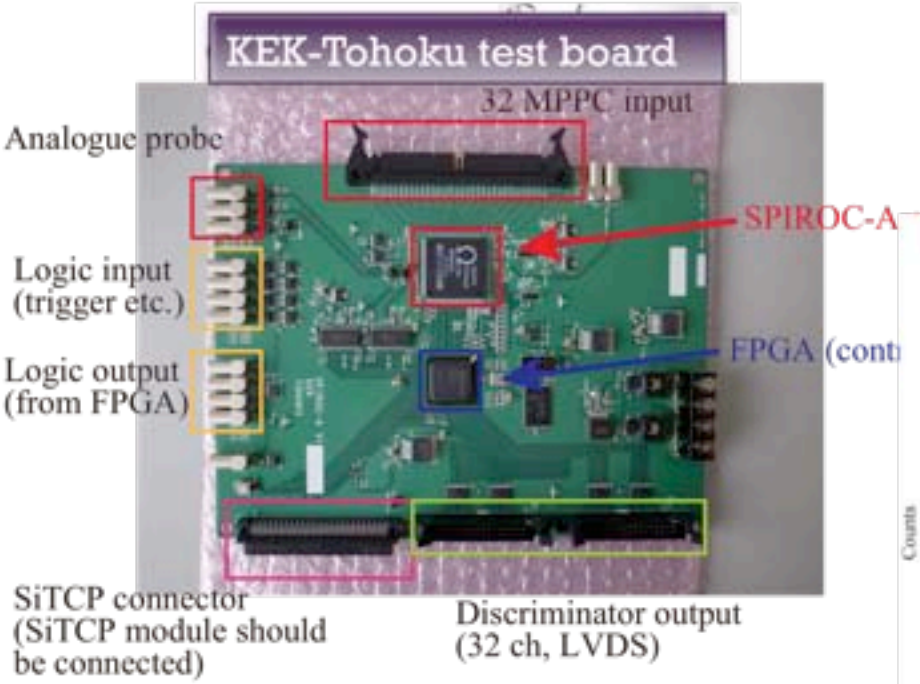
EASIROC board development

- Operation multichannel MPPC
  - EASIROC chip (32 ch operation)
  - SiTCP

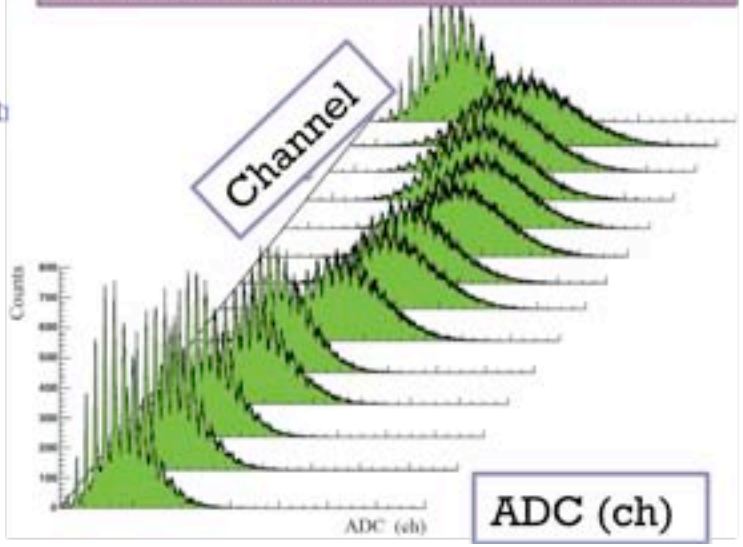
Network based operation

Data taking system
Operation parameter
- Bias voltage adjustment
- Threshold
- Gain

Data taking via network
Speed 14kHz for 32 ch data



Demonstration of Multi MPPC readout



HAL meeting (K. Miwa)

EASIROC APPLICATIONS

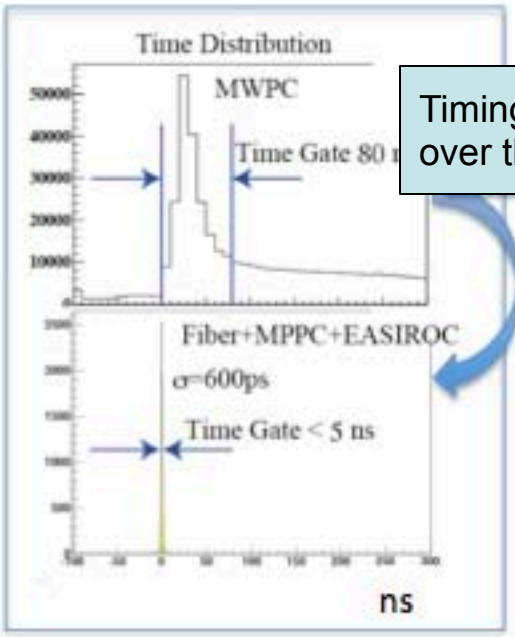
- E40 experiment and application for fiber tracker
- Muon spectrometer
- Active target for TREK experiment
- Cerenkov telescope (Tokai)
- Beam defining counter
- etc……..

- 10 groups are now testing and evaluating ~ 20 test boards
- Some of them were used as MPPC readout systems for realistic beam tests.
- Various new functions were added (e.g. Multihit TDC)by custom FPGA programming

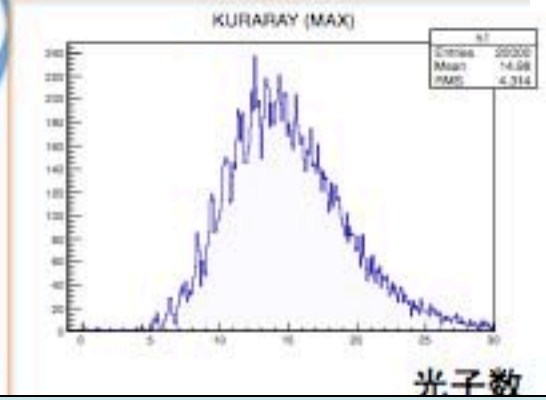
Fiber Tracker with EASIROC Readout

Using high intensity J-Parc beam (2×10^7 Hz)

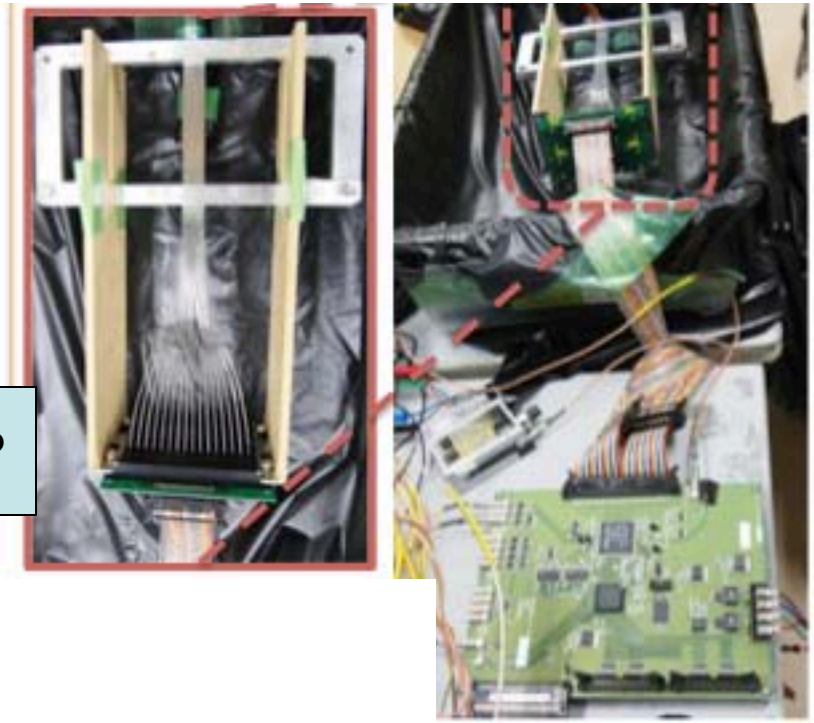
Event identification with high resolution TOF



Timing resolution was improved by 15 over the present MWPC.



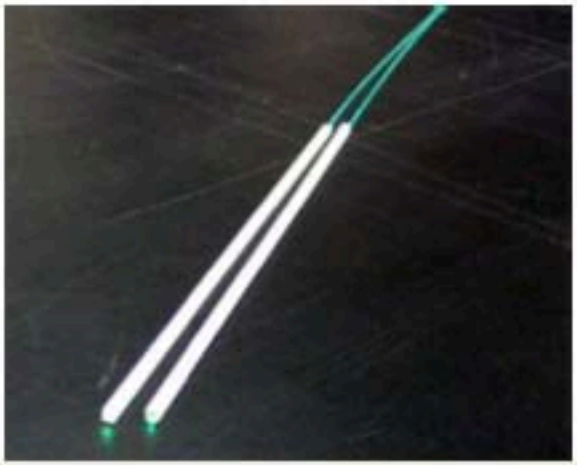
Fiber tracker prototype was developed with MPPC and EASIROC board for High timing resolution



Good detection efficiency was obtained for MIP

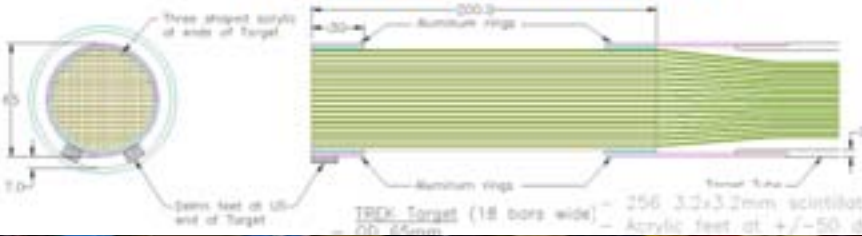
Active Target for TREK (J-PARC)
Prototype beam test on TRIUMF M11

- Test of the thin plastic scintillator (3mmx3mm) with the wave length shifter fiber using MPPC and EASIROC readout
- 180 MeV P, π, μ, e^+

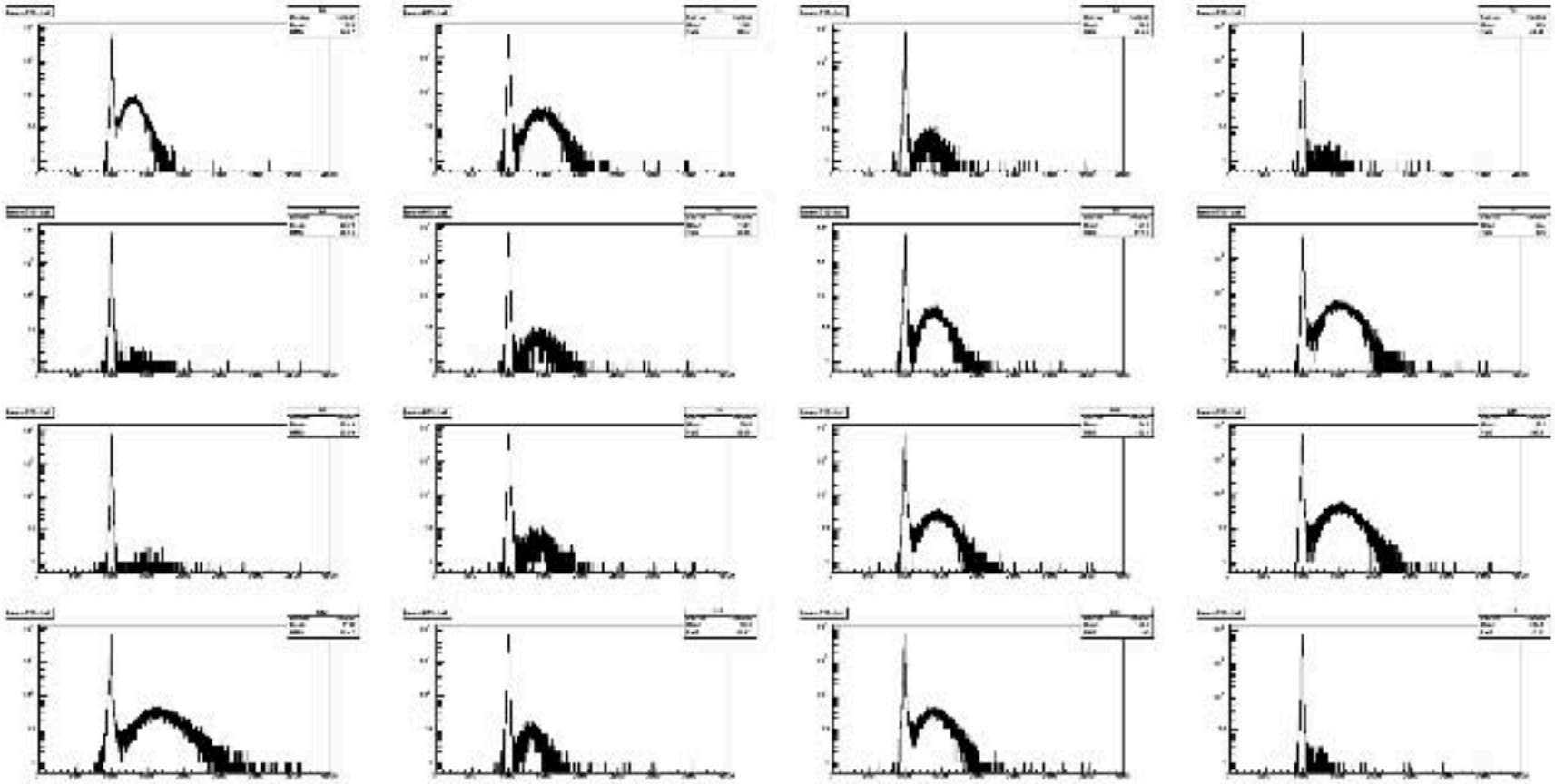


Scintillator and WLS fiber transmission

TREK Active target



ADC spectrum by EASIROC board



IN2P3

Omega

Summary

2011~2013

Orsay MicroElectronic Group Associated

Omega/KEK collaboration in 2011-2012

- Collaboration very active between Orsay and KEK/Tohoku/Shinshu
- Several subject of interests for MPPC readout
  - CALICE
  - HN diffraction
  - Medical imaging
  - …
- SPIROC for Sintillator ECAL within the CALICE collaboration

- EASIROC for many applications
  - Many joint measurements on Easiroc

- Visit of M. Tanaka in Paris in February 2012,
- Visit of S.Callier and L. Raux in Tohoku and Shinshu in March 2012

http://kds.kek.jp/conferenceDisplay.py?confId=9261

Omega/KEK project in 2012-2013

- New Chip development
  - Feedback from the further field tests.
  - Next version of EASIROC2 will be submitted in 2013.
- New Circuit boards
  - Tohoku Experiment ~5000 channels
    - VME based 32ch or 64 ch / board
    - High Throughput
  - General Easy Use
    - NIM module
    - High Voltage by Charge pumping
    - Thermometer to compensate temperature drift
- New Applications

IDEAS for NEXT VERSION of EASIROC

- Keep pin-to-pin compatibility ?
- Add a radiation Hard Slow Control (triple voting) with read back capability
- Set default value for Slow Control
- Individual PA gain setting with smaller steps
- Individual threshold adjustment
- Adding a 2nd threshold ?
- Adding an internal analogue TDC ?
- Power consumption improvement on SCA
- Add internal pipeline ADC ?
- Change trigger output polarity by Slow Control ?
- Open Collector output for OR32 output ?

Will be included
Should be included
Minor change
Difficult to add

Anyway, EASIROC2 will not be submitted before 2013

- Any other suggestion is welcome & can be discussed