Front end electronics for calorimeters at a Future Linear Collider and its synergies

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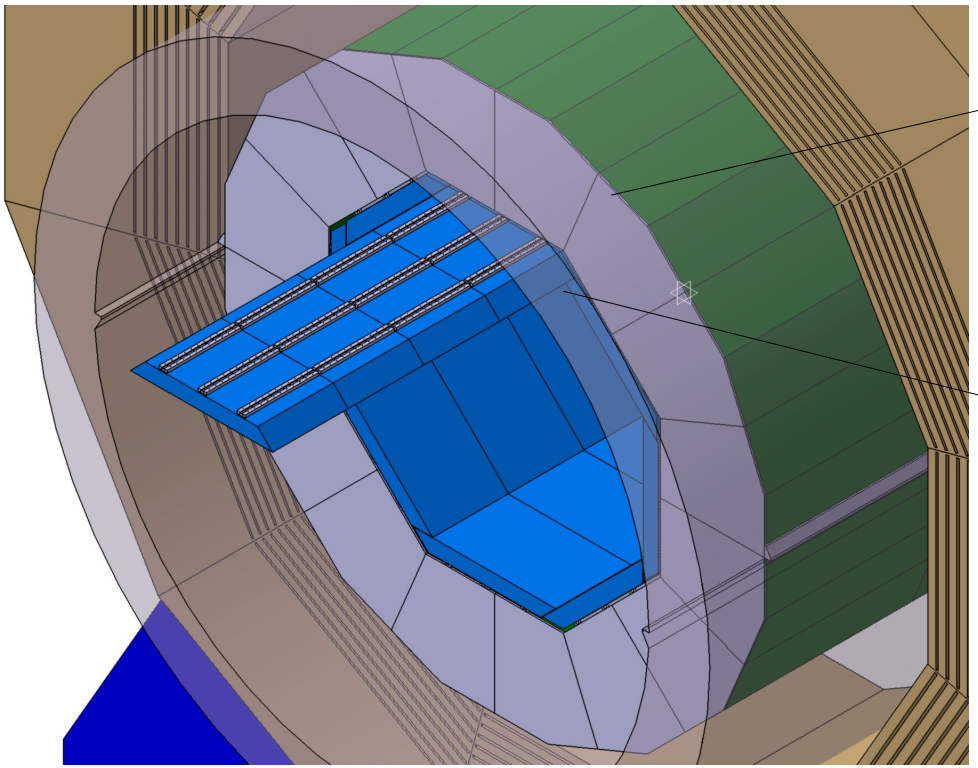
FJPPL/FKPPL Clermont Ferrand May 2012

Calorimeters for a future LC

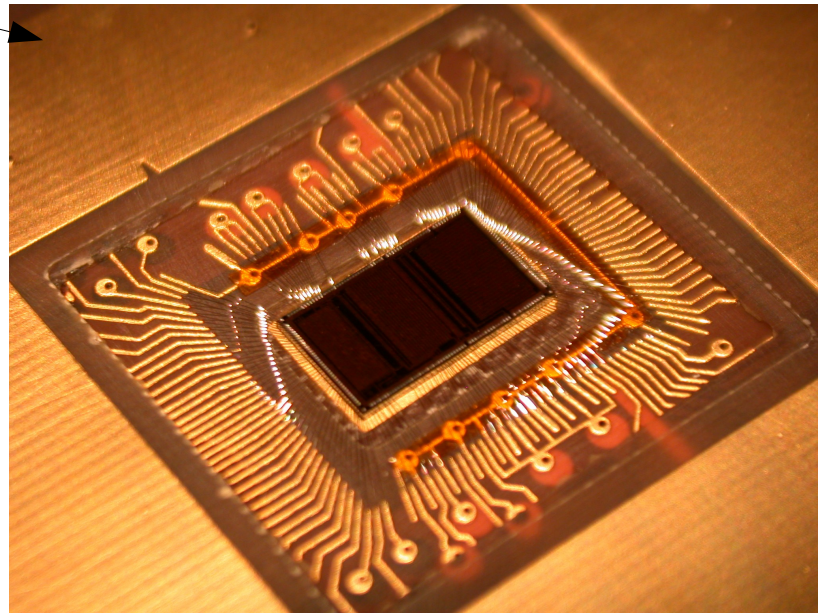
Detectors for high precision physics
At the TeV scale

Main challenges

- Compactness and hermeticity
- **Highly granular calorimeter**

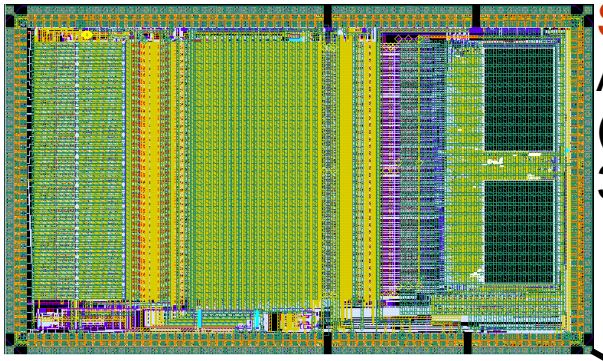


... read out by and ASIC of the ROC family

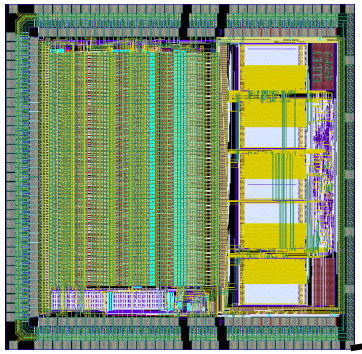


Front end ASICs: The ROC chips

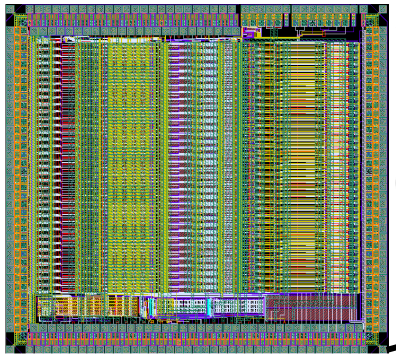
- ASICs for large scale prototype(~2m)
- Partially supported by EU (since 2006)
- ECAL, AHCAL, DHCAL



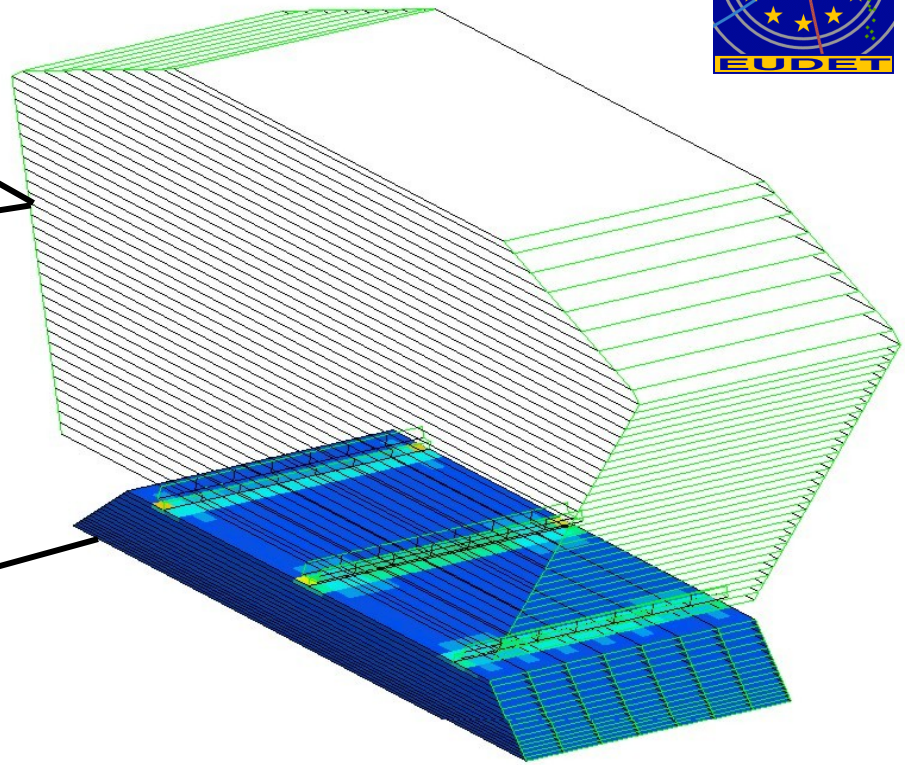
SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²



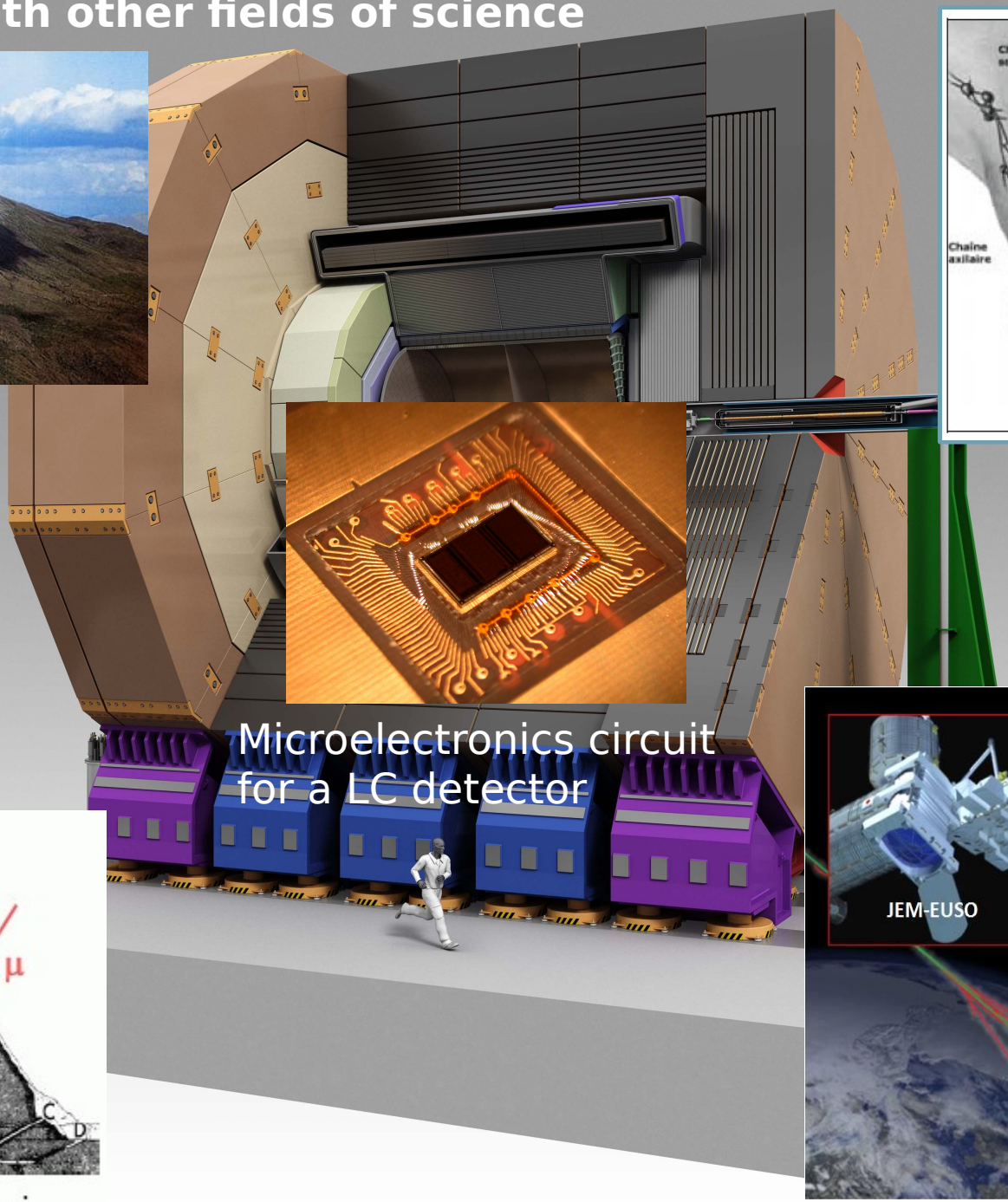
HARDROC
Digital HCAL
(RPC, µmegas or GEMs)
64 ch. 16mm²

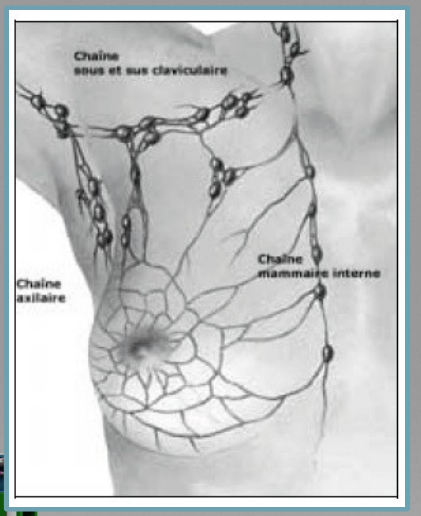


SKIROC
ECAL
(Si PIN diode)
64 ch. 20mm²

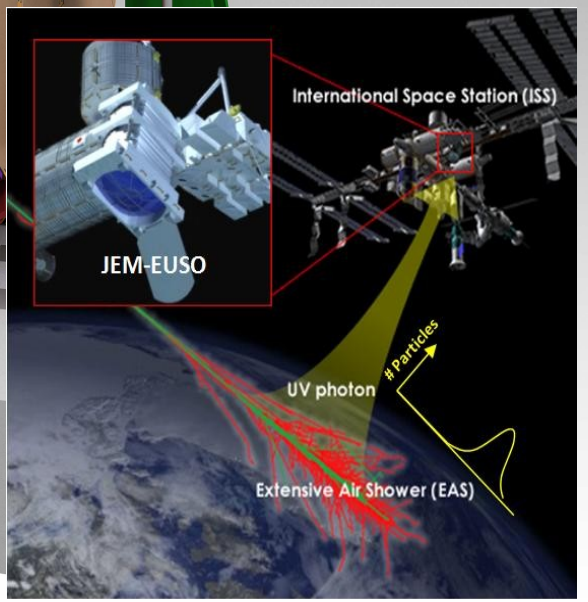


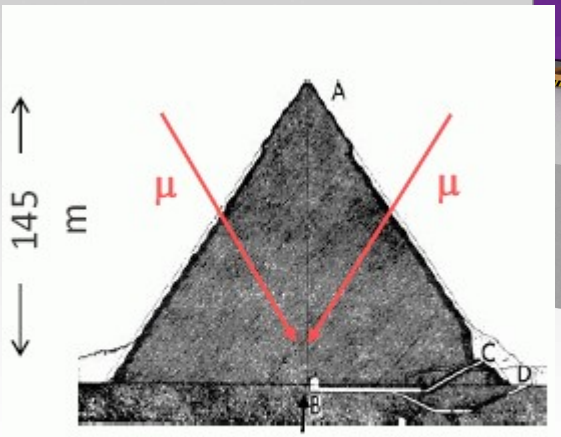
Synergies with other fields of science





Microelectronics circuit
for a LC detector

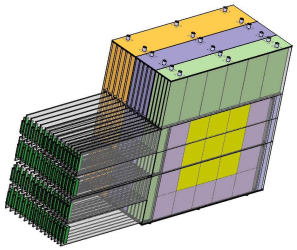


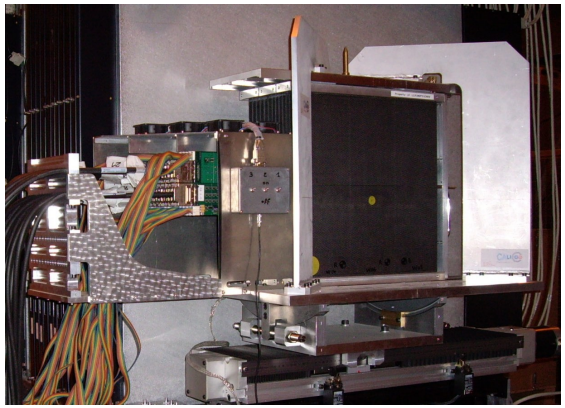


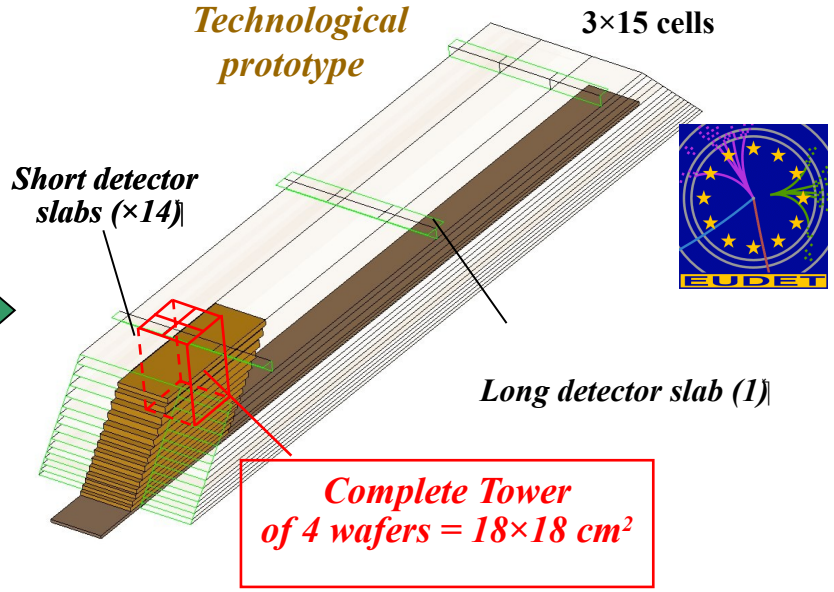
Telescope in Belzoni
chamber

Technological prototypes

Technical solutions for the/a final detector
Example Silicon-Tungsten electromagnetic calorimeter







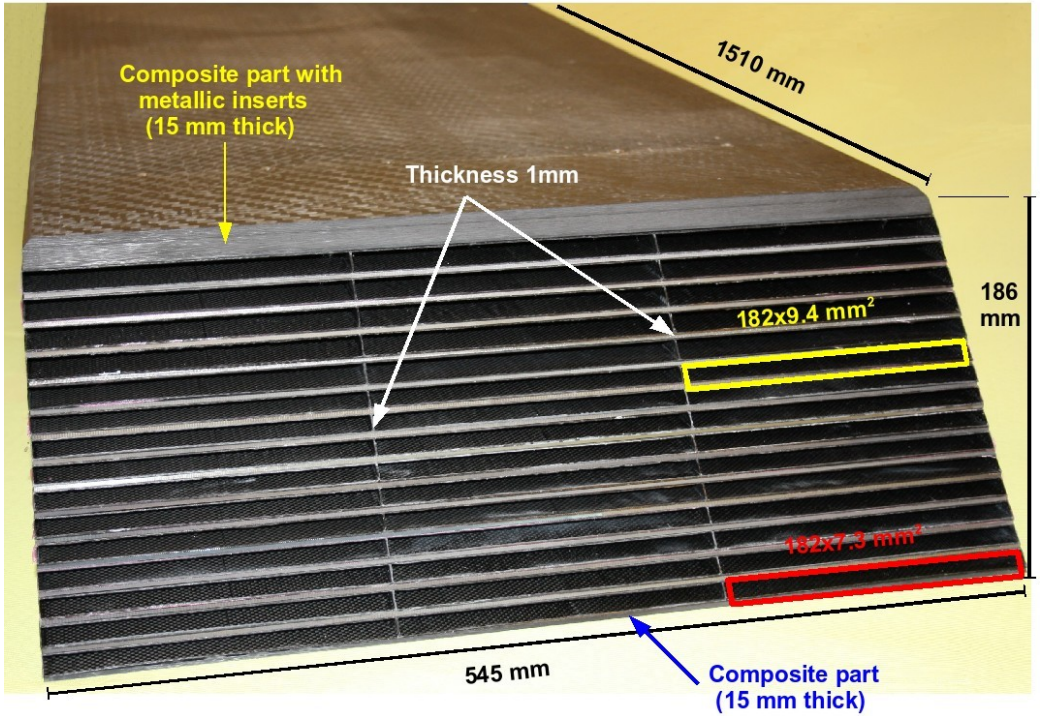
- Realistic dimensions

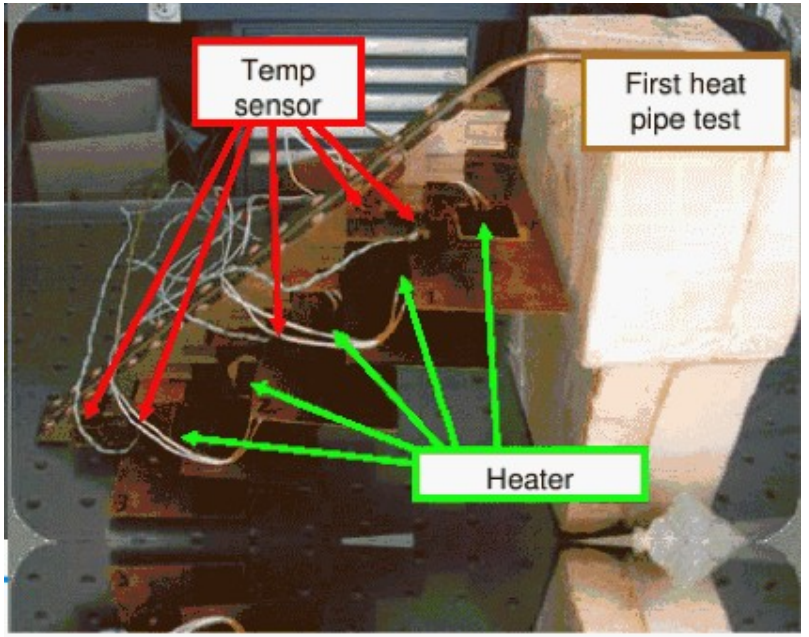
- Integrated front end electronics

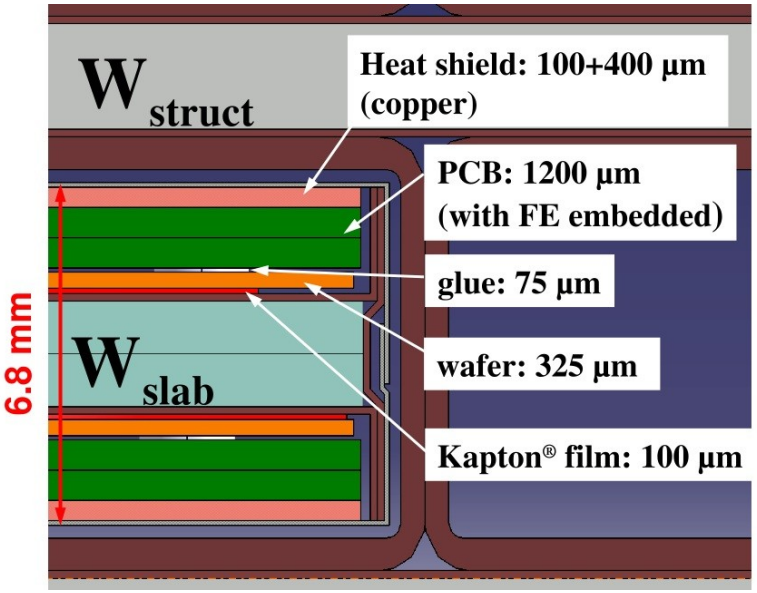
- Small power consumption
  Power pulsed electronics

- Construction, beam tests 2010 - ...

Technological Prototype – Design





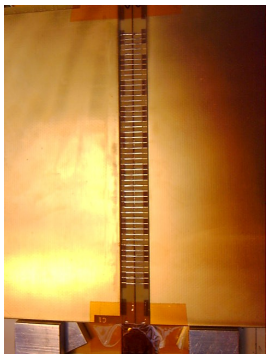


- ⇨ Gaps (slab integration) : 500 µm
- ⇨ Heat Shield: 500 µm
- ⇨ PCB : **~1200 µm**
- ⇨ Thickness of Glue : 100 µm
- ⇨ Thickness of SiWafer : 325 µm
- ⇨ Kapton® film HV : 100 µm
- ⇨ Thickness of W : 2100/4200 µm (± 80 µm)

Ecal detector layer - Principle

A layer is composed of several short ASUs:

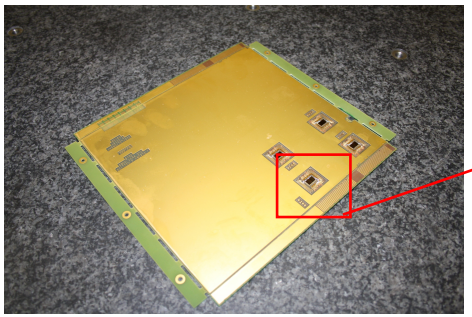
- A.S.U. : Active Sensors Units



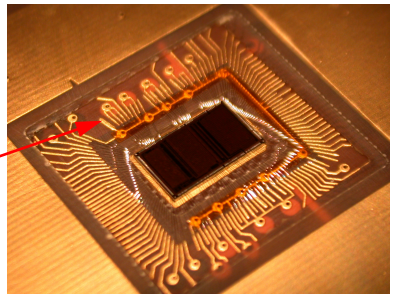
Interconnection work (see later)

Dedicated mechanical 'scaffolding' will be constructed

Chip+PCB+SiWafer =ASU



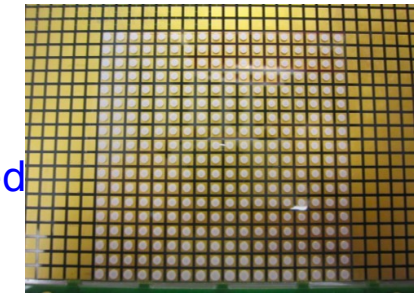
Bonding realised by CERN



Chip embedded

PCB is glued onto SiWafers

Gluing robot about to be commissioned

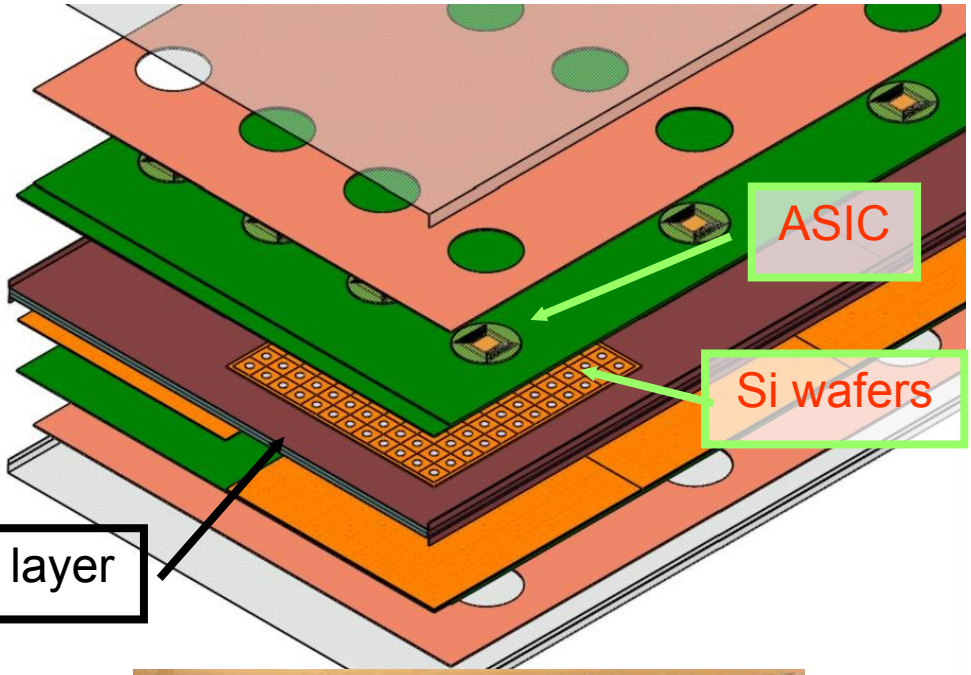


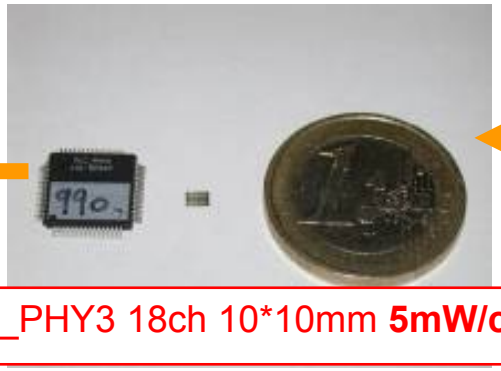
Length of layer:

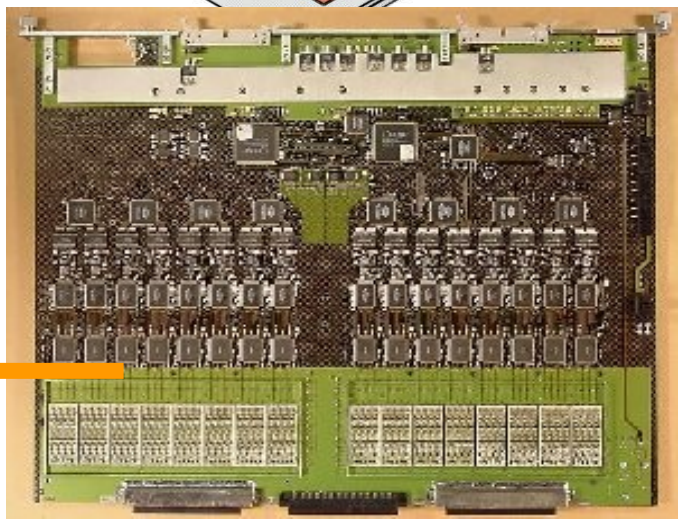
1.5m for barrel
2.5m for endcaps

Front end electronics

- Requirements to electronics
  - Large dynamic range (~2500 MIPS)
  - **Front end electronics embedded**
  - Autotrigger at ½ MIP
  - On chip zero suppression
  - **Ultra low power («25µW/ch)**
  - 10^8 channels
  - Compactness







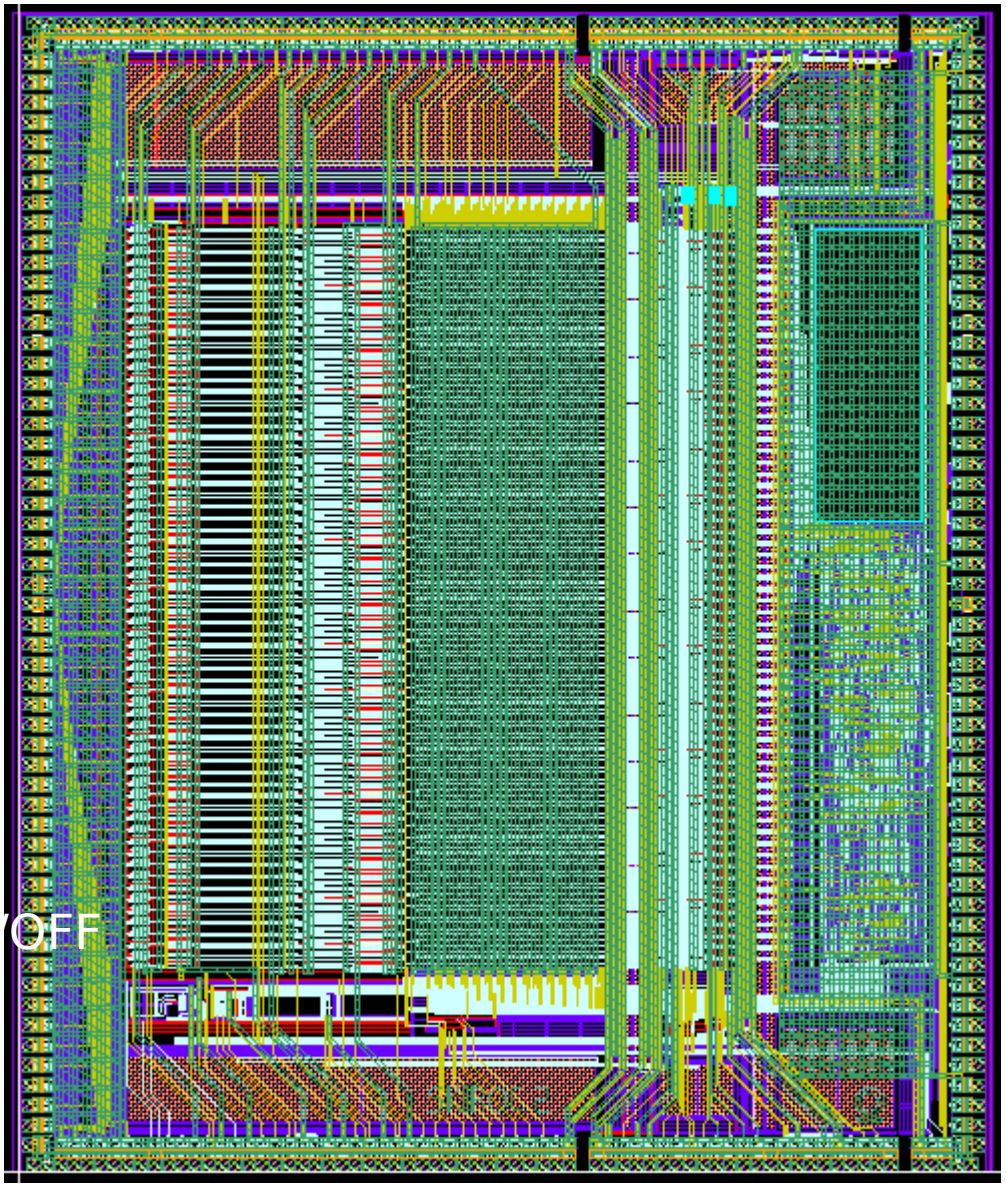
ILC : **25µW/ch**

FLC_PHY3 18ch 10*10mm **5mW/ch**

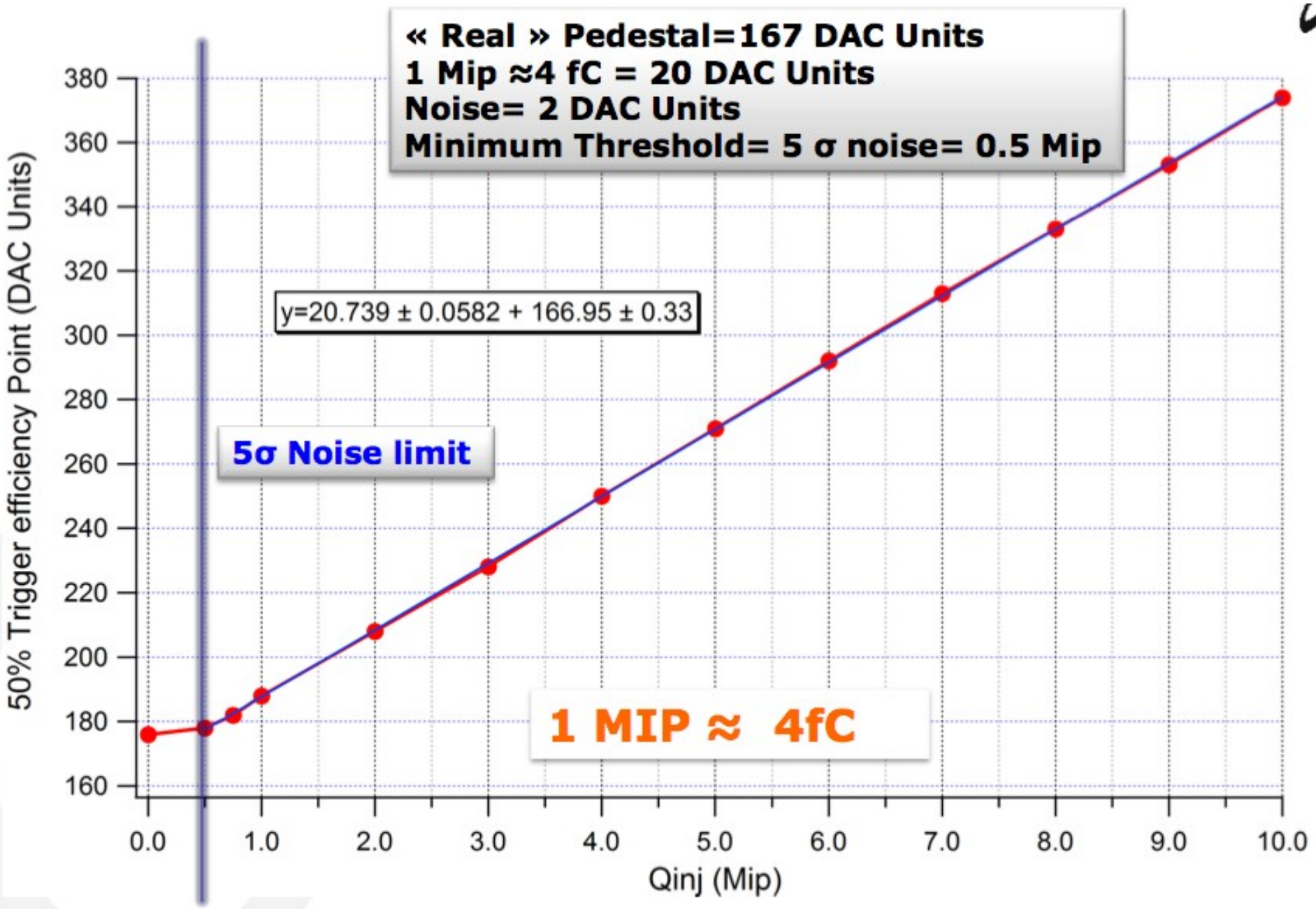
ATLAS LAr FEB 128ch 400*500mm **1 W/ch**

The Ecal ASIC - SKIROC

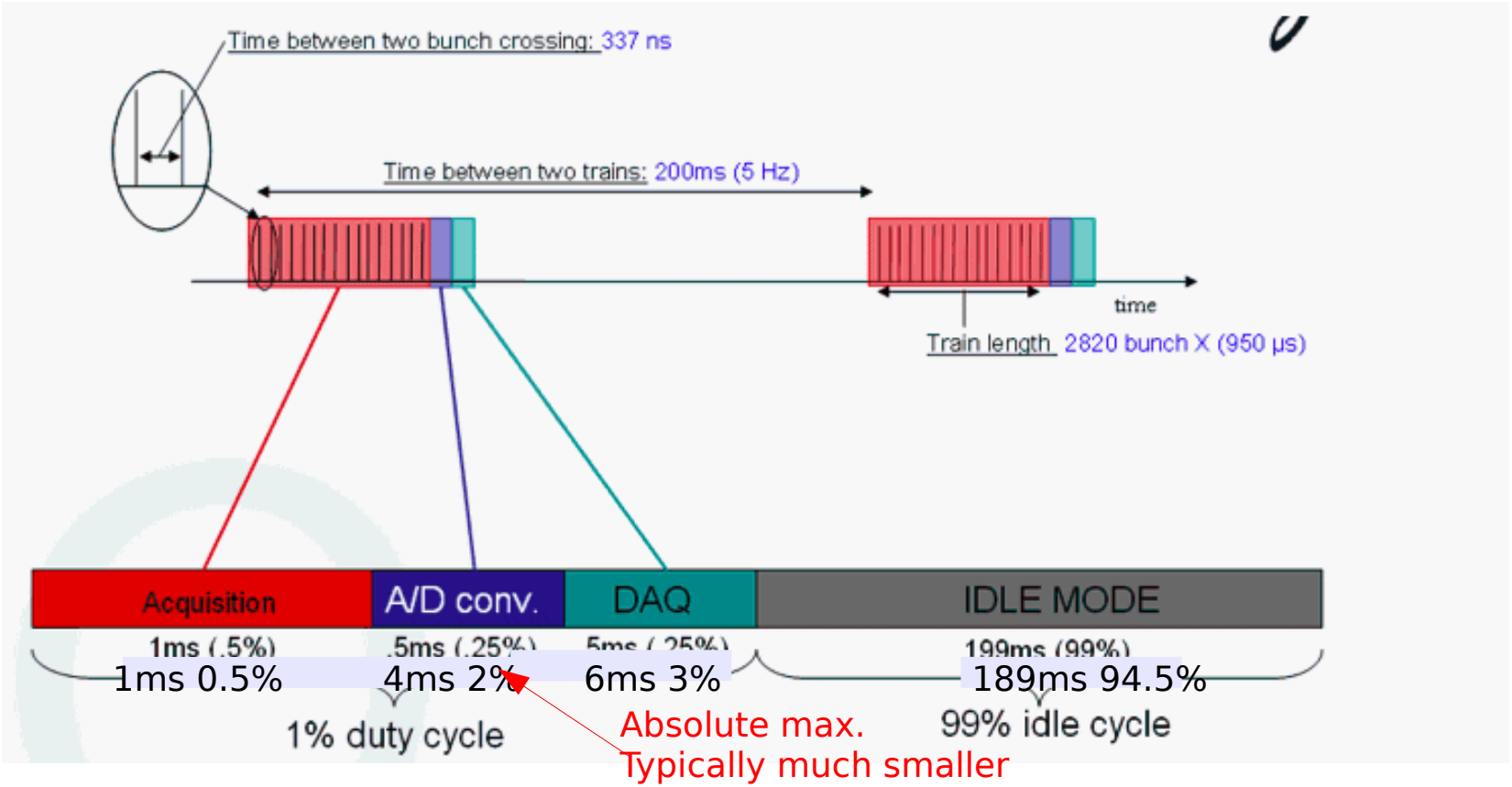
- 64 Channels
- Vss split :
  - Inputs
  - Analogue part
  - Mixed part
  - Digital part
- 250 pads
  - 3 NC
  - 17 for test purpose only
- Enhanced Power control
  - Full power pulsing capability
  - Each stage can be forced ON /OFF
- Die size
  - 7229 µm x 8650 µm



Example for SKIROC characterisation – Trigger efficiency



Power pulsing (better power gating)



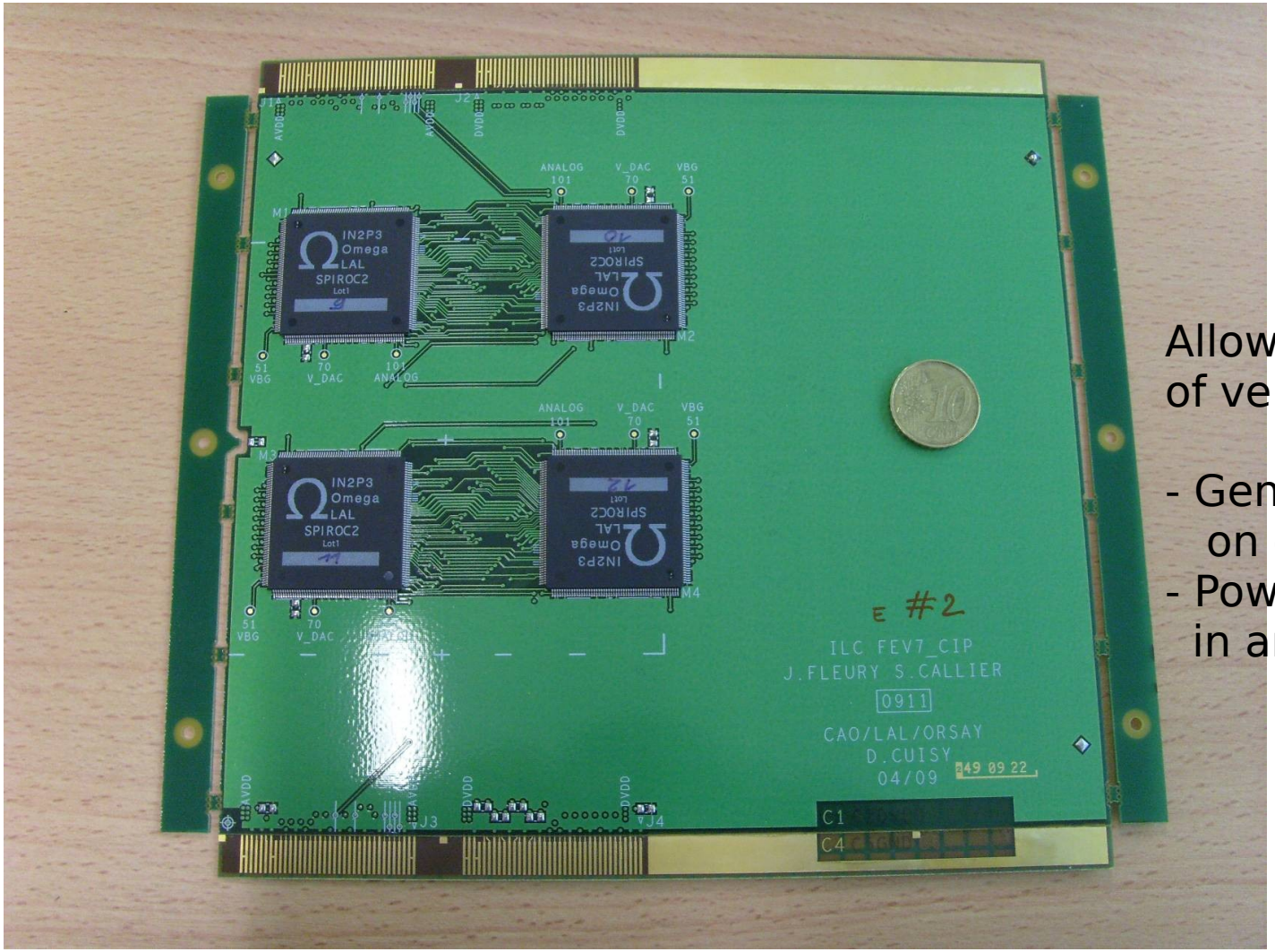
- Electronics switched on during 1ms of ILC bunch train and immediate data acquisition

- **Bias currents** shut down between bunch trains

- Mastering of technology is essential for operation of ILC detectors
  Measurements for SKIROC chip 1.7 mW <=> 27 uW/ch
  Test with SKIROC chip started in lab last week, stay tuned
  m3 of SDCHAL power pulsed with similar chip

R&D for PCBs

PCBs with 'conservative' technology FEV_CIP (Chip in Package)

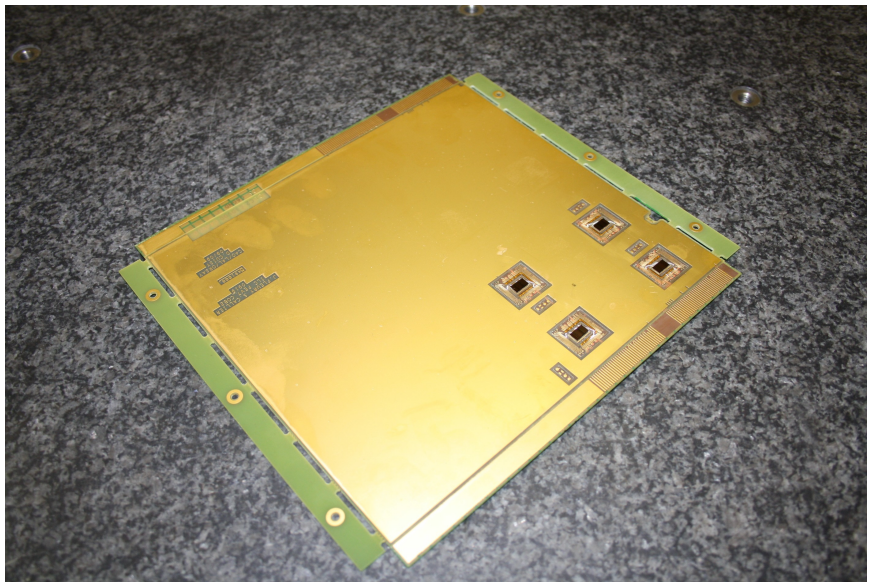


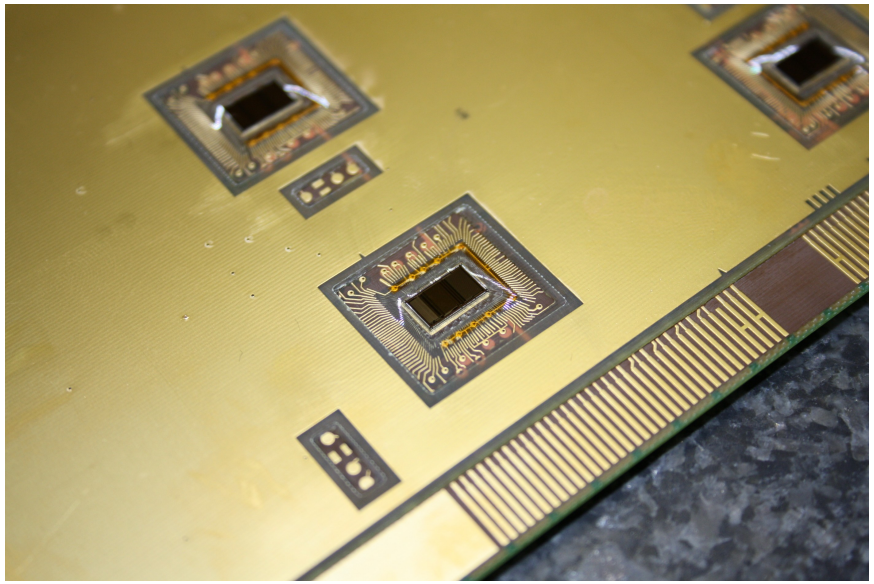
Allows us to realise a number of very useful tests

- General functionality of ASU
  on cosmic bench and in beam
- Power pulsing
  in and outside of magnetic field

Stepwise approach to address R&D challenges

The next step FEV8 with COB – Chip on board





- Circuits wire bonded inside cavities

- Ultra thin

  9 layer board with max. 1.2mm thickness

- Ultra flat

  Deviation from total flatness max. 0.5mm

  Compare with industrial standard ~3mm

- Circuits need to be encapsulated withresine

  Non trivial to realise

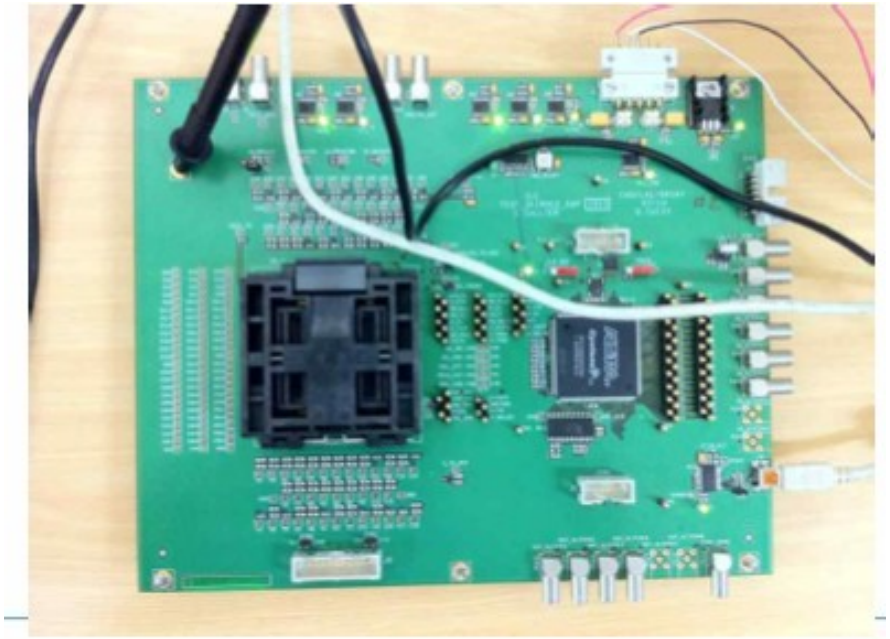
  Home made solution and idustrial solution at hand

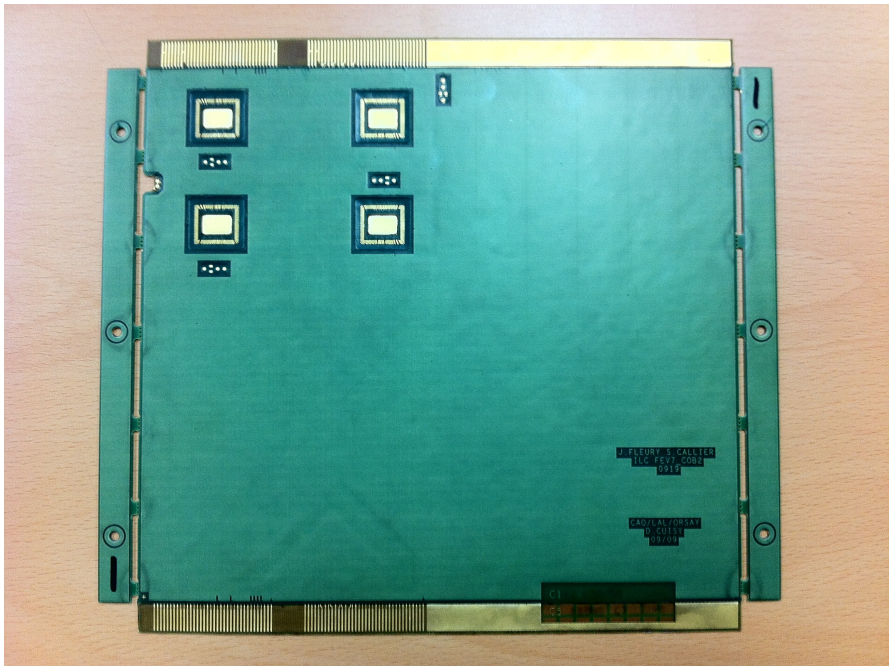
  Long term effects of chips and wire bonds?

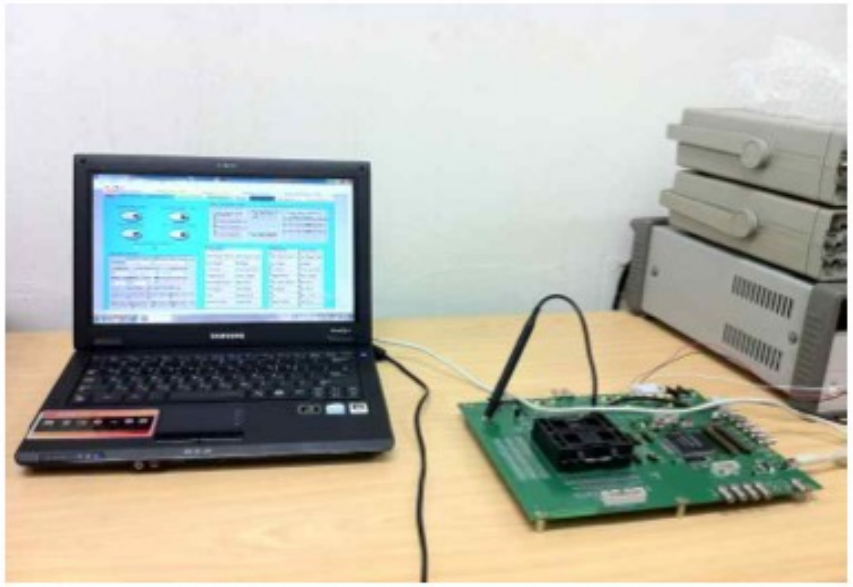
Mastering of these technological challenges is essential to meet LC detector design goals

-> A number of open points!!!

Work on Front End Electronics at SKKU – ANME Lab







Top: FEV PCB produced by EOS Company (Korea)

- Electrical tests successful
- First production
- Company needs to get acquainted to complexity

Left: Test bench for Ecal ASICs at SKKU

R&D for LC calorimeter FEE bears
synergy with instrumentation for accelerators
for medical applications (Isotopes for PET)

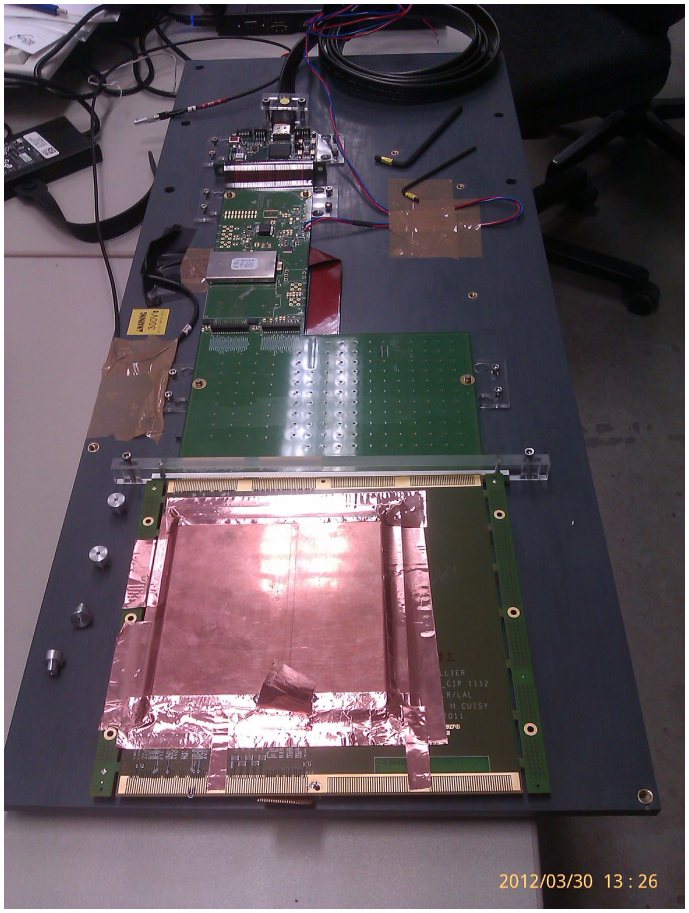
Remark: Funding request PHC Star
Got refused last week => Collaboration at risk!!!

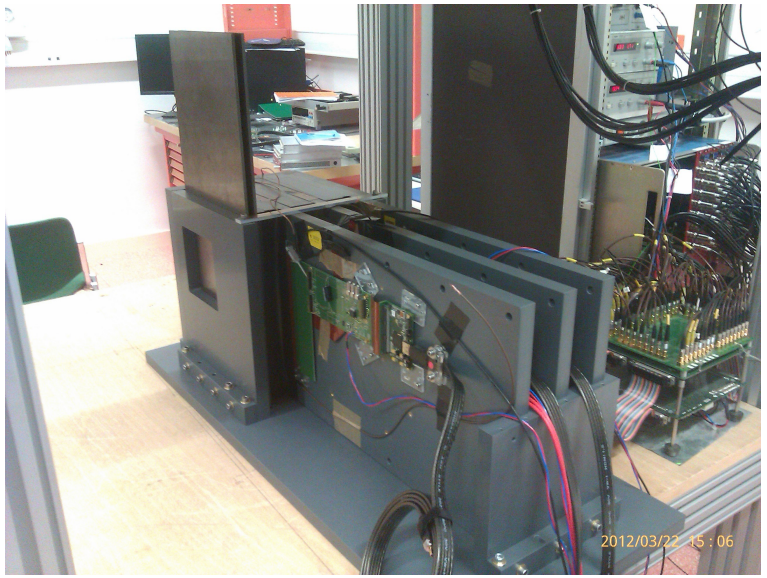
Beam test setup

- wafer 9x9 cm^2, 324 pixels 5x5 mm^2
- **2 slabs SKIROC (4 ASICs)**

  2 channels with 2 pixels and 22 channels

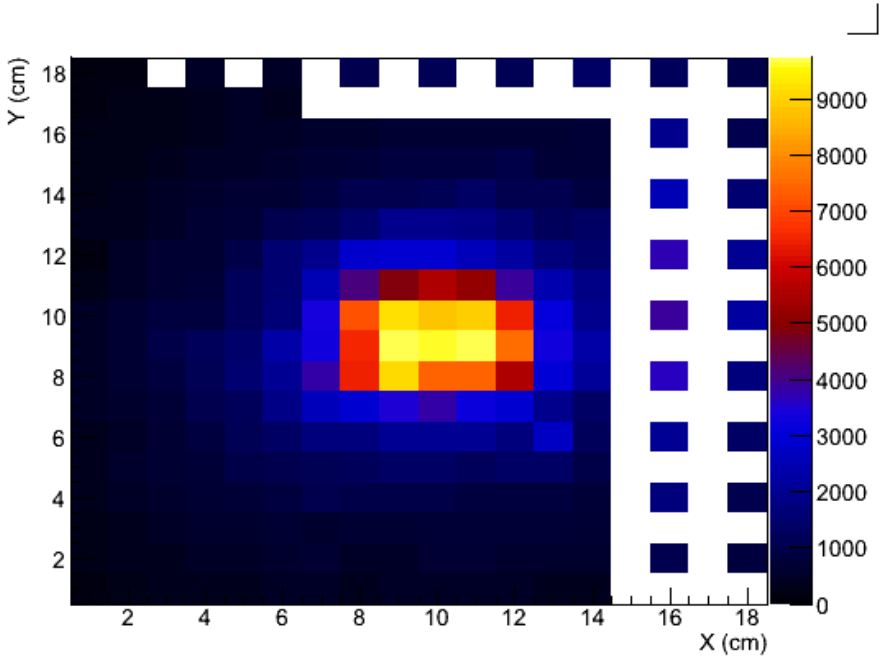
  with 4 pixels
- 2 slabs SPIROC (4 ASICs et 1 ASIC)
- Structure PVC modulable (2 configurations)
- 6 Tungsten plates of 4mm thickness

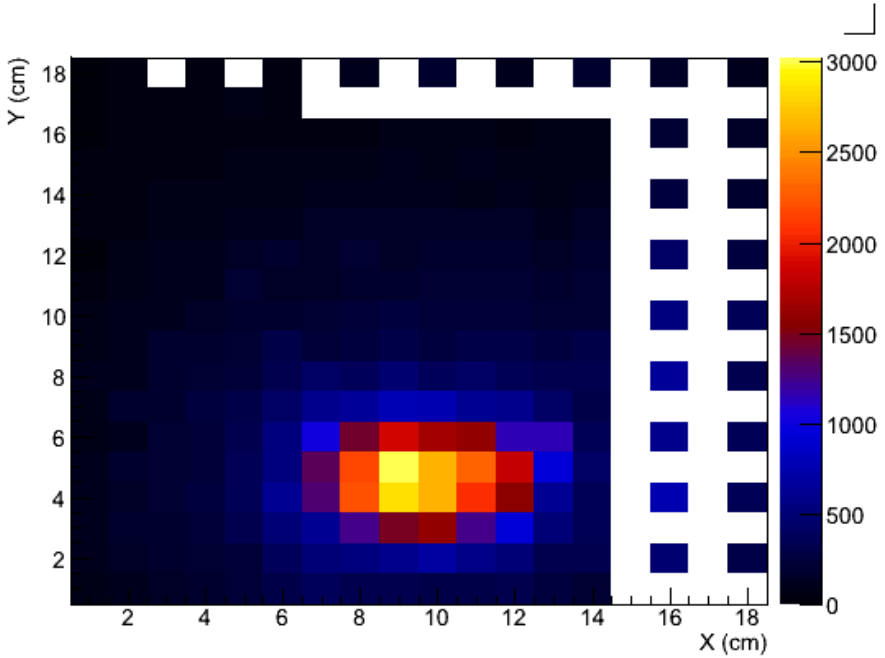




Purpose of beam test
was to bring together
for the first time the entire
equipment
-> regain of project's
momentum

First Results





Beam spot
In the middle
of layer

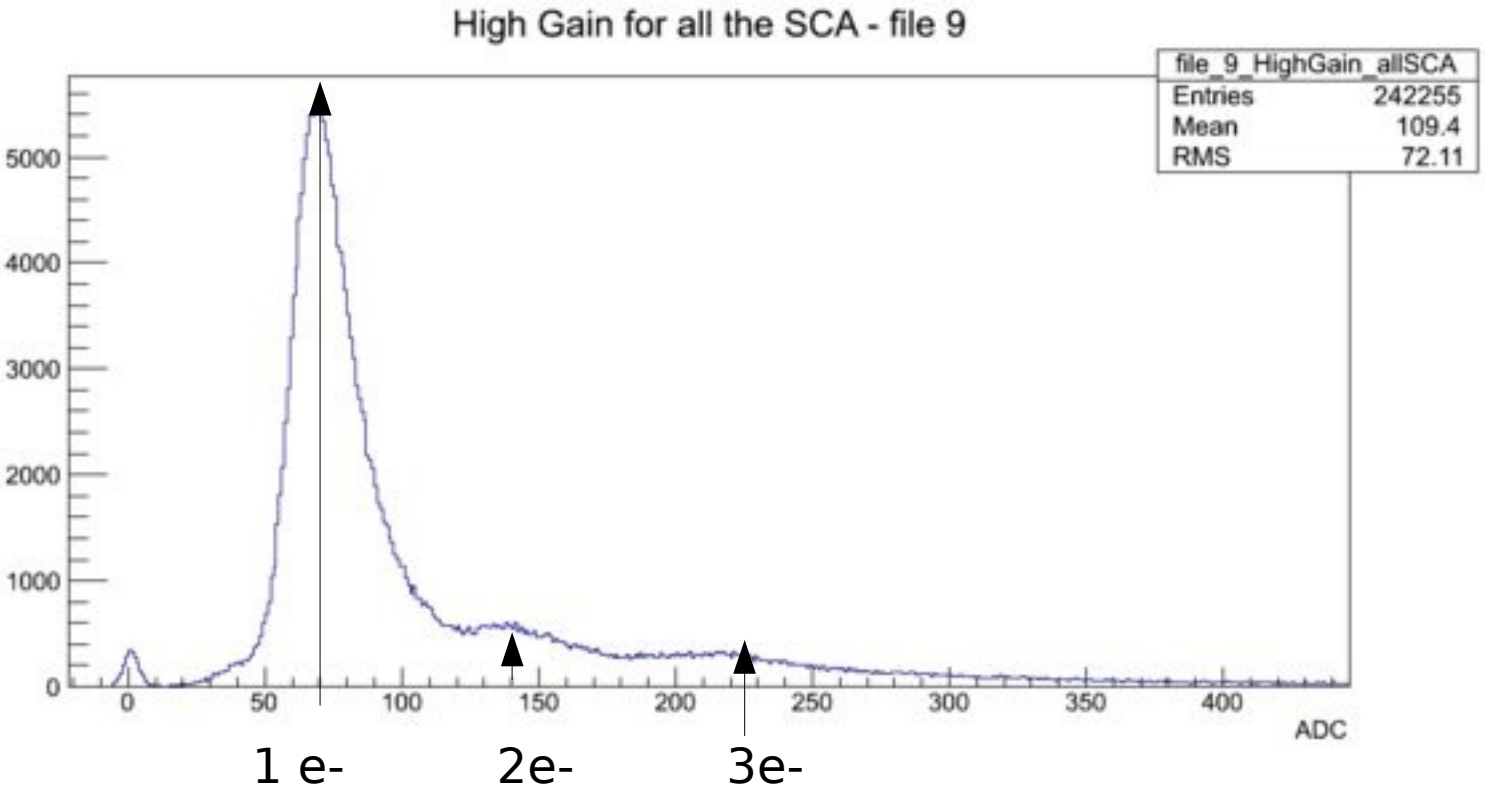
moves

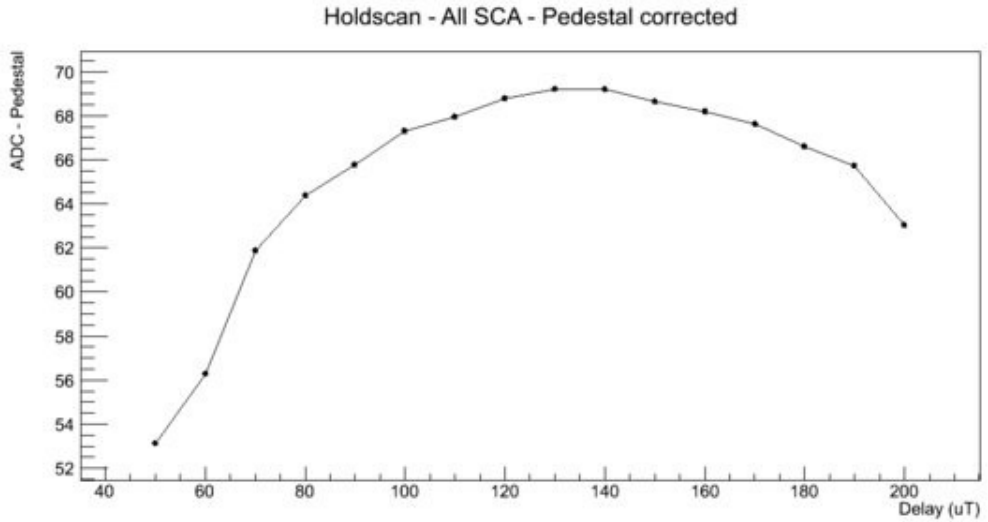
Accordingly to
Beam sport

Success after a real cold start

Congrats to those who
Put together the SKIROC/FEV8
Setup out of the box

MIP signals and further studies

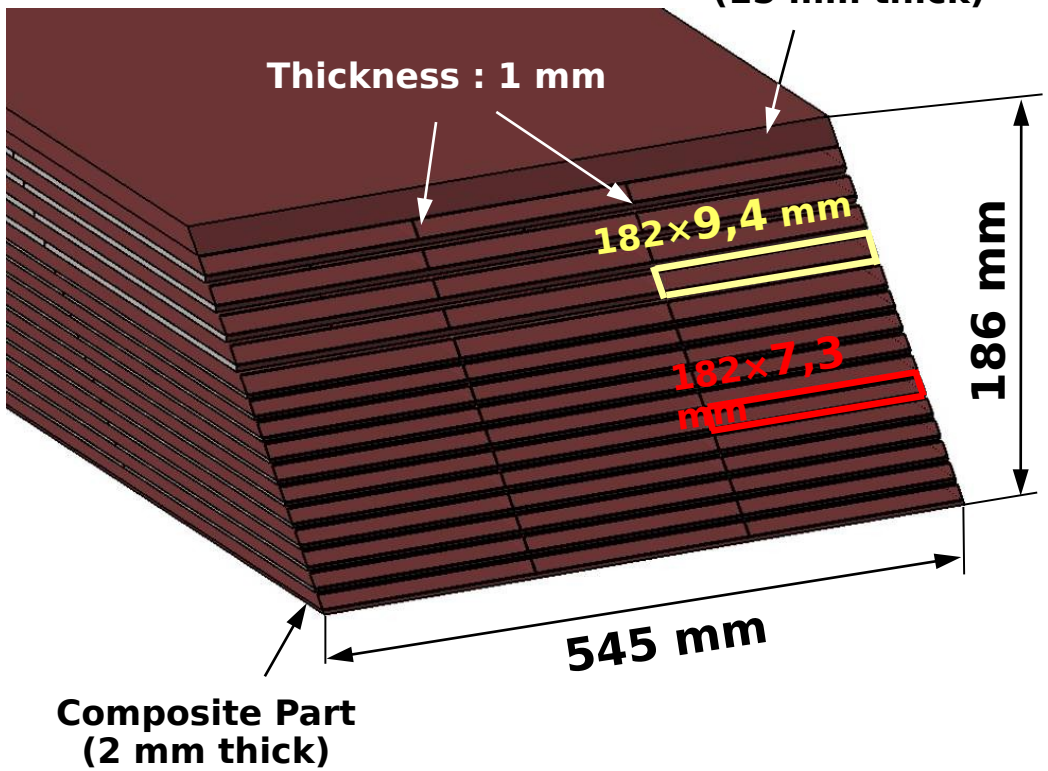


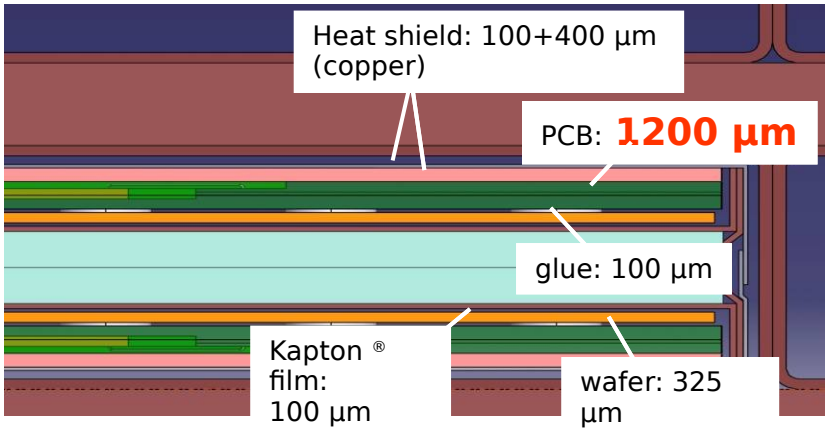


Hold scan
Curve as expected

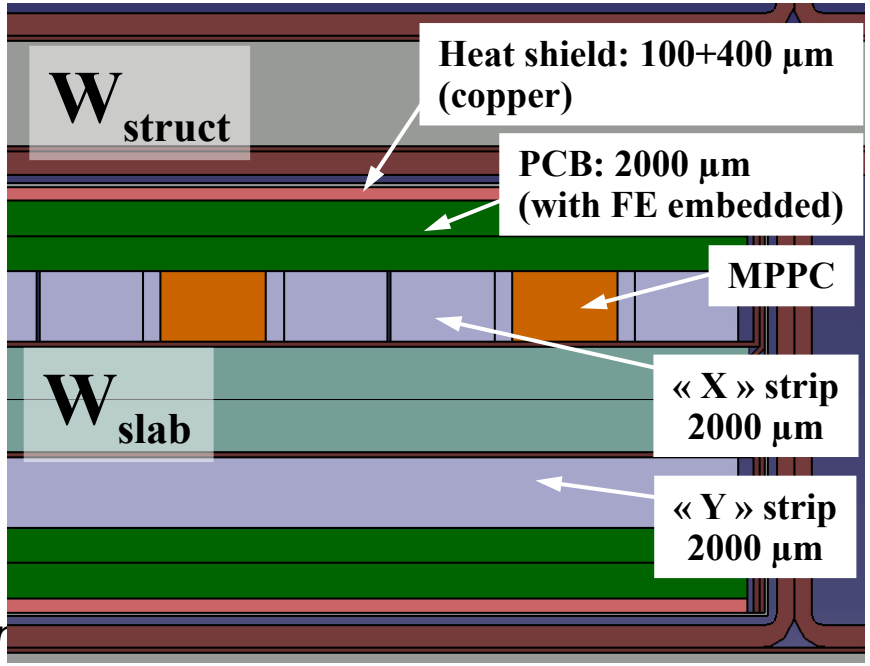
Two Ecal prototypes

ECAL W/Si





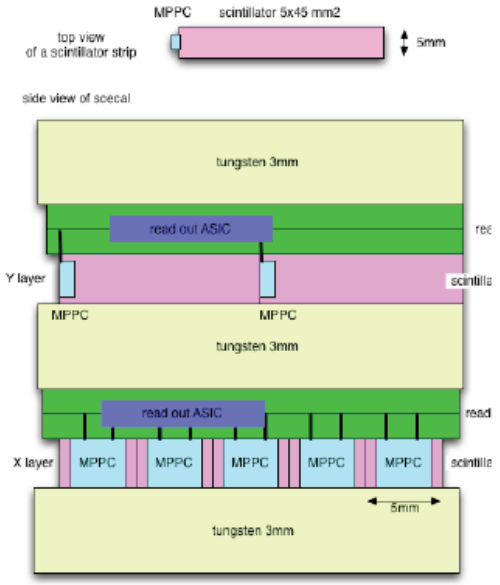
ECAL W/Scin



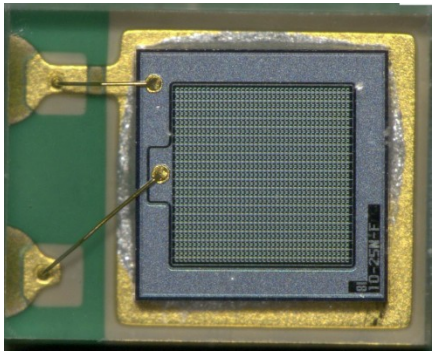
Mechanics and electronics
developed for both prototypes

ASICs for scintillator r/o

- Granular ECAL using Pixelated Photodetector (PPDs) and scintillator strips with orthogonal directions for fine segmentation (5 mmx 5 mm lateral granularity)
- Tungsten absorbers
- Physics prototypes tested in testbeam
  - 30 layers, 72 strips per layer



- Current development for finer granularity:
  - Sensor layer on printed circuit board (EBU boards):
  - 4 rows of 18 scintillator strips
  - 1 SPIROC2b for 1 row
  - Beam test: Fall 2012



@K. Kotera, T. Takeshita

Summary and outlook

- Successful R&D for front end electronics for highly granular calorimeters

- ASICs 'leave' test bench and 'enter' calorimeter prototypes

- R&D oriented towards LC offers considerable synergies with other fields of science

- FKPPL/FJPPL funds helped to establish or to launch collaboration between french groups and groups in Japan and Korea
  SPIROC, FEV boards

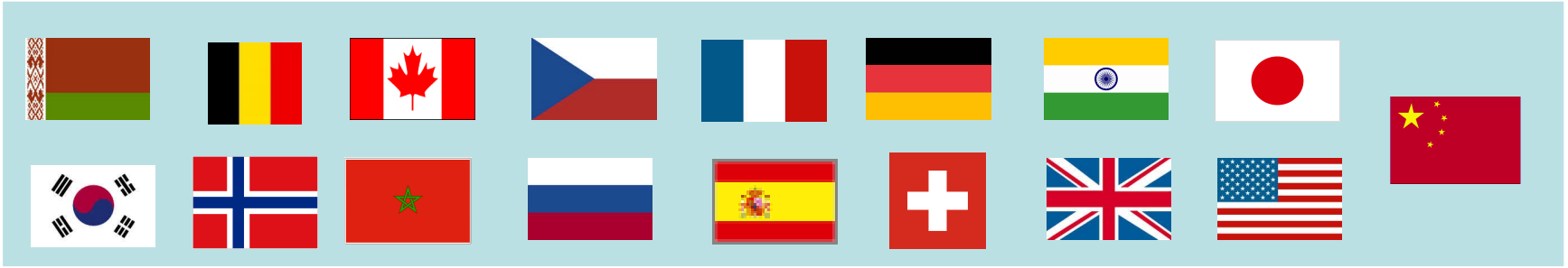
- It will clearly be difficult to maintain collaborations w/o sustained funding in the future (e.g. collaboration with Korean colleagues on critical track)

Backup Slides

The CALICE Collaboration

Calorimeter for ILC

Calorimeter R&D for a future linear collider



~330 physicists/engineers from 57 institutes
and 17 countries from 4 continents

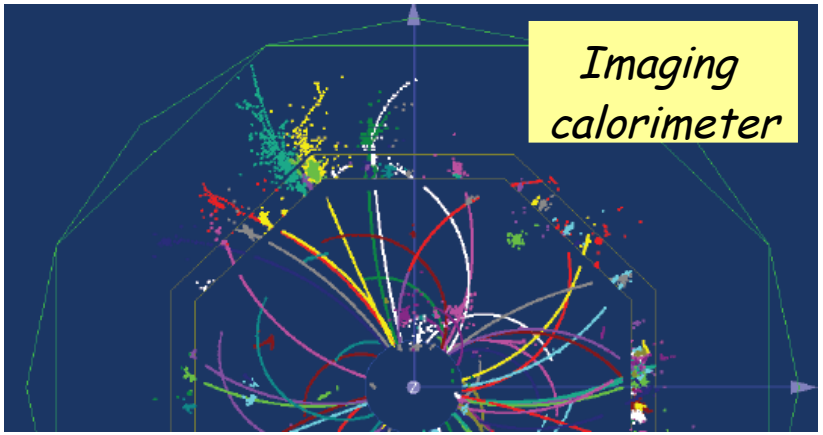
- Integrated R&D effort

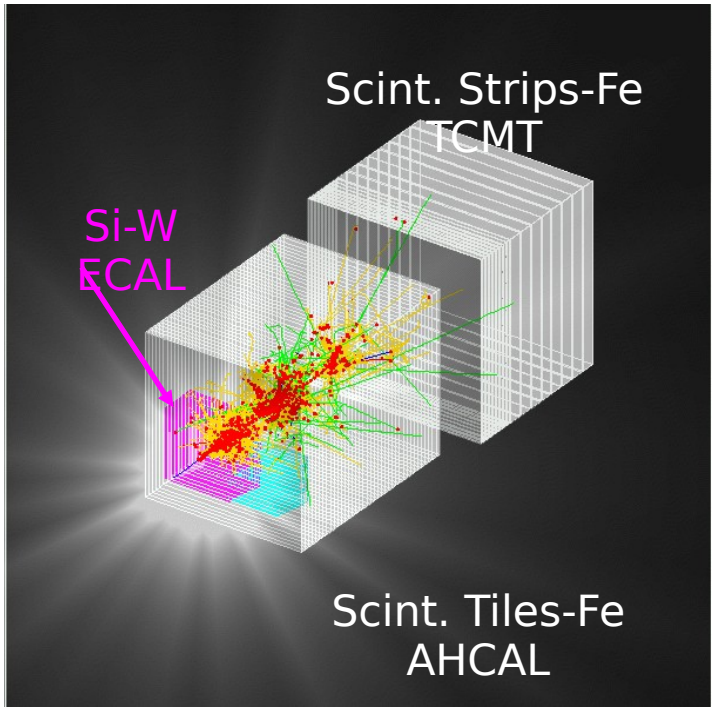
- Benefit/Accelerate detector development due to *common* approach

The Calice Mission

Final goal:

A highly granular calorimeter optimised for the Particle Flow measurement of multi-jets final state at the International Linear Collider



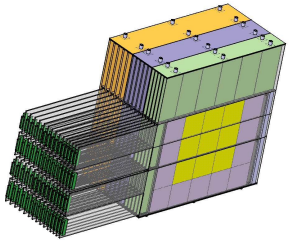


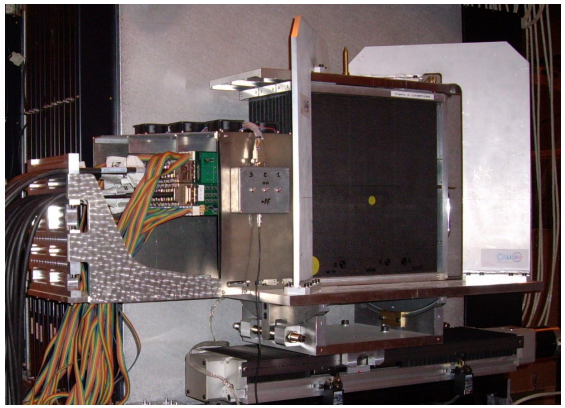
Intermediate task:

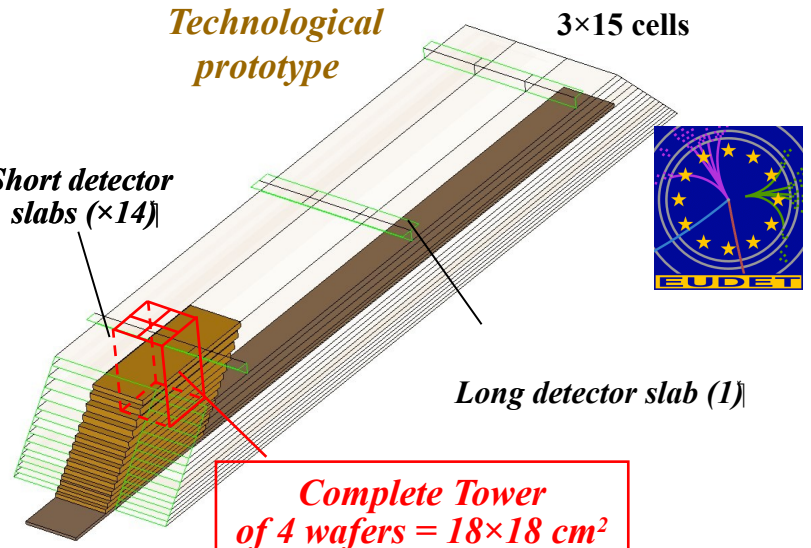
Build prototype calorimeters to
- Establish the technology
- Collect hadronic showers data with unprecedented granularity to
  - tune clustering algorithms
  - validate existing MC models

Technological Prototype

- Physics prototype: Validation of main concept
- Techno. Proto : Study and validation of technological solutions for final detector
- Taking into account industrialisation aspect of process
- First cost estimation of one module







- **3 structures : 24 X_0 (10×1,4mm + 10×2,8mm + 10×4,2mm)**
- **sizes : 380×380×200 mm3**
- **Thickness of slabs : 8.3 mm (W=1,4mm)**
- **VFE outside detector**
- **Number of channels : 9720 (10×10 mm²)**
- **Weight : ~ 200 Kg**

- **1 structure : ~ 23 X_0 (20×2,1mm + 9×4,2mm)**
- **sizes : 1560×545×186 mm3**
- **Thickness of slabs : 6.8 mm (W=2,1mm)**
- **VFE inside detector**
- **Number of channels : 45360 (5×5 mm²)**
- **Weight : ~ 700 Kg**

Parties Involved

6 Laboratories are sharing out tasks in according to preferences and localization:

Assembling of A.S.U. (industrialization, gluing ests) + backend system (DIF support) + services

of wafers

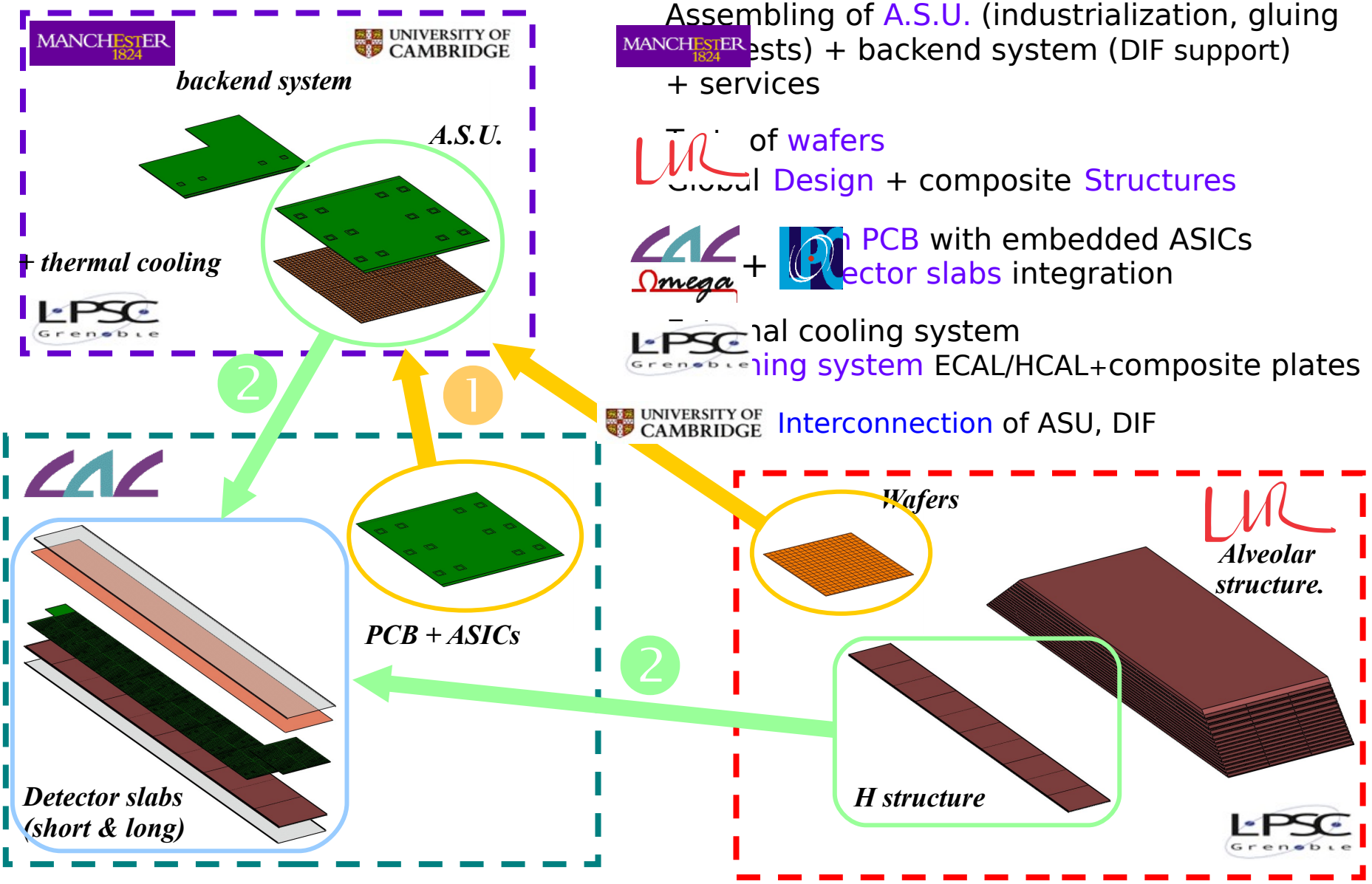
l Design + composite Structures

PCB with embedded ASICs + ector slabs integration

al cooling system

ing system ECAL/HCAL+composite plates

Interconnection of ASU, DIF



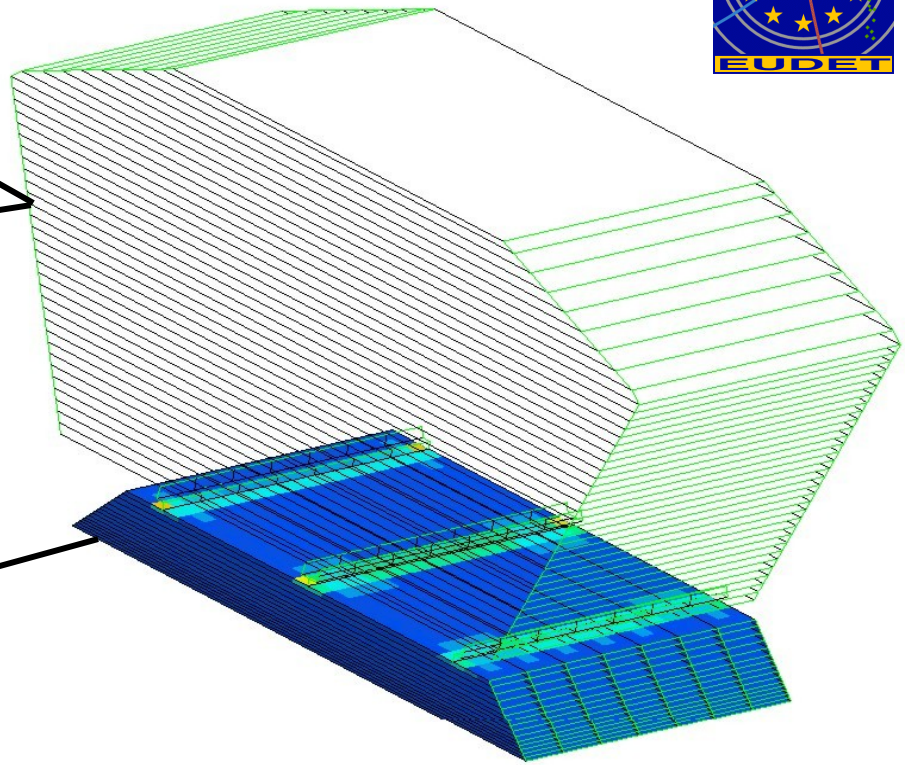
ASICs Frontales: Les Chips ROC

- Prototypes EUDET: modules à grande echelle (~2m)
- Financement partiel par EU (06-09)
- ECAL, AHCAL, DHCAL

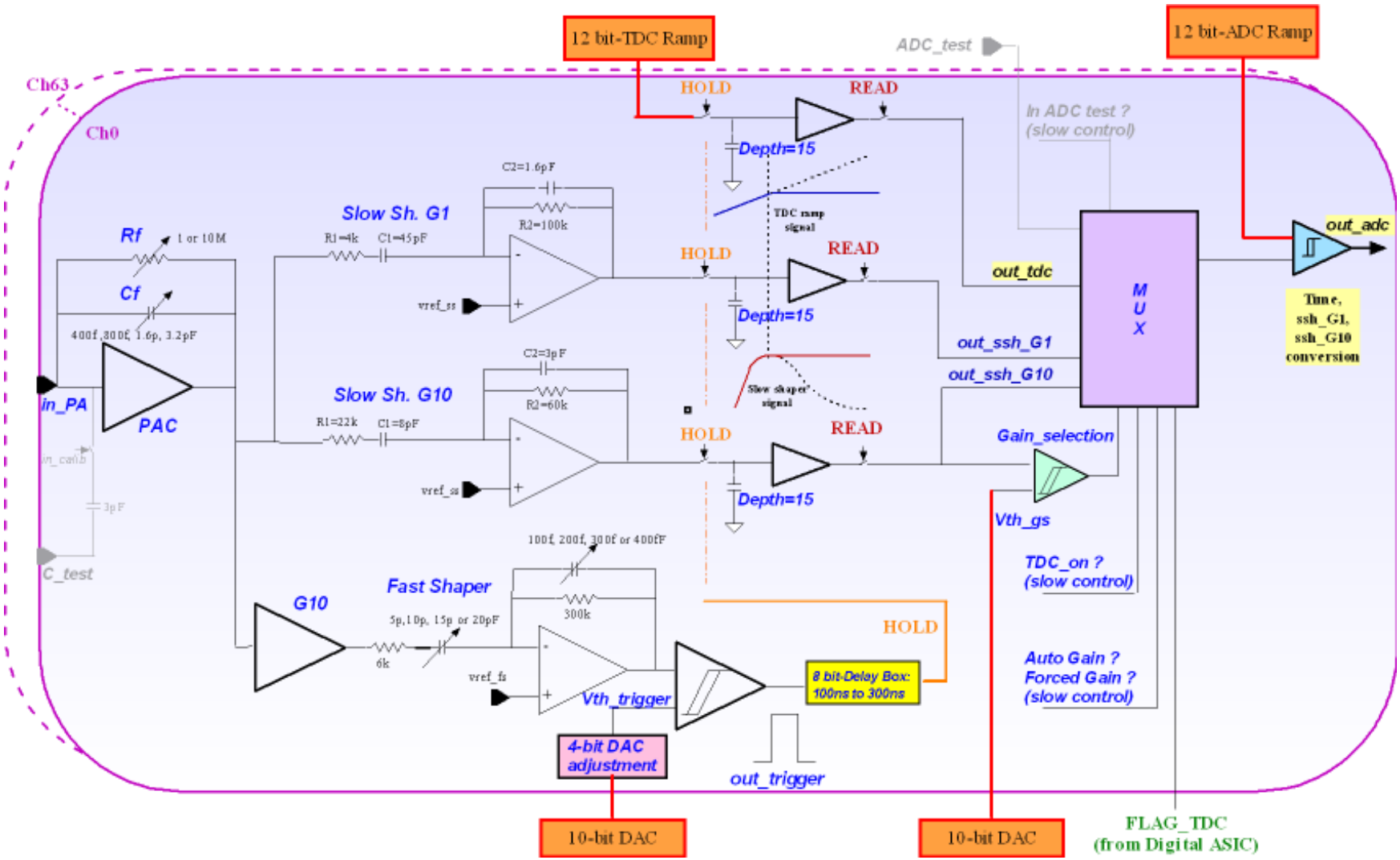
SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²
June 07

HARDROC
Digital HCAL
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept 06

SKIROC
ECAL
(Si PIN diode)
36 ch. 20mm²
Nov 06

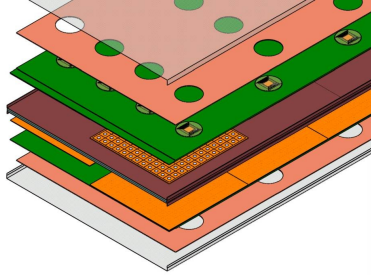


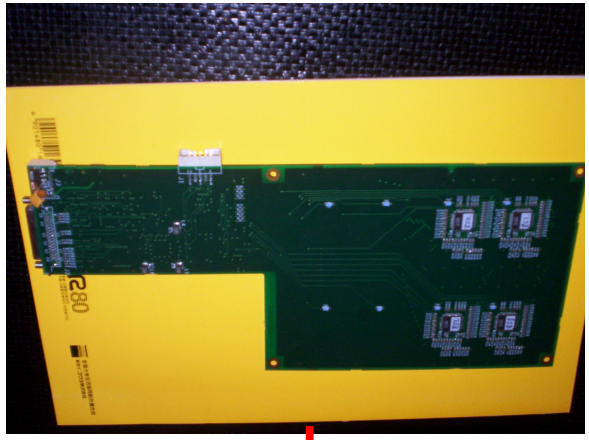
SKIROC 2 block scheme



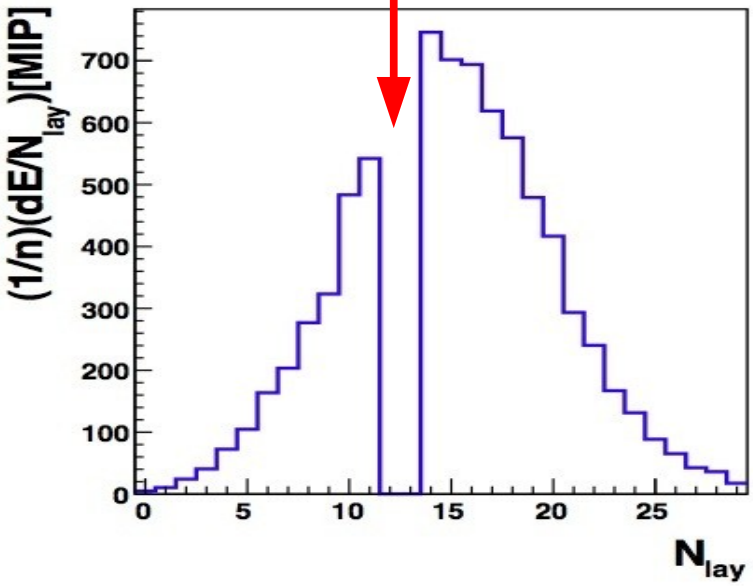
Embedded electronics - Parasitic effects?

Exposure of front end electronics to electromagnetic showers

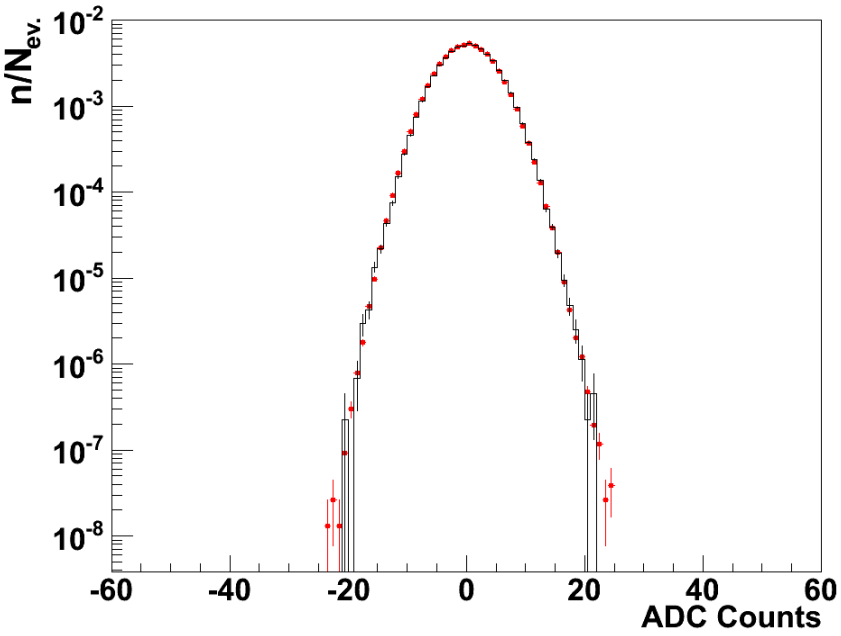




Chips placed in shower maximum
of 70-90 GeV elm. showers



Comparison: Beam events
(Interleaved) Pedestal events



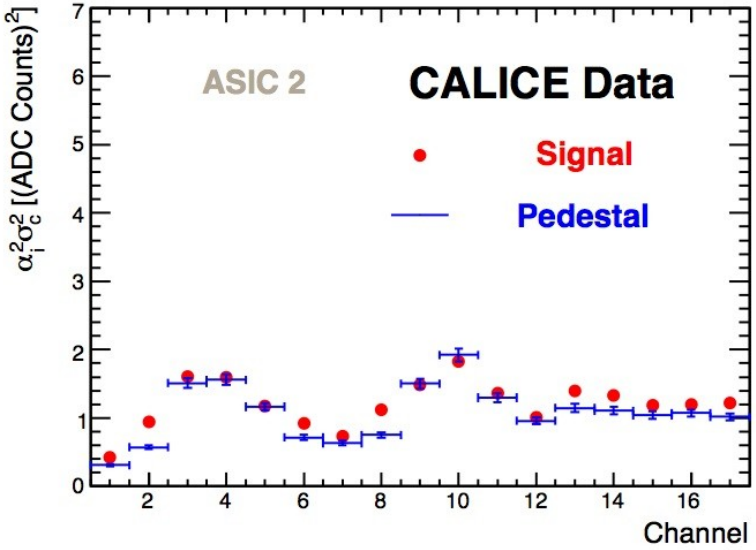
- No sizable influence on noise spectra by beam exposure
  ΔMean < 0.01% of MIP ΔRMS < 0.01% of MIP
- No hit above 1 MIP observed
  => Upper Limit on rate of faked MIPs: ~7x10^{-7}

Possible Effects: Transient effects
Single event upsets

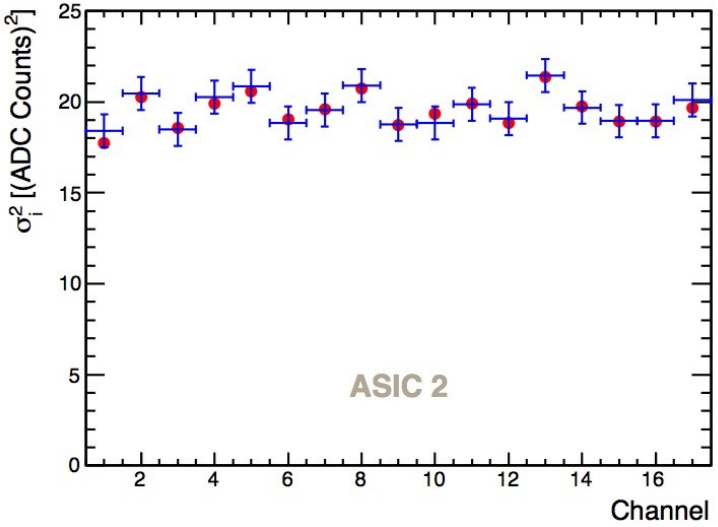
NIM A 654 (2011) 97

Detailed noise analysis

Coherent noise

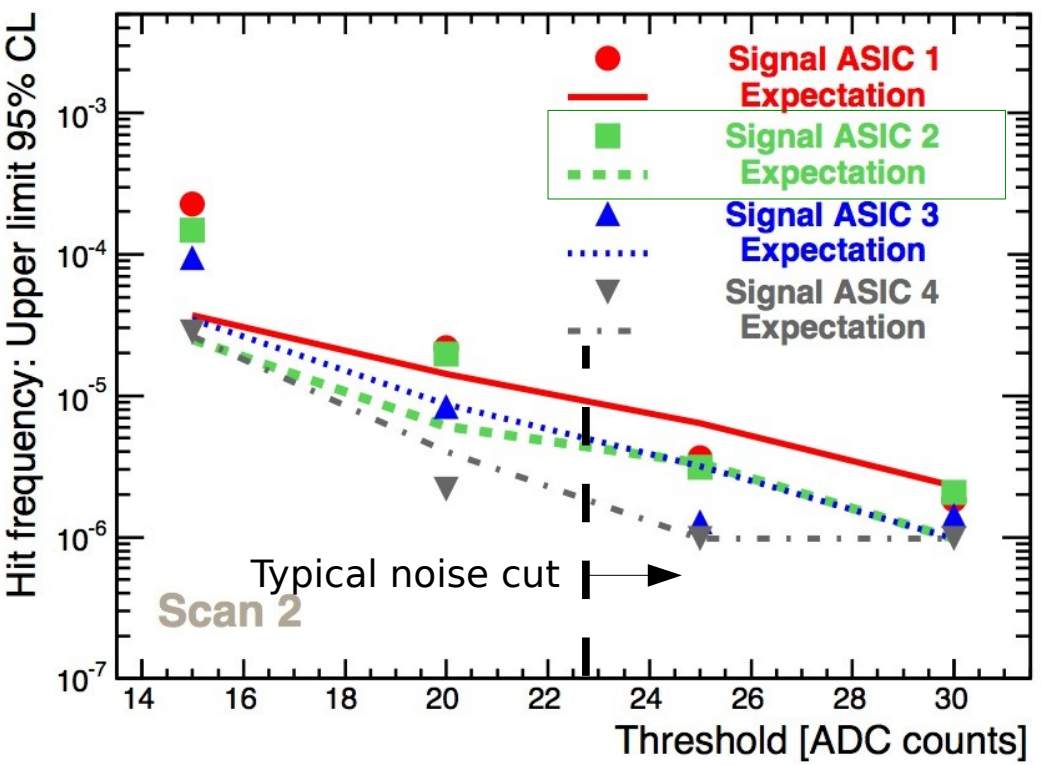


Incoherent noise



Noise pattern unchanged by shower particles

Upper limits on parasitic hits – 95% CL



Chip in beam

- Frequency of parasitic hits comparable with regular electronics noise
- < 10^{-5} above typical noise cut

Compare with 2500 cells in typical ee-> tt event

A generic DAQ system for the CALICE calorimeters (Technological Prototypes)

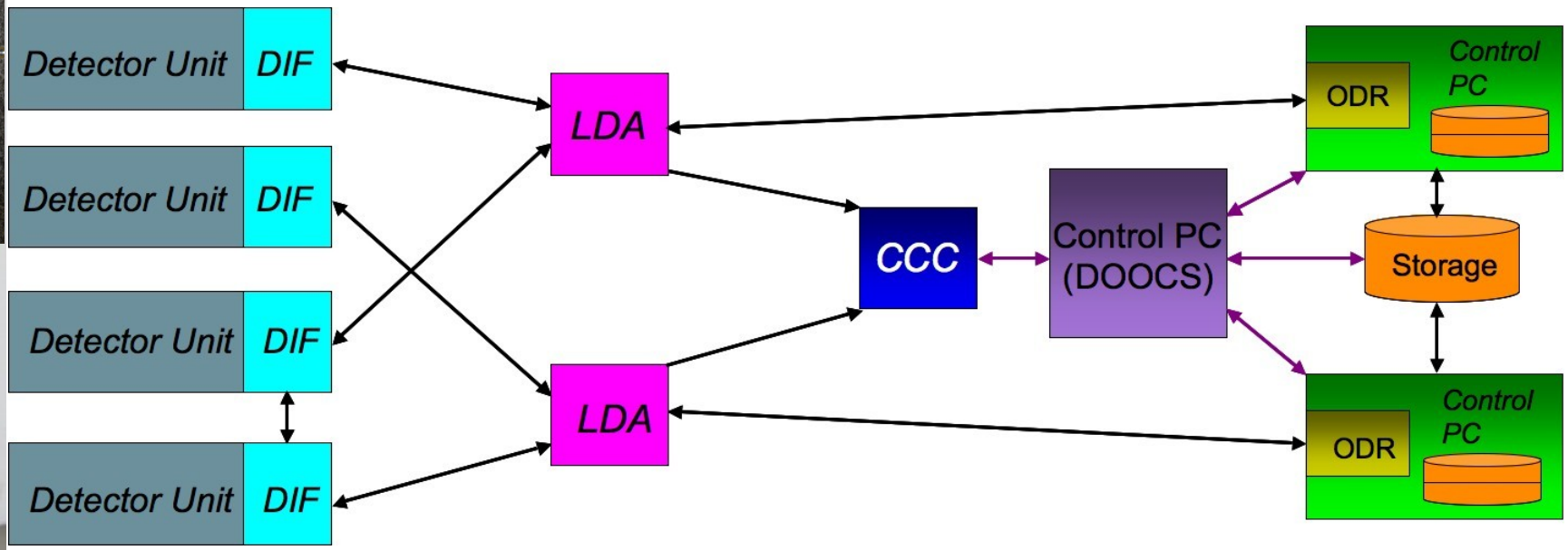
Standard

HDMI connectors
LVDS
GBEthernet
Optical links

Generic

FPGA

Scalable



DAQ chain established using SPIROC and FEV7_CIP
Since 1st quarter of 2012 SKIROC and FEV8_CIP
-> beam test in March 2012 at DESY