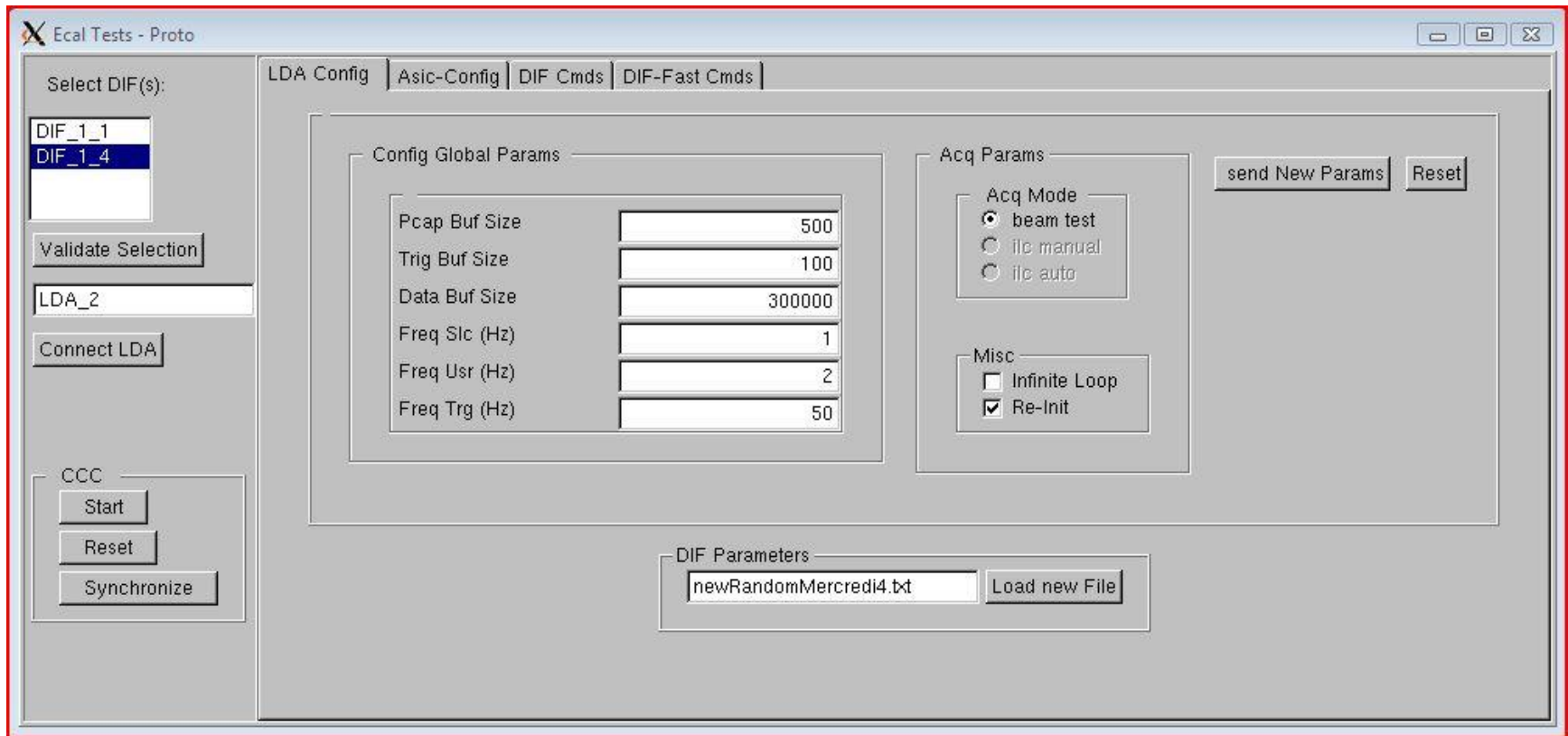


ECAL GUI - PROTO

Main window1



Asic Configuration

The screenshot shows the 'Ecal Tests - Proto' software interface, specifically the 'Asic-Config' tab. The interface is divided into several sections for configuring the ASIC.

Left Panel:

- Select DIF(s): A list with 'DIF_1_1' and 'DIF_1_4' (selected).
- Buttons: 'Validate Selection', 'LDA_2', 'Connect LDA', 'CCC' (with 'Start', 'Reset', 'Synchronize' sub-buttons), and 'Load SC'.

Main Configuration Area:

- LDA Config:** 'device type' is 'Spiroc2', 'selected file' is 'newRandomMercredi4.bt', and 'file save as:' is empty.
- External Communication Enable:**
 - External Commands: TRIG_EXT, FLAG_EXT, RAMPADC_EXT, TEST_ADC, HOLD_EXT.
 - ReadOut: 'start ReadOut1' and 'end ReadOut1' dropdown menus.
 - Power Pulsing: PA, SSH_HG_1, DLY_TRG, ADC_1, SCA, FS_1, TDC, DLY_TDC, ADC_2, BG, FS_2, DAC4B, DISCADC, DAC_1, SSH_HG_2, DISCTRG, DLY_HLD, DISCGS, DAC_2, and EN_OR36.
- Disable Charge PreAmpifier:** A grid of checkboxes for channels 0-35, with channels 0-11 and 24-35 checked.
- Internal Test Capacitor Enable:** A grid of checkboxes for channels 0-35, with channels 1-4 checked.
- Discriminator Mask Enable:** A grid of checkboxes for channels 0-35, with channels 0-11 and 24-35 checked.
- Discr 4 bit-DAC Thresh Adjust:** A grid of spinners for channels 0-35, with values ranging from 0 to F.
- Chip Global Configuration:**
 - Chip Ids: 0, 1, 2, 3, 4, 5, 6, 7.
 - Time constant: 50 ns, Backup SCA .
 - Capacitor: HG_PA_Fdck 200 fF, HG_PA_Comp 0 pF.
 - Delay: DLY_TDC_T 0, DLY_TRG_T 14, DLY_HLD_T 14, DLY_RST_T 14.
 - TDC Ramp Slope: Fast, ADC Ramp Slope: 12 bits, DACTRIGGER: 5.
 - TDC switch .

Block Transfer Commands

The screenshot displays the 'Ecal Tests - Proto' software interface, which is used for configuring and executing block transfer commands. The interface is organized into several main sections:

- Select DIF(s):** A list on the left side showing 'DIF_1_1' and 'DIF_1_4', with 'DIF_1_4' selected. Below this are buttons for 'Validate Selection', 'LDA_2', and 'Connect LDA'.
- CCC:** A section on the left containing 'Start', 'Reset', and 'Synchronize' buttons.
- Navigation Tabs:** 'LDA Config', 'Asic-Config', 'DIF Cmds', and 'DIF-Fast Cmds' are visible at the top.
- BT Data:** A central panel containing:
 - BORB:** Includes 'Bank1-Conf ROC Interface' (Chip Type: Spiroc2, Control: BT checked, Manual unchecked, Chip Number: 4) with a 'Write bank1' button; 'Bank2-I/O Slab Conf' (force PowerSel, force ROC power, rst, clk checkboxes) with 'Write bank2' and 'Read Data' buttons; and 'Bank3-RND Data Generator' (Inter Slice Delay, Enable, Nb of Packets, Packets Size) with 'Write bank3' and 'Read Data' buttons.
 - MODE:** Includes 'word#1' options (Led On, UserConn(9), Enable Roc Debug Interface, Enable SPYROC readout), input fields for 'DIF_ID' (0), 'DCCNibble(ReadOnly)' (1), and 'Firmware revision(ReadOnly)' (0), and 'Write' and 'Read' buttons.
 - RESET:** Includes radio button options (DIF, Slab, All, SC Registers, Read, Prob, Calib) and 'Send Reset' and 'Read Reset Register' buttons.
- BT Cmds:** A section on the right containing a vertical stack of buttons: 'Slow Clock Synchro', 'Firmware Revision', 'Enable Ram Access', 'Disable Ram Access', 'Acq Reset Counters', 'Write SC', 'Store SC', 'Comp SC', 'Analog Read', 'Start RO', 'Readback SC DATA', and 'Readback From Chip'.

Fast Commands

