DIF FW Status

ROC interface

Meeting interne CALICE DAQ FRANCE

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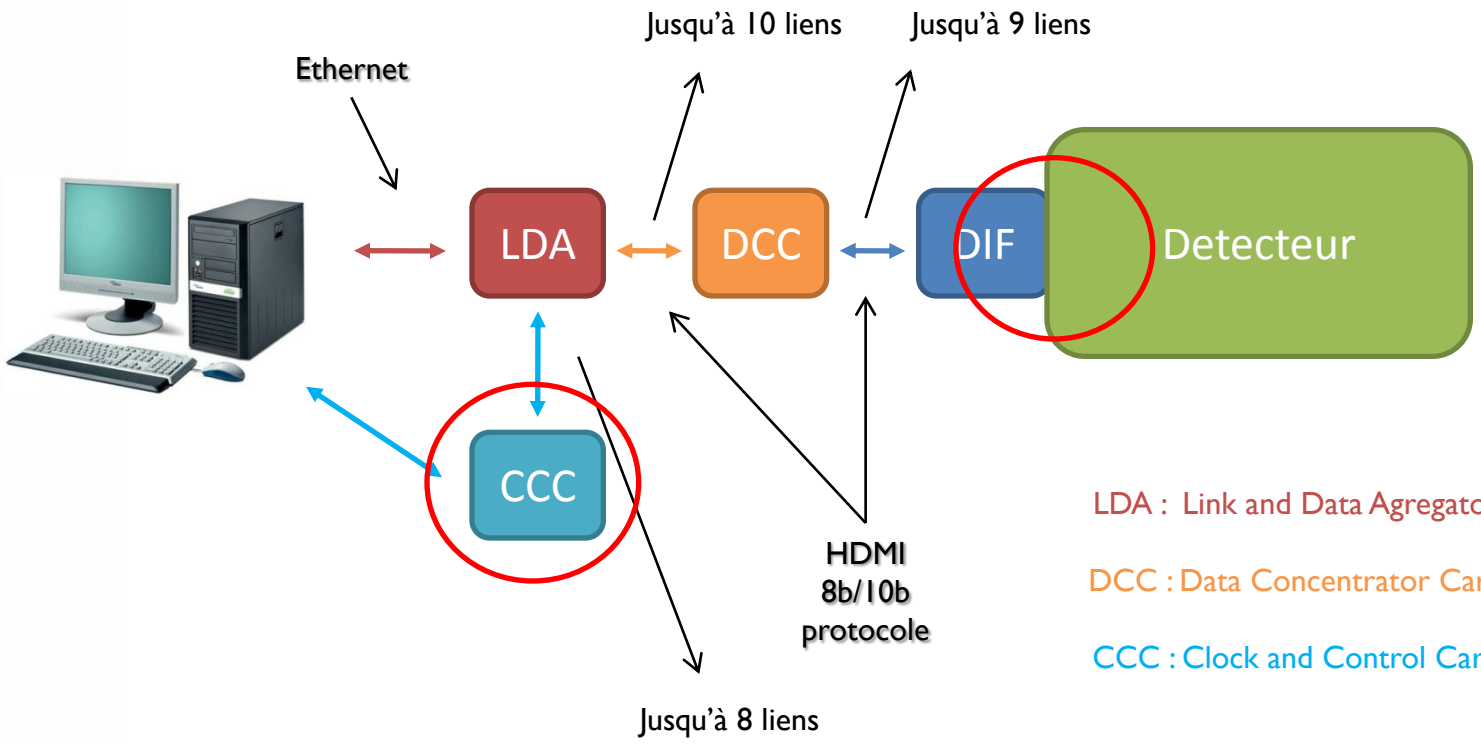
Status DAQ CALICE v.2 2011



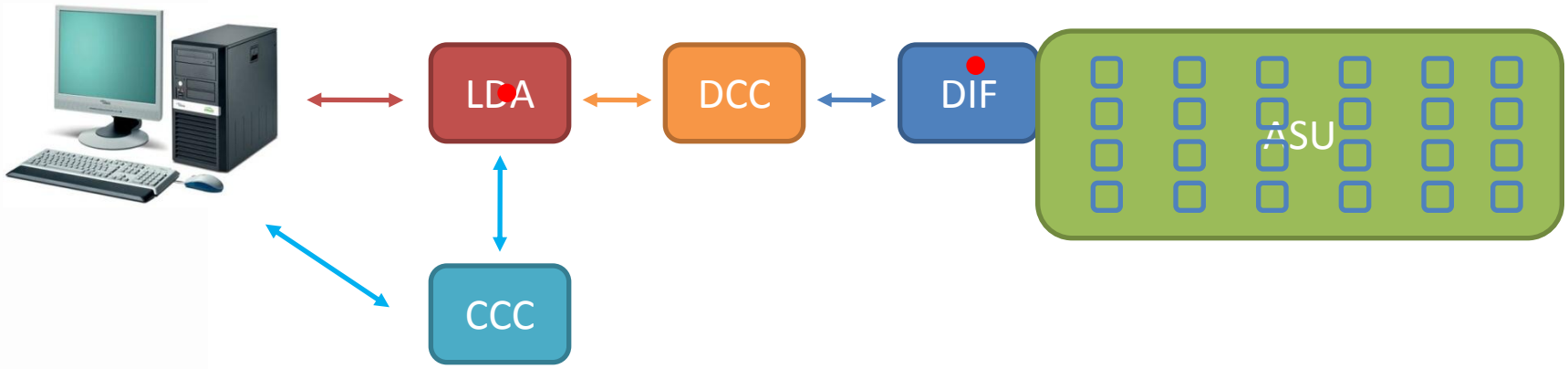
LDA : Link and Data Agregator

DCC : Data Concentrator Card

CCC : Clock and Control Card

II. CALICE DAQ v.2

Slow Control



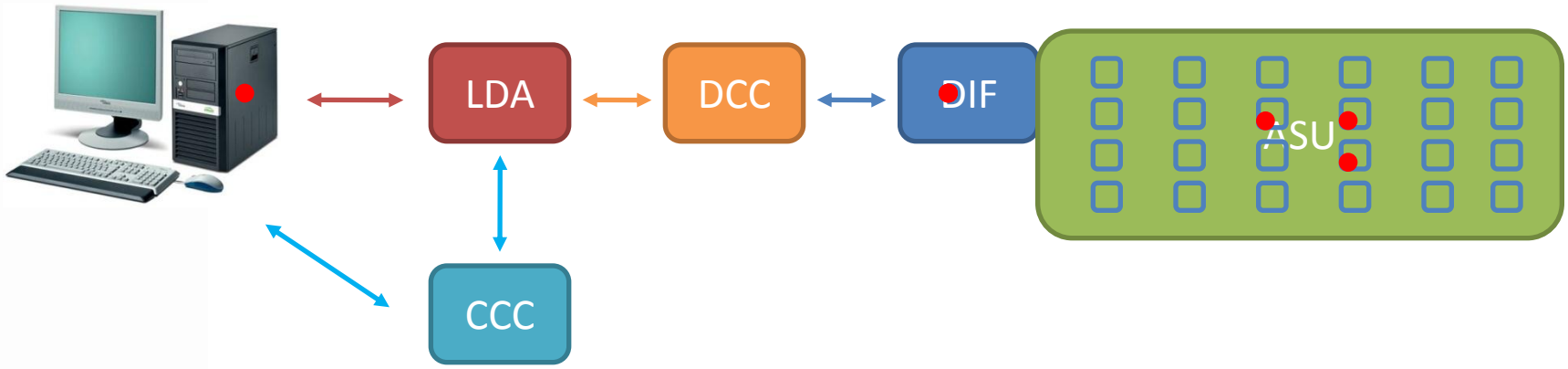
We experienced some problems to configure all the plan of the cube meter.

Is it because of the FW or because of the DAQ ?

- Each time problem on different DIFs, works on the other
- After several attempt, it work most of the time when it's not a LDA channel problem

II. CALICE DAQ v.2

Readout

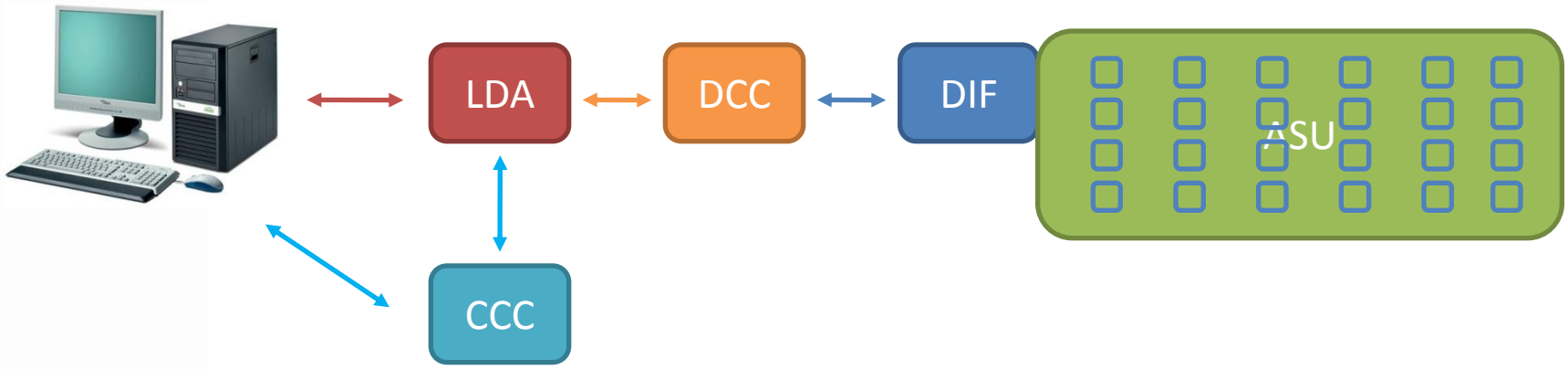


We experienced some data corrupted
Is it because of the FW or because of the DAQ ?

- LDA is suspected

II. CALICE DAQ v.2

BUG experienced

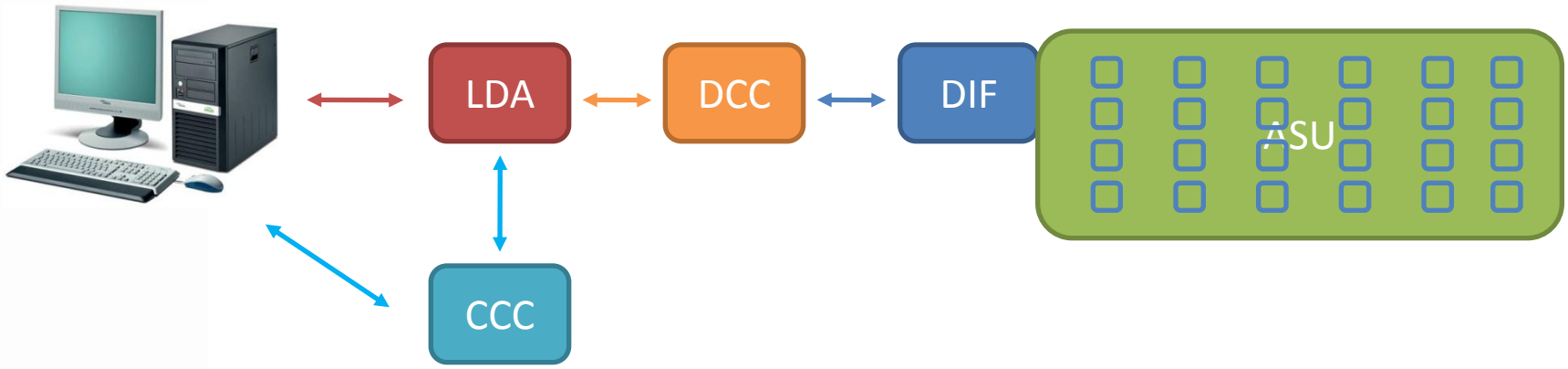


- Reset not active
- Data frame at 0, chip reset too short ?
- Power Pulsing not functional

Evolutions work on test bench at lab, but not in beam test…

II. CALICE DAQ v.2

BUSY / RAMFULL

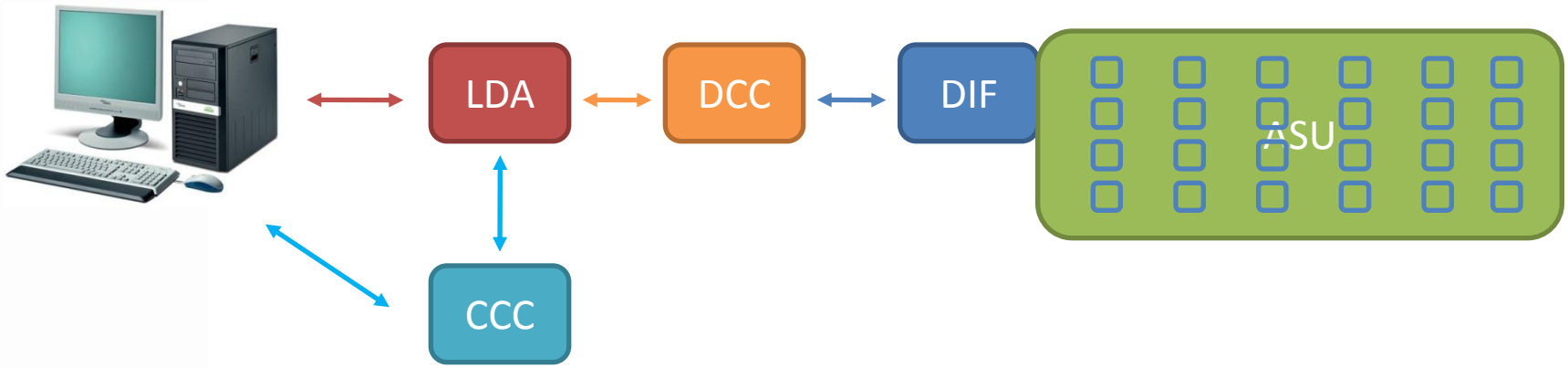


- No busy when the chip memory are being erased
- Busy directly link to ramfull signal (that means ramfull signal change when there is a SC, then commands are sent by the CCC)
- No differentiation between busy / ramfull
- Use of 2 different clocks to differentiate active and inactive busy

The system will be easier to manage with another CCC system

II. CALICE DAQ v.2

CCC

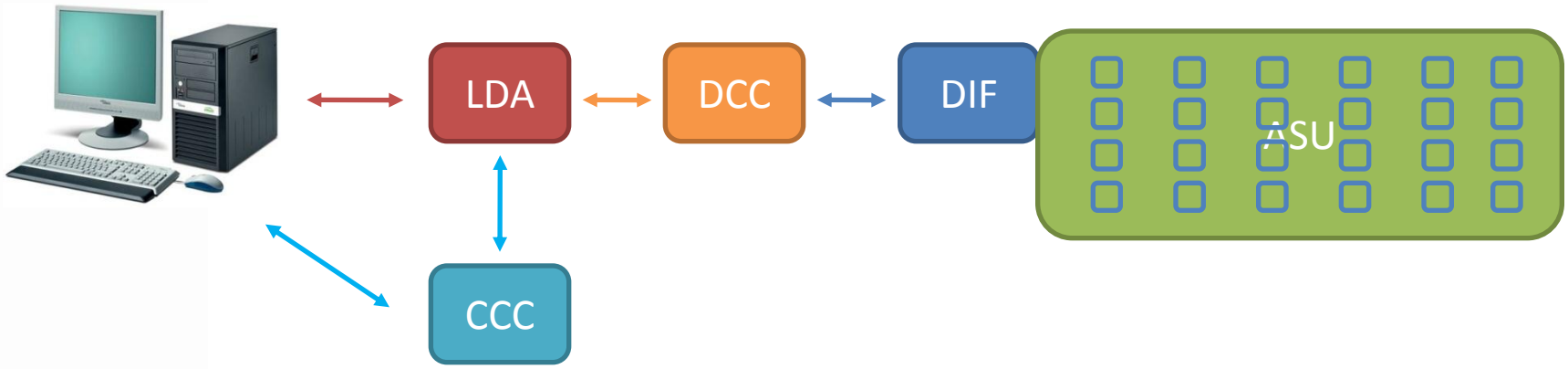


- Need to know when it can send a ramfull or start acq command (no filter for the moment, problem of ramfull during SC)
- No space to develop PP feature

Need a bigger FPGA

II. CALICE DAQ v.2

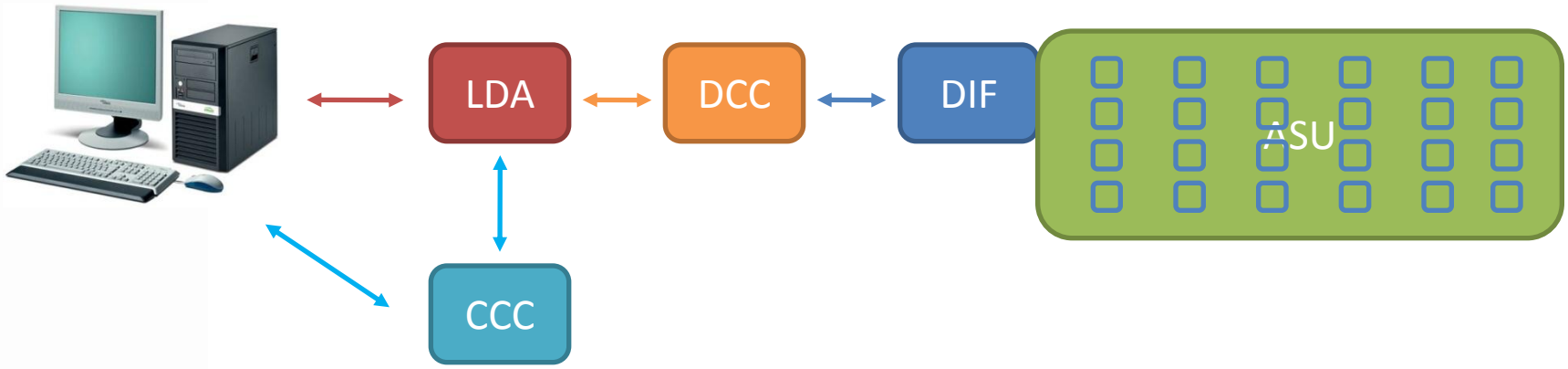
MICROROC



- Tested at LAPP and working with RPC on the same DCC
- didn’t work on beam test

II. CALICE DAQ v.2

No test bench, No work…



We can’t work without a complete test bench in each lab !!!!!!!!!

No RPC detector at lapp …