# Prototype of TRACE digitizers
# &
# GTS Upgrade

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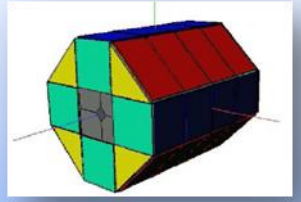
**EGAN Working Group Meeting**

June 28 2012, Orsay

# Outlines

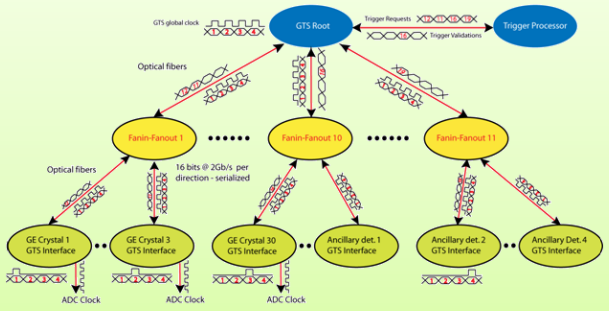
## TRACE

- Multichannel ADC prototype
- Preliminary results



## Global Timing and Synchronization

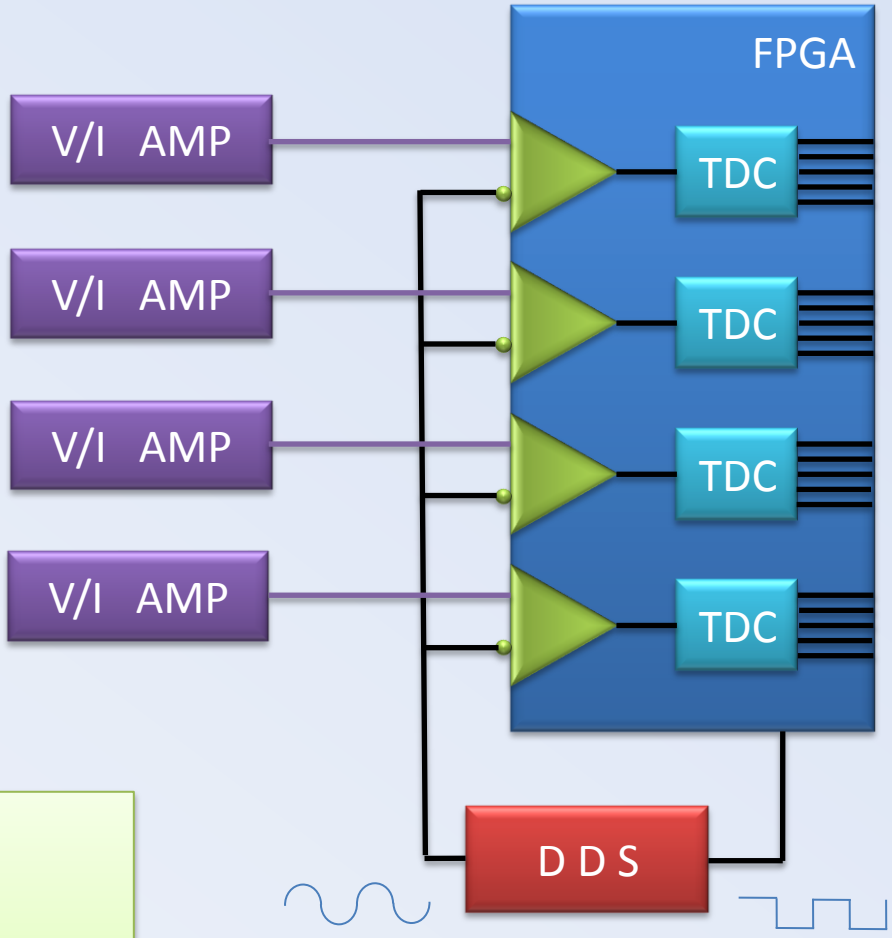
- Upgrade of the GTS firmware
  - Multiple trigger requests
  - Timestamp assignment latency
- Preliminary tests

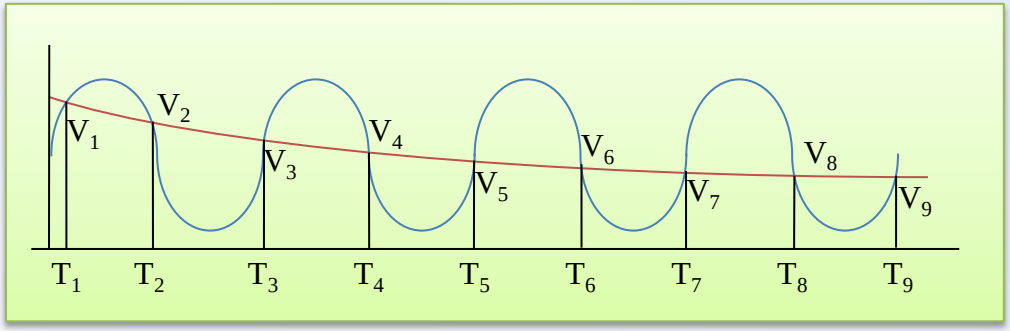


# Multichannel ADC

# FPGA as ADC

- From PA directly to FPGA differential inputs
- External digital synthesizer used to produce a $V_{REF}$ sinusoid
- TDCs measure time differences further converted to voltage




High integration?

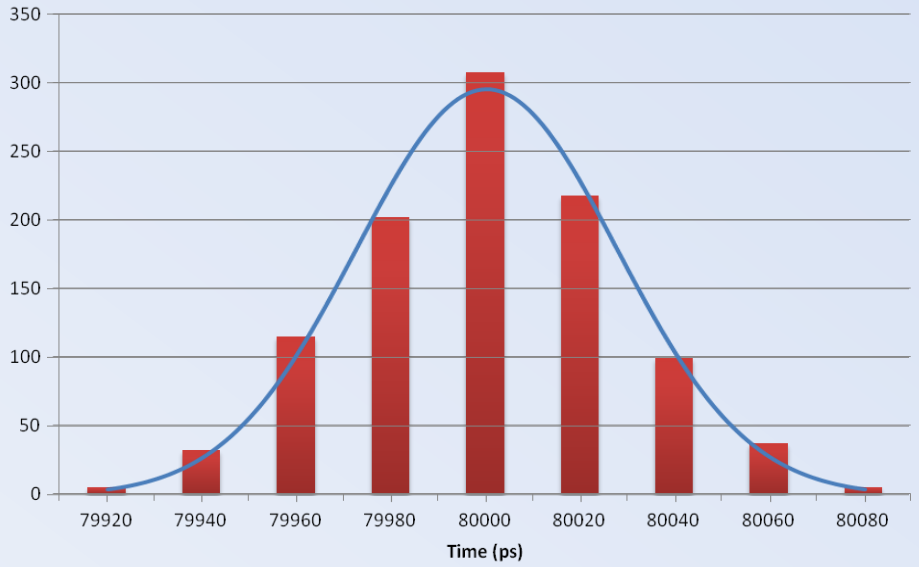
# TDC Core

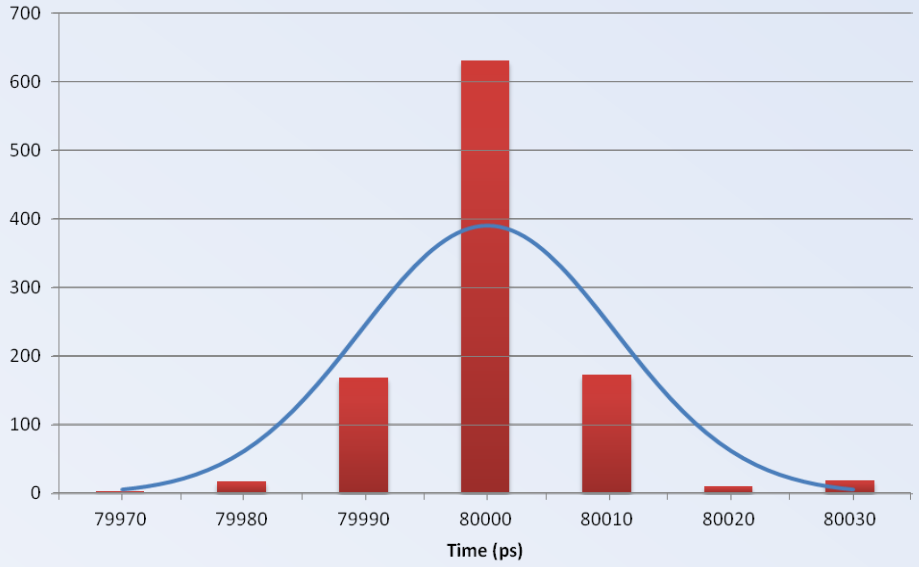
| | |
|---|---|
| Clock freq | 125-250 MHz |
| Course counter | up to 134 ms |
| Carry chain | 816 elements |
| Rearm time | 3 cycles |
| Startup calib | histogram |
| Online calib | ring oscillator |
| LSB | ~ 1 ps |
| Precision | ~ 30 ps rms |

Bubbles effect correction

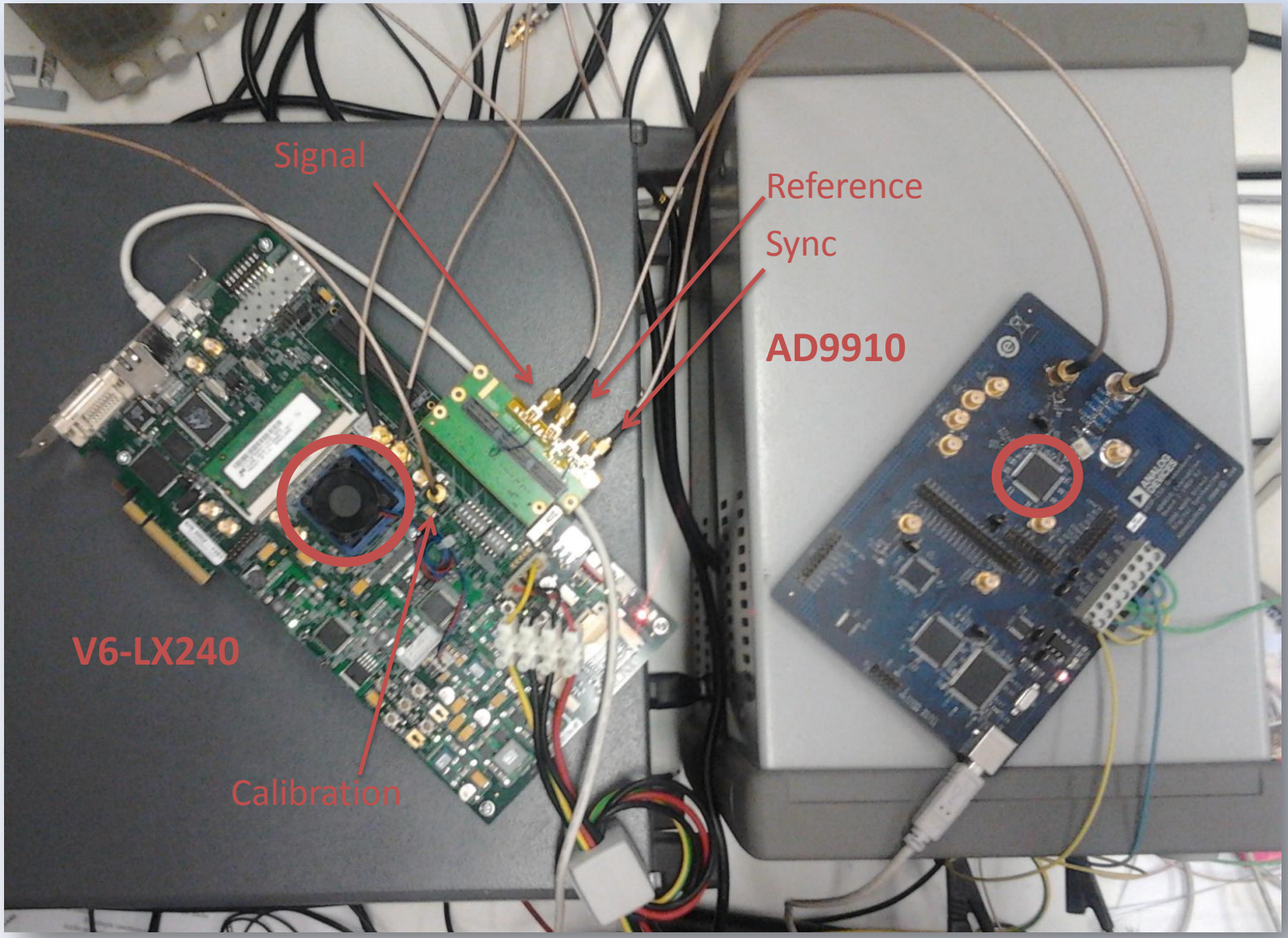
→

0000000000000000
1110000000000000
1111110100000000



# ADC Prototype



# Preliminary results

Non-uniform sampling

Non-uniform DFT

$$P(m) = \sum_{n=0}^{N-1} p_n e^{-j\frac{2\pi}{T} m t_n}$$

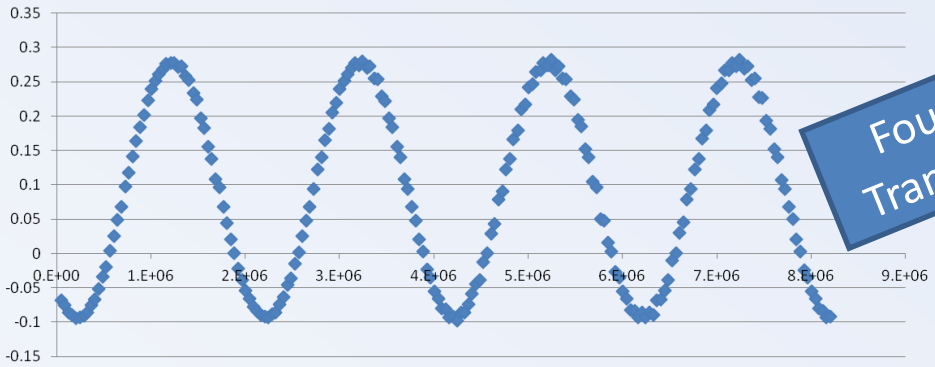
Interpolation & re-sampling

| tdc_chip Project Status (05/07/2012 - 17:49:42) | | | |
|---|---|---|---|
| **Project File:** | adc_test.xise | **Parser Errors:** | No Errors |
| **Module Name:** | tdc_chip | **Implementation State:** | Programming File Generated |
| **Target Device:** | xc6vlx240t-1ff1156 | **• Errors:** | No Errors |
| **Product Version:** | ISE 13.1 | **• Warnings:** | 43 Warnings (1 new) |
| **Design Goal:** | Balanced | **• Routing Results:** | All Signals Completely Routed |
| **Design Strategy:** | Xilinx Default (unlocked) | **• Timing Constraints:** | All Constraints Met |
| **Environment:** | System Settings | **• Final Timing Score:** | 0 (Timing Report) |

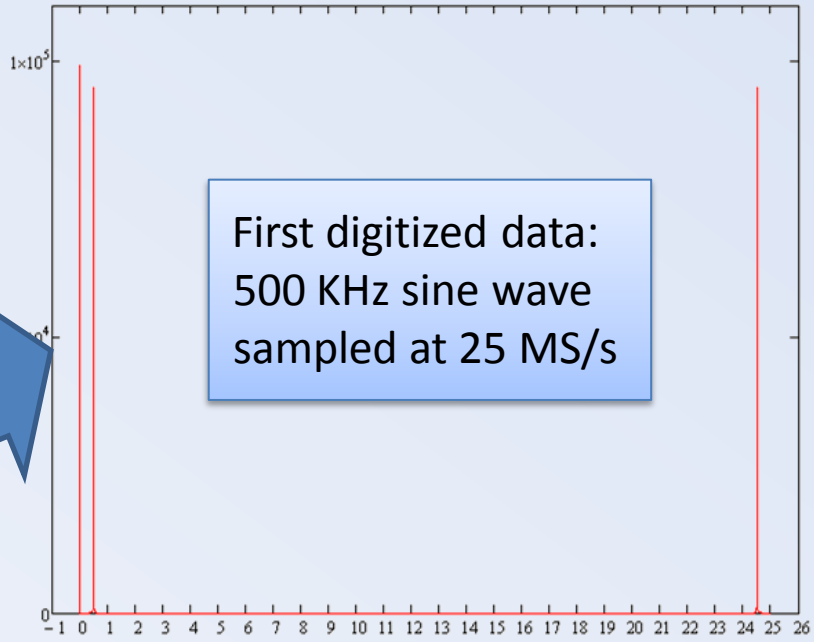
**Current Warnings** [+]

**Device Utilization Summary** [-]

| Slice Logic Utilization | Used | Available | Utilization | Note(s) |
|---|---|---|---|---|
| Number of Slice Registers | 2,744 | 301,440 | 1% | |
| Number used as Flip Flops | 2,743 | | | |
| Number used as Latches | 1 | | | |
| Number used as Latch-thrus | 0 | | | |
| Number used as AND/OR logics | 0 | | | |
| Number of Slice LUTs | 2,734 | 150,720 | 1% | |
| Number used as logic | 2,253 | 150,720 | 1% | |
| Number using O6 output only | 1,173 | | | |
| Number using O5 output only | 111 | | | |




Fourier Transform




First digitized data:
500 KHz sine wave
sampled at 25 MS/s

LVDS inputs coupling → different input standards

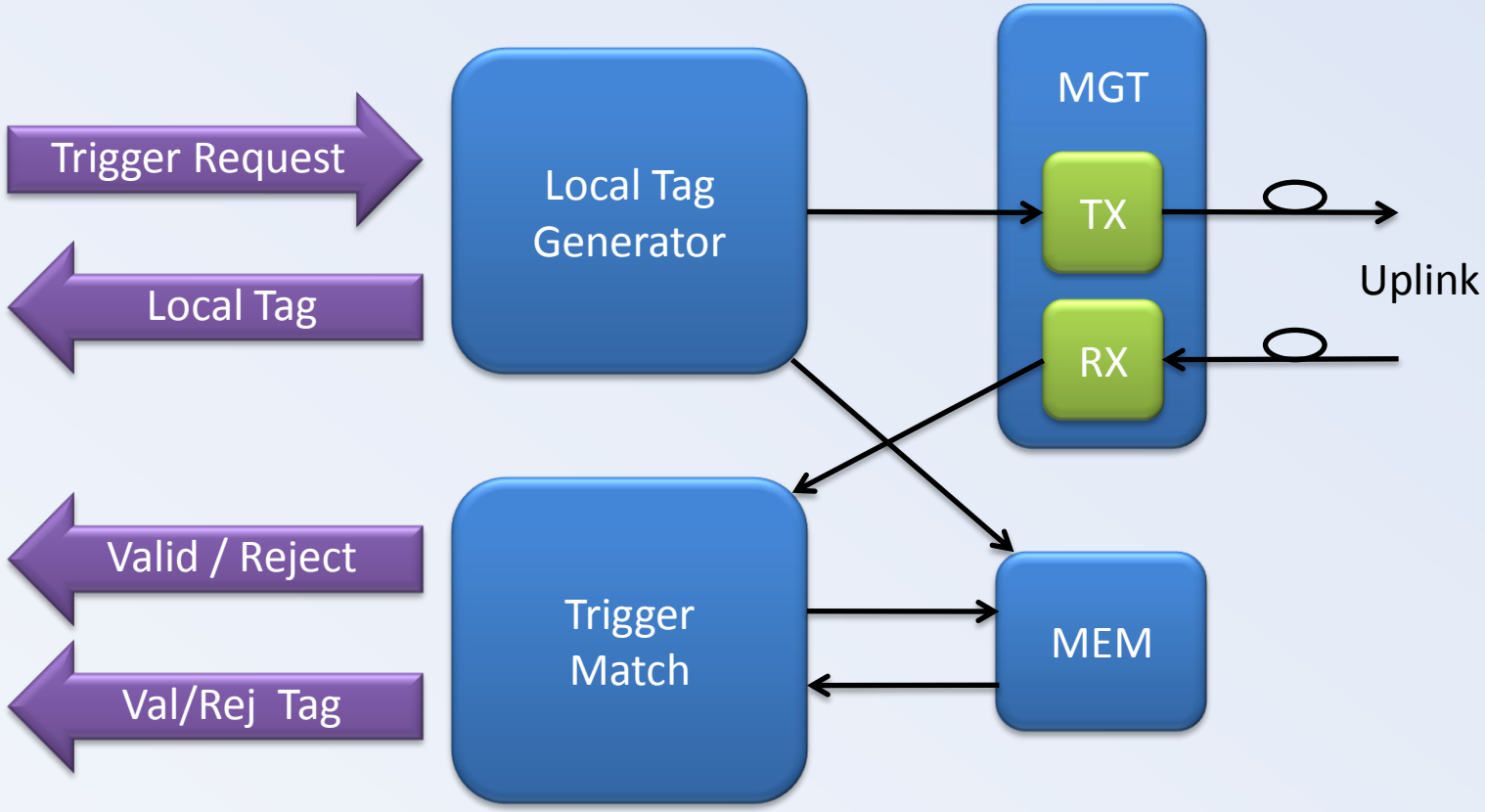
Phase jitter (sine/triangular wave) → OCXO 50ppb

# GTS Upgrade

# GTS: Functionalities

- Common clock
- Global clock counter
- Global event counter
- Trigger requests
- Error reports

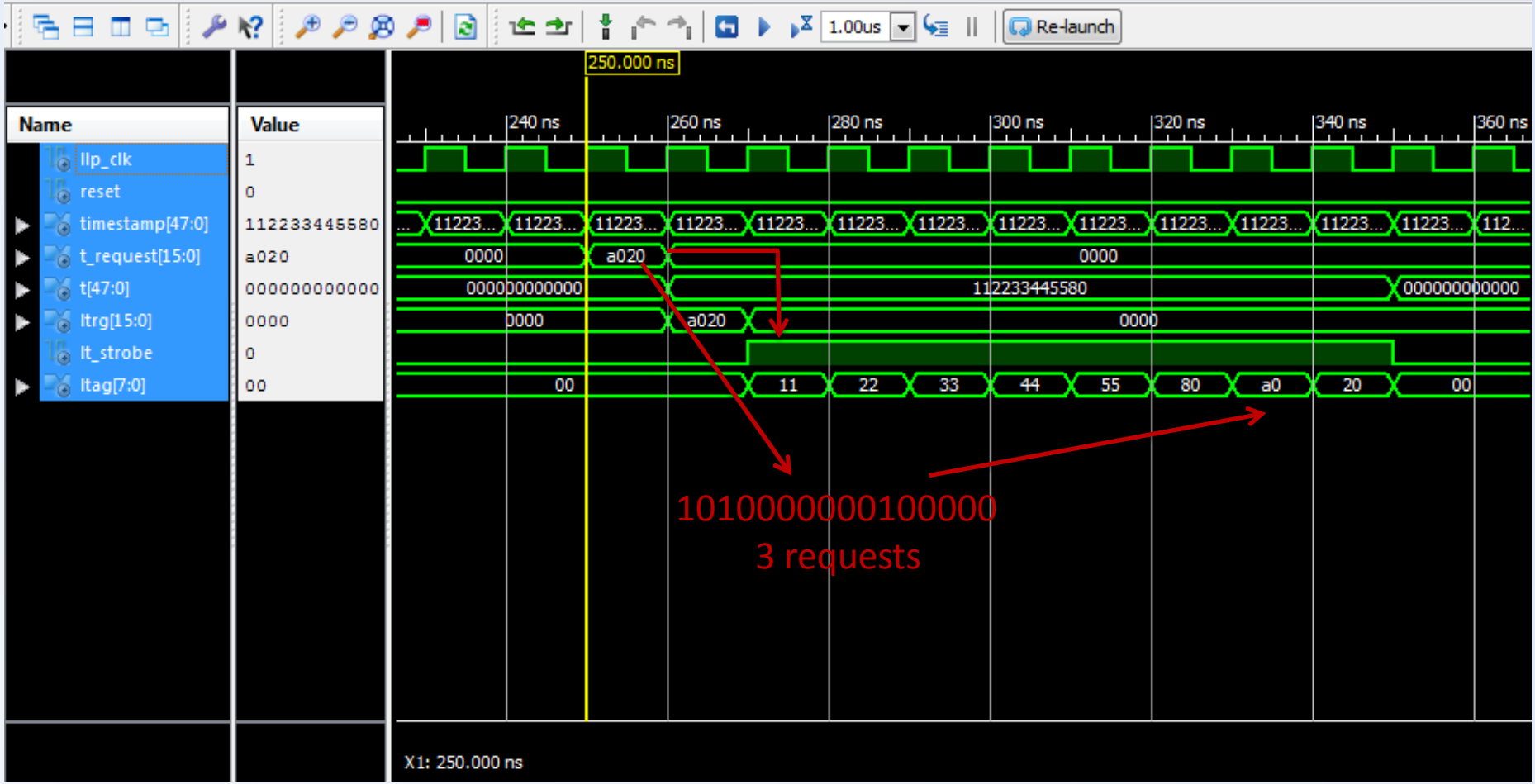
- Trigger controls:
  - Throttling of the L1 validation signal
  - Fast commands (fast reset, initialization, etc.)
  - Fast monitoring feedback from the crystals
  - Calibration and test trigger sequence commands
  - Monitor of dead time



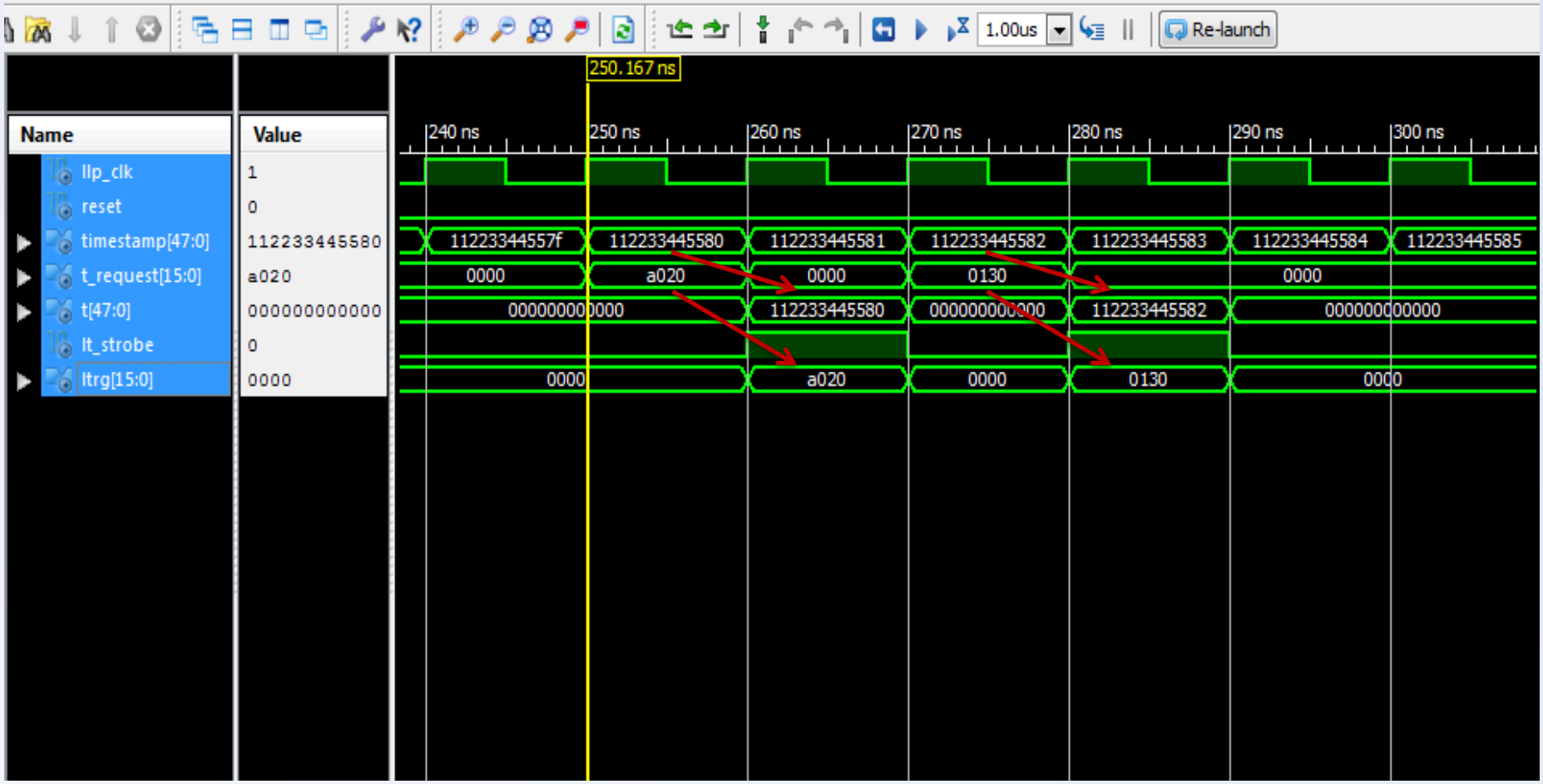
# GTS: Current Limits

- Serves just one trigger request → Interface for 16
  Parameterized with GENERICs
- Handles just one ID request → 16 ID per GTS core
  Parameterized with GENERICs

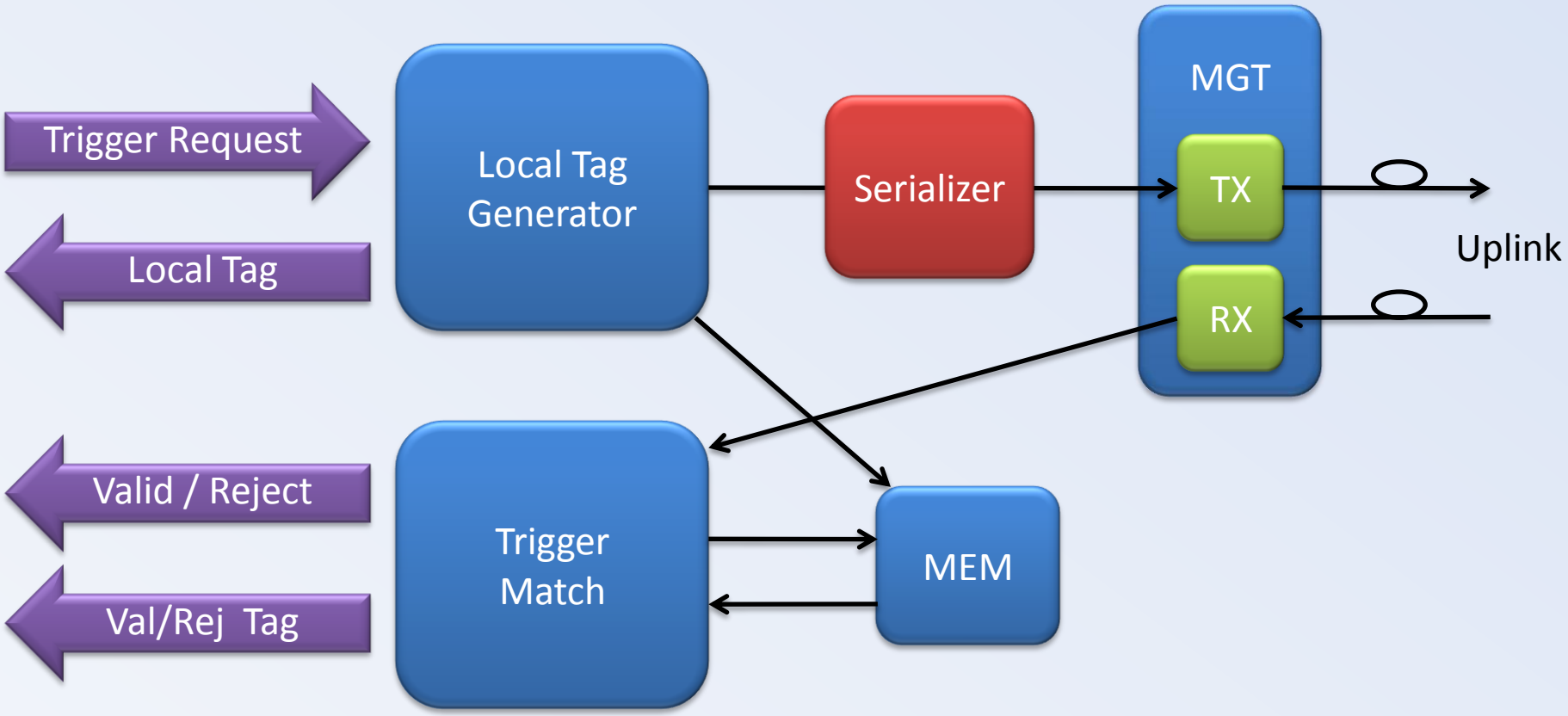
# Requests Interface (1)



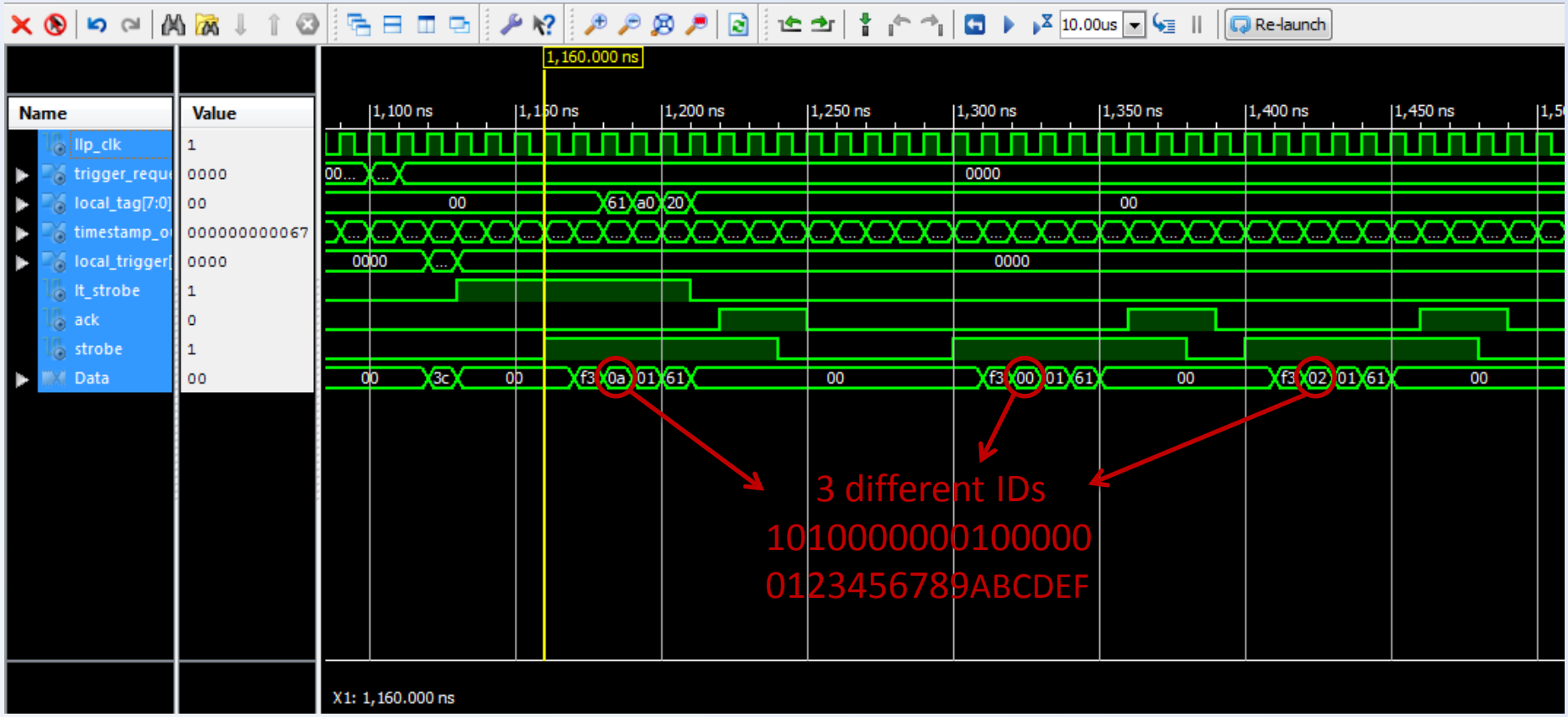
# Requests Interface (2)



# Requests Serializing



# Multiple ID Requests




START | LENGTH | TRIGGER ID | COMMAND ID | LOCAL TAG (7:0) | LOCAL TAG (15:8)

# Constraints

- Trigger IDs

256 trigger IDs
In triggerless mode (root node validates all)
Trigger processor limits the ID numbers to 40

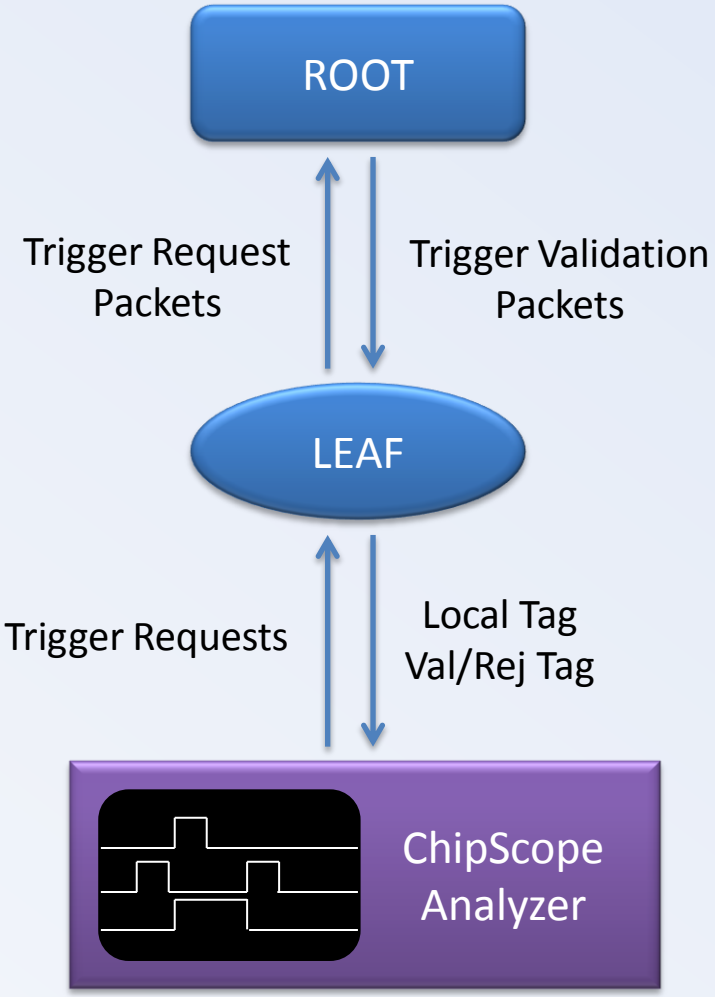
- Validations

The validation regards only local tag:

- Many trigger requests with the same local tag but different ID generate only one validation/rejection
- Complainant with the old GTS

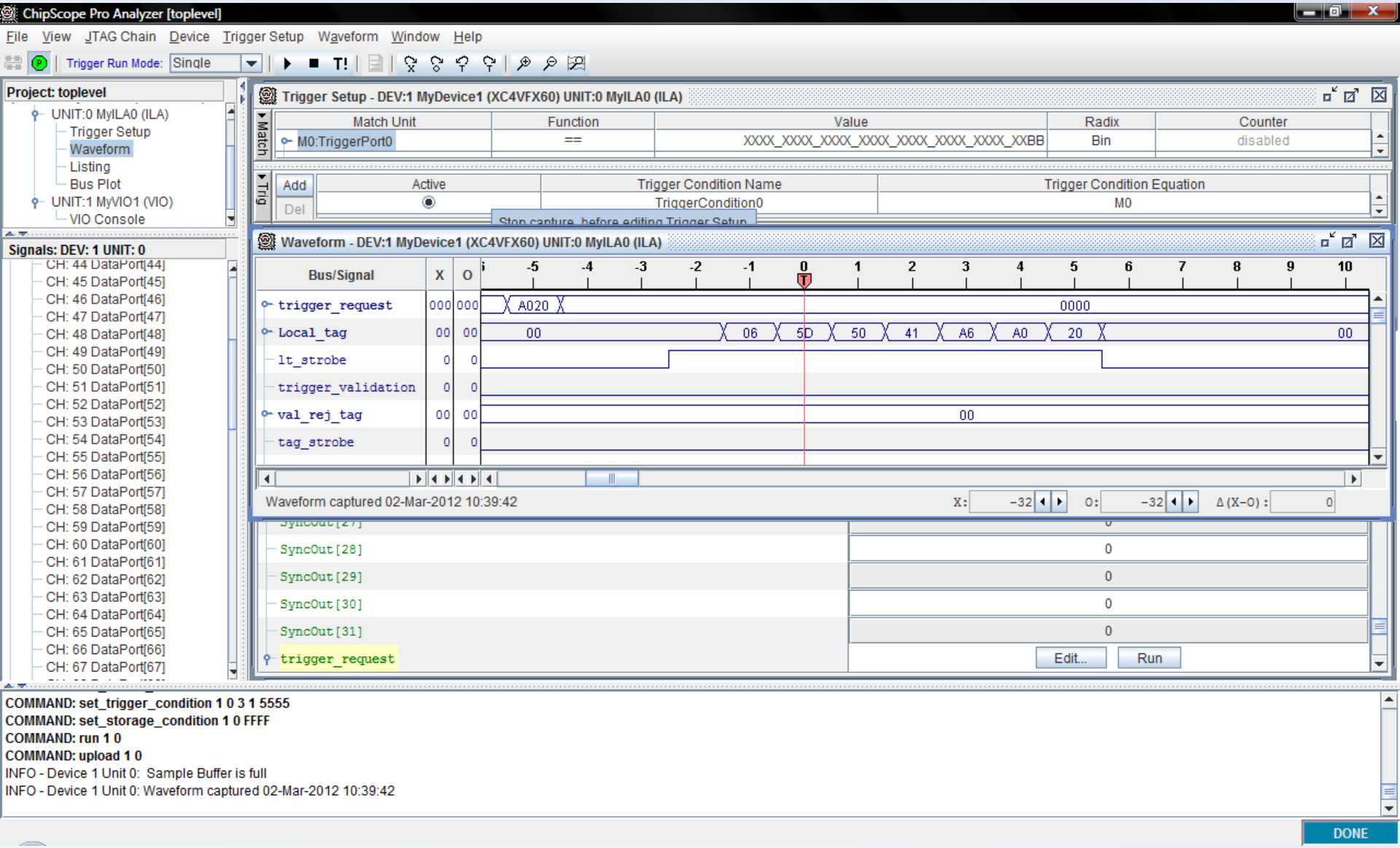
# Backup

# Test bench

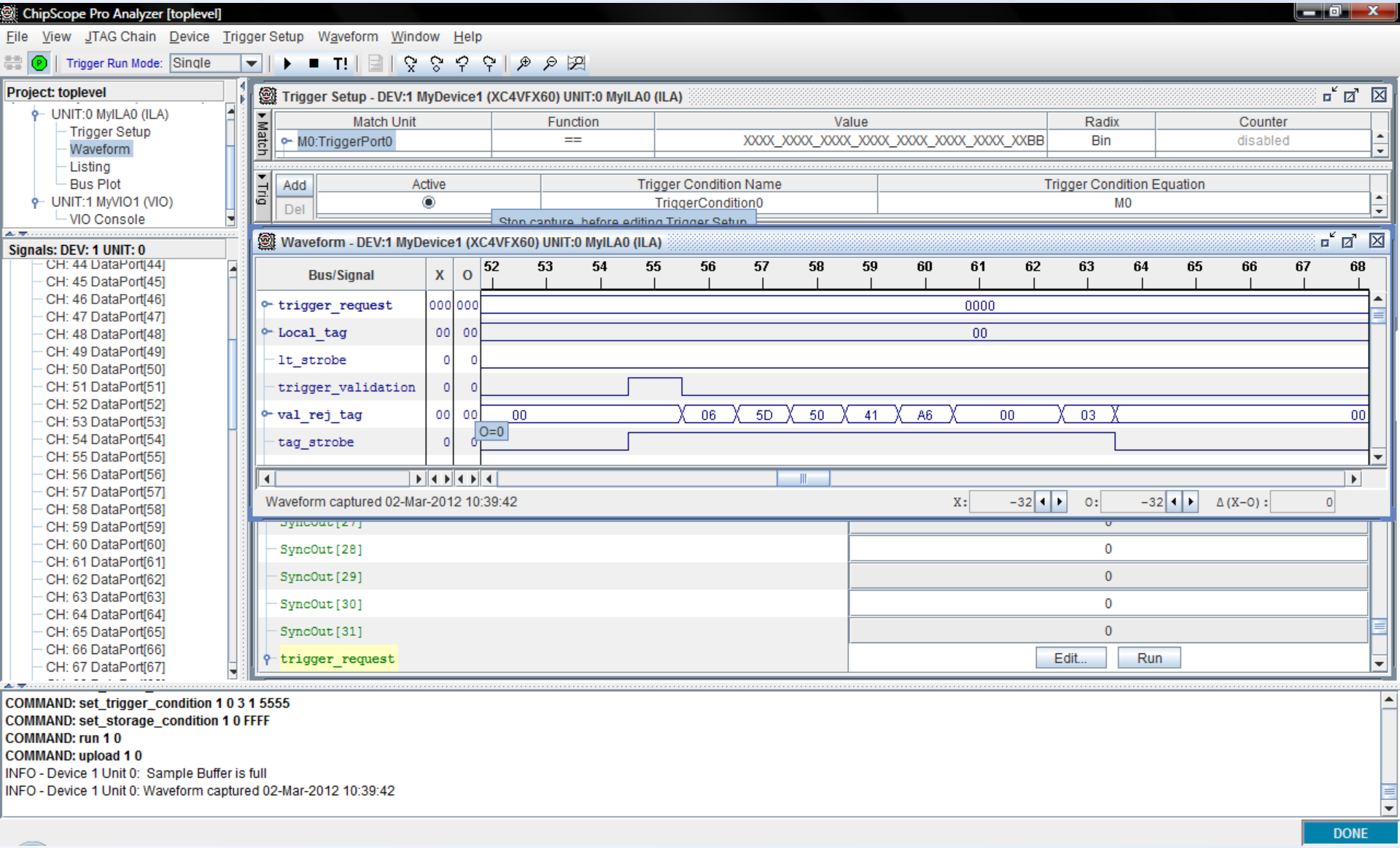



- Implemented on a GTS mezzanine (V4)
- Point to point connection
- Root node validates every request

# Test bench


ChipScope Pro Analyzer [toplevel]
File View JTAG Chain Device Trigger Setup Waveform Window Help
Trigger Run Mode: Single
Project: toplevel
UNIT:0 MyILA0 (ILA)
Trigger Setup
Waveform
Listing
Bus Plot
UNIT:1 MyVIO1 (VIO)
VIO Console
Signals: DEV: 1 UNIT: 0
CH: 45 DataPort[45]
CH: 46 DataPort[46]
CH: 47 DataPort[47]
CH: 48 DataPort[48]
CH: 49 DataPort[49]
CH: 50 DataPort[50]
CH: 51 DataPort[51]
CH: 52 DataPort[52]
CH: 53 DataPort[53]
CH: 54 DataPort[54]
CH: 55 DataPort[55]
CH: 56 DataPort[56]
CH: 57 DataPort[57]
CH: 58 DataPort[58]
CH: 59 DataPort[59]
CH: 60 DataPort[60]
CH: 61 DataPort[61]
CH: 62 DataPort[62]
CH: 63 DataPort[63]
CH: 64 DataPort[64]
CH: 65 DataPort[65]
CH: 66 DataPort[66]
CH: 67 DataPort[67]
Trigger Setup - DEV:1 MyDevice1 (XC4VFX60) UNIT:0 MyILA0 (ILA)
Match
Match Unit
Function
Value
Radix
Counter
M0:TriggerPort0
==
XXXX_XXXX_XXXX_XXXX_XXXX_XXXX_XXXX_XXBB
Bin
disabled
Trig
Add
Del
Active
Trigger Condition Name
Trigger Condition Equation
TriggerCondition0
M0
Stop capture before editing Trigger Setup
Waveform - DEV:1 MyDevice1 (XC4VFX60) UNIT:0 MyILA0 (ILA)
Bus/Signal
X
O
-5 -4 -3 -2 -1 0 1 2 3 4 5 6 7 8 9 10
trigger_request
Local_tag
lt_strobe
trigger_validation
val_rej_tag
tag_strobe
A020
0000
00
06
5D
50
41
A6
A0
20
Waveform captured 02-Mar-2012 10:39:42
X: -32
O: -32
Δ (X-O) : 0
SyncOut[28]
SyncOut[29]
SyncOut[30]
SyncOut[31]
trigger_request
Edit...
Run
COMMAND: set_trigger_condition 1 0 3 1 5555
COMMAND: set_storage_condition 1 0 FFFF
COMMAND: run 1 0
COMMAND: upload 1 0
INFO - Device 1 Unit 0: Sample Buffer is full
INFO - Device 1 Unit 0: Waveform captured 02-Mar-2012 10:39:42
DONE

# Test bench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VIO Console
Signals: DEV: 1 UNIT: 0
CH: 44 DataPort[44]
CH: 45 DataPort[45]
CH: 46 DataPort[46]
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CH: 49 DataPort[49]
CH: 50 DataPort[50]
CH: 51 DataPort[51]
CH: 52 DataPort[52]
CH: 53 DataPort[53]
CH: 54 DataPort[54]
CH: 55 DataPort[55]
CH: 56 DataPort[56]
CH: 57 DataPort[57]
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Trigger Setup - DEV:1 MyDevice1 (XC4VFX60) UNIT:0 MyILA0 (ILA)
Match
Match Unit
Function
Value
Radix
Counter
M0:TriggerPort0
==
XXXX_XXXX_XXXX_XXXX_XXXX_XXXX_XXXX_XXBB
Bin
disabled
Trig
Add
Del
Active
Trigger Condition Name
Trigger Condition Equation
TriggerCondition0
M0
Stop capture before editing Trigger Setup
Waveform - DEV:1 MyDevice1 (XC4VFX60) UNIT:0 MyILA0 (ILA)
Bus/Signal
X
O
52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68
trigger_request
Local_tag
lt_strobe
trigger_validation
val_rej_tag
tag_strobe
0000
00
00 06 5D 50 41 A6 00 03 00
O=0
Waveform captured 02-Mar-2012 10:39:42
X: -32
O: -32
Δ (X-O) : 0
SyncOut[28]
SyncOut[29]
SyncOut[30]
SyncOut[31]
trigger_request
Edit...
Run
COMMAND: set_trigger_condition 1 0 3 1 5555
COMMAND: set_storage_condition 1 0 FFFF
COMMAND: run 1 0
COMMAND: upload 1 0
INFO - Device 1 Unit 0: Sample Buffer is full
INFO - Device 1 Unit 0: Waveform captured 02-Mar-2012 10:39:42
DONE

# Conclusions

## Achieved & Expected Activities

- New Firmware — √ simulation & implementation (ChipS)
- Test bench on a small tree — o ongoing (trigger processor needed?)
- Test on a Numexo carrier