EDAQ for AIDA and LYCCA

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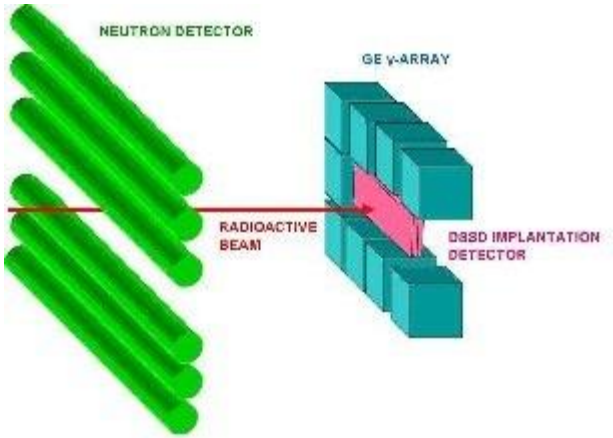
Overview

- What is AIDA
- What is LYCCA
- EDAQ for AIDA and LYCCA
- Interconnecting with other EDAQ

AIDA: introduction

Advanced Implantation Detector Array (AIDA)

UK collaboration: *University of Edinburgh, University of Liverpool, STFC Daresbury Laboratory & STFC Rutherford Appleton Laboratory*



- SuperFRS
- Exotic nuclei ~ 50 – 200MeV/u
- Implant – decay correlations
- Multi-GeV implantation events
- Subsequent low-energy decays
- Tag events for gamma and neutron detector arrays

Detector: multi-plane Si DSSD array
wafer thickness 1mm
8cm x 8cm (128x128 strips) *or* 24cm x 8cm (384x128 strips)

Instrumentation: ASIC
low noise (<12keV FWHM), low threshold (0.25% FSR)
20GeV FSR *plus* (20MeV FSR *or* 1GeV FSR)
fast overload recovery (~μs)
spectroscopy performance
time-stamping

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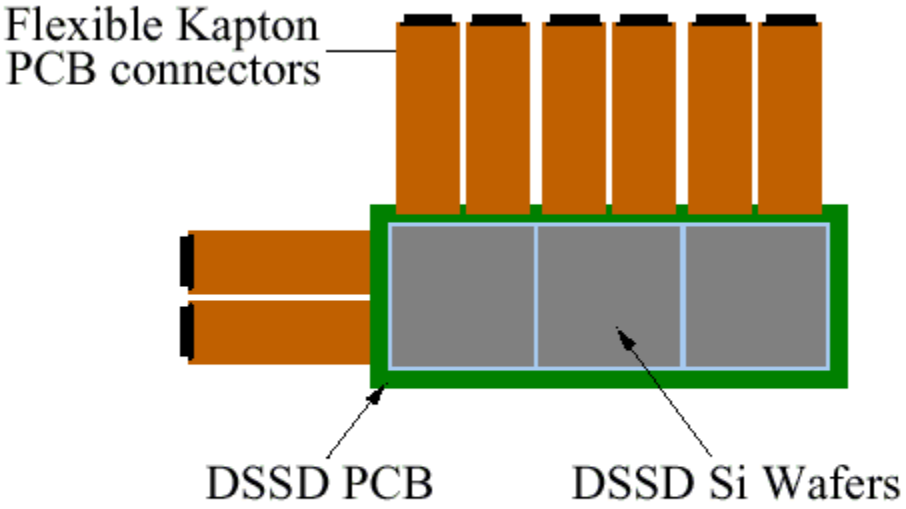
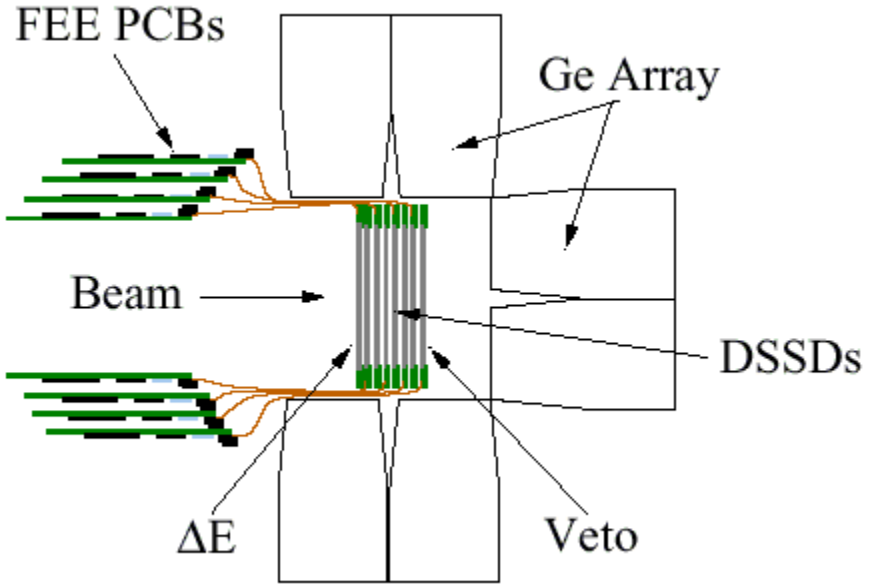
AIDA General Arrangement



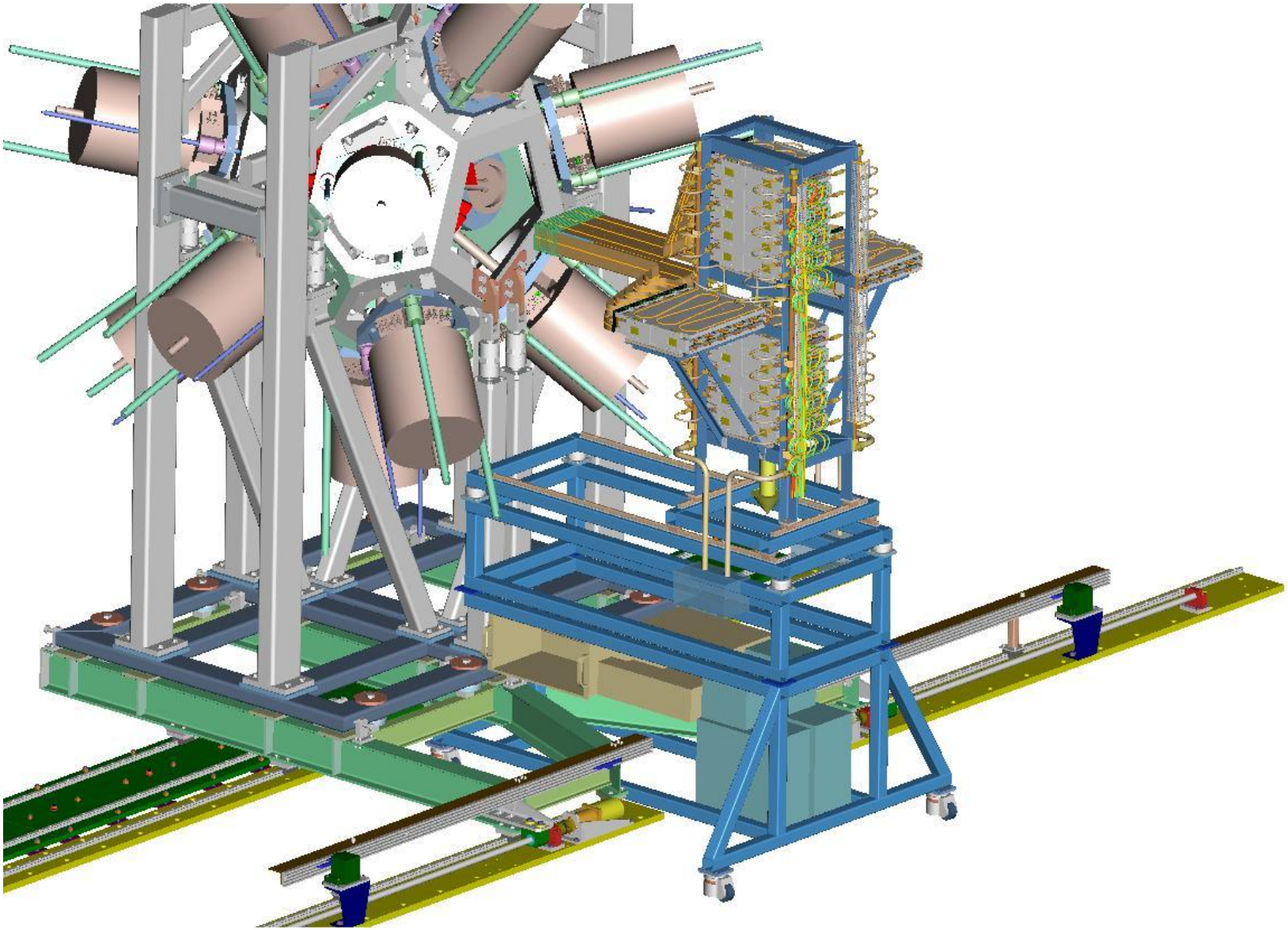


Implantation detector for RDT

Slide from Tom Davinson

2 Configurations: 8x8, 8x24cm

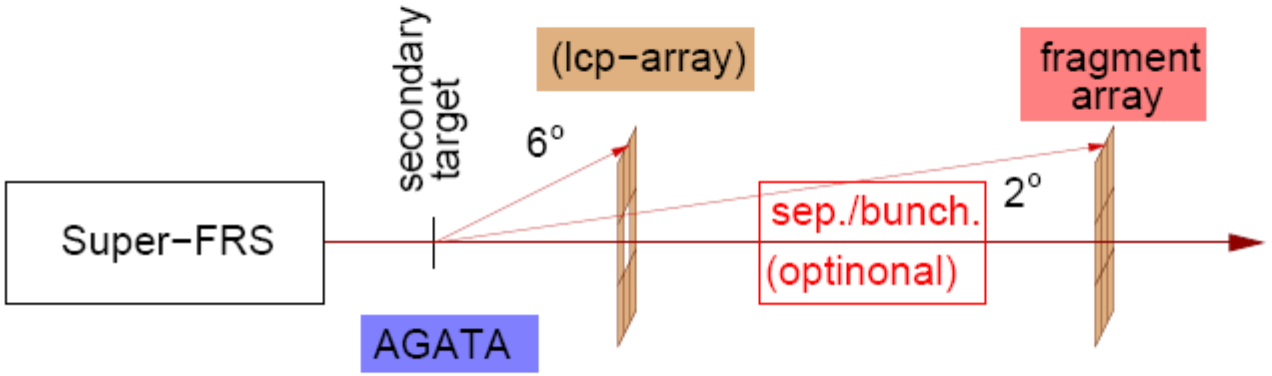
AIDA Mechanical



Lund−York−Cologne CAlorimeter (LYCCA)

Fragment identification after the secondary target

High−resolution fragment − gamma (− particle) spectroscopy



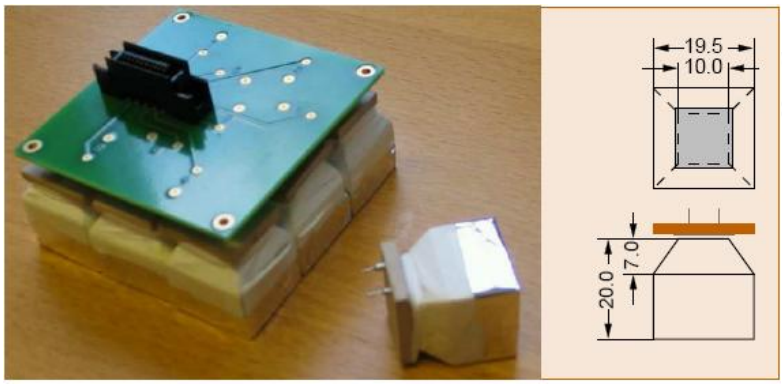
3 x 3 modules
hole in the center

5 x 3 mod. (wall)
8 x 2 mod. (f.p.)

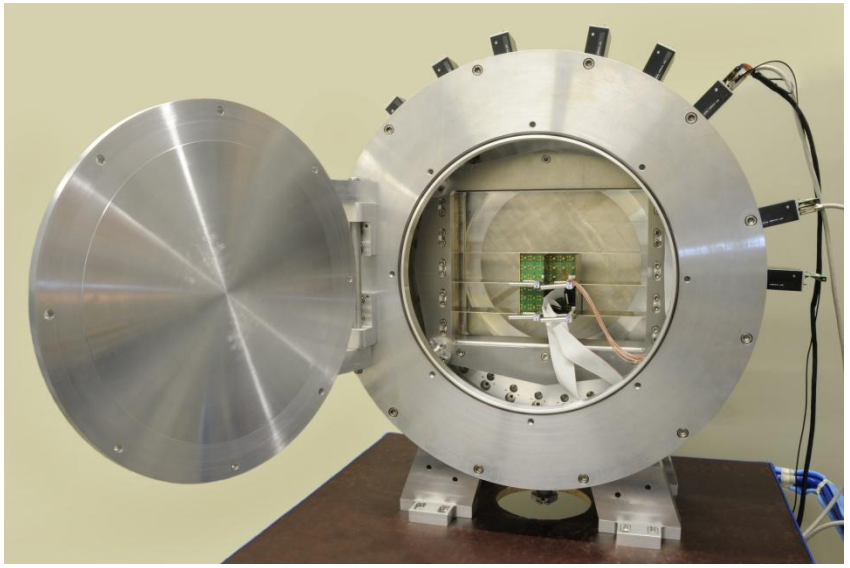
50−100 MeV/u range

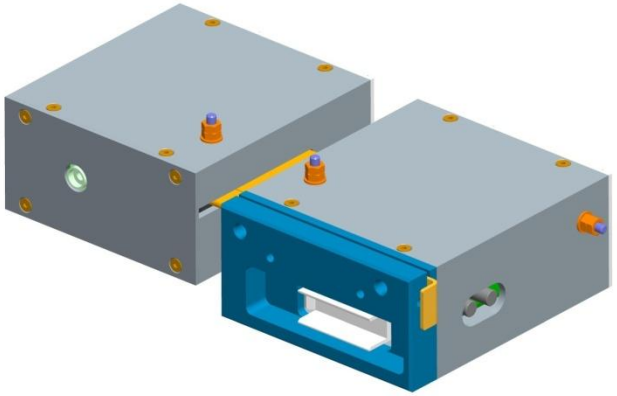
Distance secondary target − fragment array: ~3.5m

Modular.
CsI and DSSD
For E-dE



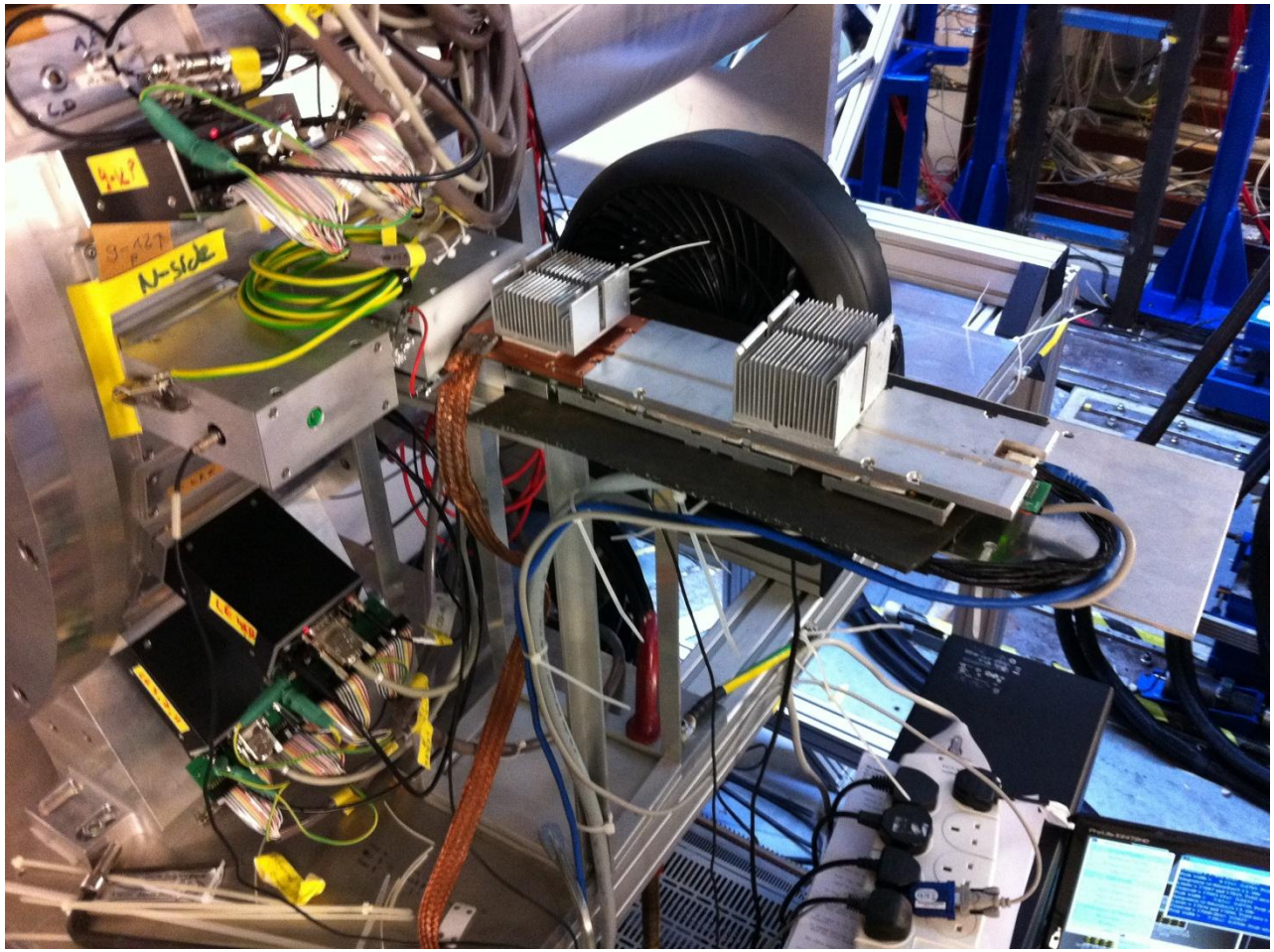
LYCCA





Initially Mesytec electronics
Later AIDA

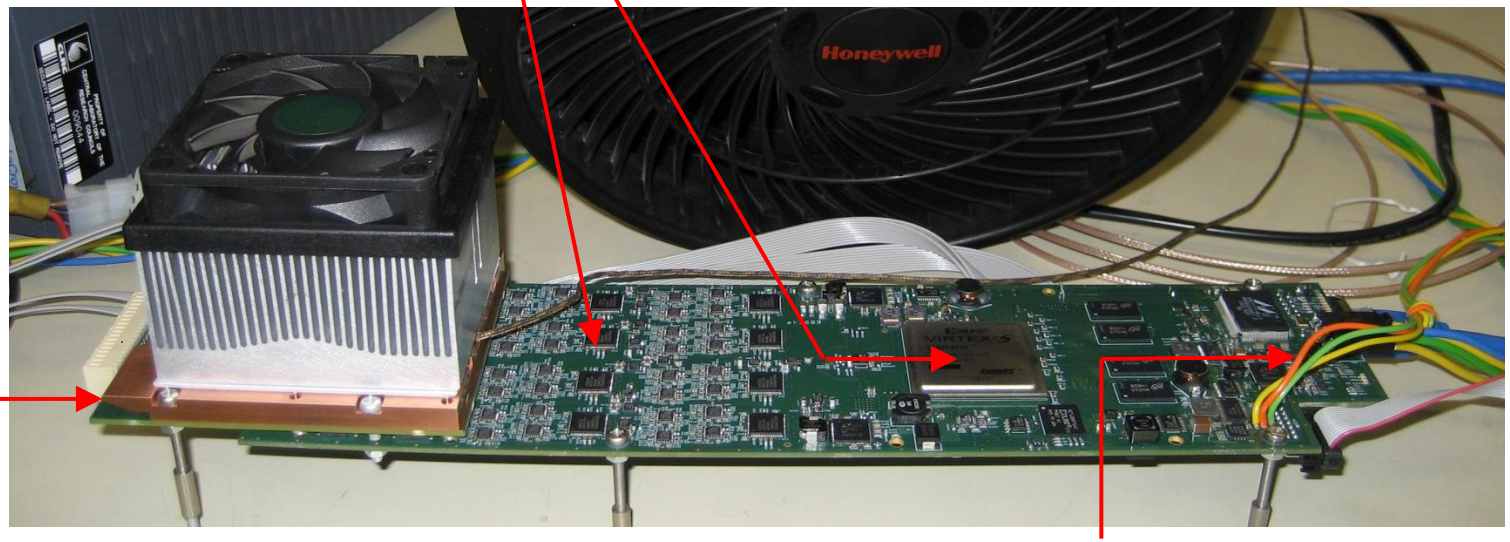
AIDA test on LYCCA (64 ch only)



AIDA FEE card (NUSTAR, DeSpec)

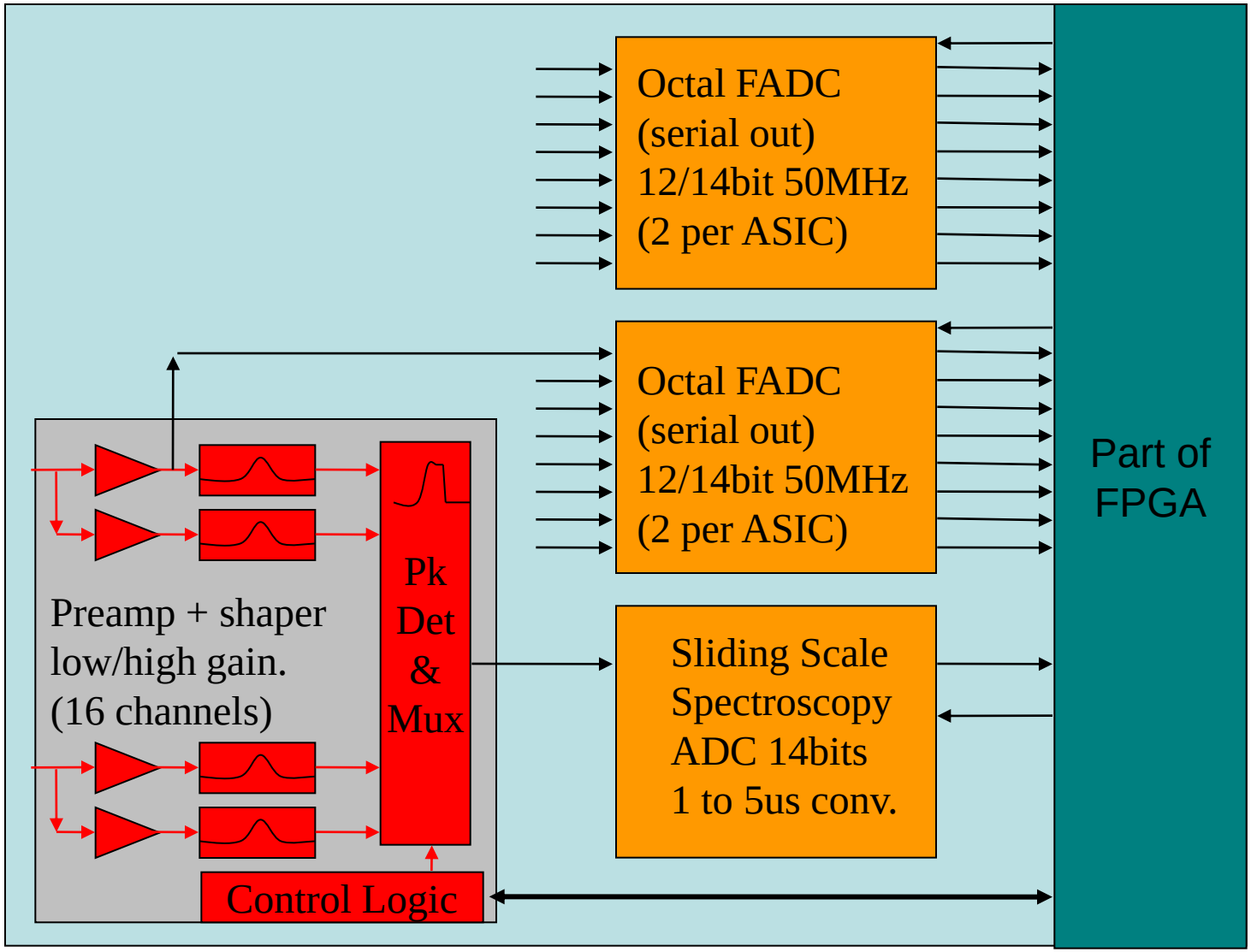
Mezzanine:
- 4x 16 channel ASICs
- Cu cover
  - EMI/RFI/light screen
  - cooling

FEE:
- 4x 16-bit ADC MUX readout (not visible)
- 8x octal 50MSPS 14-bit ADCs
- Xilinx Virtex 5 FPGA
  - PowerPC 40x CPU core/Linux OS – DAQ



FEE width: 8cm
Prototype – air cooling
Production – recirculating coolant

Gbit ethernet, clock, JTAG ports
Power



FEE for AIDA (NUSTAR, DeSpec)

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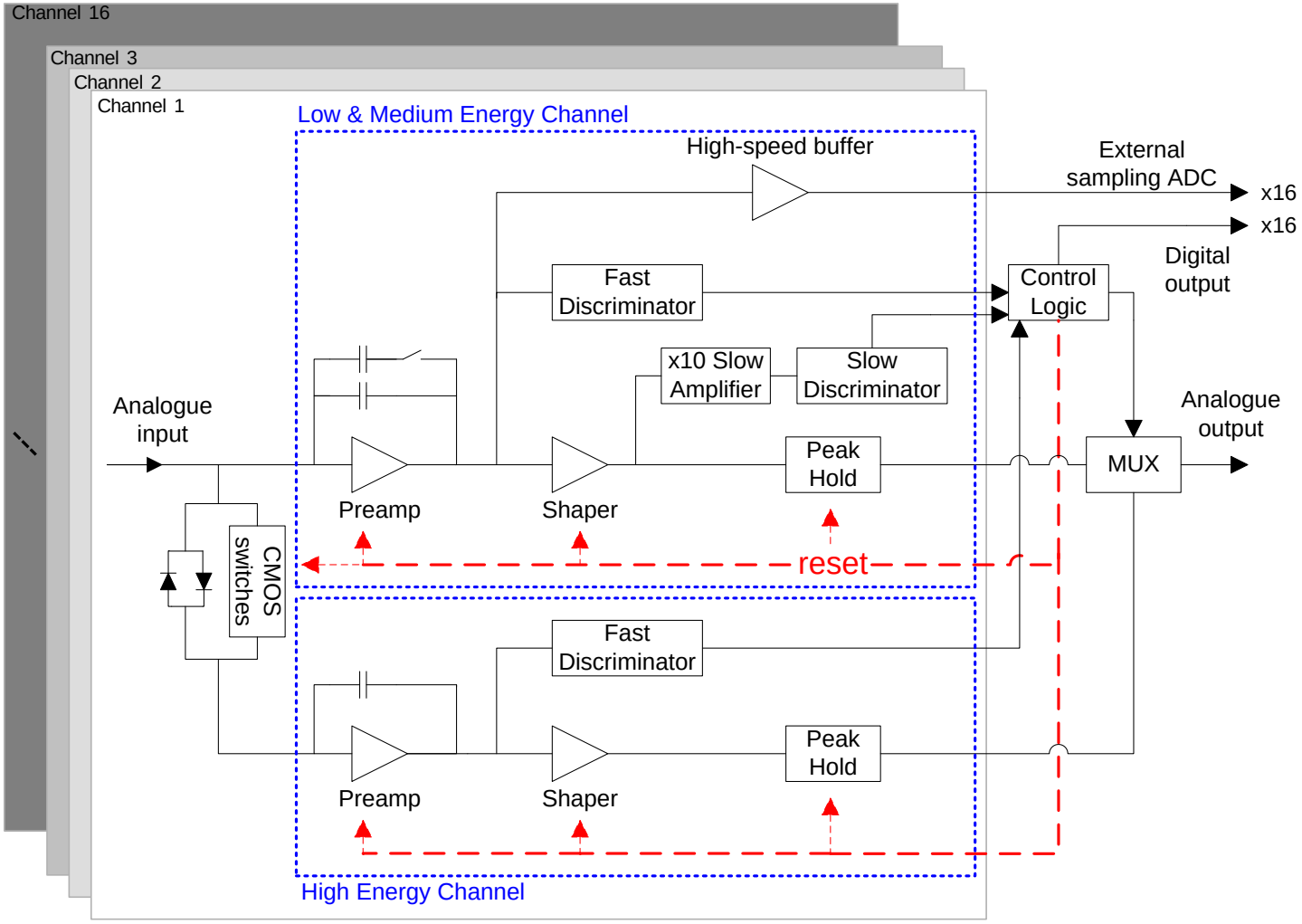
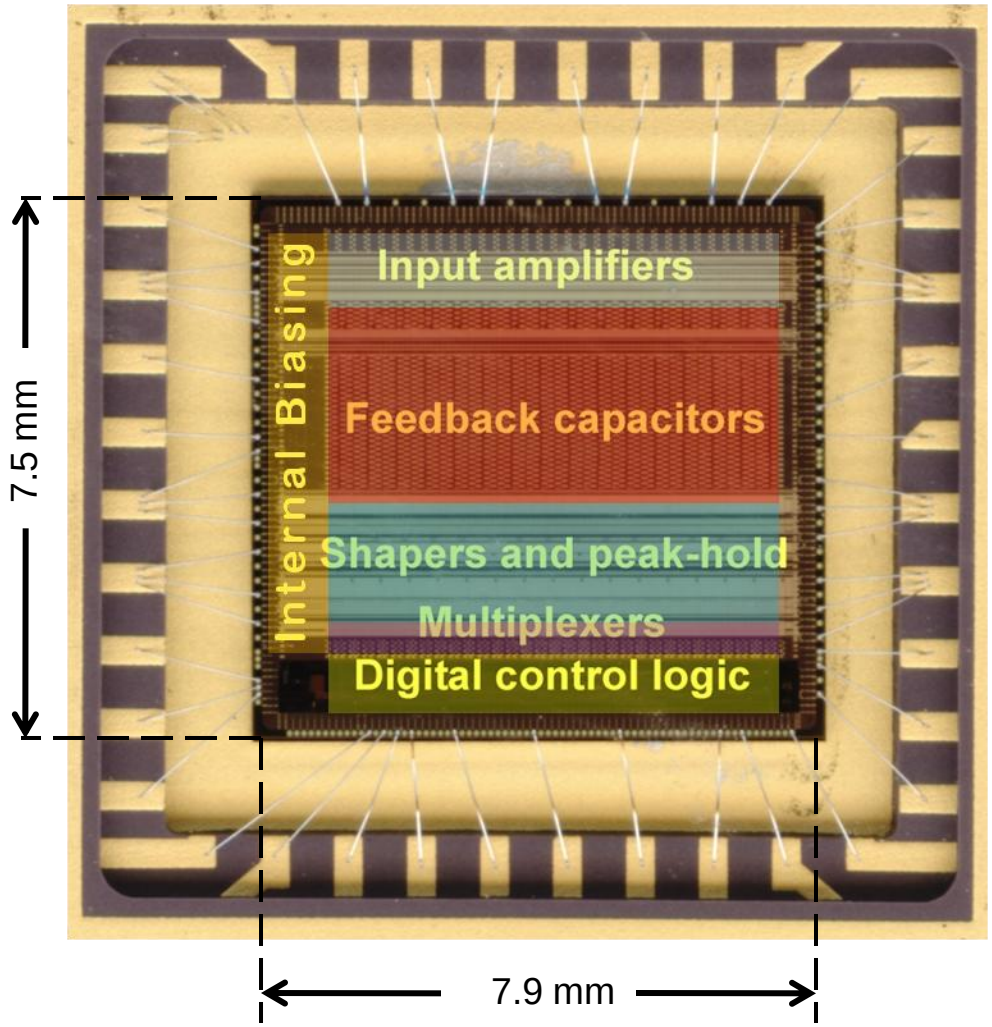
AIDA ASIC (NUSTAR)



Braga et al. 2009 IEEE NSS conf record, VOLS 1-5 P 1924-8

Layout

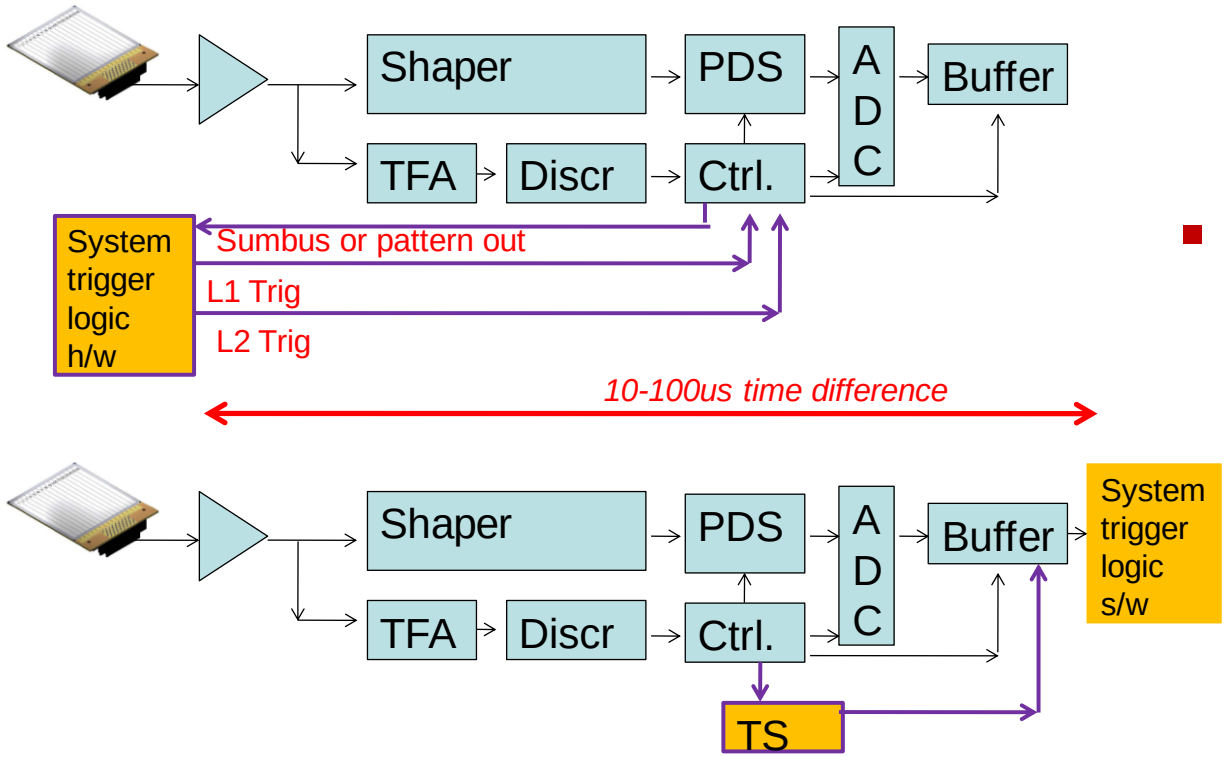


AIDA ASIC:

- 625um pitch
- 16 channels
- 2 channels/strip
- Mux'ed analogue output
- Direct digital output for external FADC
- 2 ranges: 0-20MeV/1GeV (switchable) and 0-20GeV (fixed)
- AMS 0.35um CMOS

Connecting new TS software triggered systems to existing systems

Legacy equipment usually needs an early coincidence trigger. But TS software trigger has latency. There are 2 solutions:



- *Run independently with common scalers*
- *Add extra "compatibility" output.*

How to solve the problem

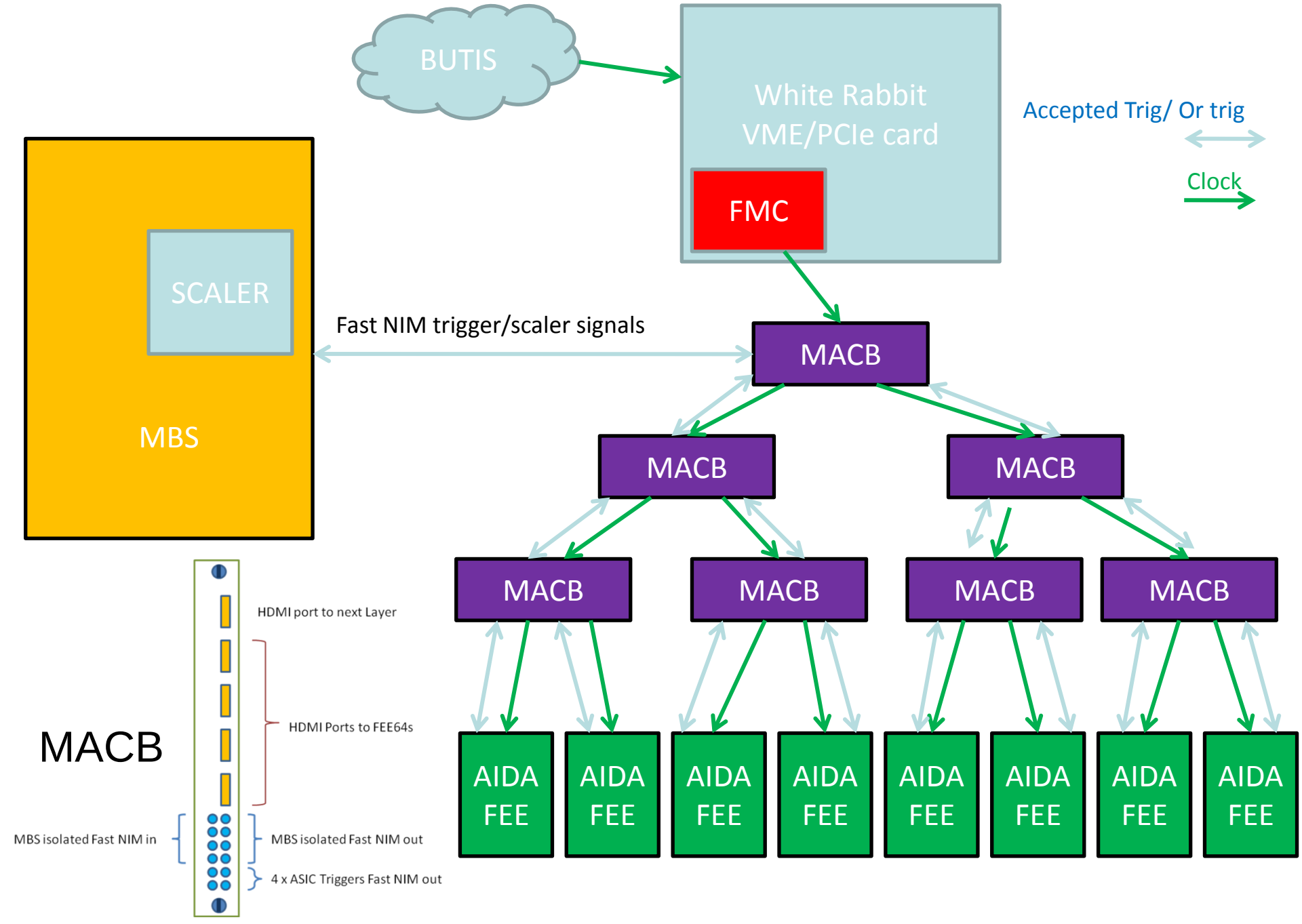
- Solutions(1):
  - Standardise on either hardware triggered or free-running systems?
    - Many reasons why we can't do this:
      - Even NUSTAR isn't all new build- legacy equipment
      - Needs investment of effort and money
      - Why change what works? (People like what they have; need a good reason to change, not just "progress".)
      - Free running users like running with no dead time and don't want to go back to hardware triggered systems

How to solve the problem

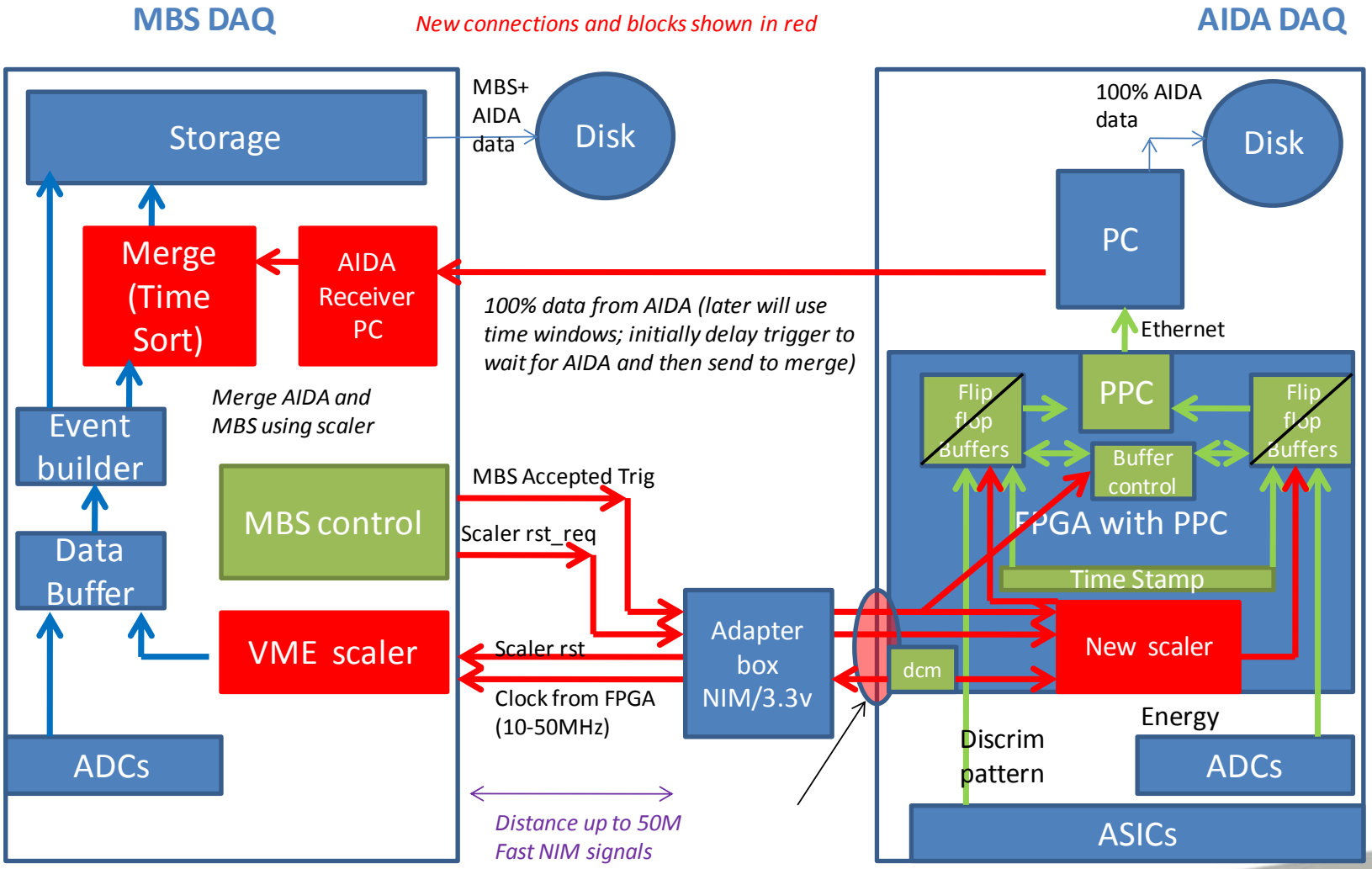
- Solutions(2):
  - Modify free-running DAQ systems to generate early information
    - More connections (1 per channel/ASIC/Si ladder)
    - More cost
    - More complexity
    - Grounding needs care or isolation

How to solve the problem

- Solutions(3):
  - Modify hardware triggered systems to share common scaler/clock with free running DAQ
    - Extra connection (but only 1 set per system)
    - Small cost
    - Small change to GUI and slow control
    - Grounding needs care or isolation
    - Few extra parameters in each event
    - Software trigger needs merge + common readout
    - No data reduction in triggered systems


BUTIS
White Rabbit
VME/PCIe card
FMC
Accepted Trig/ Or trig
Clock
SCALER
MBS
Fast NIM trigger/scaler signals
MACB
MACB
MACB
MACB
MACB
MACB
MACB
AIDA FEE
AIDA FEE
AIDA FEE
AIDA FEE
AIDA FEE
AIDA FEE
AIDA FEE
AIDA FEE
MACB
HDMI port to next Layer
HDMI Ports to FEE64s
MBS isolated Fast NIM in
MBS isolated Fast NIM out
4 x ASIC Triggers Fast NIM out

Conceptual design follows discussion between Ian , Nik and Stephane at GSI and discussion at DL between Vic, Patrick, Simon and Ian



Linked scalers to correlate 2 systems

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AIDA Status

- FEE cards built and tested (for AIDA and LYCCA)
- FEE including ASICs tested in beam
- Waiting for more beam
- DAQ working (tested in beam)
- VHDL improvements (using PSA option)
- MACB cards 1st batch built and tested