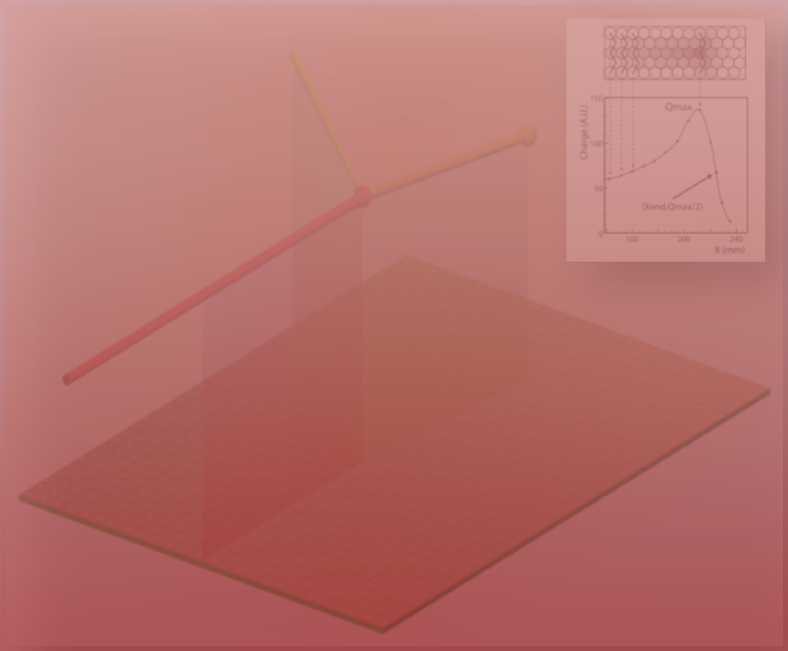

SUPPORTED BY
ANR
RIKEN
NiSHiNA
CENTER
Irfu
cea
saclay
NSCL
CENBG
GANIL
spiral2
laboratoire commun CEA/DSM - CNRS/IN2P3
GET
Emanuel Pollacco IRFU/SPhN
For the GET collaboration

GET Project Objectives

- Develop for Nucl. Physics :- Full Data Acquisition system for
  - Active Targets(Target = Gas). ➔ Nucl. Spec & Astrophys. with Radio active Beams
  - TPC ➔ Exotique Decay & EoS with RABs

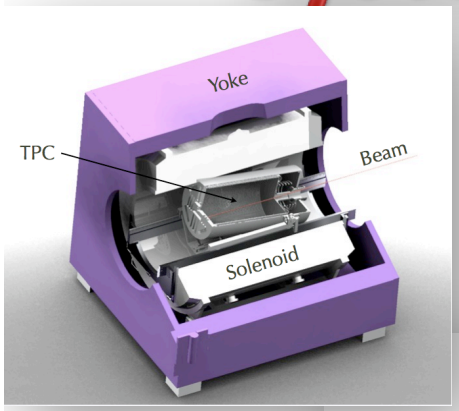
Require

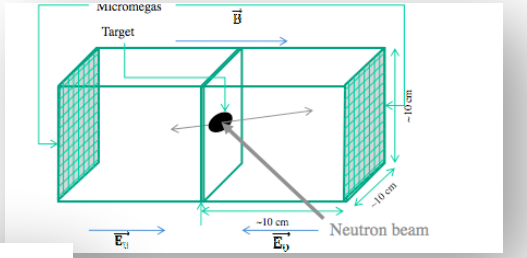
- Low detection thresholds (A,Z, E, The, Phi) for slow ions (below 300KeV),
- Dynamic range (~Z^2),
- High Luminosity & Solid Angle,
- Effective Internal TPC Trigger,
- Gas & pressure (H_2, D_2, ^3He, He …)
- Different detector Systems,
- Pad density (25-100 pads/cm^2)

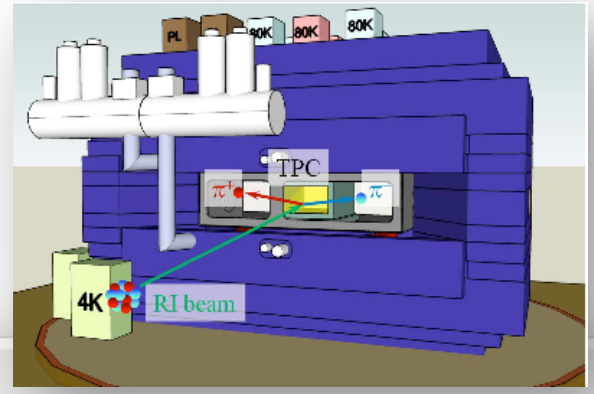


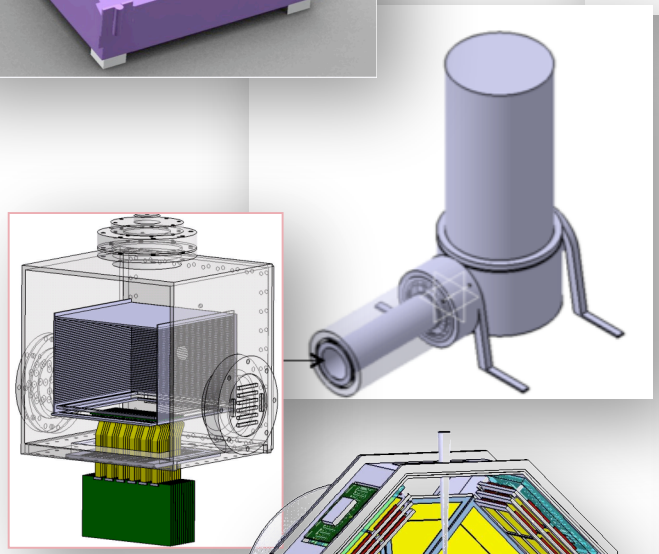
- *Opportunity to develop a generic /reconfigurable system approach for Nucl. Phys. to cover medium size systems* (256 – 32K channels).

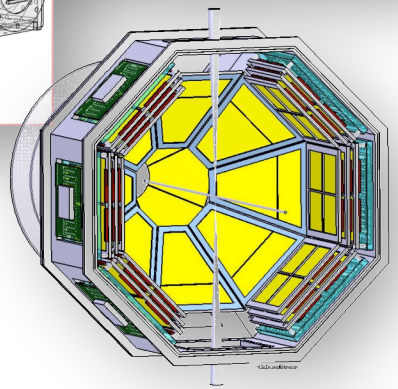
Systems to be covered by GET











- Projects employing **GET**
  - ACTAR - TPC(GANIL, IRFU, IPNO, SFTC, …) – Micromegas + Si – 20k channels
  - AT-TPC (MSU, LBL …) – Micromegas – 12k channels
  - GASPARD (GANIL, IRFU, IPNO, ...) – Si & CsI – 15k channels
  - BTD (IRFU & GANIL) – 100 channels
  - SAMÜRAI-TPC (RIKEN) – Micromegas -20k channels
  - IRFU – Industry
  - Test system - IRFU
- Under Study use of GET/ GET modules
  - S3 – (SPIRAL2+IRFI+…) – Si/gas tracker - 500 channels
  - MINOS ➔ (p;2p, γ) - (IRFU)– Micromegas - 5K channels
  - FIDIAS (IRFU) – Micromegas 5K Channels (IRFU)

100 K Channels Gas, Si & CsI

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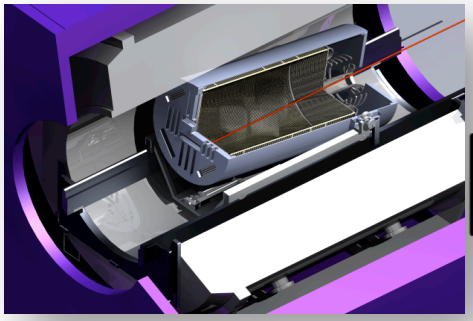
SYSTEM GET



AT -TPC

Very FE
Pre-amp/
Protection

ZAP

Embedded Systems:
T. Stamp/
0-suppress/
Formatting/
reduction/
Calibration
Slow Control

AsAd
ASIC
ADC
FPGA
PULSER
T/V/I

CoBo
FPGA
+
Memo

Mutant
Trigger
FPGA

µ-TCA

Front-End
Stab./Security
Coding

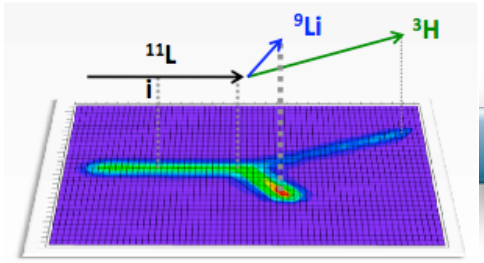
BEM

FARM
Trigger L3
Event-
Building
NARVAL
S. Control
Web
Service
Security

L0, L1, L2 Level
Trigger
Clock

SYSTEM GET

Conceptuel Design



ACTAR

irfu saclay

ZAP-PAC

irfu saclay

AsAd
ASIC
ADC
FPGA
PULSER

irfu saclay

NSCL

CoBo
FPGA

Mutant
Trigger
FPGA

µ - T C A

GANIL Spiral2

GANIL Spiral2

GANIL Spiral2

irfu saclay

GANIL Spiral2

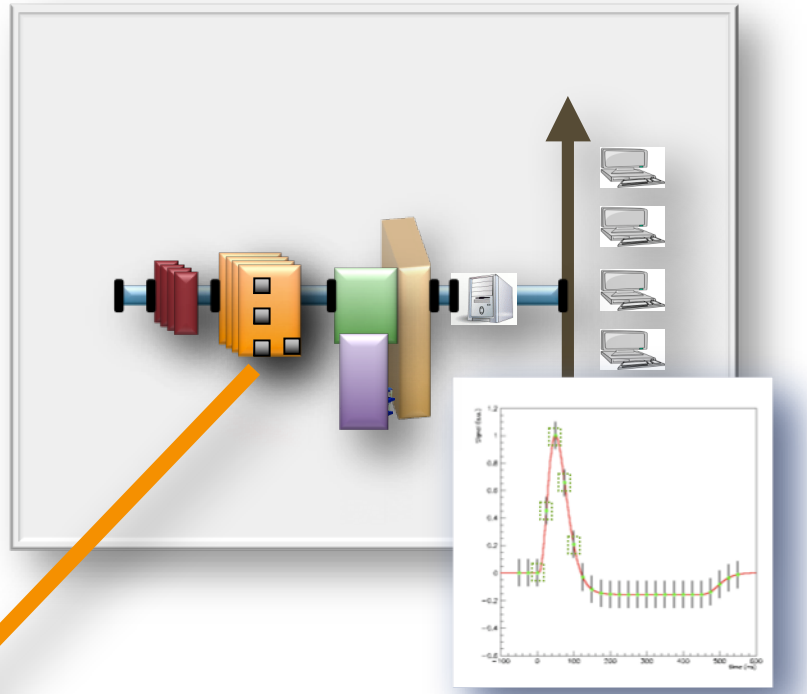
GENBG

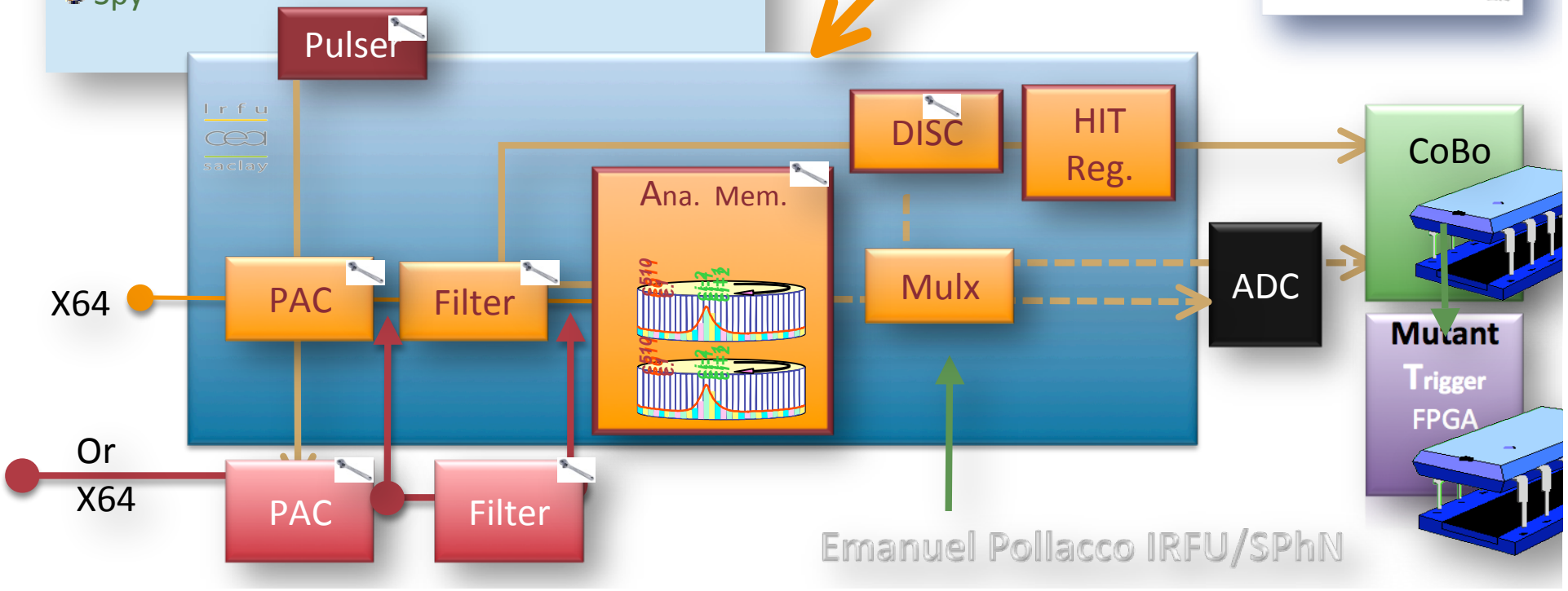
RIKEN NiSHiNA CENTER

GET

Asic AGET

- CMOS 0.35µm
- Int./Ext. PAC &/or Filter
- Gain & Disc/channel ➔ 120, 240 fC, 1, 10 pC.
- Shaping 50-1000 nsec
- Sampling rate 1-100Mhz ➔ 25MHz ADC 12/14bits
- Selective Readout – Hit Reg.
- Time Sampled/Registered Trigger
- Windowed SCA readout ➔ 128/256/512 or variable
- **2 time- consequative SCA windows**
- Pulser facilities
- Spy





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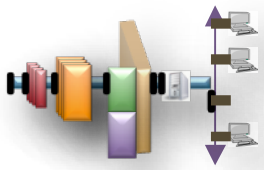
MUTANT (Multiplicity Trigger and Time stamp)



Nucl. Phys. Have Limited Experience ➔ Scenarios/Simul.

4-level triggers

L0: External trigger

L1: Time dependent Multip. trigger

➔ Self Trigger, …

L2: Hit Pattern trigger ➔ Self Trigger, calculated read pattern …

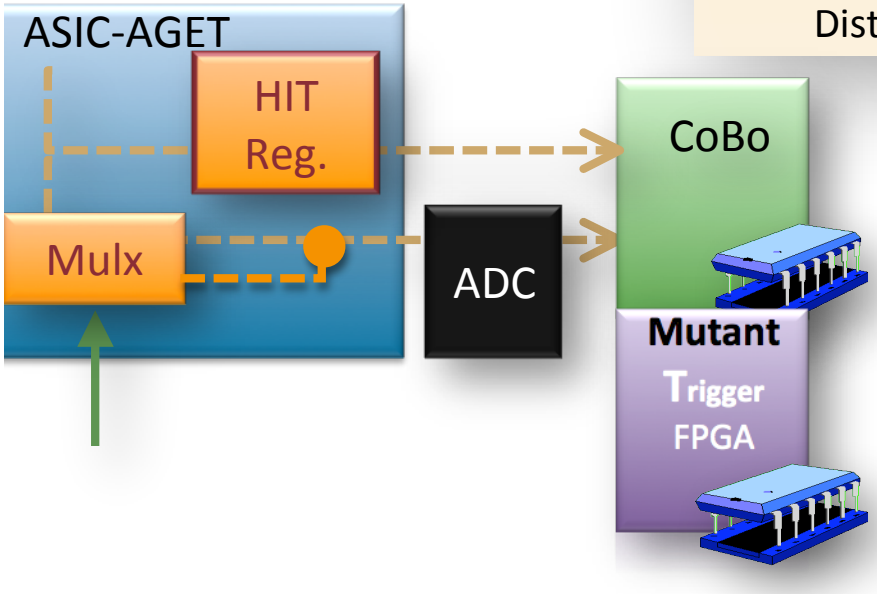
L3: Soft trigger

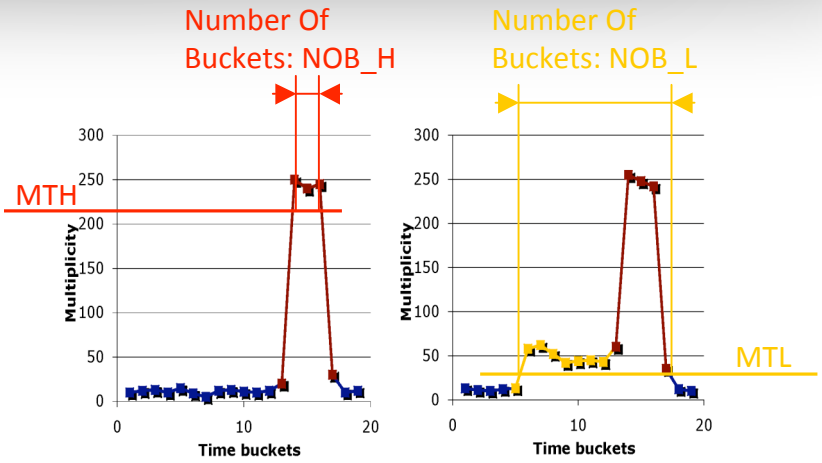
Compute the digital trigger from CoBos (25MHz)

Time stamp (48b, 10ns) and event N° (32b)

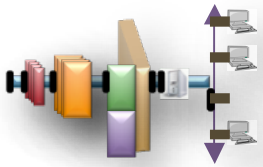
Distribute the 100MHz clock for the synchronisation

Trigger & Data Building





1 µTCA shelf typical architecture



Up to 10240 channels = 160 ASICS
on 40 ASAD boards (4 asics/ASAD)

TI ADS6422

Counting Rate
Up to 1 KHz

LVDS readout signals @ 150Mbit/s
(ADC 12bits-25MHz)

14 slot µTCA Crate
2 PM, 1 MUTANT,
10 CoBo AMC+ 1 MCH

GbE /10 GbE dual star carrier support

Up to 10 "COBO"s
With 1 COBO for 4 ASADs

MUTANT for
MUltiplicity
Trigger(s)
ANd
Time

Front End

Back End

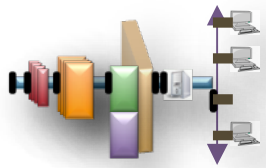
10 GbE MCH
uplink

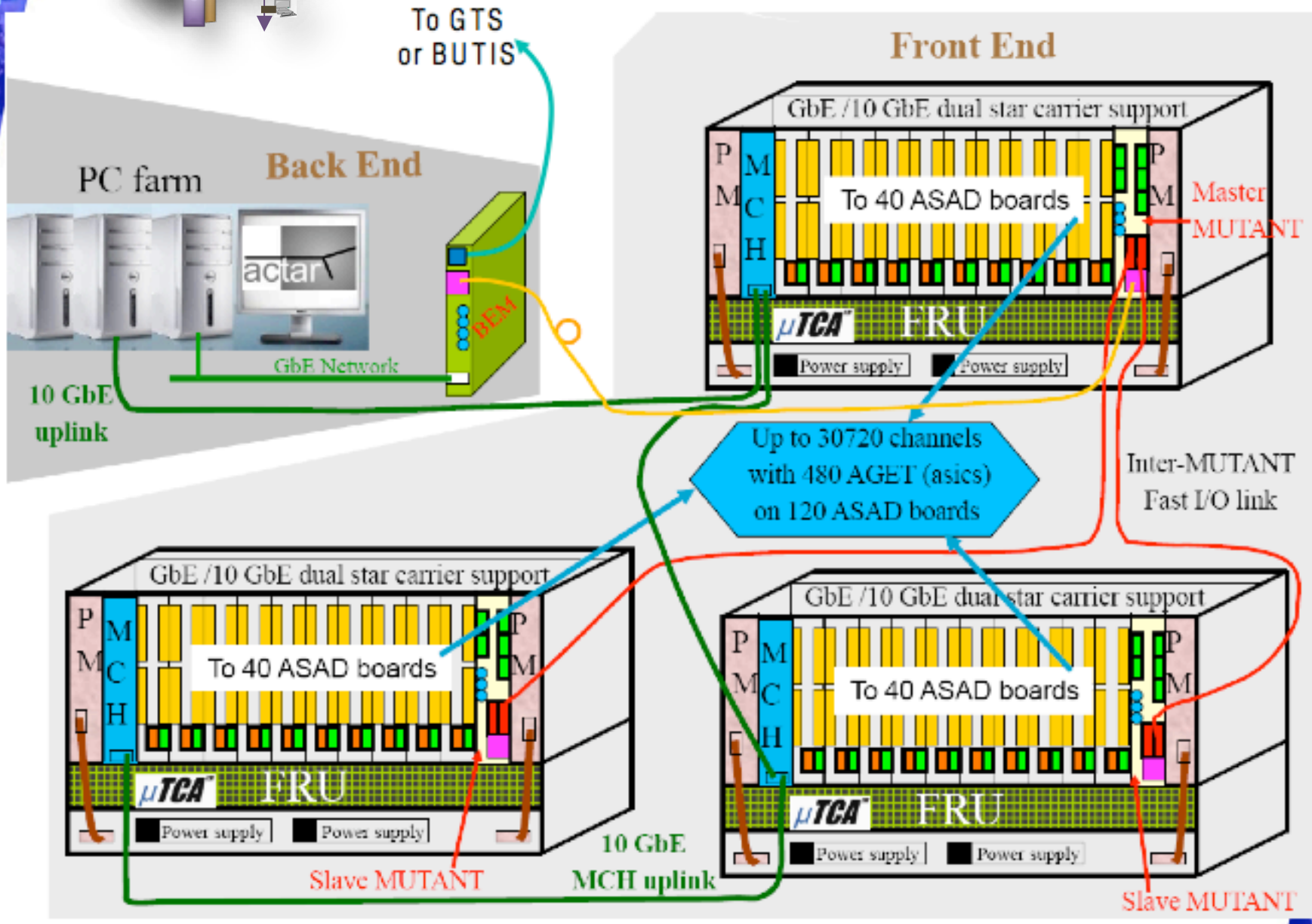
PC farm

This module could be in
the acquisition room near
the pc and the scope or
inside the external trigger system
(with GMT,CENTRUM, …)

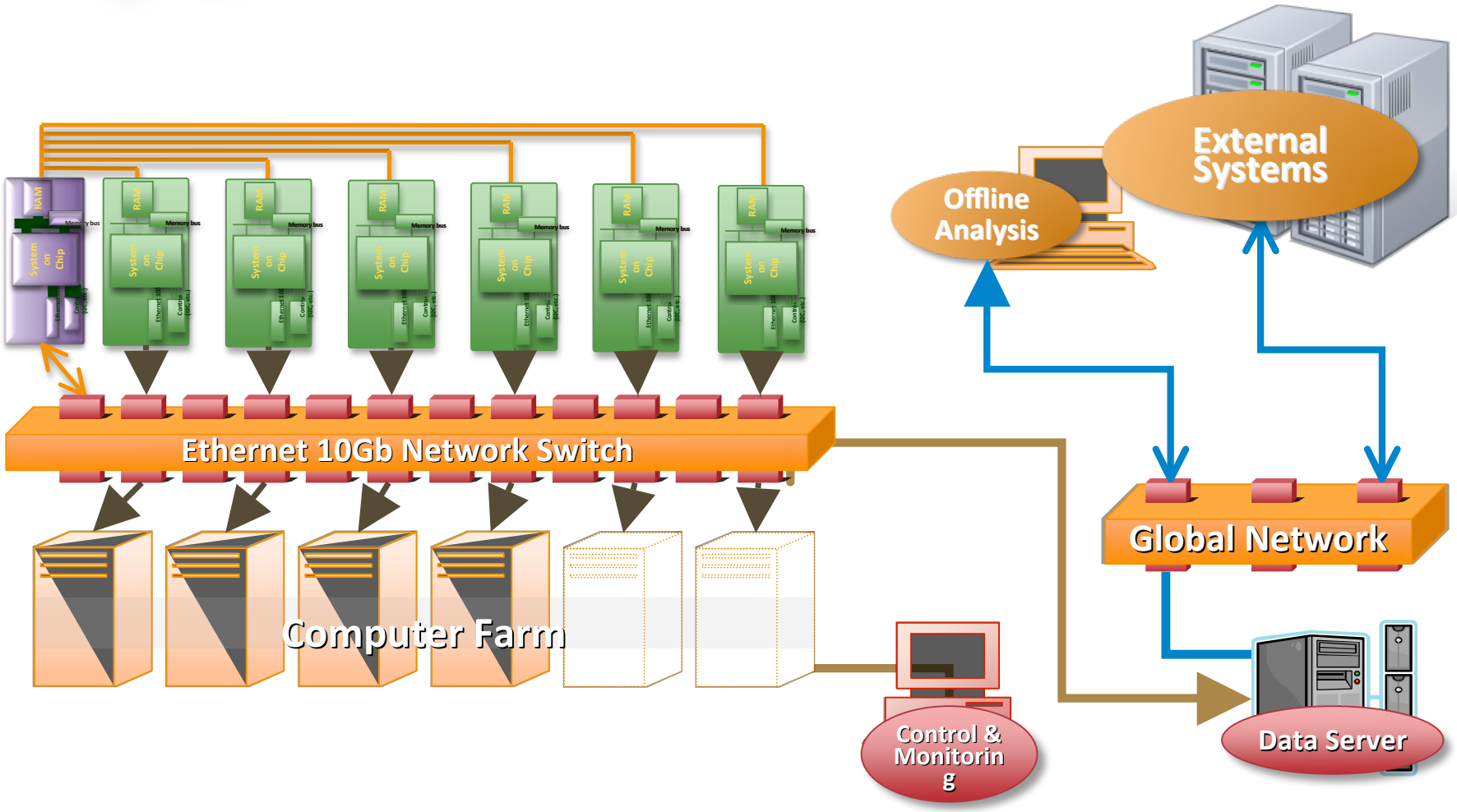
GbE network

Full architecture – 3 μTCA shelves



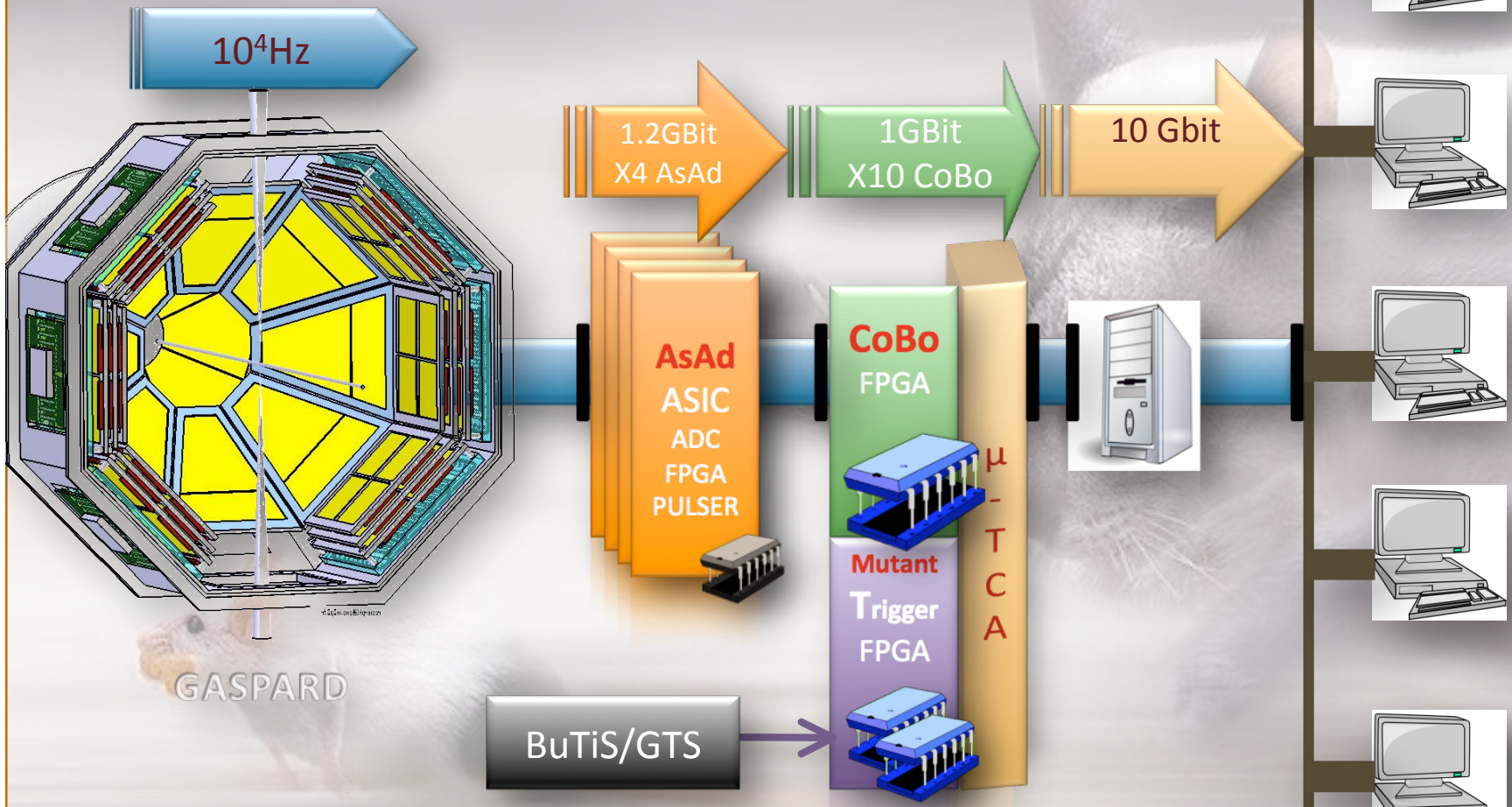


Global View of DAQ Hardware Infrastructure



Trigger & Band Width

Common Dead Time
Or
Individual AsAd Dead-Time



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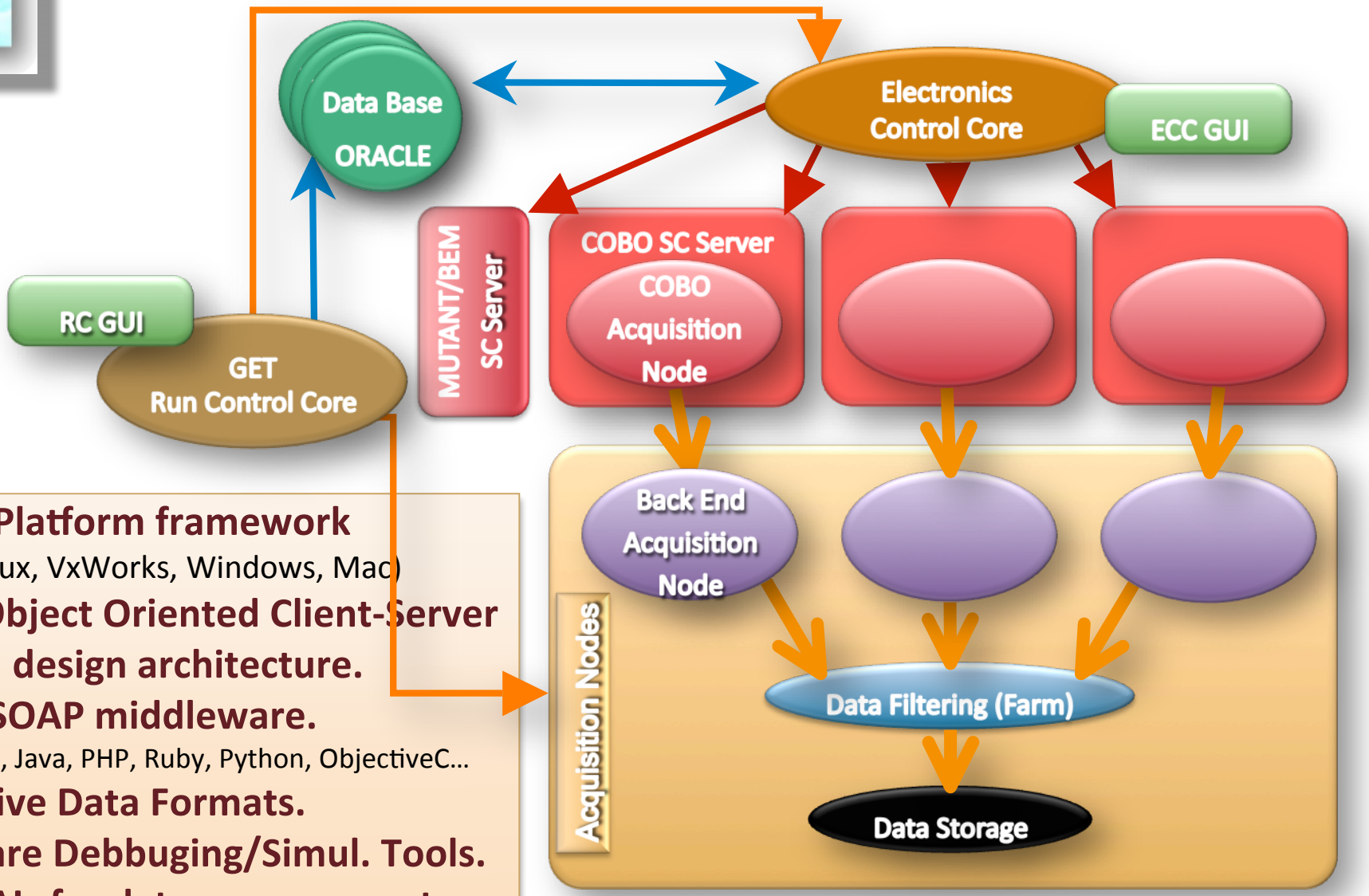
Software/Firmware developments



- **Multi-Platform framework**
  - (Linux, VxWorks, Windows, Mac)
- **Fully Object Oriented Client-Server design architecture.**
- **ICE & SOAP middleware.**
  - (C++, Java, PHP, Ruby, Python, ObjectiveC…
- **Evolutive Data Formats.**
- **Software Debbuging/Simul. Tools.**
- **NARVAL for data management (– ADA, TCP/IP).**

S. Anvar, GET coll.

Reconfigurable Approach

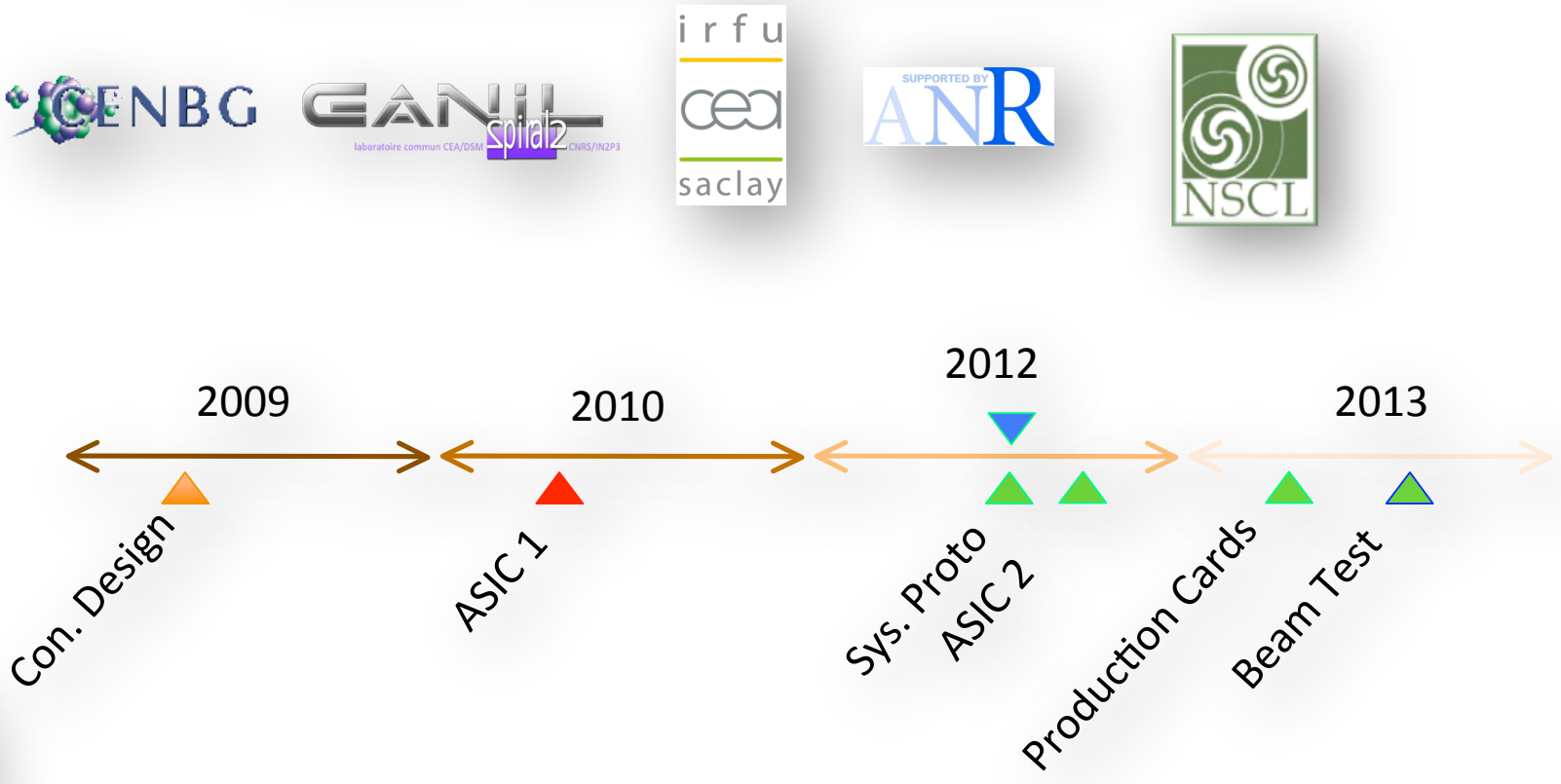
Via:- Hardware & Software Architecture
(*Documentation & Simulation tools*
Multi-lab Multi-project collaboration)

Genericity ➔ Multi-Platform (Linux, VxWorks, Windows, Mac) framework
Fully Object Oriented Client-Server design architecture.
ICE & SOAP middleware.
Evolutive Data Formats.
Software Développement /Debbuging/Simulation Tools.
NARVAL for data management (NARVAL – ADA, TCP/IP).

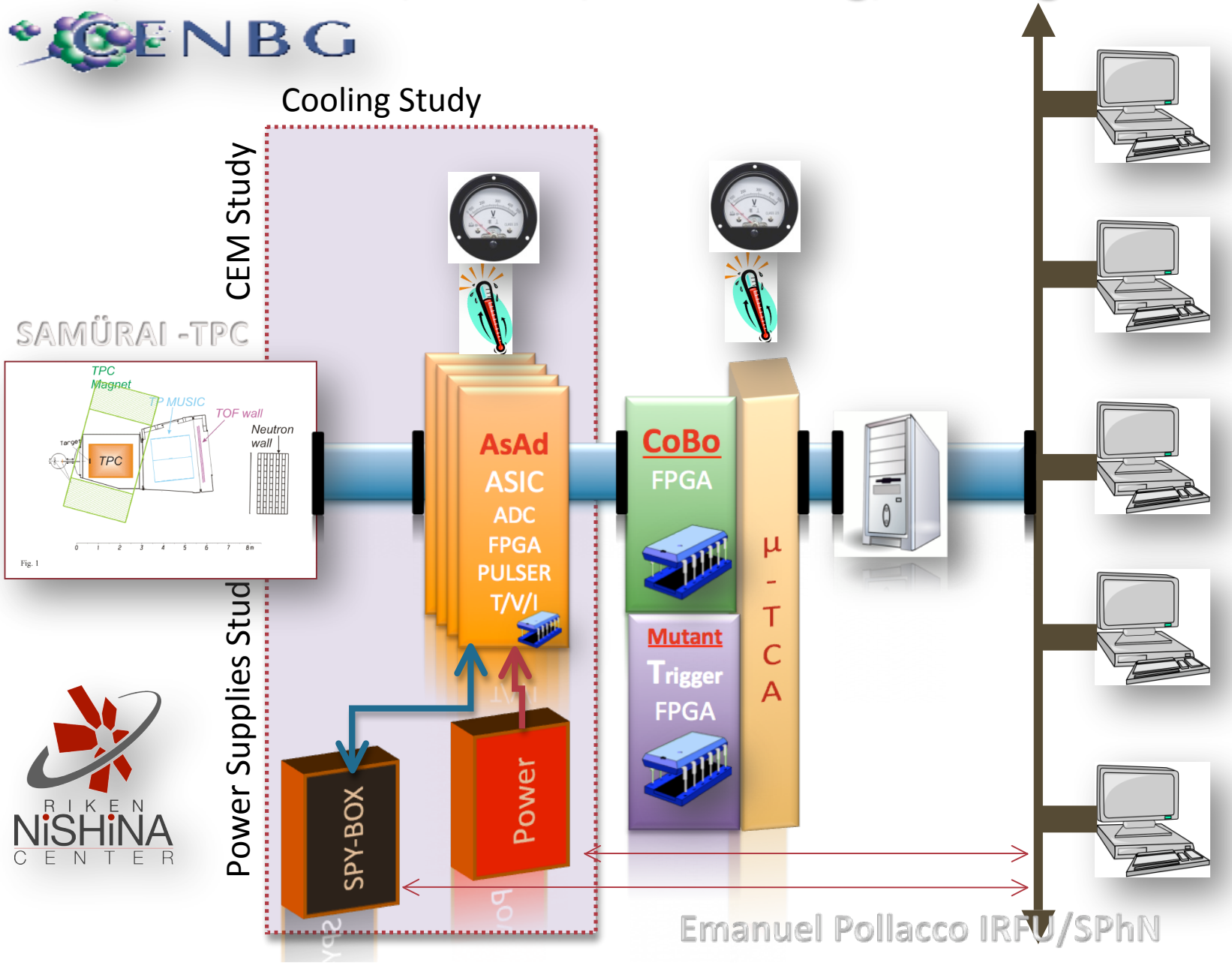
END

GET Project

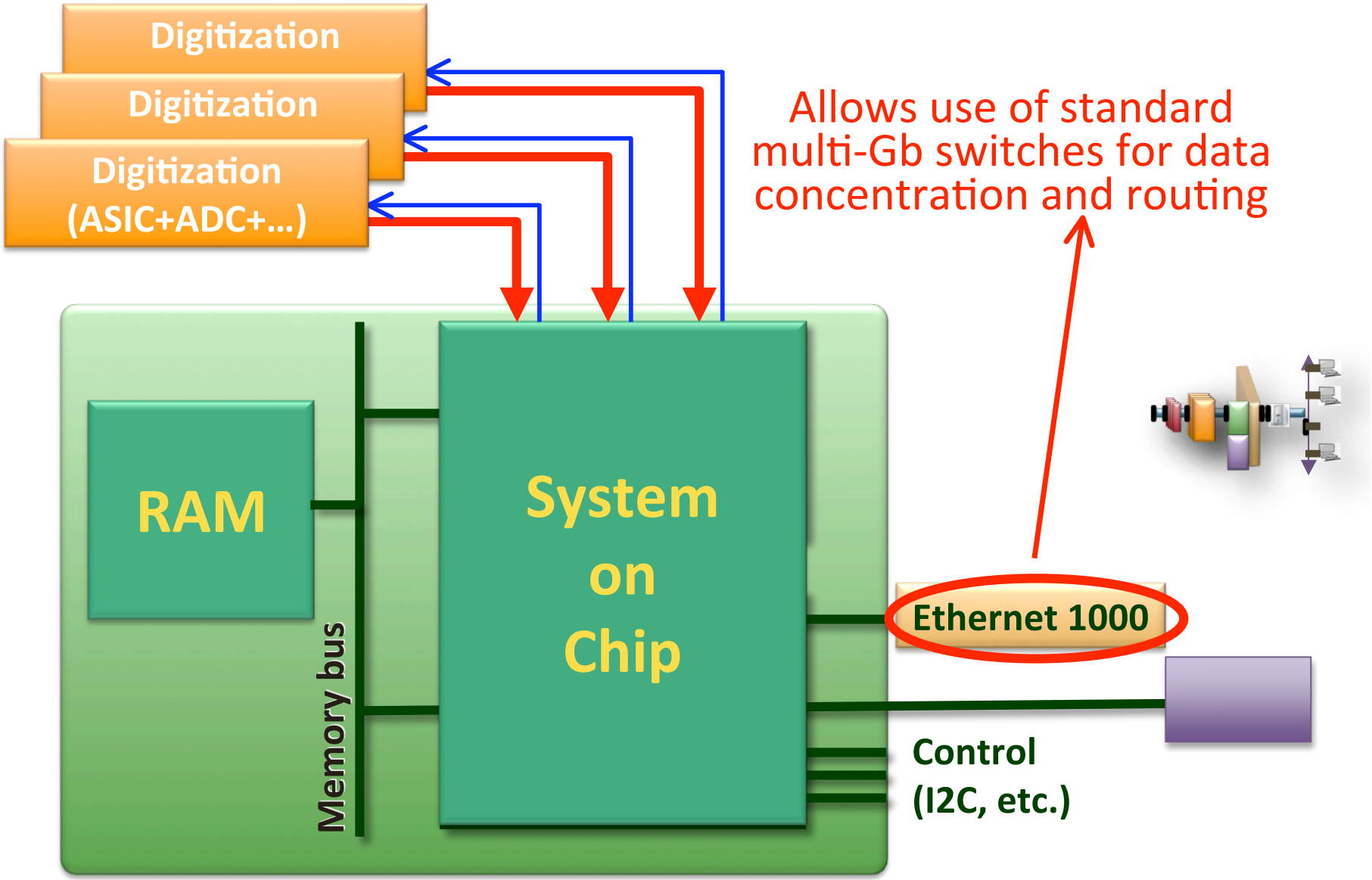
Project is Financed by ANR, IRFU, CENBG, GANIL 75% (France)
NSCL/MSU 25% (US) for the R&D program.



EMC, Connectors, Cables, Monitoring, Testing & Security

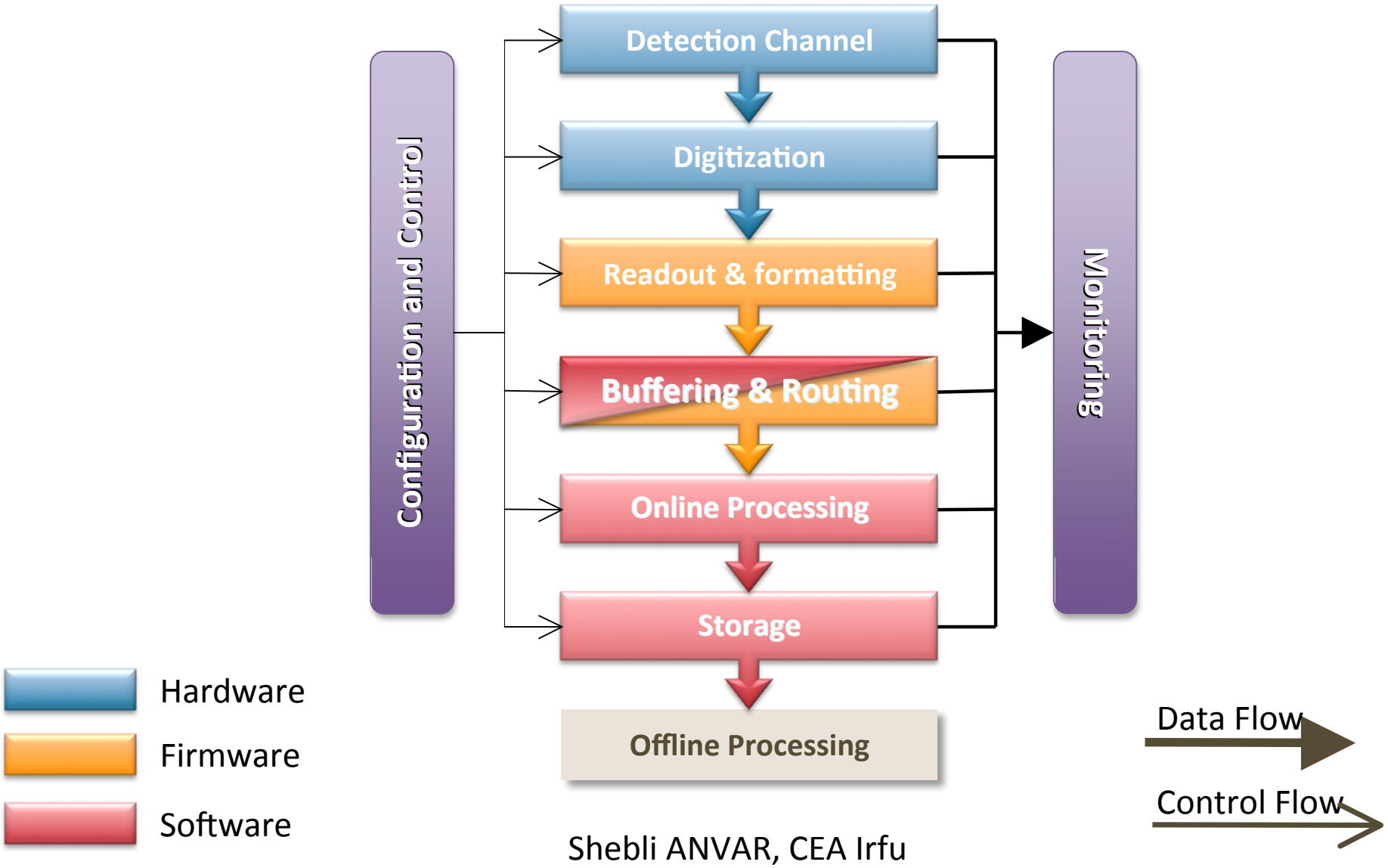


Embedded Implementation (Upstream)



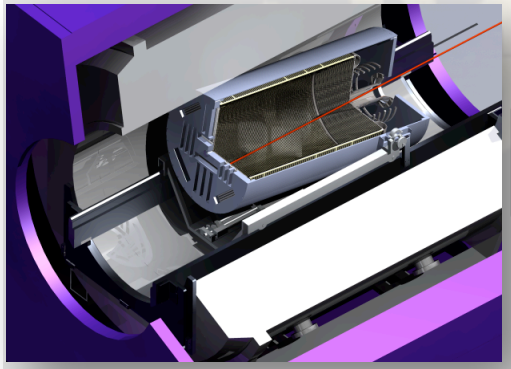
Parameter	Value
Polarity of detector signal	Negative or Positive
Number of channels	72
External Preamplifier	Yes; access to the filter or SCA inputs
Charge measurement	
Input dynamic range	120 fC; 1 pC; 10 pC
Gain	Adjustable/(channel)
Output dynamic range	2V p-p
I.N.L	< 2%
Resolution	< 850 e- (Charge range: 120fC; Peaking Time: 200ns; Cinchannel. < 30pF)
Sampling	
Peaking time value	50 ns to 1 µs (16 values)
Number of SCA Time bins	512 [new]
Sampling Frequency	1 MHz to 100 MHz
Time resolution	
Jitter	60 ps rms
Skew	< 700 ps rms
Trigger	
Discriminator solution	L.E.D
Trigger Output/Multiplicity	OR of the 64 discriminator outputs (pulse of 2*TckADC)
Dynamic range	5% of input charge range
I.N.L	< 5%
Threshold value	4-bit DAC/channel + (3-bit + polarity bit) common DAC
Minimum threshold value	≥ noise
Readout	
Readout frequency	20 MHz to 25 MHz
Channel Readout mode	Hit channel; specific channels; all channels
SCA Readout mode	512 cells; 256 cells; 128 cells
Test	
calibration	1 channel / 64; external test capacitor
test	1 channel / 64; internal test capacitor (1/charge range)
functional	1, few or 64 channels; internal test capacitor/channel
Counting rate	< 1 kHz
Power consumption	< 10 mW / channel

Control, Acquisition & Online Processing Chain



Shebli ANVAR, CEA Irfu

Number Channelling



AT-TPC

1 – 32,000

256

1024

TRIG

10240

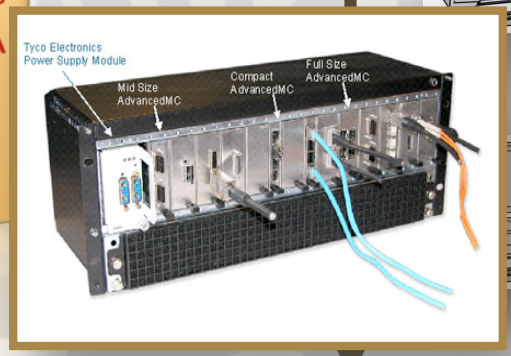
PAC

AsAd
ASIC
ADC
FPGA
PULSER
T/V/I

CoBo
FPGA

Mutant
Trigger
FPGA

μ-TCA



Channel Number – can be increased

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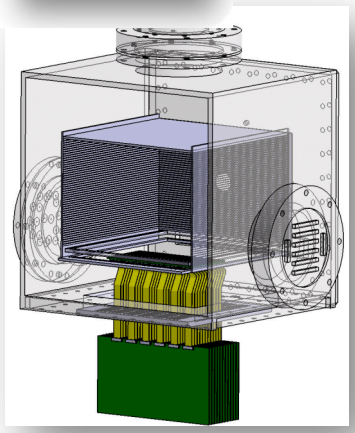
GET Overview



Front-end boards
Asic+ADC
HV, I, T monitoring

Data Readout & Trig
Zero suppress
Time stamp
3-Level trigger

DAQ & Slow control
Run control
Online analysis
Electronics control

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GENBG

NSCL

ZAP | Ext preamp | AGET | ADC

ASAD

Inspection box time alignment (Riken)

Spy box

Time reference (GSI Butis)

Clock provider

CoBo: Readout, Signal process, Gb transfer

MUTANT: Clock distrib, Trigger L0-2, Process L1 -> L2

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SLOW CONTROL: ECC, Config manager, Data base

NARVAL: Event builder, Run control, Event analysis, Storage

DAQ

GANIL spiral2 laboratoire commun CEA/DSM CNRS/IN2P3

Micro-TCA standard

The generic aspects developed in GET are software-related because we didn't have the resources to work on the firmware for this. However, the design that we made with Nathan is, let's say, "easily portable" on other applications because we developed it having in lind some level of genericity. The software genericity is implemented as a multiplatform (Linux, VxWorks, Windows, Mac) framework allowing developers to develop hardware drivers through network access, hardware slow control communication protocols using simple and easy-to-implement C++ templates. The fully object oriented (OO) client server design of the framework together with the use of the ZeroC Ice middleware allow all network accessed features to be operated by clients written in all modern object oriented programming languages (C++, Java, PHP, Ruby, Python, ObjectiveC…).

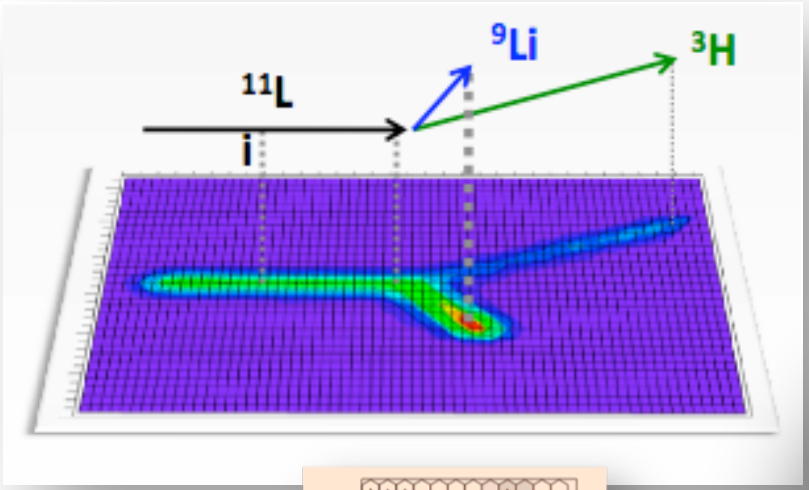
Personnel 2009/2010/2011

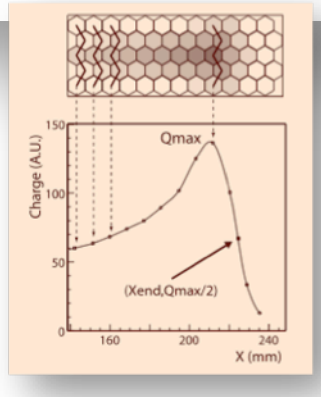
- IRFU
  - Engineers 4 + 1 CDD (24months ANR)
  - Physicists 2
- GANIL
  - Engineers 4 + 1 CDD (28months ANR)
  - Physicists 2
- CENBG
  - Engineers 5
  - Physicists 2
- MSU
  - Engineers 1
  - Physicists 4

Tasks

- Managment
- Phys Validation – Simulation
- Front-End Electronics
- Data Acquisition Hardware
- Data Acquisition Software
- Documentation
- Test Bench
- Calibration
- CEM, Cooling & Power Supplies
- PRODUCTION Study

Active Target - 20Kch

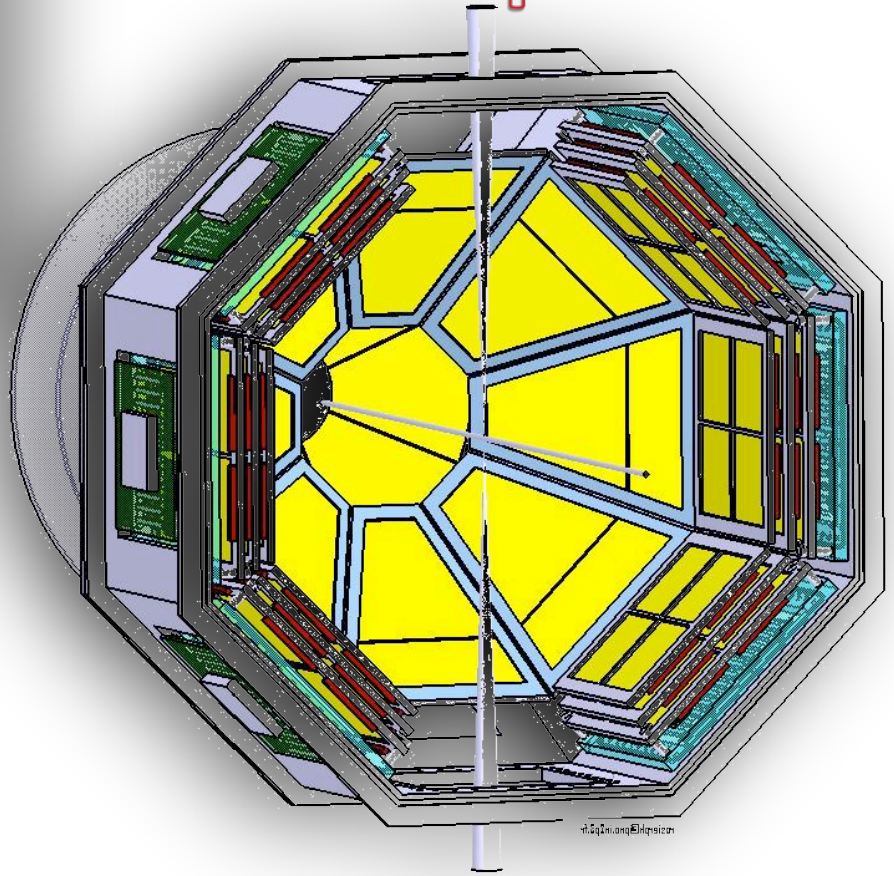




Bragg trace measure

&

Si 4pi – 12K ch



Irfu cea saclay

Systems for Nuclear Physics Today

1. Relatively low number of Channels Approx. 1,000
2. Short & Reconfigurable Experimental Setups with variety of Detector Types
3. Human & Financial Resources Low

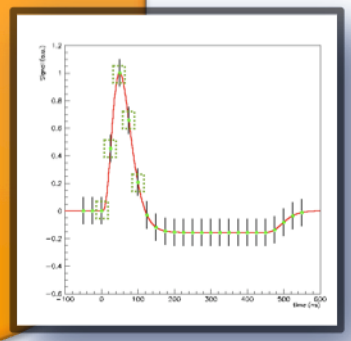
Systems for Nuclear Physics Tomorrow

1. Number of Channels Approx. 20,000
2. Short & Reconfigurable ….
3. Human & ...

Measure

1. TPC, Si, CsI … (E & T via Charge Sampling),
2. Multi-Level Numeric Trigger
3. Integrated Time-STamp
4. >1000 events/sec

Adapting Part. Phys. Techniques



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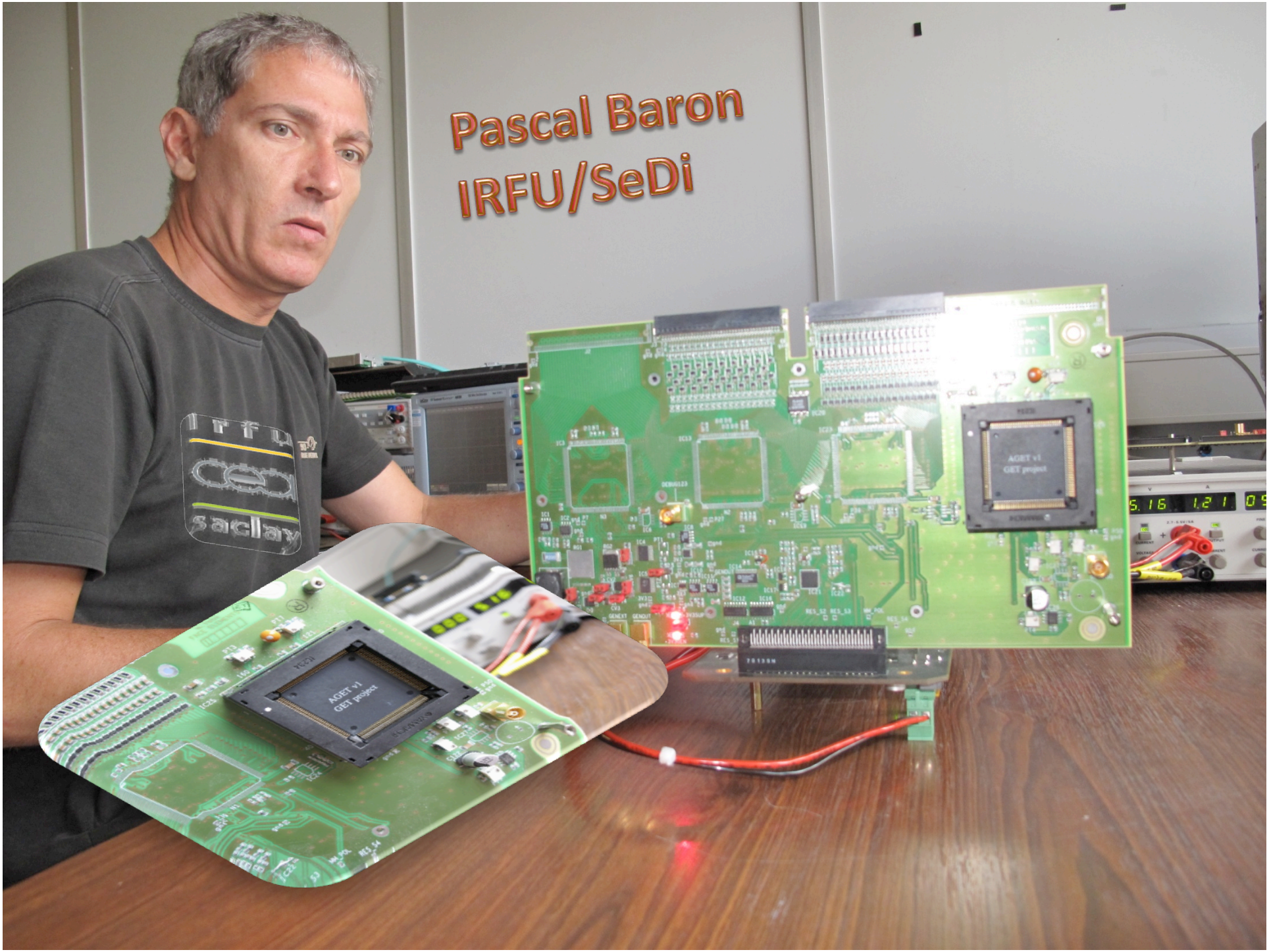
Pascal Baron
IRFU/SeDi
AGET v1
GET project