Calibration des Microroc (II)

Alex, Cyril, Giom, Jean, Max

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Previous results (I)

Experimental conditions

- Test charge: 2.5, 12.5, 25, 37.5 fC
- Pedestal offset at 7
- Send charge to group of 8 channels

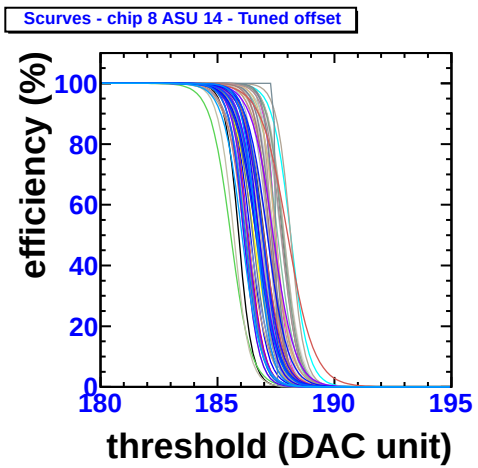
Pedestal offset

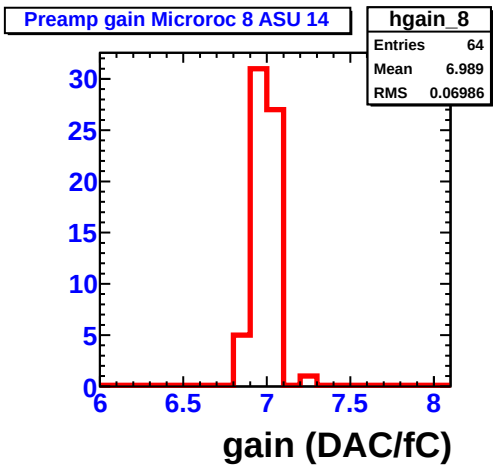
- Reduction of pedestal RMS by factor 2

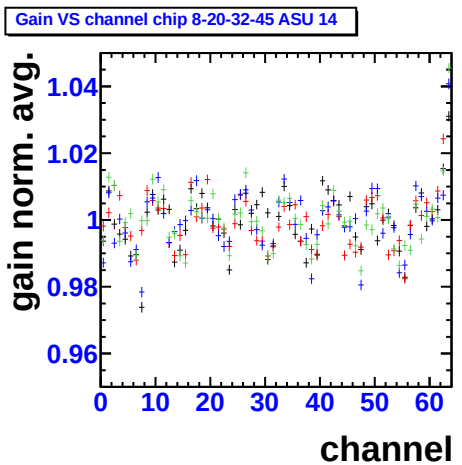
Preamplifier gain (4 chips)

- $\sim$7 DAC/fC with 1 % RMS variations
- (Small) channel to channel variations
- Noise of about 0.12 fC

Previous results (II)







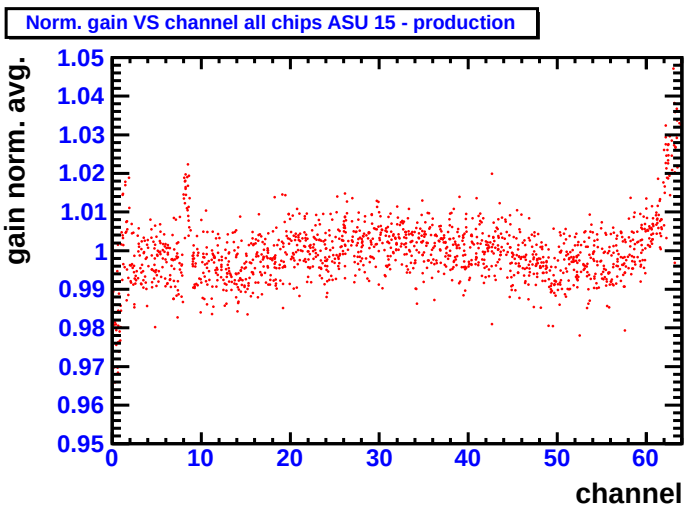
Conditions for next tests

- Test charge: 2.5, 12.5, 22.5, 32.5 fC
- Pedestal offset at 7
- Send charge to single channels

Comparison single chip & ASU chip

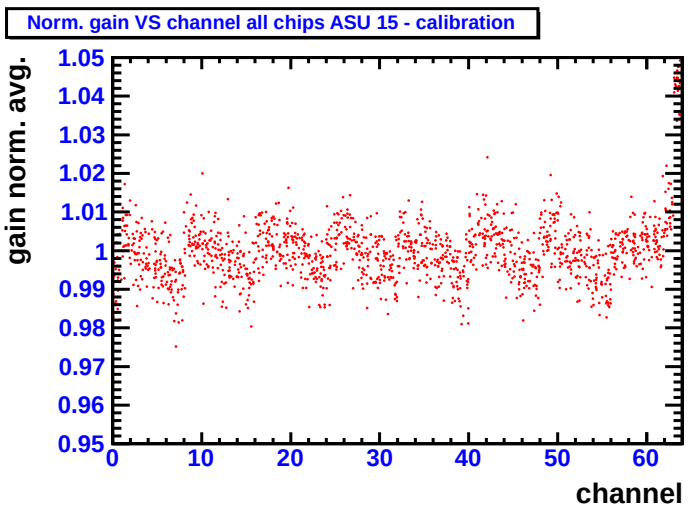
Production test

- Flat pattern
- Wrong gain channel 8
- Higher gain channel 62 & 63



Recent ASU test

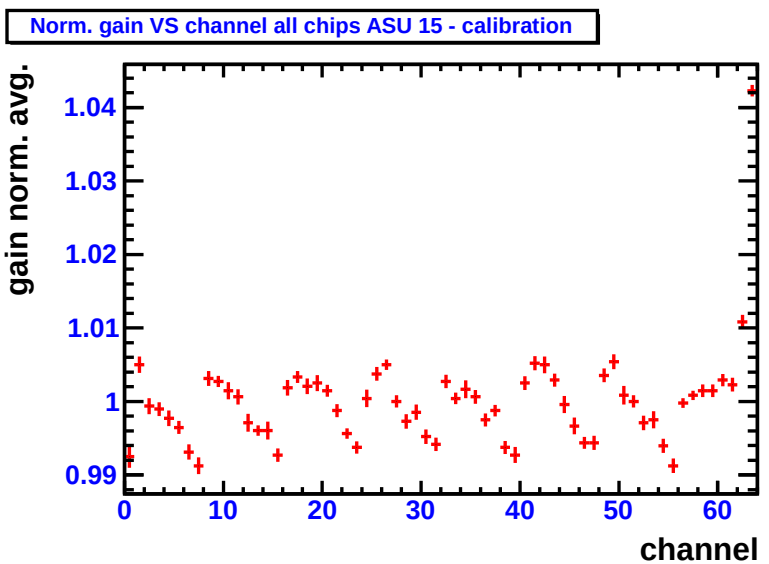
- Periodic pattern
- Variations modulo 8
- Higher gain channel 63



Channel to channel variations

Mean gain versus channel number

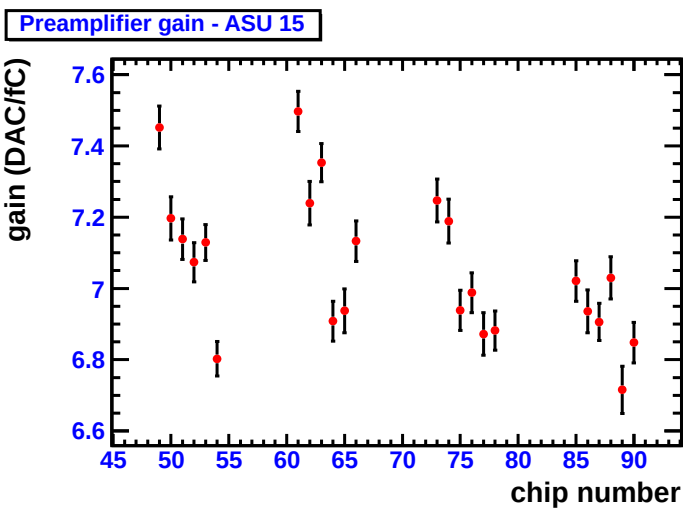
- Periodic pattern observed for all fully tested ASUs (14, 15)
- Reflect lenght variation of PCB pad to pin lines
- Channels 62 and mostly 63 are clearly far from average



Chip to chip variations

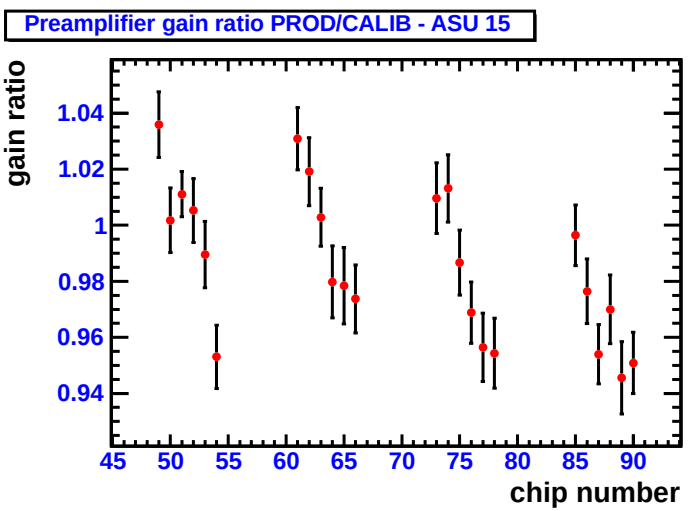
Position on ASU

- Gain drops along rows
- 10 % var. between row 1–6
- Seen for ASU 14 & 15 so far



Ratio ASU chip/single chip

- Normalise measured gain to production gains
- $\rightarrow$ attenuation of test Q



Outlook

- MICROROCs show great performance:
  Low noise (0.12 fC) and gain variations of 1 % RMS
- Channel to channel and chip to chip variations
  understood as PCB lines variations and
  attenuation of test signal from interDIF to chips
- Offset map available for all ASUs
- Next steps:
  Complete gain map of all ASU (all data reconstructed)
  Calibration with Bulk mesh Send jobs on MUST