De BABAR à Super B

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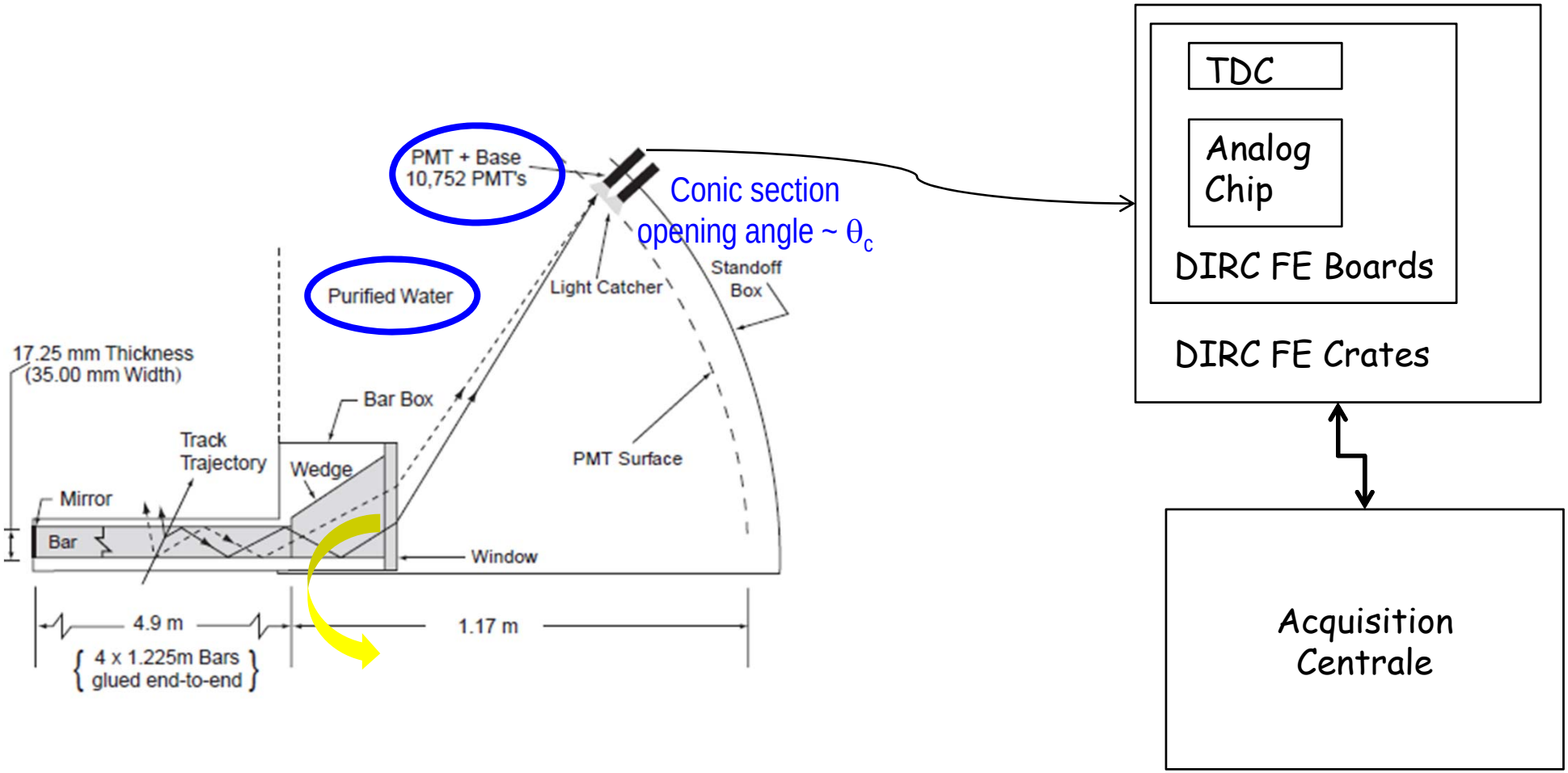
Rappel sur BABAR

DIRC : détecteur d'identification de particules



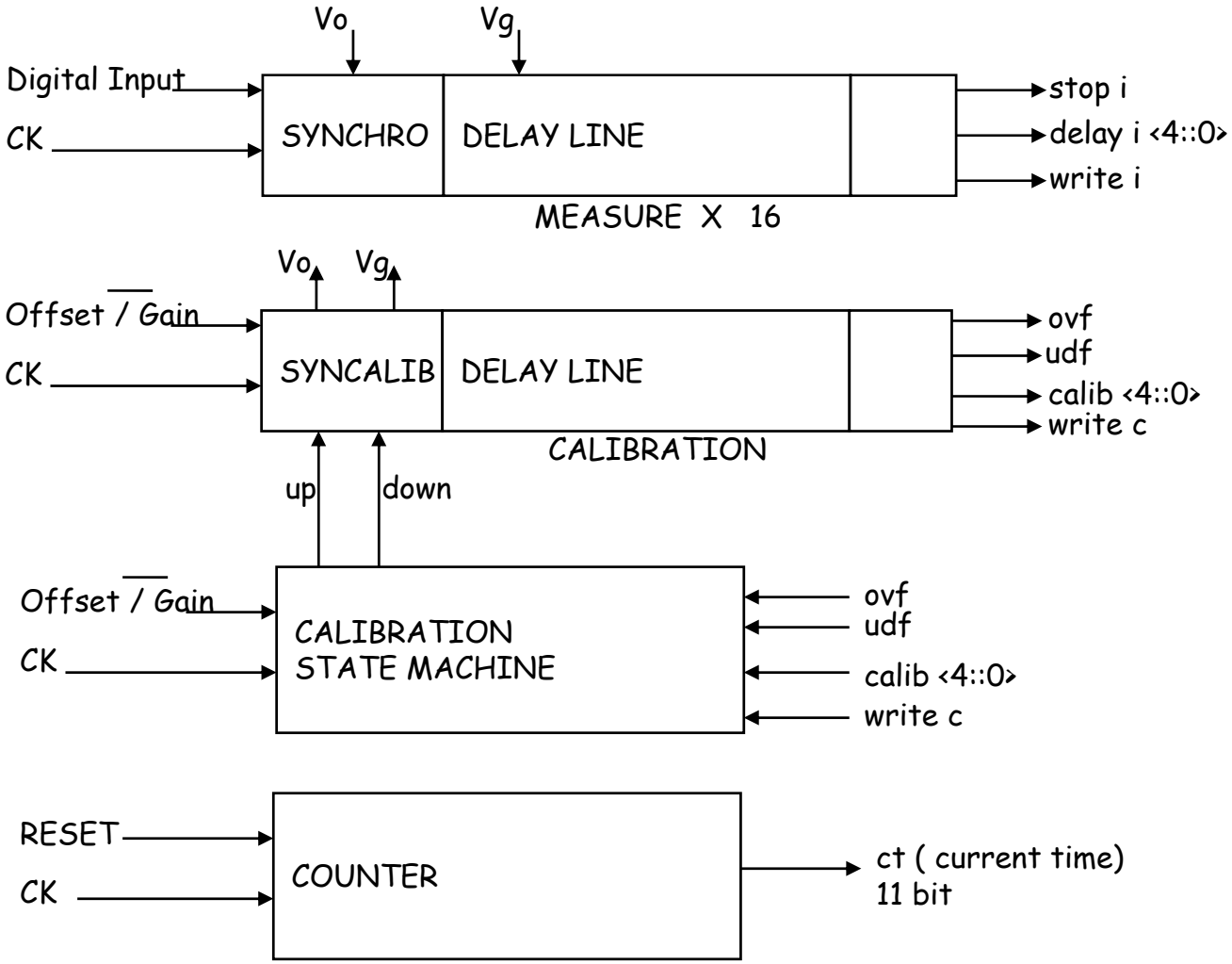
Rappel sur BABAR

- Participation au DIRC
- Mesure de temps : lsb = 500ps
- Stockage des données pendant la latence du trigger (programmable)
- Lecture des données dans une fenêtre programmable (résolution)
- Rejet des mauvaises données

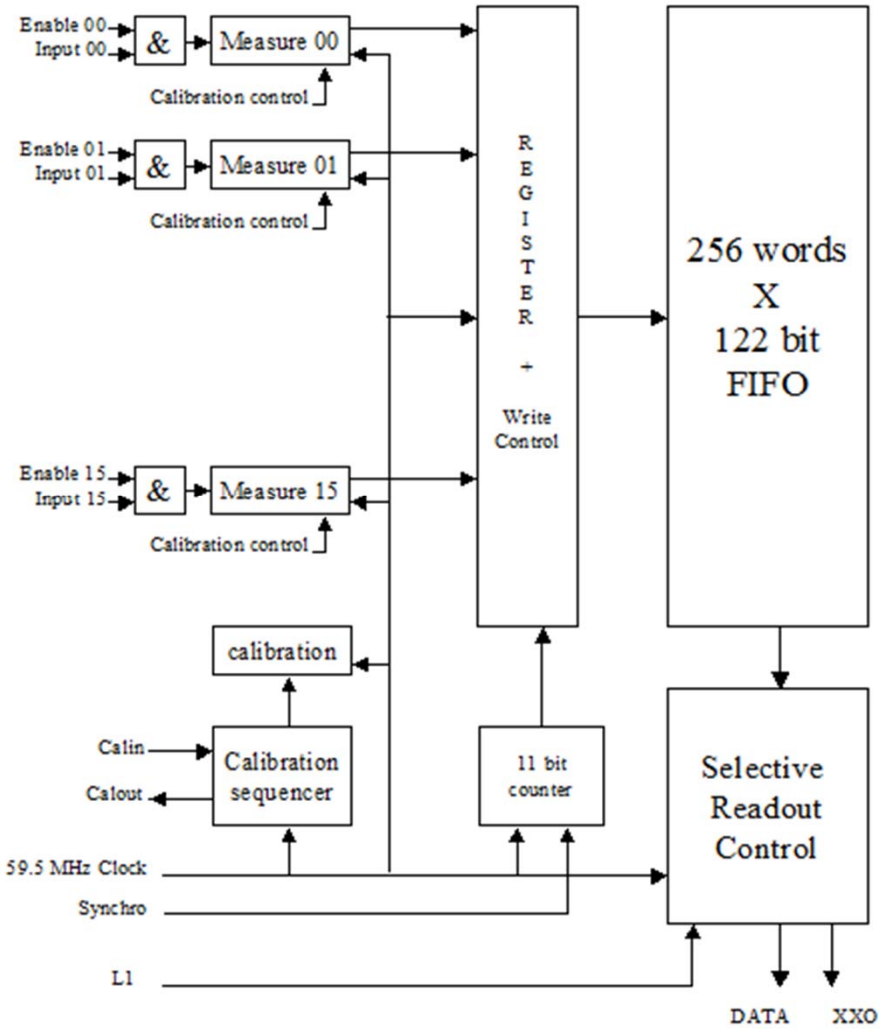
TDC2 : time to digital converter

Mesure
De temps

Calibration



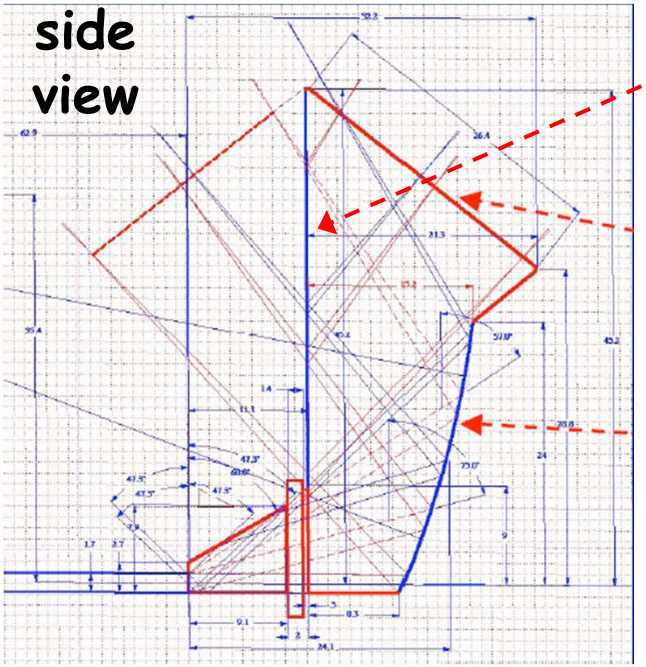
TDC 2



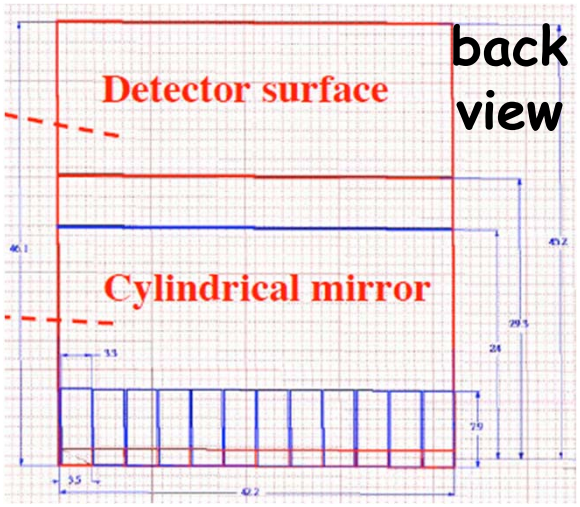
- 16 voies
- Lsb 520ps; précision 250ps
- Pleine échelle 34,4µs
- Résolution double pulse : 33,6ns
- Horloge : 59,5MHz
- Latence : 64ns → 16,3 µs
- Résolution : 64ns → 2µs
- Fréquence max d'entrée : 2MHz

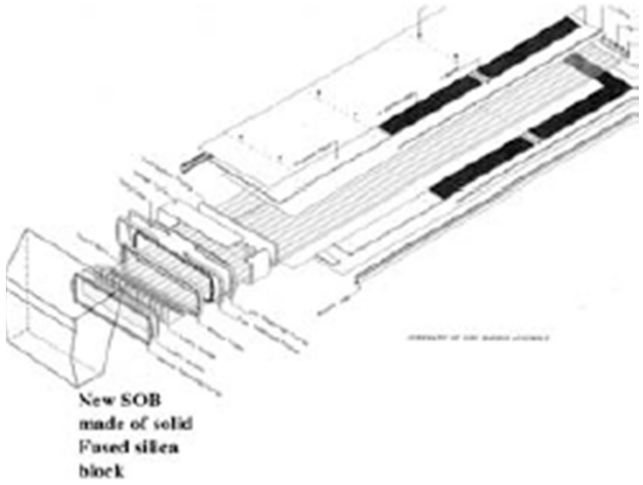
- Techno AMS CMOS 0.6µm (5V)

Super B

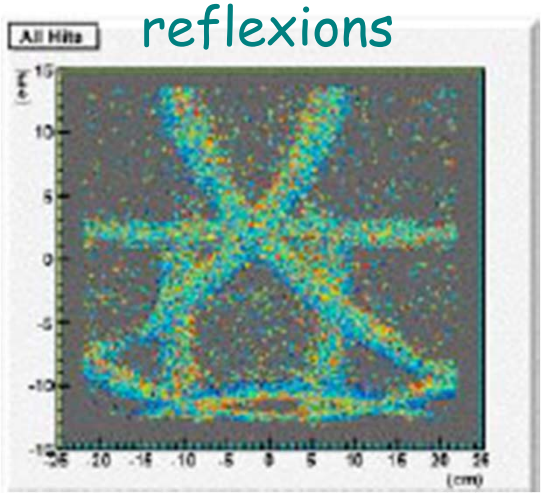


Plane mirror





Ring image is complex due to many reflexions

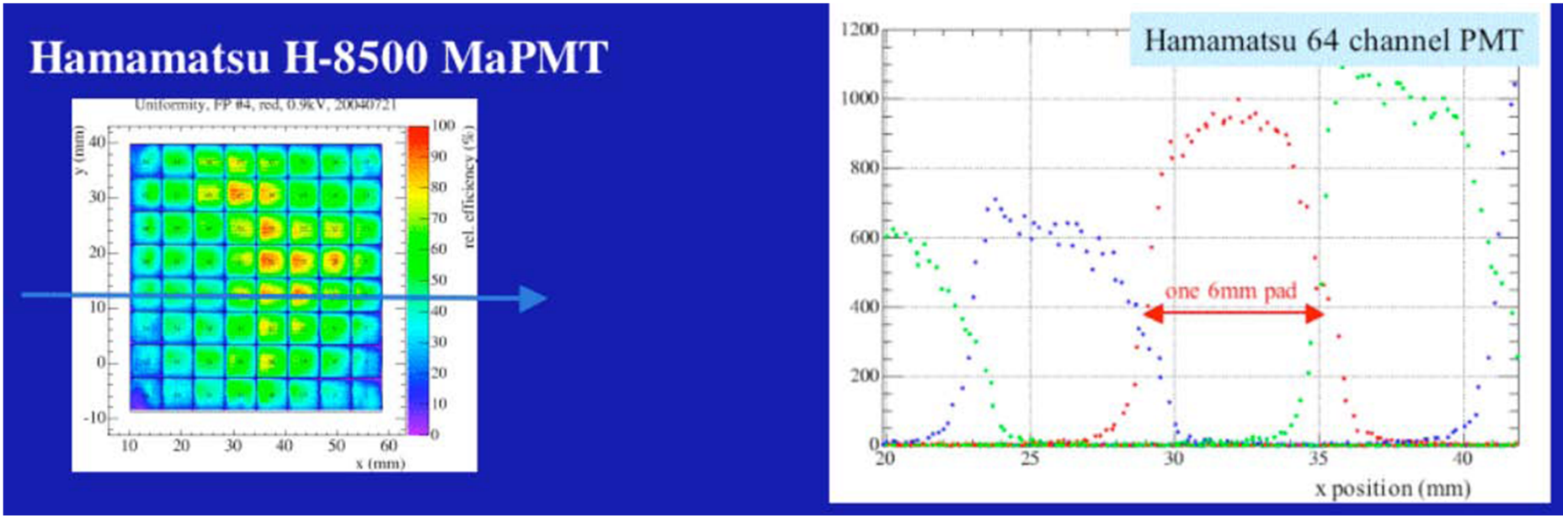


- Bruit du fDIRC dominé par des photons dans la SOB
- SOB 10 fois plus petite → réduction du bruit

Super B

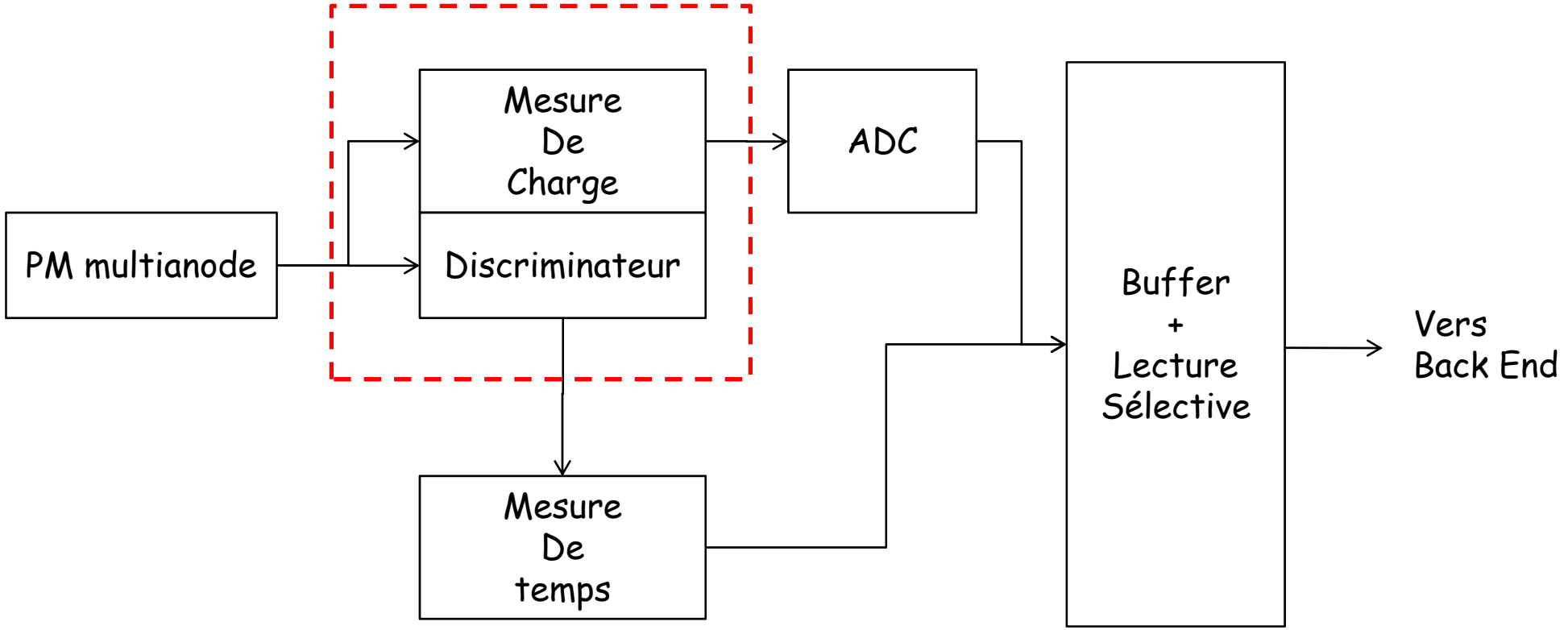
- Participation au PID (FDIRC)
- 36000 canaux
- Taux de bruit : ~1MHz par canal
- Taux de trigger : 150kHz
- Mesure de temps : résolution 100ps (170ps au total)
- Mesure de charges
- Lecture sélective des données

Mesure de charge



- PM multianode
- Mesure de charge + barycentre pour améliorer la résolution

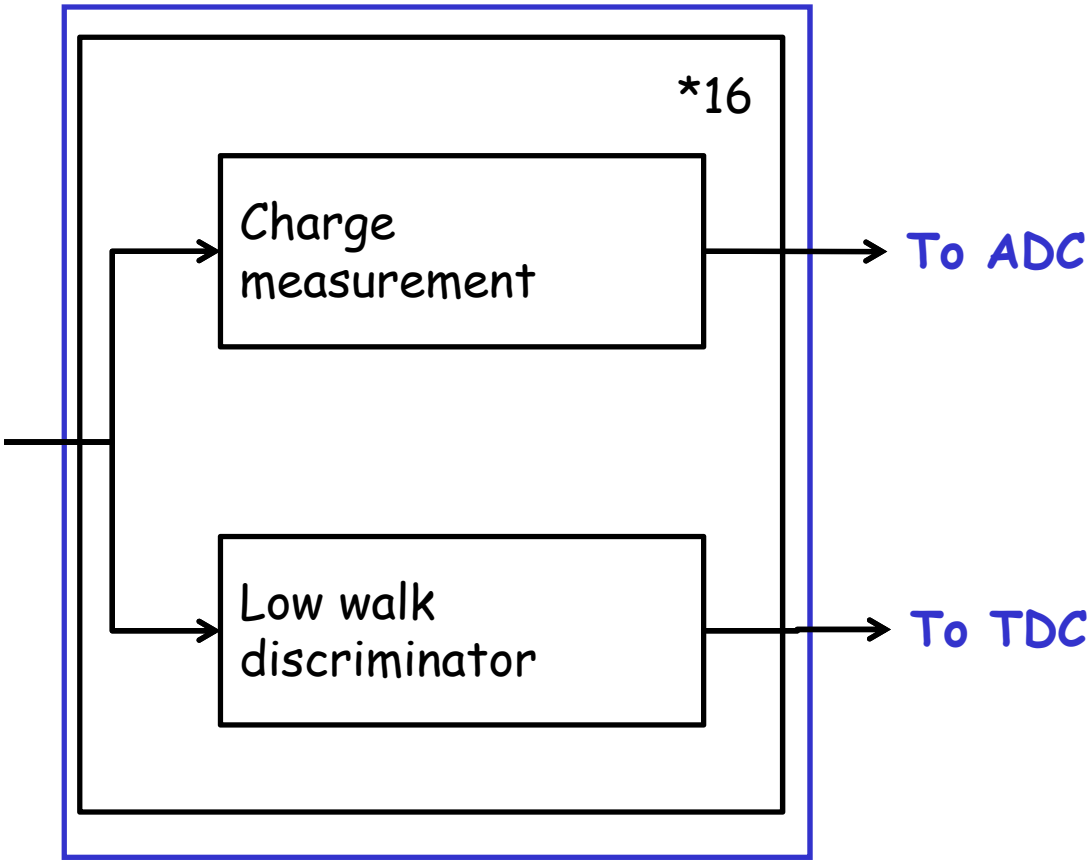
Participation du LPNHE à l'électronique du PID



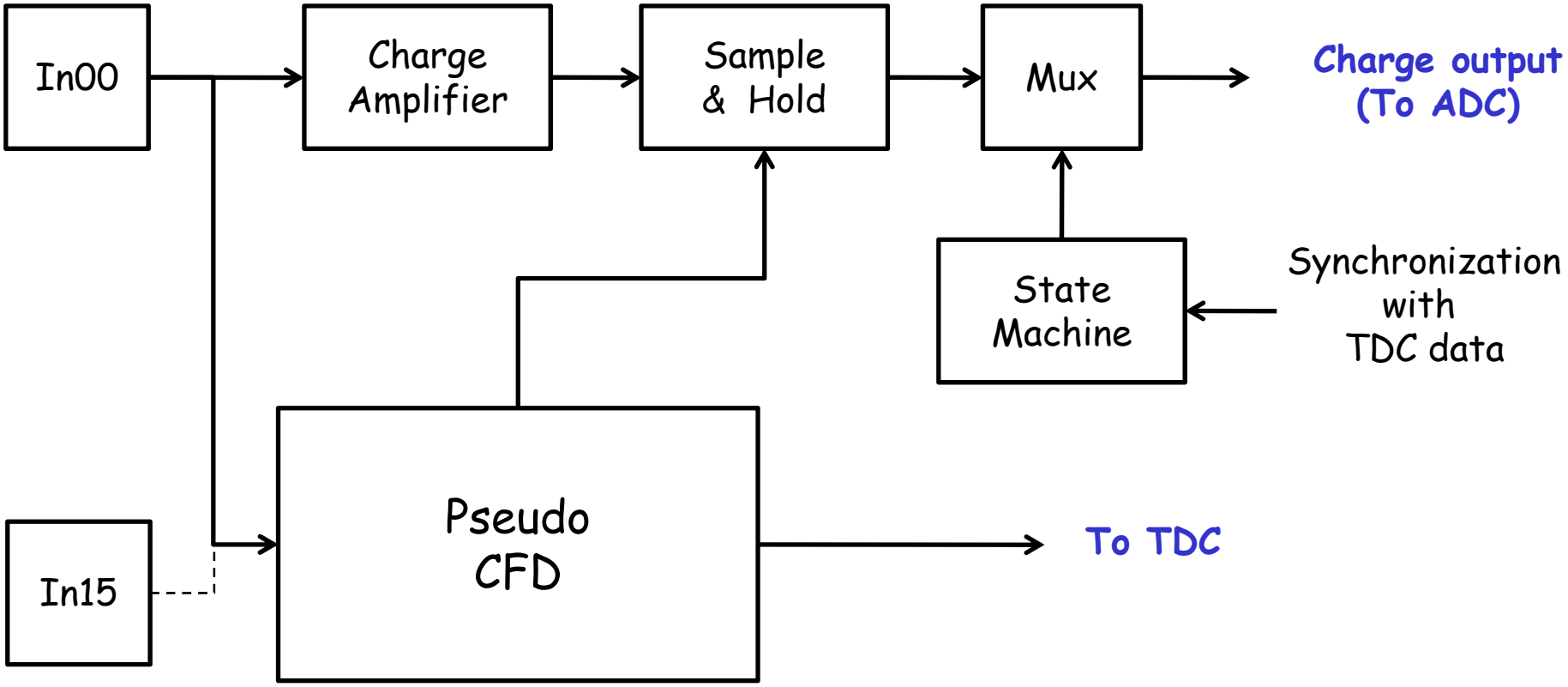
Électronique frontale du PID

PIF the Chip !

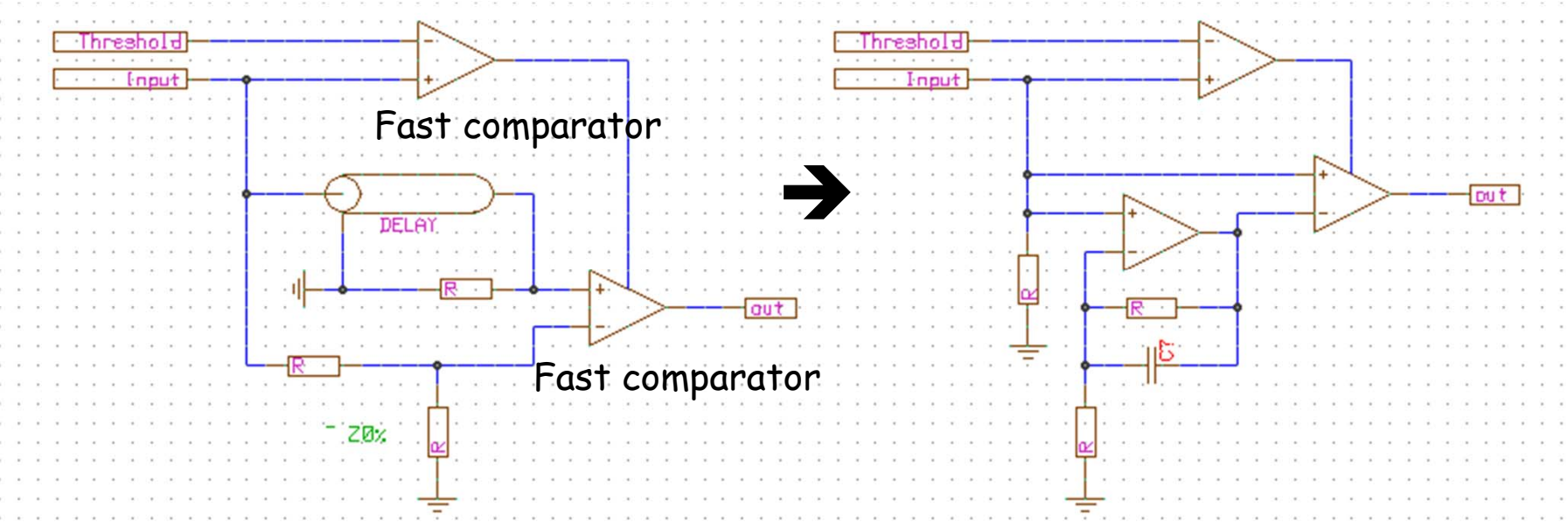
- PIF : PId Front end chip
- Dérive temporelle <= 50ps pour une dynamique de 10
- Résolution double pulse 50ns
- Mesure de charge : 8 bit
- Techno AMS CMOS 0,35µm ou 0,18µm



Proposition PIF



CFD sur Silicium

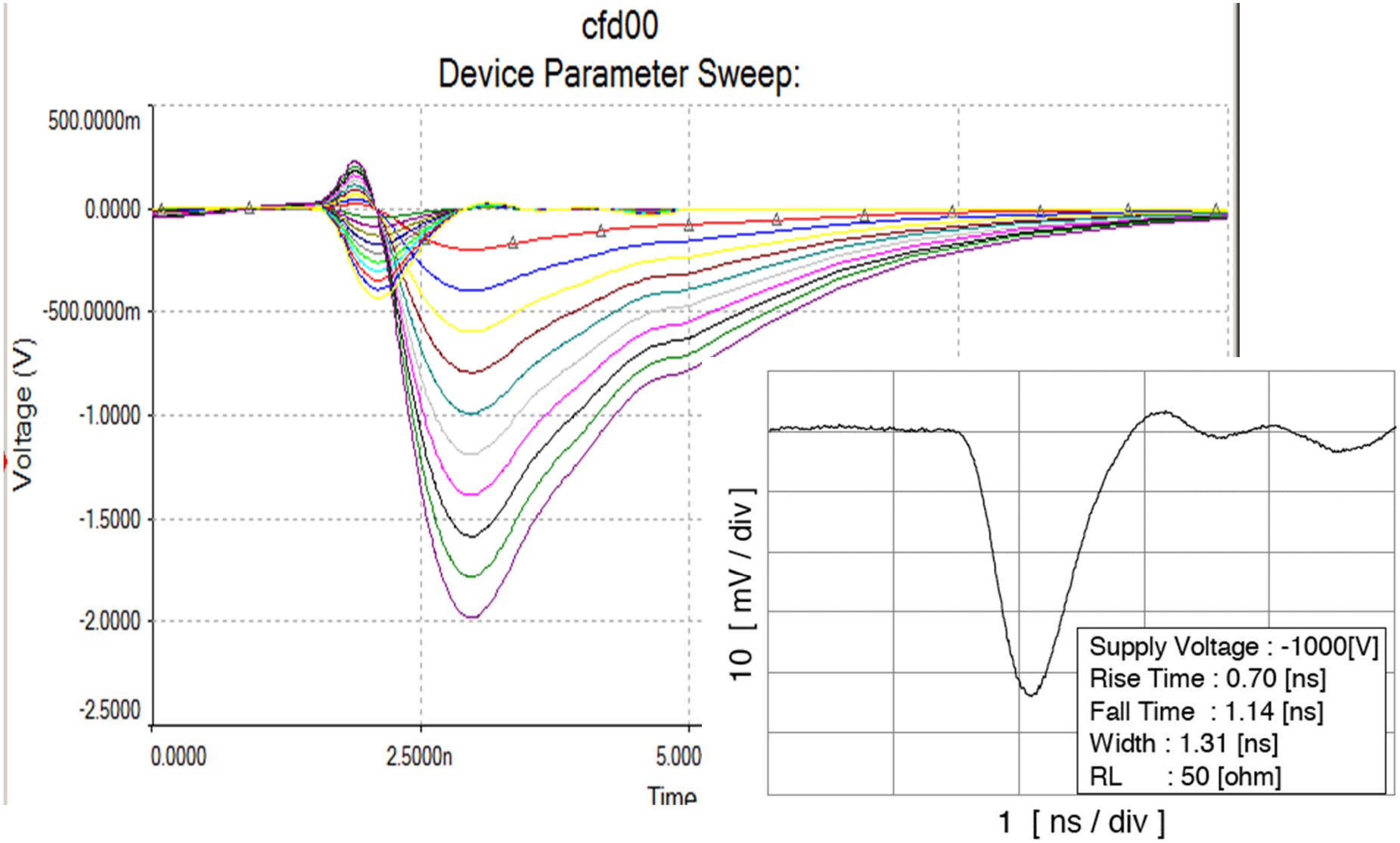


Classical CFD

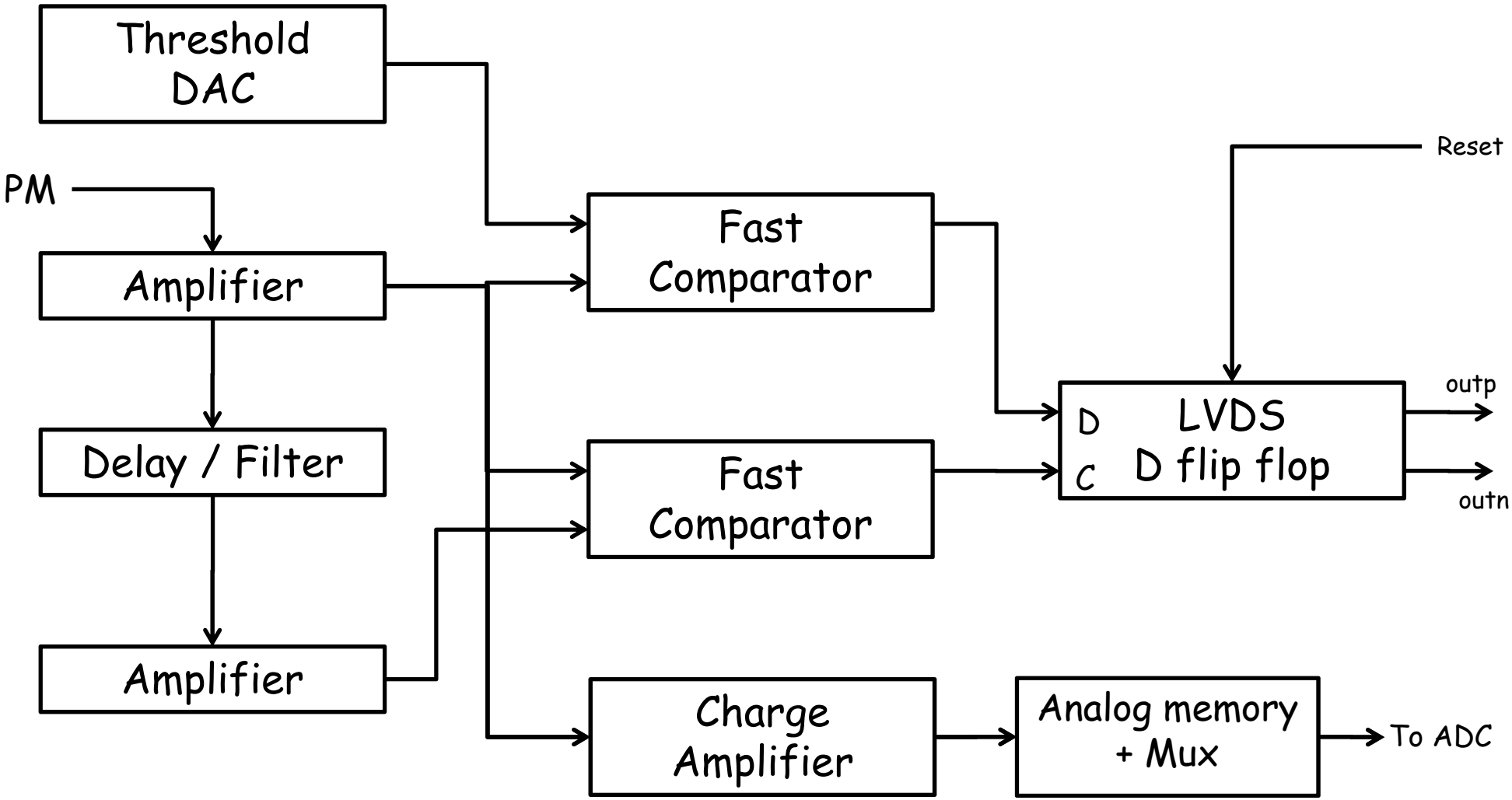
Proposed pseudo CFD

- Delay + Fraction → Gain + Integrators

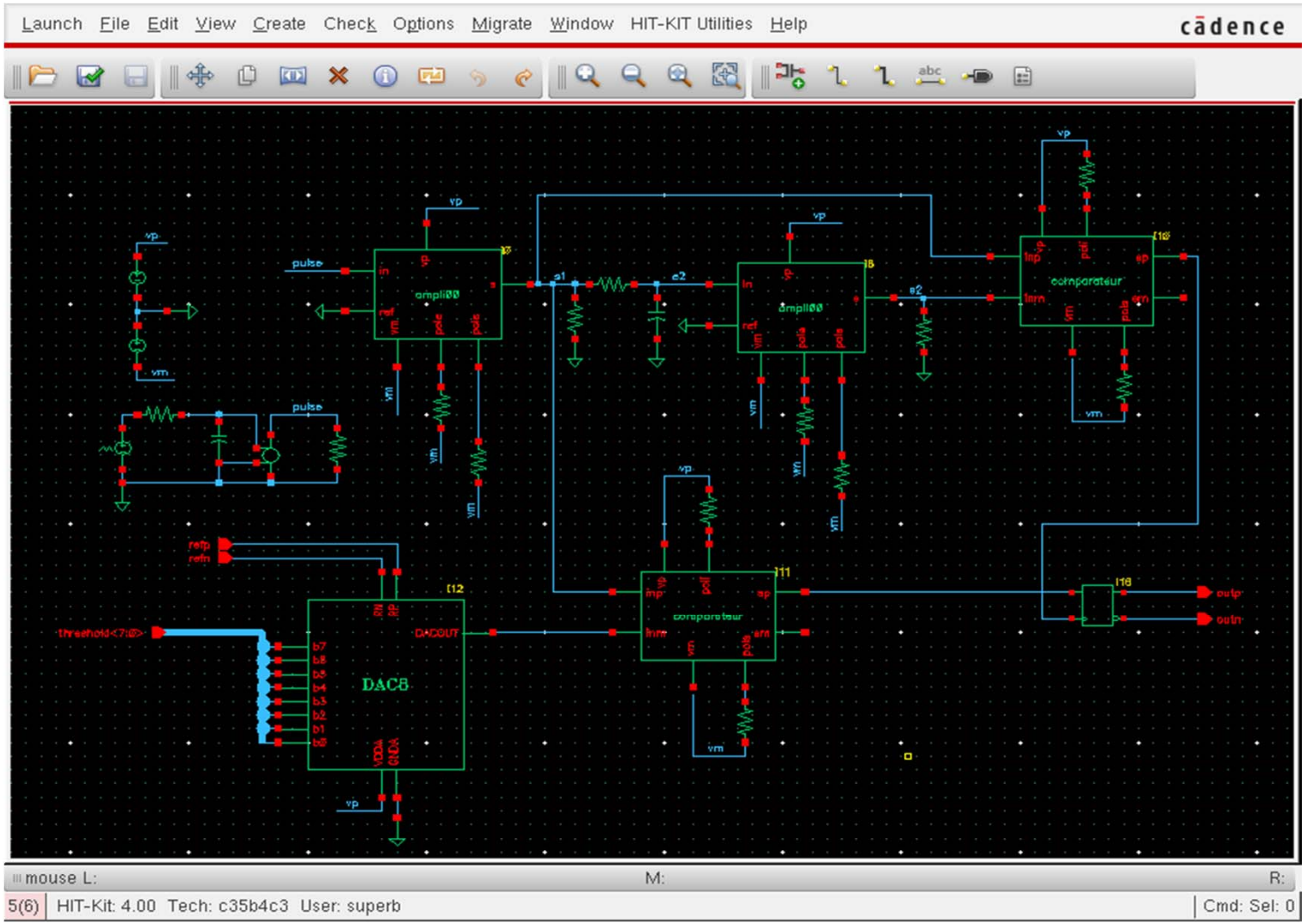
Simulations



CFD Implementation

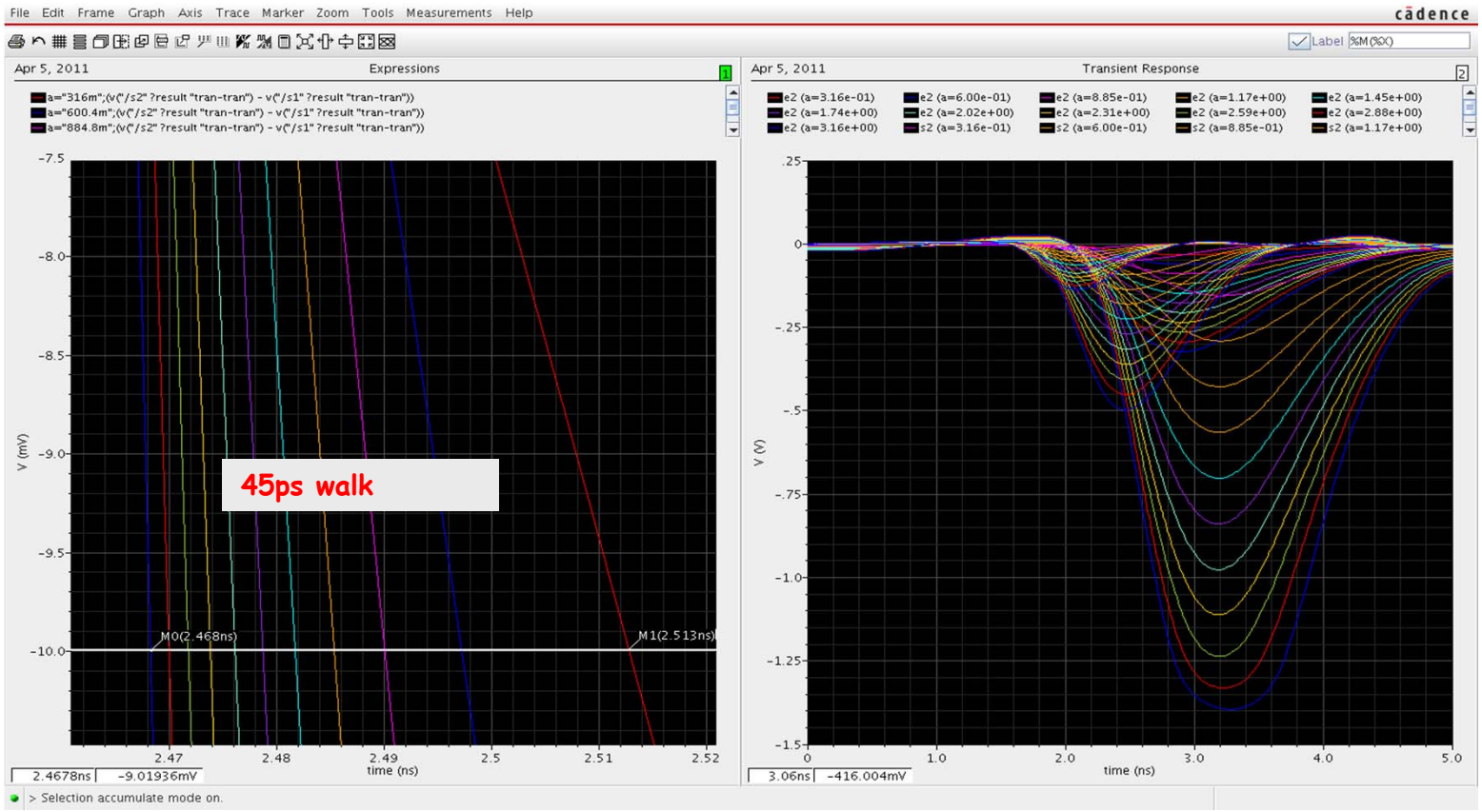


Simulations with AMS CMOS 0.35µ



Simulations with AMS CMOS 0.35µ

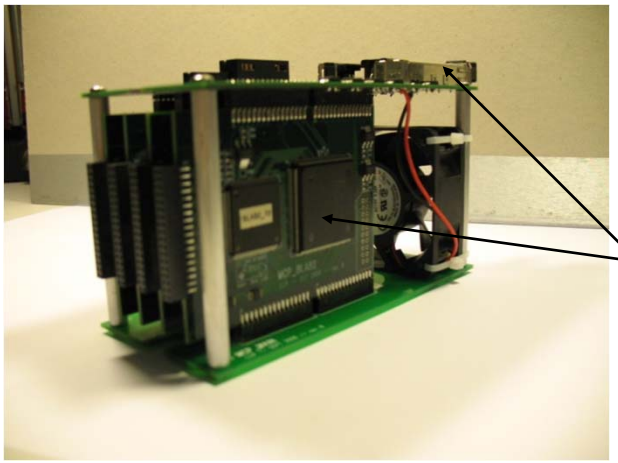
Parametric simulation : amplitude from 1 to 10



Resolution:

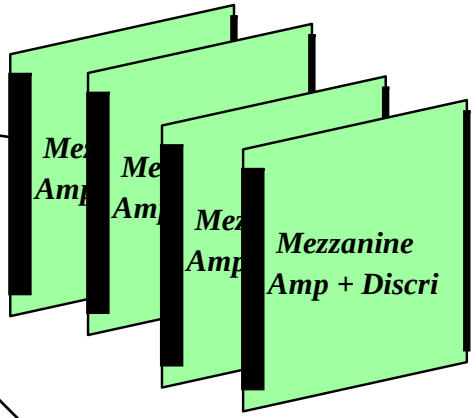
- ↳50ps for a dynamic of 100
  - ↳86ps total resolution

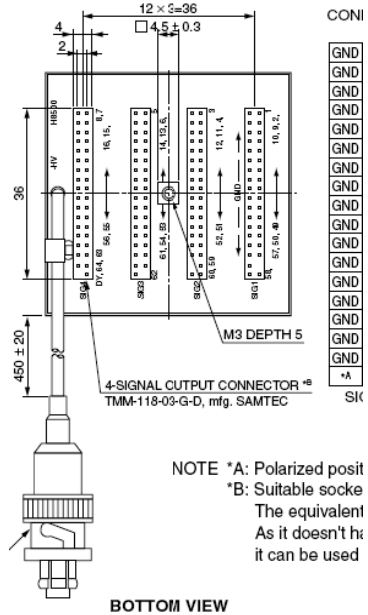
Banc de test (LAL)



Hamatsu footprint
= > 64 channels

4 boards per MAPMT.

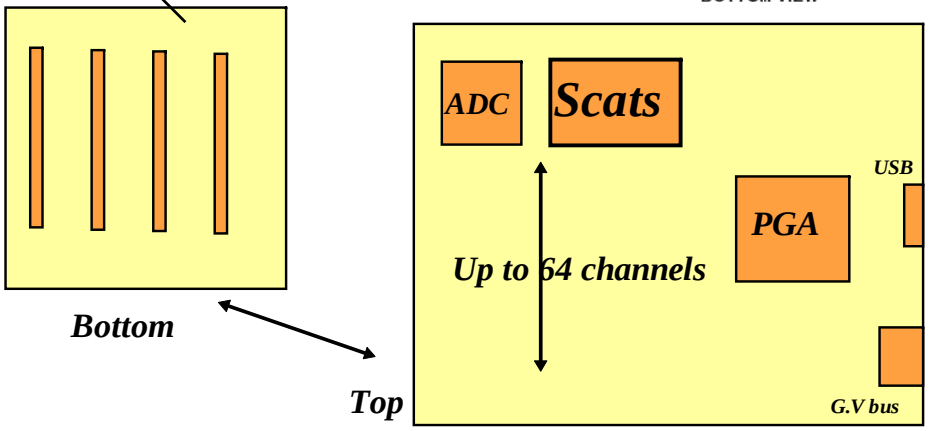




Up to 16 channels on Discri mezzanine

↳Several architecture could be implemented:

- **↳Classical CFD and Charge Amp Channel**
- **↳Simple discri and Charge Amp Channel**
- **↳PIF-like CFD and Charge Amp Channel**



Conclusion

- Le LPNHE a pris le train SuperB

Mais …

- Manque de micro-électronicien pour PIF

- Manque de chercheur instrumentaliste pour un banc de test