Proposal to the ILCSC R&D Panel on Tracking for the ILC
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The SiLC Collaboration

(Silicon Tracking for the Linear Collider)

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Abstract

The SiLC international collaboration is conducting since a few years a program of R&D with as main goal the development of a new generation of Large Silicon tracking systems for the ILC experiments. It is a generic R&D that tackles the different aspects of this tracking technology whether or not it is coupled to a gaseous detector. This document presents the motivations and the main R&D objectives of this collaboration, namely R&D on Mechanics, Sensors and Electronics as well as the tools that are developed in order to achieve these challenging R&D goals. This includes simulation developments and studies and set-up and running of various Lab test benches and Test Beams. The already achieved results are presented including the development of the collaboration and its collaborative efforts. The milestones and R&D needs are discussed as well. Emphasis on the synergy with the construction of LHC trackers and their upgrade is also stressed.

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Several members of the SiLC collaborations are members (HIP Helsinki, LPNHE Paris, Charles University Prague and IFCA Santander) or associated partners (IMB-CNM/CSIC Barcelona, IEKP Karlsruhe, University of Liverpool, State University of Moscow, State University of Obninsk, IFIC/CSIC Valencia, HEPHY-Vienna) to the EUDET, FP6 I3 E.U. project.
Several contracts between different partners of SiLC, these last years:
Contracts CICYT-MEC/IN2P3-CNRS between LPNHE and IFIC and IFCA
Contracts DOE of LPNHE with SCIPP-UCSC and SLAC or FNAL .
Contract France-Japan: LPNHE and KEK
Collaborative contacts with CERN (A. Honma and A. Marchioro)
Collaborative contacts with DESY (especially for the beam test infrastructures)
Collaborative contacts with B. Cooper and M. Demarteau at FNAL.

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Introduction

This proposal presents the ongoing work of an international R&D Collaboration, ***SiLC*** (**Si**licon tracking for the **L**inear **C**ollider) that concentrates since several years on the developments of a new generation of Large Tracking systems based on the use of the Semi-conductor technologies. This proposal follows quite a natural plan for the presentation. It starts with a first section (Part I) that describes the present status of the Collaboration in terms of partners, their personal interests and expertise in the field. This section also outlines what R&D on tracking is needed for the ILC, why Silicon tracking technologies is well adapted to the requirements pointing at the same time where are the still weak points of this technology and the ways to improve them. It finally discusses the roles of Silicon tracking components in detector concepts with or without a central Gaseous detector, i.e. a TPC device.

The second part presents in some details the various R&D objectives that are tackled by this collaboration, presenting the achieved first results, the ongoing work and the future prospects for the next 3 to 5 years. The main R&D objectives are focusing on the three basic topics: R&D on Mechanics, R&D on sensors and R&D on Electronics. It is followed by a part that describes the tools the overall collaboration have at disposal or is developing. This includes the various types of simulation packages, the Lab test benches and the Test beam program that actually started in 2006 and will extend these next years. All this test activities is closely related to the EUDET, E.U. Infrastructure Program under the FP6 program to which a part of the SiLC Institutes are directly participating but that it is being largely opened to all the other SiLC collaborators including those from Asia and US.

The last part, Part IV, discusses the organization and resources matters as well as the milestones. At the end is added a list of references especially pointing to some presentations or written documents that may be useful to read in order to complete this proposal.

PART I: Collaboration , R&D Motivations

The Main goal of the SiLC R&D collaboration is to develop the ***next generation of large Silicon tracking systems*** especially focused on the ILC case but with a clear synergy with LHC present construction and future upgrades of the tracking systems. The synergy also extends in various ways to the applications of this tracking technology to astro particles experiments.

The SilC collaboration was started in 2002 and the launched collaboration was requested to submit a proposal to the PRC DESY, in May 2003 [1]. The collaboration already gathered a fair fraction of the Asian, European and USA Institutions that are taking part to this enterprise. The work of the collaboration was reviewed 2 years later, in May 2005 by the same committee [2]. Early 2006, some components of this collaboration took an active part in the setting up and writing of the EUDET E.U. proposal of the FP6 call for applying for funding on a project based on developing the infrastructures for test beams.

It is important to point out that this is a ***generic R&D collaboration*** i.e. that addresses all the main issues concerning the design, development and construction of a Silicon tracking system for the ILC, whereas or not there is a TPC as central tracker.

I-1:The Collaboration

The collaboration presently gathers about 20 Institutes and 90 to 100 people. The detailed list of Institutions and of SiLC collaborators is given in pages 3 and 4. The main features of the R&D Collaboration are summarized here below:

- ***Generic R&D*** on Large Silicon Tracking system for ILC: this is made possible by the fact that SiLC gathers teams that are part of the GLD, LDC and SiD. Many of these teams have signed Detector Outline Documents (DOD) of more than one detector concept. This makes SiLC a unique place to compare tracking for several detector concepts.
- ***Worldwide:*** the collaboration gathers Institutes and Laboratories from Asia, Europe and USA as shown on the list of participants. Many of the participants have been or are already collaborating on other experiments.
- A ***large expertise on the various aspects of the whole field*** is widely spread in the collaboration. This comes from the involvements of these teams in previous experiments or experiments in construction (LEP especially DELPHI, B Factories with both Babar and Belle, Tevatron especially CDF, all the LHC experiments (ALICE, ATLAS, CMS, LHCb and TOTEM) and also astro particle experiments as in particular GLAST).
- ***Synergy with LHC and the LHC tracking upgrades:*** Many SiLC collaborators, as just stated above, are taking an active part to the construction of the Silicon Trackers at LHC and consequently are being involved soon in the R&D for the upgrade of those devices at the LHC. Moreover there are close contacts with the CERN teams involved in these tracking systems and it will be clear in the description of our work how this synergy impacts on various of our R&D objectives.
- ***Important R&D infrastructures in several Labs in SiLC***
  Several Institutes have developed over the time very well equipped Laboratory or workshop facilities to develop, test and build the various components of such devices.
  Among the best equipped Institutes: HIP Helsinki, Liverpool University, CNM-IMB/CSIC in Barcelona, IFIC/CSIC-University of Valencia, Torino University, IEKP Karslruhe, Moscow State University and SiLaB, Korean Institutes [3].
- ***Close contacts with International Labs*** (CERN, DESY, FNAL, KEK) where test beams have or will be occurring. These contacts are established between different Institutions in SiLC because of their past or ongoing collaboration with experiments in these Laboratories.
- ***Collaboration contacts with Industrial Firms:*** because of the already strong expertise of many teams in various aspects of the fields and the connections they developed with Industrial Firms, the collaboration is benefiting from already established collaborative contacts with Industry. New ones are also being developed corresponding to the needs on novel technologies. These collaborative contacts will be mentioned in various parts of this R&D proposal, let's list among the already existing collaborative contacts: ETRI, Micron, E2V, Hamamatsu HKP, VTT and SiLab for the sensors; ST Microelectronics, UMC (via EuROPRACTICE and IMEC), IBM (via MOSIS and CERN) for the Deep Sub Micron FEE chips developments or TSMC for the TOT alternative. Several firm for building boards including sophisticated treatments of Silicon devices (thinning, bump bonding), also including Microelectronics Laboratory (IMB-CNM/CSC in Barcelona).
- ***EUDET involvement:*** Several SiLC Institutes are part of the EUDET E.U. project as members: HIP Helsinki, LPNHE Paris, Charles University in Prague and IFCA-University of Cantabria (4 members) or as associated Institutes: IMB-CNM/CSIC in Barcelona, IEKP University of Karlsruhe, Liverpool University, Moscow State University, Obninsk State University, IFIC CSIC– University of Valencia, HEPHY-Vienna, which are part of this EUDET project, as the ***SiTRA*** (***Si***licon ***Tra***cking) activity (See subsection IV-4-1 and [4]) .

This involvement of some of the SiLC collaborators in the EUDET project is beneficial for the whole collaboration (see Part IV). The infrastructures developed within EUDET are made indeed available to all the SiLC collaborators.

[1] T. Blass et al., The SiLC Collaboration, *SiLC Silicon Tracking for the Linear Collider*, PRC-DESY R&D 03-02, Submitted April 10, 2003 and Addendum PRC-DESY 03-02 update 01 (03), see also: http://www.desy.de/f/prc/html/documentation.htm
[2] T. Blass et al., The SiLC Collaboration, *SiLC Silicon Tracking for the Linear Collider*, Status Report, PRC-DESY R&D 03-02, Update 03(02), submitted May 26, 2005, see also: http://www.desy.de/f/prc/html/documentation.htm
[3] The Website of these various Institutes gives access to their Lab facilities, see for instance: http://www.cnm.es/ , http://www.vtt.fi/, and various Labs presentation during the SiLC collaboration meetings.
[4] SiTRA is part of the European project on Infrastructures: *EUDET: Detector R&D towards the International Linear Collider,* see: http://www.edudet.org/

I-2:Why R&D on tracking is needed?

The needs for an R&D on the tracking system are discussed both in terms of the Physics requirements for the next machines and especially the ILC and of the Machine environmental imposed stringent conditions.

I-2-1 Physics motivations on tracking (required tracking performances by Physics)

To exploit the physics potential at the International Linear Collider (ILC) highly performing detectors are required in order to achieve very small systematic uncertainties. Tracking detectors will need a perfect 4π coverage up to very low polar angles, an excellent momentum resolution and a good two-track/two-hit separation. Furthermore very low mass materials are required to be used for the detector components, services and all frames and structures in order not to hinder the energy reconstruction in the calorimeters. The optimal layout, as well as the best detector technology for each angular region which can be afforded, need therefore to be studied in detail.

While there are still many unknowns on what direction physics will take and hoping for new findings at LHC some quite general arguments can anyhow be formulated regarding the operation energy of the ILC:

1. Top physics will remain an important topic to be studied with high accuracy even after LHC being started. First to better understand and measure some of its Standard Model properties such as its mass. Second to signal for new physics in processes and signatures for which LHC could not be sensitive enough such as polarizations and asymmetries for which the tracker is essential. Identifying and reconstructing b-jets, leptons including the $\tau-$lepton, the jet-jet invariant mass and the jet-charge are of most relevance for observing top final state topologies,

2. Higgs physics either in the Standard or beyond the Standard Model will be probably found at LHC but understanding its nature and properties in detail will still need complementary studies at the ILC. Reconstructing two lepton invariant masses with high accuracy will be very important in most of the final state topologies of these analyses,

3. Search for SUSY final states, so important to know about the nature of the dark matter, will require an excellent performing tracker enabling for the identification of lepton and quark flavours together with an almost perfect 4π coverage to avoid inefficiencies in missing energy studies,

4. Exotic physics covering many models such as Extra Dimension, little Higgs, composite models etc.., will require in general the best possible jet energy and direction reconstruction plus flavour identification mainly for b-initiated jets. This has to be accomplished in hostile conditions due to the jets being very energetic and collimated.

Quantifying the above arguments in studies performed for the ILC conclude that the detectors need to have a very high hermeticity, with the only hole of about 5 mrad given by the beam pipe, one order of magnitude better than LHC track momentum resolution and one order of magnitude less material in the tracker.

Seemingly insignificant changes in the design of some other subsystem or the accelerator may lead to a significant shift of the optimum parameters. Similarly, new physics insights [from the LHC] may change the accepted dogmas. Therefore, a continuous effort is needed to keep the simulation infrastructure up-to-date.

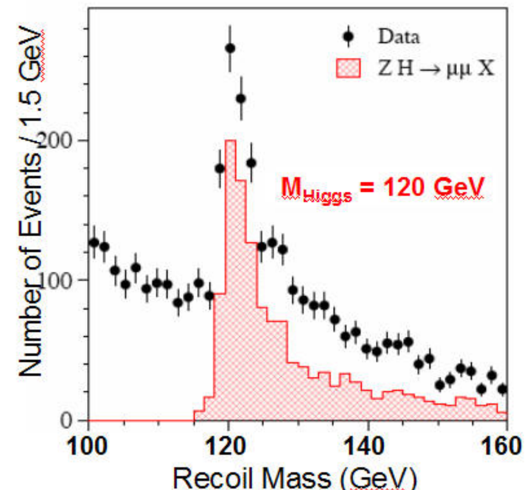
How the two basic tracking strategies (i.e. all-Silicon or Silicon+TPC) compares in terms of Physics achievement (including on certain crucial regions as the large angle region) needs to be carefully studied. The association of the detector tracking technologies, either gaseous or silicon and the accuracy required in the various angular and detector regions necessary to meet the physics goals also needs to be understood. Where to use silicon detectors either based on strips and /or pixels technologies complementing or replacing other tracking subsystems is one of the main objectives. All these key questions are on the to-do-list of the SiLC collaboration and are indeed underway.

Hence to accomplish the above challenges a complete R&D program needs to be developed for the whole ILC detector concept and in particular for its tracker.

Track parameter resolution

The **core business** of the tracker is the determination of the particle momentum with highest precision. Is is therefore only natural that the transverse momentum measurement is the most important design consideration.

The ability to reconstruct the Z bosons from their leptonic decays sets the required performance of the central tracking system. The Z reconstruction is needed, e.g., for the study of the reaction $e^+e^- \rightarrow ZH \rightarrow l^+l^-X$ used to extract the Higgs boson mass by the recoil mass method. The accuracy on the measurement of the recoil mass against the Z decay will only be limited by the expected beam energy spread (about 0.1% at the ILC). The "figure of merit" is to reach a resolution $\Delta(1/p) \leq 5 * 10^{-5}$ (GeV/c) $^{-1}$ **in the central region**, for momenta greater than about



50 GeV, where the multiple scattering starts to dominate the resolution.

The recoil method consists of making a fit of the recoil mass spectrum using as free parameters the Higgs boson mass, the mass resolution and the signal fraction. A template is used to parameterize the signal shape by using HZ simulation which includes initial state radiation and beamstrahlung, and an exponential for the background shape. The figure[1] shows the recoil method mass peak for a 120 GeV Higgs boson.
The resolution of the Higgs boson mass obtained by this method is independent of the nature of the Higgs boson decay, and by itself gives a precision of about 150 MeV for a Higgs mass of 120 GeV with an integrated luminosity of 500 fb^{-1} and center of mass of 350 GeV. When combined with 4-C fit in Higgs boson hadronic or WW* decays, the precision can be improved . The expected $\delta(M_H)$ resolution goes from 40 MeV for a Higgs mass of 120 GeV (in this case the 5-C fit of the four-jet channel gives better resolution than the recoil method) to 70 MeV for a Higgs mass of 180 GeV.[2] The accuracy in the mass measurement can be improved if the track momentum resolution improves beyond the level of $\Delta(1/p) \leq 5 * 10^{-5}$ $(\mathrm{GeV/c})^{-1}$.

The accurate determination of the centre of mass energy (c.m.e.) is a prerequisite for this and other physics studies. One undesirable aspect of the ILC is Beamstrahlung, the induced photon radiation from an electron or positron of the beam in the field of the colliding bunches, which produces an average energy loss of the order of 1.5%. Fortunately , the luminosity spectrum can be obtained from data by studying the acolinearity distribution of Bhabha events, with an experimental error much lower than the natural beam energy spread of $\leq$ 0.1%, if in the **forward region**, the resolution $\Delta(1/p)$ is better than $\leq 3 * 10^{-4}$ $(\mathrm{GeV/c})^{-1}$ and the angular resolution $\Delta(\theta) < 2 * 10^{-5}$rad for $|\cos\theta| < 0.99$.

To make precise mass measurements, as for M_W from a cross section threshold scan for the above cited M_H from the recoil mass spectrum, those effects of Beamsstrahlung must be well quantified.

Beamsstrahlung photons can interact and produce hadronic final states, deteriorating the performance of the physics analysis. Studies[3] indicate that this contamination is mainly produced at low angles, so the degradation on the resolution of Higgs boson mass is only a few MeV. But it can be more important in processes such as as WW-fusion.

Another possibility which can give an even better resolution of the c.m.e. is the method of the luminosity weighted c.m.e.., by using muon pair production, $\mu\mu(\gamma)$, and radiative returns $Z\,\gamma$, where the Z decays to muons. This method was already used at LEP, but the improvement on the momentum resolution expected in ILC indicates that it could be the best method for the determination of the c.m.e.[4]

Other physics process which can be measured with a high precision are the masses of new particle produced in the supersymmetry cascade process $e^+e^- \rightarrow$ a pair of sleptons$\rightarrow l^+l^-$ plus neutralinos. In this case the technique of the end-point of the lepton spectra can be used[4 5].

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[1] J. A. Aguilar-Saavedra et al. TESLA Technical Design Report, DESY-2001-011, 2001
[2] P. García-Abia et al. hep-ex/0505096
[3] K. Desch et al. LC-PHSM-2004-009
[4] M. Battaglia et al. hep-ex/0603010 (2006)

[5] S. Gerbode et al., LCWS 2005, hep-ex/0507053

The slepton mass is determined from the endpoints of the momentum distribution of their decay lepton. In the case of non degeneration in mass between the neutralino and the slepton, provided a good track momentum resolution, studies shown that the dominant effects on the accuracy of the slepton mass are the beam energy spread and radiative tail, and the dependence on the momentum track resolution is soft. But in the case of nearly degeneration, the tracker momentum resolution determines the accuracy of the determination of the slepton mass, due to its strong influence on how sharply the spectrum falls at the upper end-point.

Most of the precision studies are very much related to the tracking resolution and can be very much improved if the performance of the tracking is better. If the track momentum resolution is good enough, some physical process, as $H \rightarrow \mu^+\mu^-$ can be distinguished from the main background $e^+e^- \rightarrow W^+W^- \rightarrow \mu^+\mu^-\nu_\mu$ anti$-\nu_\mu$ from the distribution of the di-muon invariant mass as a sharp resonance peak[6].

Taking into account those physics goals, the **design** specification requires a large tracking volume, large magnetic field, excellent Rf resolution and a large number of measurement layers.

The transverse momentum resolution for high momentum tracks shows only marginally sensitivity on the tracker material. As it was indicated above for low momentum tracks, on the contrary, multiple scattering dominates the momentum resolution. Therefore, there is a certain tension between the requirement of excellent transverse momentum resolution for particles at low and high momentum.
The low mass of electrons renders them particularly sensitive to the tracker material. For the energy measurement of high-energy electrons the electromagnetic calorimeter clearly is in a better position. In this case, the role of the tracker is reduced to the identification of the electron, i.e. the rejection of clusters in the EM calorimeter due to photons (from π^0 decay). Reconstruction of low energy electrons with sophisticated algorithms (i.e. Gaussian Sum Filter) yields a competitive energy measurement.
Naturally, the track impact parameter resolution is of crucial importance for the vertexing and flavour tagging performance, a vitally important tool in the selection of a large range of signal topologies. The resolution is, however, entirely dominated by the performance of the vertex detector and depends only marginally on the layout of the intermediate and outer tracker elements. Therefore, arguments based on impact parameter resolution provide little or no guidance for the design of the SiLC elements.

Pattern recognition

The second class of requirements is related to pattern recognition. The physics programme relies on "excellent pattern recognition". The definition of specifications for pattern recognition is not straightforward. Most guidance comes from the tracking efficiency, which is intricately related to the pattern recognition. The overall efficiency of the track reconstruction in the ILC is required to be greater than 99 %.

The efficiency should be evaluated in relation with the purity that is required. The optimum working point should be chosen for each specific analysis.
There are three main sources of impurities. Fake tracks are more or less random combinations of unrelated hits that happen to satisfy the track model. These can generally be rejected efficiently by the application of track quality cuts, at a small price in efficiency. For

[6] M. Battaglia and A. De Roeck, Snowmass 2001 Summer Study, hep-ph/0111307

distorted tracks the parameters are mis-measured due to the inclusion of one or more extraneous hits. As these trajectories essentially satisfy the track model, they are not easily rejected by the usual cuts. The third source of impurity is the background from unrelated bunch crossings. To reject this latter category (a sub-set of) of the tracker layers should provide an accurate time-stamp. Given the technologies envisaged for the vertex detector, this is likely the task of the SiLC detectors. Given the spectrum of the pair background due to beamstrahlung the natural choice seems to be the tracking layers immediately beyond the vertex detector.

The obvious way to achieve the required "excellent pattern recognition" is by "brute force" over constraining of the global track fit, i.e. by adding more layers. A tracker with a large number of detector layers yields robust tracking performance that is essentially insensitive to layer inefficiencies. The down-side of this solution is the degradation of the overall detector performance due to the extra layers.

The alternative road to "excellent pattern recognition" is toward a layout and layer technologies with intrinsically good pattern recognition properties. In this approach, ambiguities are generated at a very low rate and can largely be resolved locally. It requires a layout that minimizes the extrapolation uncertainty: small distances between layers and little material. Even more importantly, the layers should measure two coordinates and the occupancy should be kept low. In this case, the challenge is to develop a technology that satisfies these requirements at an acceptable cost, channel density and power consumption.
Realistic detector solutions are a blend of both approaches. In the following a few special cases and their specific requirements are discussed.

Long lived particles, Conversions
Reconstruction of particles that do not traverse the whole tracking volume presents a challenge to pattern recognition.

Control of the tracking efficiency for the products of decays that occur beyond (the first layer(s) of the vertex detector) is of particular interest to flavour tagging. A significant fraction of (energetic) b-jets decays beyond the first vertex detector layer(s). Long-lived particles like Lambda's and K0s and photon conversions are an important source of misidentification of jets initiated by a light quark.

Decay products of photon conversions can originate at any point in the tracking volume. Reconstruction of the tracklets and their vertex allows recovering photons that would otherwise be lost, particularly interesting when the photon is one of a pair originating from decay of the Higgs boson.

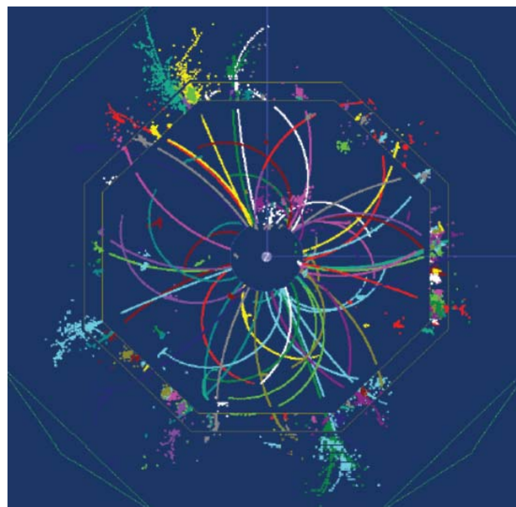
Reconstruction of non-prompt tracks requires a flexible seed-generation scheme. Ideally, it should be possible to initiate track reconstruction cleanly and efficiently in any set of [consecutive] layers.
Moreover, reconstruction of tracks that leave hits in only a sub-set of detector layers poses a special challenge to the pattern recognition performance of ALL layers. Sub-systems cannot rely on the combination with other detectors, but should be able to resolve the ambiguities locally. This implies that all layers should provide precise space points and sets a severe constraint on the allowed occupancy.

Particle flow

The ILC experiment(s) intend to take the requirement for jet energy measurement a step further than what has been achieved in previous experiments. A key concept to achieve this goal is „particle flow“.

Quite generally, the effectiveness of the approach is limited by the imperfections in the association of calorimeter clusters and charged tracks: overlapping showers, track reconstruction inefficiencies and confusion.

While the basic concept is not new, new opportunities arise as a new generation of calorimeter concepts has emerged. The highly granular, longitudinally segmented devices allow to "track" the whole build-up of the shower. Individual particles in the shower are clearly recognized in figure below. These calorimeters are very well suited to the association of tracker and calorimeter information that is central to the particle flow concept.



The adoption of the particle flow concept leads to stringent requirements on the reconstruction of all – primary and secondary - particles in the event. Efficient and pure track reconstruction cannot be limited to prompt tracks with relatively large momentum.

The reliance of the particle flow approach on the matching of tracker and calorimeter information intricately links the design of both subsystems. The distance and material between the last tracker measurement and the face of the calorimeter has become a crucial parameter. Thus, pattern flow requires a careful layout of the tracker and especially of the routing of its services.

Tau-lepton jet reconstruction

Efficient reconstruction of the tau lepton is mandatory, given the relevance of the third lepton in many new physics scenarios, most notoriously in the Higgs sector of the Minimal Supersymmetric extension of the Standard Model. Approximately two-thirds of t-leptons decay hadronically. The decay of energetic t-leptons yields extremely collimated jets. This feature is exploited by applying a tracker isolation criterion that rejects much of the contamination due to hadronic (mini-)jets. Reconstruction of the displaced decay vertex [ct is 45 mu m] and determination of the vertex mass allow to further refine the selection.

Efficient track reconstruction in the narrow t-jets poses a stringent requirement on the two-track resolution of the whole tracker.

In **conclusion**, two major classes of detector requirements have been discussed, as well as how their origin in the challenges of the ILC physics programme.

The main design consideration for the tracker is the transverse momentum resolution, driven by the requirement of precise reconstruction of heavy resonances decaying to muons.

The second requirement is excellent pattern recognition. The tracking efficiency should be greater than 99 %. The rate of fake and distorted tracks should have negligible effect on the performance. A precise time stamp should be provided to reject the background from unrelated bunch crossings.

Reconstruction of decay products of long-lived particles and photon conversions require pattern recognition to converge even if it acts on a sub-set of the tracker layers is available. This requirement implies that the ambiguity of hit association in ALL layers should be minimal.

The particle flow concept sharpens the requirements on pattern recognition in two ways. The requirement of efficient track reconstruction is extended to all tracks, including secondary and low momentum tracks. Moreover, the association of tracker and calorimeter information requires a careful layout, especially of the tracker services.

Finally, reconstruction of energetic tau-jets poses a severe constraint on the two-track resolution.

The somewhat qualitative nature of several arguments in this contribution reflects that still a lot of simulation work on many of these issues has to be undertaken in some detail. The SiLC collaboration is preparing to tackle and hopefully remove some of the uncertainties in the next year, thanks to a task force that is taking place on the simulation front (See section III-1).

I-2-2 Machine Environmental more and more stringent constraints, Machine Detector Interfaced related issue

In an e+e− linear collider, the detailed design of the accelerator beam transport close to the interaction regions (IR) must be strongly coupled to the detector design and influences several aspects of the physics program. For this reason, a collaboration of both accelerator and experimental particle physicists has formed to specify and study what has been named the Machine-Detector Interface (MDI) system. In the context of the Global Design Effort (GDE) set up to design the TeV-scale International Linear Collider (ILC), the MDI system is recognised as having a very high priority. The overall goals of the MDI are to control and minimize beam induced backgrounds in the detector, enable beam diagnostics in the vicinity of the detector as needed both for beam parameter tuning at the Interaction Point (IP) and for several physics analyses (e.g. energy calibration, polarimetry, fast luminometry and very forward $\gamma\gamma$ veto) and more generally to ensure optimal conditions for the experimental physics program (e.g. magnitude of crossing-angle at the IP, minimum radius for the vertex detector, optimal distance between the last optical element and in IP,…).

I-2-2-1 Beam Induced Backgrounds Sources

A number of different processes create backgrounds related to the beam which are potentially problematic for the detector. The main sources of such backgrounds are:

- Beamstrahlung created in the interaction of the tightly focussed electron and positron beams. Beamstrahlung has a two different components:
    - Photons, radiated into a very narrow cone in the forward direction;

  - Electron Positron pairs, radiated into the forward direction, but, different then the photon, sensitive and deflected by the central magnetic field of the detector solenoid.

- Synchroton Radiation, created in the beam delivery, in particular in the final focusing elements.
- Muons created by interaction between beam elements and tails in the electron or positron bunches, and transported through the tunnel into the detector.
- Neutrons created mostly in beam-line elements both up- and downstream of the experiment.

Although particles from the beamstrahlung go primarily into the very forward direction, and mostly exit the detector together with the outgoing beam, a small but still significant fraction obtains a large enough transverse momentum to hit detector or beam line components, and interact with these. Particles created or backscattered in these interactions are a major source of background in the detector.

I-2-2-2 Background Estimation

The consequences of the different background sources discussed in the section above have been studied in simulation for all detector concepts. To simulate the beam-beam interaction the Guinea Pig and the CAIN programs have been used. The output from these programs is the subjected to a complete and detailed simulation of the different detectors, which are based on GEANT3 and GEANT4. The simulations have been done, for the nominal parameter set, but some studies have been performed for a range of parameters as well (see Fig.1).
The most recent studies include an Anti -DID field and are based on a 14 mrad crossing angle scenario. In a few cases the changes of results expected for different crossing angles (2 and 20 mrad) are shown for comparison [1,2,3].

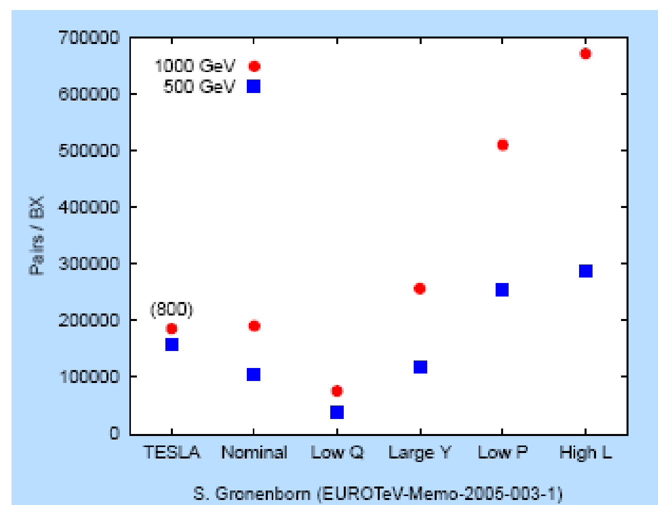


Fig1: ILC Beam Parameters set.

- *Pair Background*

Electron Positrons pairs are created in great number in the interaction of the primary electron - positron bunches. They travel mostly in the direction of the outgoing beams. The magnetic field will tend to focus one type of particle, and tend to defocus slightly the other, depending on the direction of travel. A small number of pairs obtains a large enough transverse momentum to enter directly into detector components. By far the dominant source of backgrounds however are secondary particles, created in the interaction of pairs with detector or machine elements. These secondary particles travel back into the detector, and create background hits.
The detector most sensitive to this is the vertex detector. Its innermost layer sits at in a radius of between 1.3 and 1.55 cm from the interaction point. The number of hits outside the Vertex detector radius of around 15 cm very quickly becomes rather small. For a SI based tracking system as SIT they are not a real concern. For a TPC based tracking, where a large (O(100)) bunches is integrated into one picture of the tracker, they are potentially more important. The total occupancy of the TPC in this case is far below one percent, and does not present a problem.
In a few rare cases, pairs induced background creates particles of high enough energy to actually create tracks in the detector. Their number is small and does not present a problem.
The pairs background produces a significant neutron background in the detector. Most of these neutrons are created in the in electromagnetic showers in the hot regions of the innermost calorimeter, and the closest beam elements. The origin of neutrons is illustrated in Fig 2, together with their energy spectrum. These neutrons are important for a number of reasons: The Si-based vertex detector and trackers are sensitive to damage. In the detectors equipped with a gas filled TPC the neutrons can create spurious hits in the gas. The possibly most affected detector however is the end cap of the calorimeter, in particular the hadronic calorimeter, where the neutrons create spurious hits, and contribute to the confusion term in the particle flow measurement.

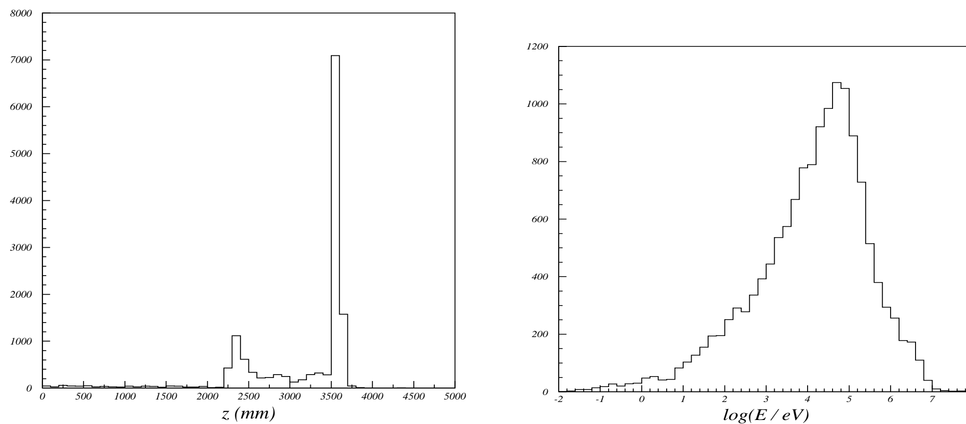


Fig. 2: Position of the major sources for neutron background in the detector as function of the position along the beam (left) and the enrgy distribution of the neutrons which reach the TPC(right). Courtesy of P. Bambade.

- *Photon background*

A by-product of the beam-beam interaction is a large number of photons, which are radiated primarily in the forward direction. These photons carry a significant amount of energy. They

follow within a very narrow cone the direction of the incoming beam, and are thus mostly exiting the detector the detector through the outgoing beam hole. Nevertheless there are tails in the distribution of these photons to larger transverse momenta, so that some photons hit the different elements in the beam line in the very forward direction. Similar to the case with pairs, these photons initiate showers in the forward detectors, and some particles from these showers make it back into the detector. Next to pairs, particles created from beamstrahlung photons are the second most important background in the detector.

Others sources as synchroton radiation from final doublet quadrupoles, beam halo from the main linac and collimation system and backscattering from losses in the extraction line has to be estimated with the standard full detector programs as MOKKA or using accelerator programs as BDSIM.

- *Implications for sub-detectors*

The implications of the background numbers on the sub-detectors have been studied with different levels of detail. While the vertex detector is closest to the beam pipe and therefore suffers most from background hits, a lot of studies have been performed and the design of the vertex detector has been optimised with respect to the expected background fields [3].
For all other sub-detectors an estimation of the expected occupancies has been made from simulation studies. As the occupancies per readout are expected to be on the percent level or less, no problems from the pair background are foreseen.

For the TPC the situation might be more complicated. The backgrounds do not only lead to hits increasing the occupancy, but also to the production of charged ions in the TPC gas. As the reconstruction of the tracks depends critically on the knowledge and uniformity of the electric field in the TPC this extra charge might lead to field distortions deteriorating the achievable resolutions. Detailed studies about these effects are underway, preliminary results are shown on [3].

In the case of the FTD there are some preliminary results (Figs: 3 and 4) from [3].
But a detailed calculation taken into account the full parameters space of the ILC is necessary to optimize the forward region.

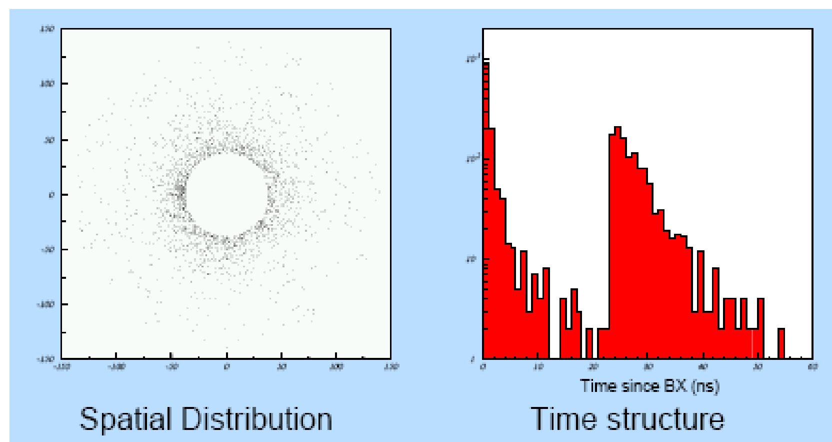


Fig3: Hits on the innermost FTD (overlay of 100 BX) calculated by MOKKA.

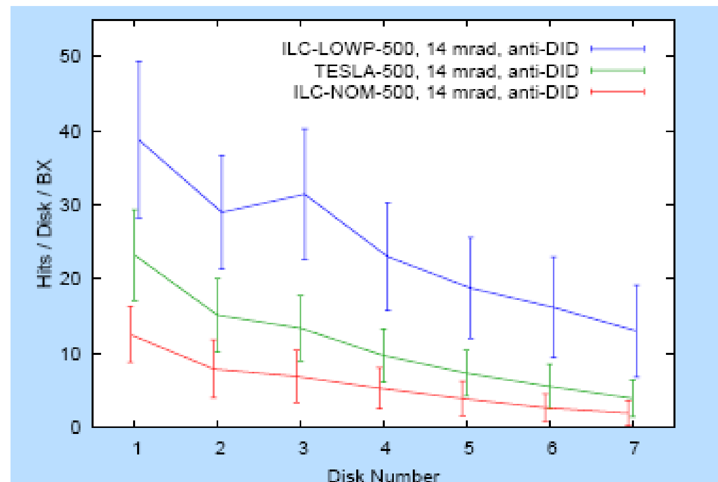


Fig. 4: Hits per disk per bunch crossing for the FTD, for different parameters set of the ILC with a crossing of 14 mrad.

I-2-2-3 Outlook

The understanding of the interaction region of the ILC and its impact on the detector performance has matured remarkably over the last few years. Good simulation tools are available and serious studies have been done to understand the background situation. It should be noted that the SiLC collaboration includes collaborators that are part of the MDI and beam experts. This is a real asset that we are starting to take more and more advantage of. It is especially crucial for the studies that are undergoing now on the design of the innermost parts of the various detector concepts (with or without a TPC as central tracker). It will be an essential tool to develop the R&D on the sensor technology, on the Front End Electronics related issues and to better include in the detailed simulation tools especially in these regions.

In general designs of the interaction exist now which seem to control the backgrounds at a level acceptable for the detectors. A particular emphasis of the recent past has been the implementation and the consequences of an anti-DID field, beneficial for the operation of the accelerator at large crossing angles. It appears that with an anti-DID field backgrounds are controllable and not significantly worse than at small crossing angles.
As already stated, the background numbers shown here for FTD are still preliminary. A detailed optimisation of the forward region is under way and will most probably influence the background numbers. When this is finished, the full parameter space of ILC parameter sets and detector configuration has to be explored in full detector simulations.
Besides the pair induced backgrounds, other background sources, e.g. muons produced in the linac and collimation system of the machine, backscattering from losses in the extraction line, have to be reviewed. Equally important is the progress on the understanding of the detector tolerances.
A note of caution though is in place: all conclusions rely on simulations, and have not been tested experimentally. Therefore a significant safety factor should be assumed in the design of the detectors, maybe as large as a factor of 10, for all background rates.

[1] K. Buesser, “MDI Questions to the Detector Concepts”, Snowmass 2005.
[2] K. Buesser, “The Large detector with Relistic Magnetic Fi elds”, Snowmass 2005.
[3] A. Vogel, “Beam Induced Bacgrounds in the LDC Detector”, ECFA ILC Workshop Valencia 2006

1-2-3: Technological requirements and constraints

Some general remarks should be added related to special features of this R&D topic, i.e.:

- It is a very challenging R&D programme that relies on several high tech aspects.
- These technological fields are highly skilled and competitive; it thus require close collaborative contacts with industrial firms.
- It therefore also require strong collaborative efforts to avoid dispersion or duplication and for sparing money.
- It needs high expertise in several aspects; inheriting expertise from previous experiences is a real asset as well as inheriting the industrial established contacts.
- These fields are rapidly evolving technologies in contrast with the agenda to built the detectors. Therefore there is balance to be found between not freezing solutions too quickly and keeping in line to be ready in time

These facts must be taken into account for the various aspects of this R&D, and so does SiLC.

I-3: Why Si tracking?

To answer to this question this subsection reviews the pros and cons of this tracking technology and emphasizes the roles of the Silicon trackers in a tracking system with or without a gaseous central detector.

I-3-1 Pros and cons of this tracking technology

The expected performance of the tracking system for the ILC calls for a detector that should provide an excellent track separability and spatial resolution. Since the early 80's, when the first silicon sensors using the planar technology for their fabrication were employed in a particle physics experiment, silicon has become a must for the tracking devices. The reason is that being a condensed medium it provides the means for an excellent spatial resolution, its 1.1 eV band gap is low enough to ensure prolific production of charge from a particle traversing it, but high enough to avoid high dark current values so, provided that the environment is not excessively harsh, the operating conditions are quite comfortable. In the ILC environment it provides stable, robust and reliable operation with no need for continuous calibration -just for the electronics- and does not have any particular requirements for handling or environmental conditions, like pressure or temperature. It is also a low Z element with excellent mechanical and thermal properties which makes it ideal for a tracking device where the multiple scattering is a concern (and it certainly is for the ILC). Its mechanical properties allow to build these sensors in various shapes and sizes allowing for many different geometries and implementations of the required granularity: pixels, strips, etc. Finally, though the scientific applications are of great importance, they are dwarfed by the use of silicon detectors for mass industry products (CCDs, CMOS imagers, photonics, etc.) and so it does its associated electronics.

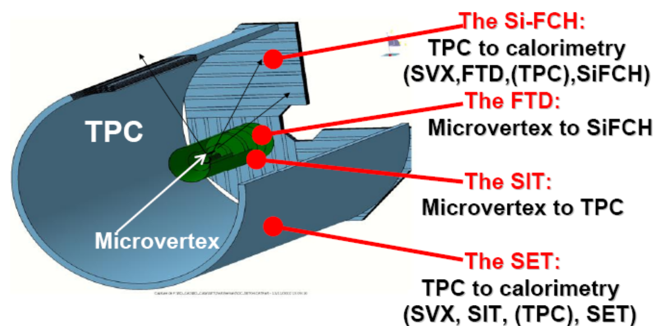
However, the same reasons that make silicon a material beyond compare in a tracking detector define the issues that should be carefully considered when building a system based on this type of sensors. On the one hand, large areas are to be covered in a tracking system with a material which is produced in sizes which are small in comparison. Constructing the support structures that will hold the small silicon pieces together without spoiling the excellent material budget of the silicon is challenging, especially if very stringent constrains on mechanical stability drive the design of such a system so that the spatial resolution is not spoilt. On the other hand, the provided spatial resolution and granularity require a huge amount of electronics channels, making the power consumption and connectivity the main

concerns of the system. Extracting the signal out of the sensors into the data acquisition system is a challenging subject where speed and reliability are of paramount importance. Even if the front-end electronics are carefully designed to keep the power consumption and noise requirements as low as possible, the huge amount of channels may require a careful temperature control of the system in order to avoid an increase of the electronics noise and thermal runaway situations which occur when the high temperature induces higher dark currents in the sensors which, in turn, translate in an increase of the temperature.

I-3-2 The Roles of the Silicon tracking

The GLD, LDC and SiD detector concepts mainly differ by their tracking strategy and the role they give to Silicon tracking. The two first ones propose a TPC as central tracker whereas SiD proposes an all-Silicon tracking system. Whether or not there is a TPC, the tracking system needs Silicon tracking. How to best include Silicon technology and why, in a tracking environment with a TPC, is studied, by several members of the SiLC collaboration. The Korean Group is instrumental for the GLD Silicon tracking system, currently made of 4 layers between the vertex detector and the gaseous device, and a set of 7 disks similar to the inner forward design in LDC. LPNHE proposes a Silicon tracking system complementary to the TPC in LDC. In parallel, LPNHE and other teams in SiLC are taking part to the all-Silicon tracking system as elaborated within the SiD concept. Being in the same R&D collaboration is a real asset: SiLC is a unique place to study and compare these various tracking concepts.

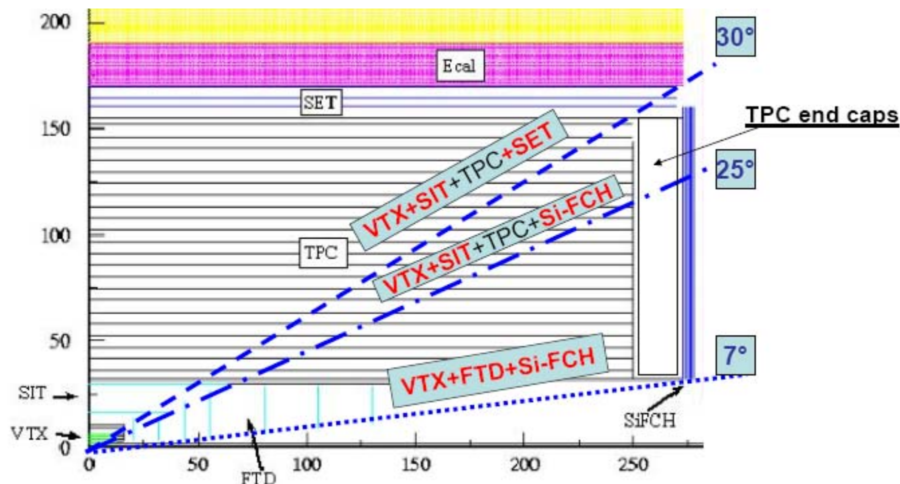
Let's discuss the various possible solutions and the roles of Silicon tracking [1]. If a TPC, an ensemble of Silicon detectors is proposed, surrounding the TPC and forming the *Silicon Envelope* [2]. It consists of 4 tracking components: two in the central barrel with one in the innermost region, near to the vertex detector (called Silicon Internal Tracker, SIT in LDC) and the other one at large radius, just in front of the e.m. calorimeter (called Silicon External Tracker: SET in LDC). Similarly in the Forward/End Cap region, there is the set of disks tracking (called Forward Tracking Detector, FTD [also called here SiFCH for Silicon Forward chambers] in LDC) and the Silicon layer(s) just in front of the End Cap e.m. calorimeter (called the End Cap Tracker, ECT). Figure here below gives a schematic view of this system.
This Silicon ensemble provides improvements of performances especially in momentum resolution, ensures the complete coverage of the tracking system, provides a calibration tool for systematics effects in the TPC, and provide redundancy to the overall tracking system.



Schematic view of the Silicon Envelope as a system of Si trackers surrounding a central TPC.

Each of its component play a role of link: SIT is the link between the vertex detector and the gaseous device; SET is a link between the TPC and the calorimeter and can give a very useful entry point for the tracking in the calorimeter and the set vertex detector plus SIT plus SET acts as a useful standalone tracking system in the barrel; FTD is a link between the vertex detector and the ECT, useful in a region where the TPC is almost not anymore active; ECT

links the TPC (and /or the FTD) with the End Cap calorimeter. A detailed study simulation of the various improvements that such a system add to the central gaseous device is discussed in Annex I.
The role of completing the full coverage of the tracking thanks to these various components is presented in the Figure here below.



Schematic view of the full coverage of the tracking part down to almost 7° with respect to the beam axis, thanks to the various components of the Silicon Envelope.

The approach of GLD is in some respect similar but it should be stressed that instead of having two components surrounding the TPC in the barrel, GLD choose to have only one the BIT (Barrel Internal Tracker). Unlike the SIT, the BIT is made of 4 Silicon layers and thus provides with the vertex detector a real tracking. The BIT is more like a tracker whereas SIT acts more like only a "linker" if not associated to the SET.
It is also interesting to remark that the proposed Silicon Envelope is a kind of "stretching" into two parts of the Silicon barrel tracker considered in a all-Silicon alternative (SiD), and thus allowing the insertion of the gaseous device in between. This makes that the solutions proposed for the different components of the Si Envelope are easily applicable to the SiD case.

To conclude Part I, it is clear that a lot of questions have to be answered about the best design of the Silicon tracking system in the various scenarios. SiLC after first preliminary studies that led to useful contributions is now addressing all these issues in close collaborative contacts with the various detector concepts[3] to which the SiLC teams are also actively participating and with an increased strength in expertise and manpower (see next sections).

References:

[1] A. Savoy-Navarro, *Si Tracking: the Role, Design and Main Issues*, talk at the LCWS05 Workshop, March 18-22, 2005, SLAC, published in Proceedings of LCWS05 Workshop.
[2] J.E. Augustin, M. Berggren, A. Savoy-Navarro, *Study of an external Silicon Tracker: SET*, LC Internal Note: LC-DET-2001-075 also in: http/www-flc.desy.de/lcnotes/ and also:
J.E. Augsutin et al, A Silicon Envelope for the TPC, LC Internal Note: LC-DET-2003-013 See also: http/www-flc.desy.de/lcnotes/
[3] Visit the Websites of the various detector concepts and their DOD.

PART II: R&D main objectives

II-1:Mechanics R&D

Why an "R&D" on mechanics,
Because of main issues to be faced by the next generation of large Silicon tracking systems: low material budget, simplicity of the design and construction and robustness; but even more stringent requirements

II-1-1: Developing CAD designs for various detector concepts

A series of preliminary CAD design (CATIA-based) and detector studies have been done addressing the various components of the Silicon tracking system in an ILC experiment. The main emphasis was on

- simplifying as much as possible the overall design, by trying to limit the number of different types for the fundamental elements of the detector architectures (sensors and elementary modules or ladders)
- paying special attention to the overall material budget
- already addressing general integration issues (integration with the other subdetectors in the neighbourhood, cabling and environmental issues, cooling and alignment)
- already anticipating large scale construction (automatization, semi-automatization, transfer to industry, new tooling needs)
- Developing mechanical prototypes for preliminary mechanical studies

This first series of studies were instrumental for exploring the various possible geometries or new ideas (Silicon Envelope around a TPC central tracker), as well as for developing the GEANT-based detailed simulations. Indeed this has been crucial to define the geometry data base (DB) for the various studied alternatives. An example of this is given in the Part III-1 on simulations with the GEANT-4 picture of the various components of the Silicon tracking in the LDC concept case.
As examples here below are some of the preliminary designs performed for the case of a Silicon tracking system with a TPC central tracker. However let us stress that many of these very preliminary studies are easy to adapt to the case of an all-Silicon tracking system.
As described in subsection I-3, the Silicon tracking system in an experiment with or without a gaseous central tracker, can be subdivided into 4 components: the inner and the outer layers in the barrel and the same two equivalent parts in the end cap or forward/backward regions. There is an undergoing activity in the mechanical side, to study possible CAD designs in these various components.

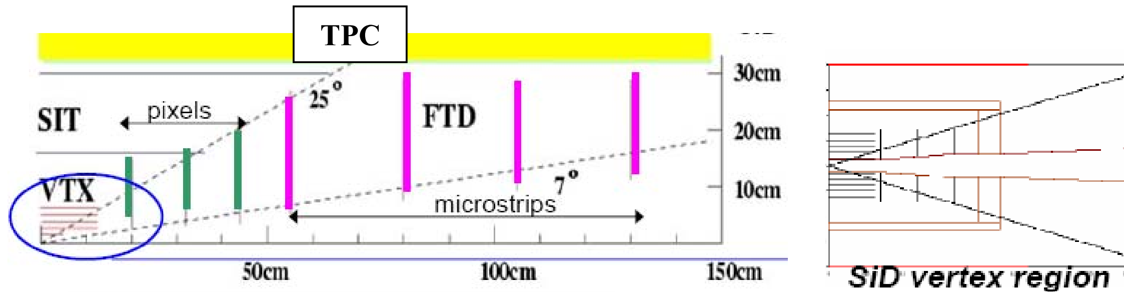
These CAD studies (sort of simulation detector design studies) are very important in order to understand all the various issues tà be confronted when constructing these various components and when integrating them in the overall detectors. Besides they allow building mechanical prototypes for various studies as for instance the thermo-mechanical studies with realistic prototypes. Besides it is an essential tool for the detailed simulation studies.

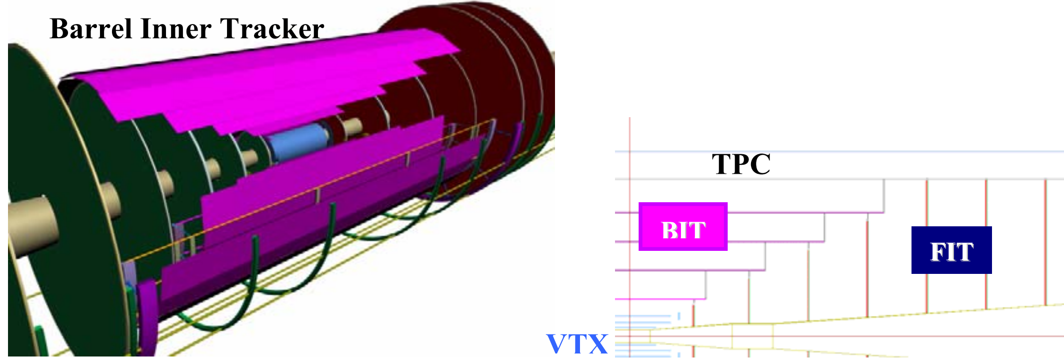
We give here below some examples of the ongoing studies:

Example 1: The innermost components

In the three detector concepts: GLD, LDC and SiD, the innermost tracking part around the vertex detector present essentially the same geometry: internal layers in the barrel and small disks in the forward/backward regions as sketched in Fig here below. The main issue that will be discussed in the section on sensors is about the choice of Silicon sensor technology. Here the strips may be or will be replaced by pixels at least for certain parts. The environmental conditions are in some sense more stringent here also for instance in terms of material budget; of integration with this environment (vertex, beam pipe etc..), need for more sophisticated

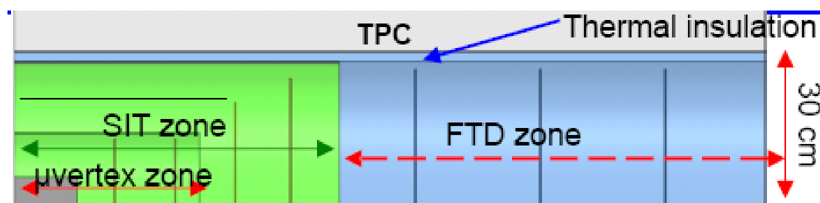
cooling, more difficult alignment conditions. Very preliminary studies were started some time ago and are reported here below. The study is being pursued now with a stronger effort, see section on sensors (especially on pixels), as new teams are joining and interested in working in this special part of the Silicon tracking system (see Section on sensors, pixels and on Simulation).





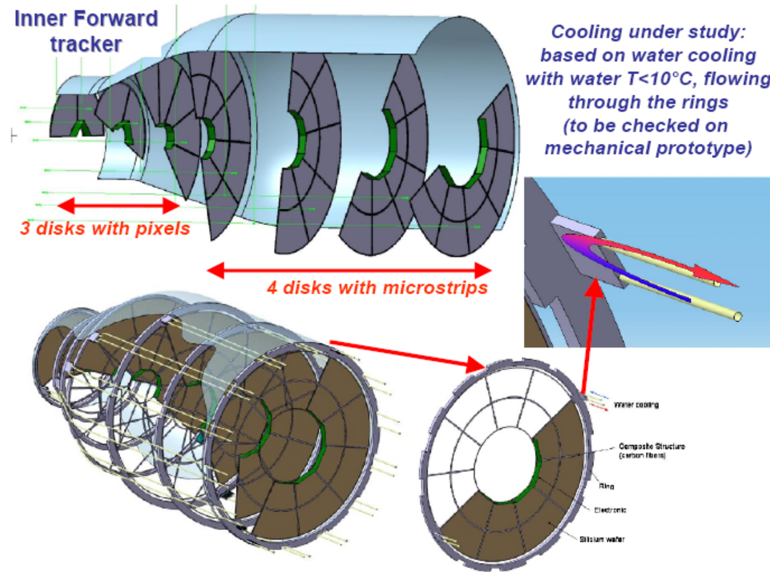
Some examples of innermost Silicon tracking components in the LDc concept (top left), in the SiD case (top right) and in the GLD (bottom)

It should be pointed out here that when looking at the schema of the Silicon tracking near the vertex detector, the three detector concepts: GLD, LDC and SiD have similar ideas in several aspects. The SiLC collaboration has been promoting (see presentations at the Snowmass Summer studies on ILC), the option of considering that the first one or even the two first Silicon layers in the barrel parts plus the first 3 to 4 disks in the forward innermost region could be considered as a "***natural extension***" of the vertex detector. This would translate into possibly borrowing (with some adaptation) the technology used for the vertex at least for part of these components in particular for the central barrel. The ways to integrate these Silicon tracking devices near the beam pipe region is under study. As sketched here below the possibility to integrate these devices within a thin thermal enclosure acting both for thermal and electronics (Faraday cage) insulation.



Schematic view of the inner barrel and forward components of the Silicon tracking near the vertex detector, in the LDC concept case.

This schema is translated in a very preliminary approach for the inner forward disks, just to give an idea of the type of studies that are undertaken.

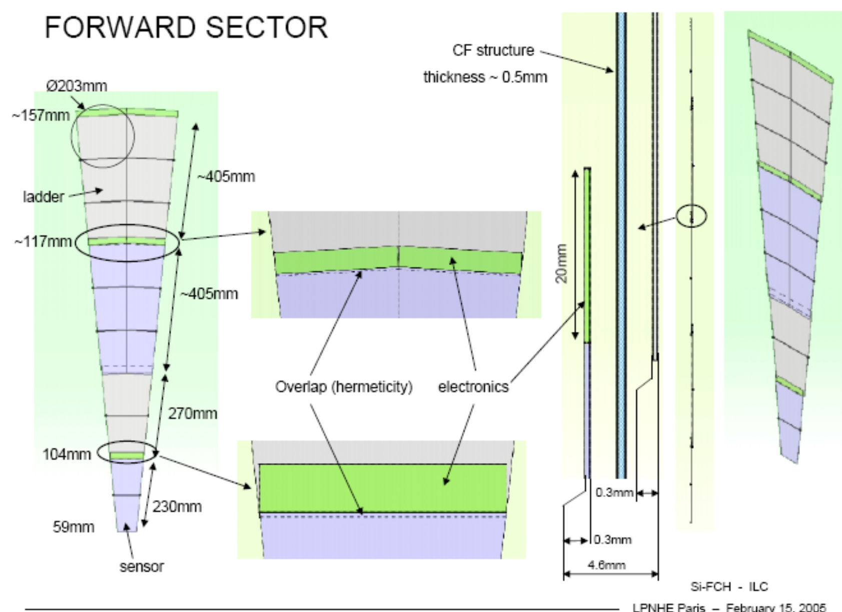


CAD design as a very preliminary attempt for studying the overall inner forward Silicon tracking in the framework of the LDC concept.

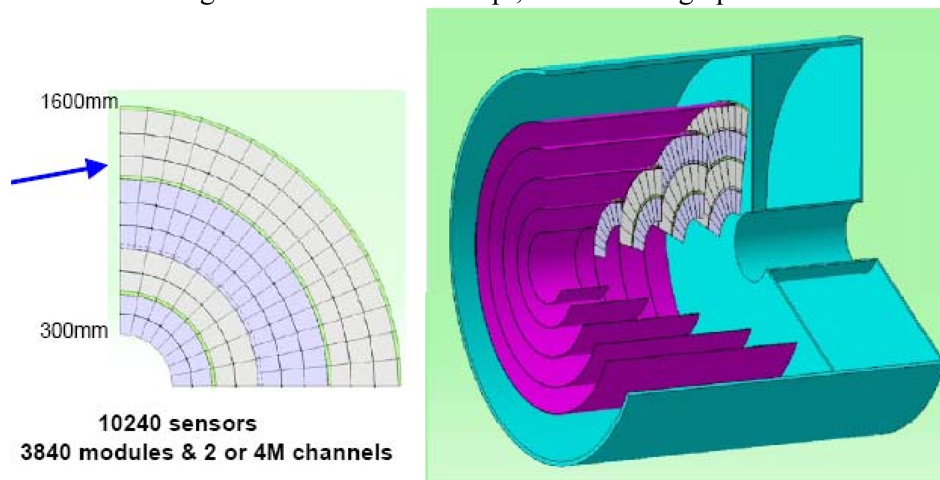
This CAD study has been completed by a thermo-mechanical study on the cooling system for such a system in this peculiar environment, thanks to a mechanical prototype featuring the part of this Silicon device and of the possible thermal insulation.

Example 2: CAD design for the End caps Silicon devices

Another region of great importance in the overall design of the detector is the large angle or End Cap layers that are sitting near the End Cap calorimeters. Two geometries have been studied, the projective and the XUV options. Some examples of possible designs in both options are presented here below.

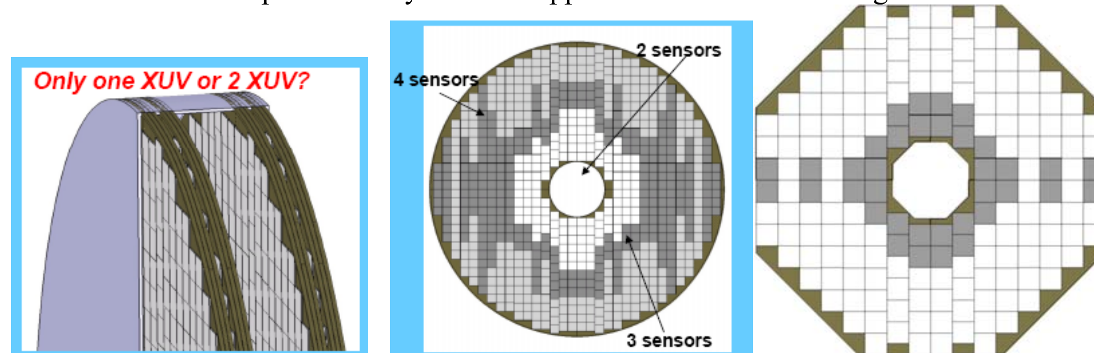


The projective approach design is shown in the Figure here above, for the outermost layer, in the case of a large radius detector concept, i.e. extending up to 160 cm radius.



A projective large radius layer quadrant (left). The projective End Cap design applied to the case of SiD (right)

These preliminary design studies show the feasibility of this option even applied to large detector size. It also shows one feature that makes this approach less attractive, namely the number of different size sensors of a peculiar trapezoidal shape each. This is a feature confronted by the builders of End Cap Silicon trackers at LHC. Many of them are questioning this approach and would recommend a simpler approach in order to reduce the number of different types and size of sensors and elementary modules (or ladders). Therefore we have considered another option namely an XUV approach as shown in the Figure here below.



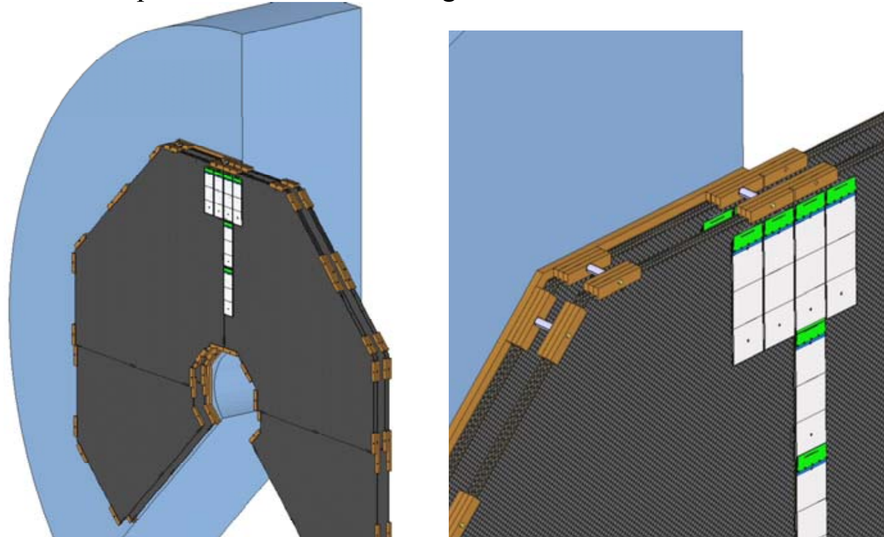
The XUV design applicable again both in a all Silicon or Silicon + TPC case. On the left: two XUV modules for the LDC concept case. On the middle, one layer with 10x10cm² sensors assembled in ladders with 2, 3 or 4 sensors each depending of the radius. On the right one layer with an octagonal frame and made of 20x20cm² sensors, assembled in ladders with only one (grey) or 2 sensors (white).

Note that this architecture is easy to adapt to the overall frame of the calorimeter i.e. a cylindrical or octagonal frame. The figure here below shows some details of the structure designed in this XUV approach, and to the paid attention, already at this very early stage, to the integration of these sub detectors.

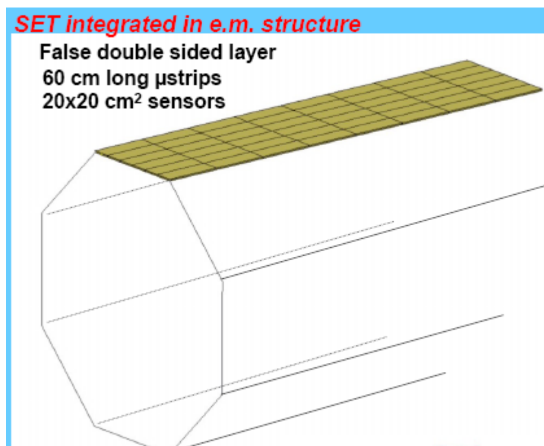
The attractive features of the XUV approach are that it is:

- Simple to design
- Easy to built

- Easy to adapt (integrate) to the design of the sub-detector surrounding it.
- Possibly based on use on a single sensor,
- Possibly based on the same ladder construction than the large layers in the central barrel,
- Therefore "universal" type of sensor and of ladder construction for these Silicon detector components that cover the largest area of the Silicon trackind ensemble.



Integration of the XUV Silicon End Cap layers with theEnd Cap calorimetry



The Figure on the left side shows a schematic view of the largest radius Silicon layer made with the same types of sensors and elementary modules than in the XUV case for the End Caps layers. This is also a possible design for the SET (Silicon External Layer) proposed by siLC for the LDC concept.

The effort on CAD designs include now the design of detector prototypes that will be built for the test beams this year and the following ones. Much work need still to be done, indeed this is just a beginning. But SiLC is now benefiting of the increase in manpower and expertise on this item as the LHC construction is touching to its end. Several aspects of the R&D on Mechanics are discussed in the next subsections.

II-1-2: The elementary modules

A particular attention is devoted to the elementary module that will be the key piece or fundamental tile to build the overall detector architecture and to ensure the requested detector's performance from both mechanical and physics points of view. The main issues to be confronted are therefore to have a elementary module, easy to build and assemble, with an overall very low overall material budget (depending the location the aim is to have from 0.5% in the innermost region up to 0.8% in the outermost regions, all services included), possibly as

unique as possible (avoiding the plethora of different modules depending the tracking component). The elementary module is indeed closely related to the front end electronics on-detector. In some sense there constitute a unique device although these two aspects will be discussed in two different sub sections (II-1-2 and II-2-1). It should be also noted that SiLC is considering different possible strip lengths (*typically from 10cm up to a maximum of 60cm; There is also a "long ladder" approach for the all-Silicon case (SiD) with strips as long as one meter or even more, proposed by SCIPP-UCSC, see II-1-2-2*) for the elementary module and that the unification will be more at the level of the basic micro strip sensor size that could be used for all or most of the applications, i.e. tracking components (see discussion on this topic in previous sections).

II-1-2-1 A novel approach to construct them

The design and efficacy of carbon fibre shells as a support structure for the SiLC tracker will be investigated. There is considerable expertise within the Collaboration in this area. For example, Liverpool engineers designed and manufactured the supports for both the inner layer of the CDF vertex detector, layer00, shown in Figure 1, and the mechanical support frame for the tracker of the Muon Ionisation Cooling Experiment (MICE), illustrated in Figure 2. The layer00 design provides a low mass cylindrical rigid support structure of radius about 1.5 cm which allows some azimuthal overlap of the CDF strip sensors and incorporates cooling channels. The MICE support is of a much larger scale: the diameter of the carbon fibre ring shown in Figure 2 is about 50 cm. Studies of the support for the SiLC tracker will include variants in which the sensors are attached directly to a carbon fibre shell and also designs in which the sensors are first assembled into ladders and these are then attached to a support frame.

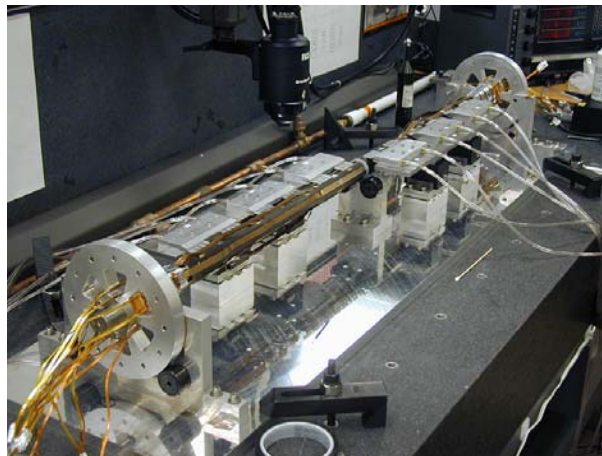


Figure 1 Silicon strip sensors being mounted on the innermost layer of the CDF vertex detector, layer00, at Liverpool; visible is the carbon fibre structure, to which some of the sensors have been attached.

The ladder designs which will be investigated by the Collaboration include foam sandwich structures. These are being studied for the vertex detector of the ILC by the LCFI group, who have demonstrated that both silicon carbide and reticulated vitreous carbon foams can be used to construct stable, extremely low mass ladders.

Figure 2 Part of the carbon fibre support frame for the MICE tracker which was designed and manufactured at the Oliver Lodge Laboratory in Liverpool.

II-1-2-2 The Long Ladders approach

The International Linear Collider will offer a vast potential for precise, definitive tests of the Standard Model and the exploration of a wide range of possible extensions to the Standard Model. The precision and reliability of the detector must meet this challenge. Given this, there is a natural direction for silicon microstrip R&D: to develop the capability to read out long sensor ladders (of 1-2 meters in length) with a minimal number of electronic channels. In addition, the electronics should be versatile enough to provide an optimal solution for reading out shorter strips in the high-rate environment encountered in the forward tracking system. Although the SCIPP LSTFE development is being done with both short and long strips in mind, we believe long strips to be the more challenging limit, and our current design is thus optimized for use with long ladders (~1.5m) of daisy-chained sensors.

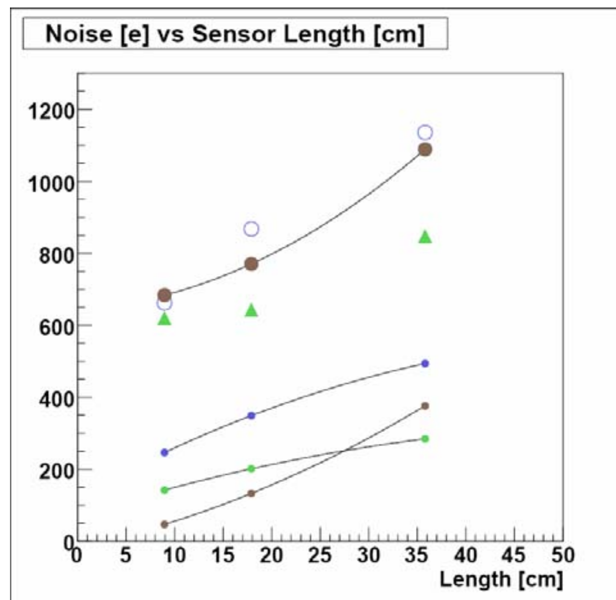


Figure 1: Noise contributions as a function of ladder length, for a ladder composed of GLAST sensors read out by the LSTFE-1 prototype chip. The open circles represent measurement with the actual ladder, while the green triangles represent the measurement made with the ladder replace by a discreet capacitor of magnitude equivalent to that of the ladder (assuming C = 1.2 pF/cm). The small blue, brown, and green circles represent the contributions from leakage current, strip resistance, and bias

resistance, respectively. The quadrature sum of the individual noise sources (large brown circles) is in good agreement with the measurements. The information in this plot is somewhat new, and is in the process of being confirmed.

To limit the noise contribution from the readout electronics, the current LSTFE prototype (LSTFE-1) features a fairly long shaping time (~1.3 μs). We are finding that, at this shaping time, if sensors are not designed with long shaping-time, long-ladder applications in mind, their design will limit the length of the ladder that can be effectively read out by, regardless of the performance of the readout chip.

Figure 1 shows a tentative measurement of the noise associated with reading out ladders made of GLAST sensors with the LSTFE-1 ASIC, as a function of ladder length from 8 to 36 cm (we will soon test a 72 cm ladder). The open circles represent the measured noise, while the large brown circles represent the quadrature sum of all identified individual sources of noise: readout electronics (green triangles), leakage current (blue circles), bias resistance (green circles), and strip resistance (smaller brown circles). For these short- and intermediate-length ladders, the readout electronic noise dominates, although we believe that we will reduce this somewhat for the next (LSTFE-2) version of the ASIC prototype.

Tentatively, then, with the large bias resistance (35 MΩ) chosen for the GLAST sensors, and the low leakage current (~ ½ nA per cm per strip) they achieve, the relative contribution from these sources should be relatively small for long ladders, even with some improvement in the readout electronics noise. More concerning at this point, however, is the contribution due to strip resistance, which grows faster than linearly with strip length due to the combined contribution of capacitance and resistance to the electron-equivalent contribution of Johnson noise from the strips. For the GLAST sensors, which have a resistance of about 3 Ω per cm per strip, the 64 μm wide strips are roughly five times wider than they would be for a 50 μm pitch detector, leading to a contribution 2-3 times less than one might expect for a 50 μm pitch detector. Thus, strip resistance is a potentially large contribution for long ILC ladders. This contribution may be addressed to some degree by using high-conductivity aluminium, maximizing the strip width, maximizing the strip thickness, increasing the readout shaping time, and optimizing the shaping behaviour of the readout. At this point, however, it seems that some concerted attention should be paid to addressing the contribution of strip resistance to the readout of long ladders. Design of microstrip sensors for use at the ILC, if intended to be used in long (> 0.5m) ladders, must be done with a realistic notion of how the various noise sources will affect the final system. Specifications for bias resistance, leakage current, and especially the nature of the readout strips, must be carefully considered.

II-1-2-3 Developing the tools for constructing the modules:

The construction process of a module has a number of aspects that should not be decoupled from the installation and integration issues. A bottom up process, starting just from research on components and building up to the final system design leaves, at the end of the day, very little room for recovery from inadequate decisions. One of the most important lessons from the LHC trackers (CMS and ATLAS) is that the whole system should be developed in parallel from the very beginning.

Of paramount importance is the early engagement of industry in the process of the component design and integration onto the module in order to achieve realistic production procedures and schedules. Failure in doing this has shown to be some of the hardest problems in the production of the ATLAS tracker, with very tight schedules. Involvement of industry in the

production of the module itself has always been a subject of conflicting debates. Both the ATLAS and CMS tracker collaborations opted for multiple production lines, favoring redundancy, flexibility and safety. Yet, this approach is expensive in tooling and resources: the cost of maintaining a number of teams committed for 3 to 4 years can be as expensive as

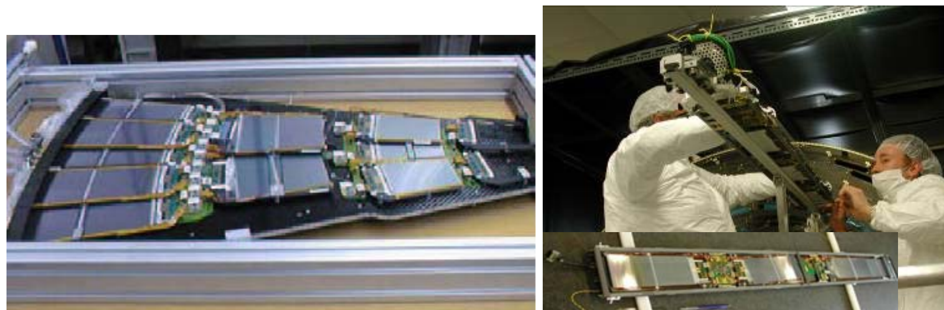


Fig.1. Left:A CMS petal, the basic structure of the forward detector. Right: A CMS rod, the basic element of the outer barrel detector and the basic way to insert it..

the components. Ten institutes participated in the ATLAS-SCT collaboration to assemble their 15392 sensors into modules, while almost twice as much did it for 24328 sensors of the CMS tracker. One of the key lessons learned when building such trackers is that design should be kept as simple as possible and with the minimum of different shapes for sensors and components. Fig. 1 shows the 2 basic components of the CMS tracker: a petal for the forward region (left) and a rod (right) for the outer barrel.

Many other aspects of the module concept influence the production process. The module could be built to tolerances, eliminating internal calibration constants. This has the advantage that the quality assurance assumes a much more influential role. However, the complexity of the module construction may increase.

The collaboration may decide on building a scalable system, with the bonus of having modules completely decoupled and with a final performance which is identical to the first laboratory measurements. In contrast this is an approach in which the services proliferate. One may decide to design the system from bigger substructures that relief the global system by taking over some of the services load. The advantage is that one can test many system issues like cooling, if any, multi-module running etc., before the final assembly of the modules into the final structure.

In any of the cases, it is desirable to automate as much as possible the assembly of these modules. Automated assembly allows producing the modules in a minimum amount of time, quality is reproducible and uniform, the risk of damage due to manual handling of components is minimized and tracking of components can be an integral part of the system. However the level of automation should be kept within a reasonable margin due to the price and uniqueness of the modules. Again, in the case of the LHC trackers, all production steps were automatized, using fully automatic sensor testing, fast industrial like hybrid testers, automatic assembly robots and modern automatic bonders.

The assembly of the modules consists, typically, on the following steps: identification and survey of the components, application of glue, pick-up and placement of components in the desired location and verification of the internal alignment. The fact that all components are flat objects suggests using a gantry type assembly robot to perform these tasks. Equipped with a camera and a pattern recognition system it can identify and survey the components.

Different types of glue dispensers can be used to apply the required glue patterns. A high precision tool head is needed to perform the pick and place using vacuum suction. The whole process should be controlled and documented by software such that the required operator

Fig.2. (Left) CMS gantry. A precision robotic assembly machine, where sensors are automatically aligned and glued. (Right) ATLAS assembly station.

intervention is reduced to a minimum. Related systems are available commercially. However, the mechanical accuracy of a few microns which is usually required for some of the alignment steps is normally beyond their capabilities and, further, they do not provide the desired flexibility and user access. For all those reasons a system like that will have to be developed. The main components of such a system would be, as already mentioned, a 4 axes (x.y.z and XY rotations) gantry robot on a solid base, a camera system with software for pattern recognition, such that by measuring a number of fiducial marks on the components one can accurately align the module components, glue dispensers and a metrology system to verify the correct assembly. The latter could well be performed by the system itself using the camera. Fig. 2 shows the CMS robot employed to align and glue the sensors and the ATLAS-SCT assembly station.

It is also very important to start developing a sort of production database that will allow tracking components and the tests performed on each of them. This is very important not only from the managerial point of view since it also allows for an efficient quality control procedure and permits to optimize the components distribution among the places where the production is taking place. Of equal importance is the establishment of a well defined QA procedure.

II-1-3: The large structure architectures and new materials studies

A typical detector designed for experiments at the high energy collider is installed around an interaction point, has a cylindrical symmetry and consist basically of several subsystems assembled as a “matrioska” doll.

If the accuracy of the measurements is a major concern for the different elements, normally the more stringent specifications are based on the innermost element, typically the tracker.

The actual detecting elements allow us to work with an accuracy better than 10-15μm when we wont to locate the particles trajectory in the space. In order to fully use this very high intrinsic resolution of the detecting elements, it is very important that all parts forming the tracker not to spoil the basic resolution when the detector is assembled.

The mechanical design of the structures is usually based on deflection and not on stress. Therefore it is necessary to maximize the rigidity of the constituent elements. The rigidity can be expressed in general by the product of the Young’s modulus, E, time the length or time the area, depending on the type of stress.[1]

Taking into account the minimization of the multiple scattering, the rigidity can be written as EX_0. This expression depends only upon the material.
As consequence, both, the Young's modulus and the radiation length must be as high as possible. We can use this expression as selection criteria (a good material for a tracker must be light, high X_0, and stiff, high E) and, finally, this will lead to a choice similar to the one for aeronautics and aerospace field.

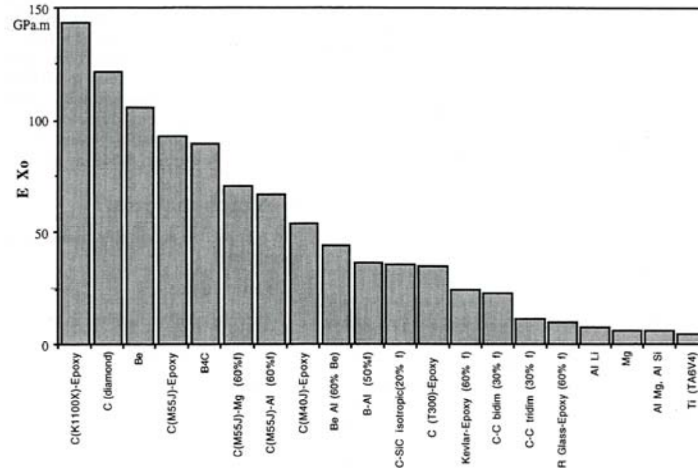


Figure 1. ***EX_0*** **product for some materials**

Environment

A structure is not stable only if the mechanics constraints are satisfied, but we must taking into account that a tracker must operate into a very harsh ambient. Radiation, temperature and humidity and possible coupling effects between them should play an important role when considering position stability of the order of 10-15µm and aging of the order of 10 years or more.
Behaviour of composites imbedded into a strong radiation field is not well understood. Common resin, epoxy or cyanate, withstand high doses, but, up to now, is not demonstrated that a displacement of a micron level will not occur and moreover that the other environment conditions will not even be coupled.
Temperature range inside a tracker volume can be easily controlled and, moreover, the coefficient of thermal expansion of the carbon fibre is close to zero in the direction of the fibre. Is possible to play with the stacking sequences and obtains structures with a well thermal controlled displacement.
When composite materials are exposed to humid environments for long periods of time, their mechanical properties can be altered, in particular if the humidity field is cyclic. Moisture has been observed to cause damages by delamination in stratified structures and debonding at fibre-matrix level. Several studies,[2],[3],[4] both theoretical and experimental, have demonstrated that also displacements of several microns will occur when a composite material is embedded into a humid cyclic field. Coating the exposed surface with "hydrophobic materials" can put obstacles or can delay the effect of the moisture.

Materials

When designing composite material structures it is imperative that material properties be available. The purpose of having a complete set of "typical" properties is to be able to design composites structures with a minimum of testing confirmation, after several run of finite

elements simulation, better if the stochastic simulation is used. In this case is useful the knowledge of the scatter that may occur in the properties.

1. Typical properties – Fibres

The carbon fibres are classified into three subfamilies: high strength/low modulus, intermediate strength and modulus and high modulus/low strength.
Due to the reason written above, we are interested to the last family.
The typical mechanical properties of some HM fibres are collected into the following tab.

Fibre type	Strength (MPa)	Modulus (GPa)	Strain (%)
M46J	4210	430	1.0
M55J	4020	540	0.8
M60	3920	590	0.7
K13D2U	3700	790	0.5
K1100	3100	965	0.5

The last two fibres are interesting because their very high thermal conductivity (900-1000 W/m ^{o}K) and are used for heat transfer in cooling system.

2. Typical properties – Matrix

The matrix for fibre composites can be classified into two categories, metallic and non metallic. Only the second one is interesting for us, and in addition, for typical properties of advanced composites for structural application, only structural resin system are good candidates. Structural resins are defined as resins that have modulus greater than 3 MPa and tensile strength greater than 100 MPa. Structural resins are polyester, epoxy, cyanate ester and phenolic.

New materials

During the last years new class of materials has been investigated. At this goal was born the nanocomposites and the nanotubes.
The nanocomposite is a plastic based material with very thin reinforcement, of the order of few nanometres. The mechanical properties, as Young's modulus and tensile strength are incremented up to 50%.
The nanotubes, discovered 1991, are base on the fullerenes, one of the families of carbon allotropes. They are molecules composed entirely of carbon, in the form of sphere, ellipsoid or tube. The nanotubes are cylindrical fullerenes, are few nanometres wide, but can be up to several millimetres in length. The nanotubes exhibit high tensile strength, up to 100 GPa, and high Young's modulus, of the order of TPa.
These new categories of composite materials are under wide investigation for practical application in the field.

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II-1-4: Construction of prototypes and needed tooling

Testing the module concept is of paramount importance. There are a number of aspects to be considered when trying to ascertain the performance of a module. This includes mechanical stability, electrical performance and feasibility of the construction process. Building prototypes should also serve as training towards and refinement of the final construction procedure. The whole process of building the prototypes is an iterative routine in which the final design of the components evolves in parallel and, also important, provides the means to unveil the practical issues that will hinder the production process. The prototypes should serve very well defined purposes as outlined below.
On of the most important issues to be determined is how the electrical performance of a module varies while increasing the complexity of the system. There are various steps that need to be followed during that process that go from single chip characterization to ASIC performance on the module and, finally, module performance in a system. All of them need a number of modules that should be constructed during the development phase.
On top of the workbench tests made on the modules, the so called system test measurements are of overriding importance. They allow to demonstrate that the performance does not degrade when increasing the complexity of the system, moving from single chip to module and, finally, to an environment as close as possible as the nominal running conditions. In the case of the SET and the ETD, one could run together a few ladders mounted in a structure that could exercise the concept of the support, service distribution and grounding. In the case of the SIT and the FTD the concept is less developed but one could use a quadrant of a disc or a cylinder for the case of the FTD and SIT respectively. The aim of the system test measurements, from the electrical performance point of view, is to study possible intermodule effects, like cross talk in the overlap regions as well as checking the immunity of the modules to malfunction of any neighbour. A characterization similar to the one made on a single module should be done in order to compare the performance parameters.
Finally, using test beams will determine the response of the modules to real particles and should allow for the determination of tracking efficiency, spatial resolution, signal over noise ratio, charge scale determination, that is, proper threshold calibration in terms of charge in the event of choosing binary electronics, timing, etc. This tests on the beam can be done both at CERN and DESY.

II-1-5: Alignment systems

Precise alignment and positioning are crucial systems in order to be able to build and to achieve the very high spatial resolution performances requested for such detectors in the ILC environment. Adding the smallest possible material budget in the overall tracking system is another crucial issue.

The SiLC collaboration is considering two alignment systems

- The ***Frequency Scanned Interferometry (FSI) system*** as developed by the University of Michigan at Ann Arbor. This is the system that was considered since the beginning by SiLC (see proposal and status reports to the PRC-DESY) and it is indeed pursued by our collaboration. This system is also part of the SiD R&D proposal presented to this panel and therefore we refer to this proposal, as proposed by K Riles, for the details of this system and its present status. It is foreseen to have the first realistic tests with this alignment system, with a prototype adapted to our requirements, hopefully by next year (see Part III-3), as discussed in our last SiLC Collaboration Meeting after the presentation of this system (see slides presented by Haijun Yang at the SiLC meeting in Barcelona).
- A new project for alignment started in the SiLC collaboration in 2006, called the ***hybrid approach***. It is developed by the IFCA/CSIC-University of Cantabria and is part of the EUDET E.U. program of SiTRA. It is based on the existing expertise on alignments system of the IFCA team as well as on their learning experience at the CMS experiment.

The FSI system aims to have much below the one micron resolution accuracy, while the hybrid approach should succeed to get 2 to 3 microns resolution. Comparison of these two systems on realistic basis, i.e. when included as prototypes in a test beam and possible complementarities will be part of the tests as well as of foreseen simulation studies, SiLC will undertake with those two systems.

Hybrid approach: Integrated co-linearity monitors and offline track alignment.

The usual limiting factors in the accuracy of an optomechanical position monitoring system based on laser sources and photosensors are: *mechanical transfer* between the monitored imaging sensors and the active particle tracking elements; and *non-straight propagation* of the reference laser lines. Quite often, extremely precise position monitoring systems suffer from poor accuracy due to the previous two factors. The approach we propose here will solve the first issue and reduce the effect of the second one.

The concept: a natural hardware alignment for silicon-based trackers.

This conceptual design is based on its successful application to the AMS-1 tracking system [1], and on the current developments for the CMS silicon tracker alignment. Externally generated laser beams play the role of pseudo-tracks that will allow for a “fast” initial alignment to be further refined with the track-based offline alignment algorithms.

The main aspects of the proposed concept are the following:

- Collimated laser beam (IR spectrum) going through silicon detector modules. The laser beam would be detected directly in the Silicon modules. The alignment readout is fully integrated in the silicon readout; tracks and laser beam share the same sensors removing the need of any *mechanical transfer.*
- No external reference structures. All the elements of the alignment system (laser beam collimators, steering optics, etc.) are mounted directly on the tracker elements.
- No precise positioning of the aiming of the collimators. The number of measurements has to be redundant enough to reconstruct the detector without any knowledge of the laser beam initial parameters.
- Optical and tracking data will be *combined* to optimise the alignment procedure.
- A minimal impact of the alignment system on the layout of the tracker, easy mechanical integration and negligible contribution to the total material budget.
- Based on previous AMS-1 experience we can project that few microns resolution are expected.

R&D goal: Improving Si-microstrip sensor as photodetectors

From the point of view of the instrumentation, the two keystones of this hybrid approach to the tracker alignment are: non-magnetic hard-radiation fibre collimators, delivering a extremely pure Gaussian beam and the modification of the Silicon modules for increasing sensor transmittance.

The first issue has been already solved in the context of the CMS global alignment for the visible part of the spectrum. Custom-made titanium collimators with a fused silica optical system deliver almost pure Gaussian beams. For our particular application we need to modify the optical design to adapt it to the near IR range.

Due to the short penetration depth of visible light in silicon, only IR lasers can be used for thick layers (300-500 μm) of this material. Depending on the actual sensor layout, transmittances between 20-30% have been measured in the IR region. Absorption of the silicon in this zone is still high enough to produce a signal measurable by the module electronics. Unobstructed propagation through the sensor multilayer is ensured by locally removing the aluminium from the backside electrode (see Fig 1). A multilayer antireflection coating (ARC) is then used to increase the overall transmittance. The geometrical deflection of the beam after the module can be kept at a minimum by mirror polishing of the surfaces of the sensor to optical quality. Further increase of the transmittance ratio can be obtained by thinning of the strips in the area treated with the coating. Both measures (ARC and strip thinning) have been successfully applied by AMS, obtaining an increase in transmittance of 20% with respect to the standard sensor (50% average transmittance at λ=1082 nm). Figure 2 shows a magnified view of the alignment window with the ARC (pink region) surrounded by the bare silicon sensor (blue).

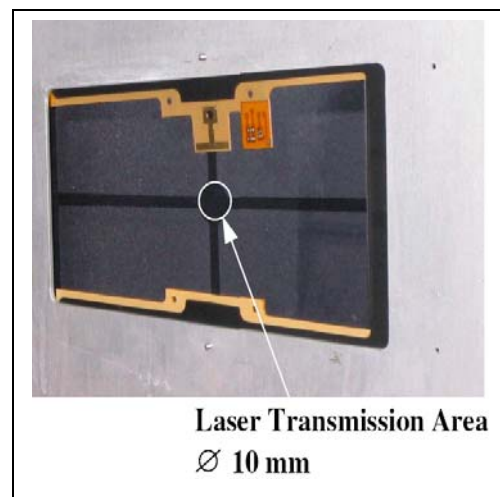

Figure 1: Backplane of a CMS Silicon module. The Al removed alignment area is clearly visible. The laser transmission area has a diameter of 10mm as indicated by the circle.

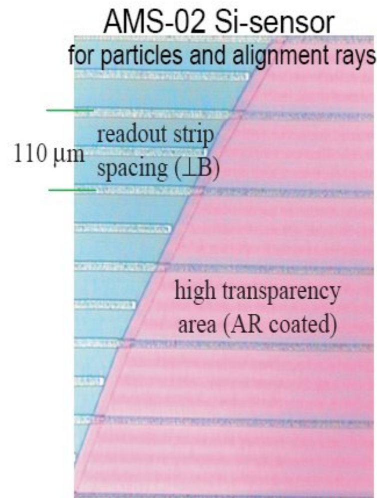

Figure 2: Transition area between uncoated (blue) and ARC (pink) areas. Aluminium readout strips (110 µm pitch) have been thinned by 2 µm. Metallization for capacitance coupling to the electrodes has been removed entirely from the alignment region.

A dedicated test stand for the optical characterization of the Si-modules will be built to measure the sensor coatings and treatments. The characterization of the silicon modules as optical devices is already very well understood since we have carried out this work already on semitransparent amorphous silicon sensor developed for the alignment of the CMS experiment [2].

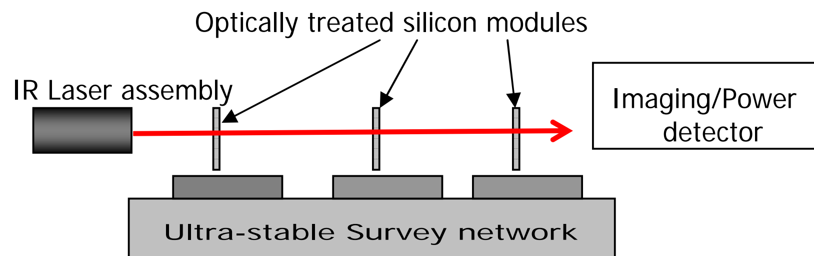

Figure: Schematic view of the proposed alignment system (Lab test bench)

Beyond the antireflection coating, another crucial improvement involving directly the Si-sensor structure will be the replacement of the conventional non-transparent Aluminium backplane and electrodes by a transparent conducting oxide, such as Indium Tin Oxide (ITO) or Aluminum doped Zinc Oxide (AZO) [3]. Besides improving the transmittance of the strips, the interference pattern of the propagated beam will be smoothened due to the lessened backreflected intensity.

We have simulated the optical performance of this new design from the point of view of transmitted and absorbed laser intensity. We have taken the CMS silicon sensor as reference, where the Al electrodes have been substituted by thin layers of ITO (approx. 100 nm each). Figure 3 shows the transmittance, reflectance and absorbance of the new design over a wide wavelength range. Displayed in the plot is the almost 30% transmittance improvement with respect to the AMS best result. The absorption in the silicon layer ranges between 5-10%, depending on the deposition process and on the working wavelength. In the less favourable case (absorption ~5%), a signal of 200 equivalent MIPs can be achieved.

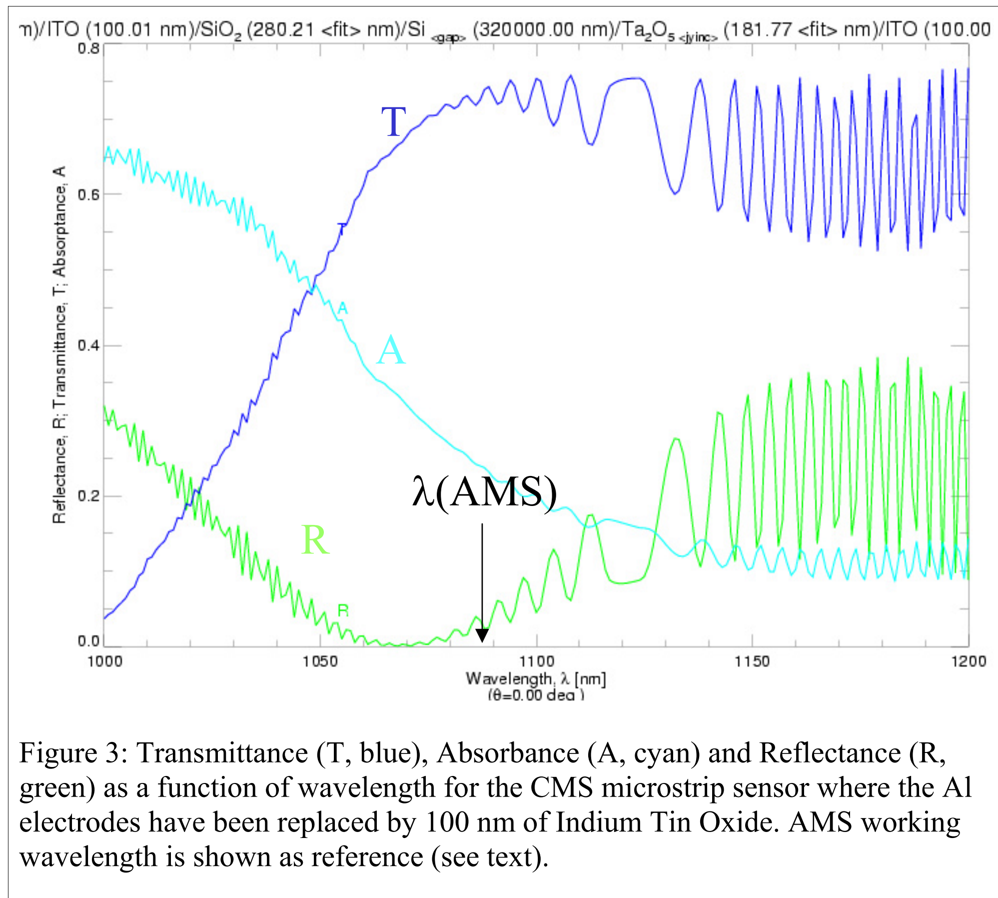

Figure 3: Transmittance (T, blue), Absorbance (A, cyan) and Reflectance (R, green) as a function of wavelength for the CMS microstrip sensor where the Al electrodes have been replaced by 100 nm of Indium Tin Oxide. AMS working wavelength is shown as reference (see text).

We will produce several small size prototypes at the Centro Nacional of Microelectrónica (CNM) –another SiLC member institution- with and without semitransparent electrodes to compare its performance both as particle detectors and as photodetector (Sub section II-2-2-3).

The Lab test bench will be ready by Spring 2007 at IFCA. The sensors will be manufactured by IMB-CNM/CSIC, optically tested by IFCA. The FE and readout electronics will be built by LPNHE, similar to the ones used for the Silicon detector sensors.
IFCA foresees to have a first alignment prototype ready for the CERN test beam in July 2007.

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2. Nuclear Instruments and Methods in Physics Research A 440 (2000) 372-387
3. T. Minami, "Transparent conducting oxide semiconductors for transparent electrodes", Semicond. Sci. Technol. 20 (2005) S35–S44

II-1-6: Cooling systems

The cooling system is an essential piece of the Silicon tracking detectors because it is crucial first to preserve the detectors from warming up and thus avoid an increased noise and secondly, to find a solution not too expensive in terms of added material budget. The mechanical staffs at LPNHE are developing a cooling system for the Silicon tracking prototypes, taking as starting point the now well estimated main source of energy dissipation

in these detectors, namely the on-detector electronics, also under development in this Lab. In 2006, the work was focused on developing mechanical prototypes of the detectors and of the cooling system in order to reproduce realistic conditions of run in the Lab, and to test the foreseen cooling solution as well as the modelling of the simulation-based studies. The results of this preliminary work (see Fig. 3) will be used to build the first cooling prototype in 2007.

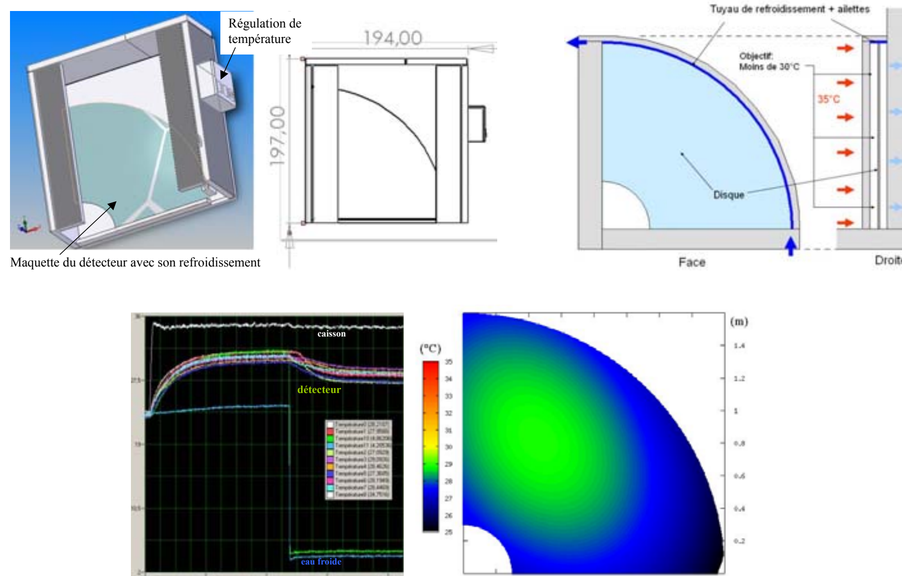


Figure 4: prototyped cooling system and mechanical detector structure for tests at LPNHE Lab (top); obtained results (bottom left) and modelling of the simulation package (bottom left)

The insulating envelop will be used to locate the detector prototypes. This work should be pursued in collaboration with IFCA and Liverpool University and other members of the SiLC collaboration.

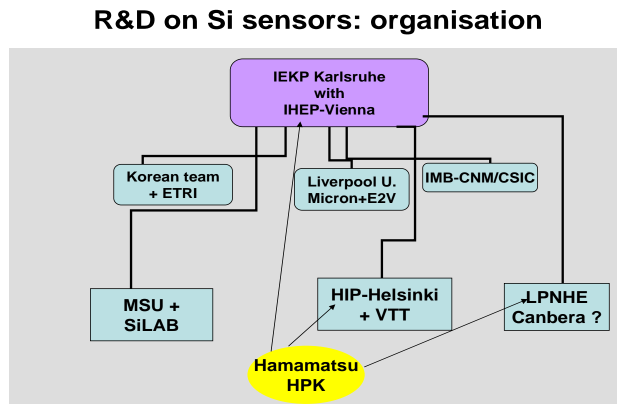
II-1-7: Integration issues and push pull issues

As already quite clear from previous sections, this R&D and especially the Mechanics R&D is developed keeping in mind since the very early stage, the integration issues. This is indeed mandatory for the tracking components that are all to be integrated in the internal part of the overall detector and in crucial regions, in between other sub detectors. This is requesting information from the other sub detectors that are not yet available. Exchanging experience from previous experiments or the construction of various LHC detectors is indeed an asset.
The push pull possible case is another important issue that we will add in this R&D in order to estimate the particular consequences on this sub detector.

II-2: New sensors R&D

The SiLC R&D collaboration is benefiting from a large expertise and also good contacts with several founders. Besides there are some Institutes like HIP (with VTT) or Korean Universities (with ETRI) that are in close collaborative contacts with a firm or which have the needed facilities for doing themselves R&D on sensors (IMB-CNM in Barcelona). Moreover another asset of our collaboration is the expertise developed by IHEP Vienna and IEKP Karlsruhe, in developing dedicated test benches for Quality Control Test in close collaboration with the vendors as Hamamatsu HKP and St Microlectronics.

An organized effort has thus been launched, schematized in the flow chart here below:



In this scheme, the Institute that has a close collaborative contact with a foundry acts as the direct contact with the firm and also contributes to the characterization of the product (test benches). The overall data are sent to the coordinating body, namely IEKP Karlsruhe in collaboration with HEPHY Vienna. This is the place where all the data are sent and analyzed and where the product is submitted to the QTC procedure as explained in II-2-4.

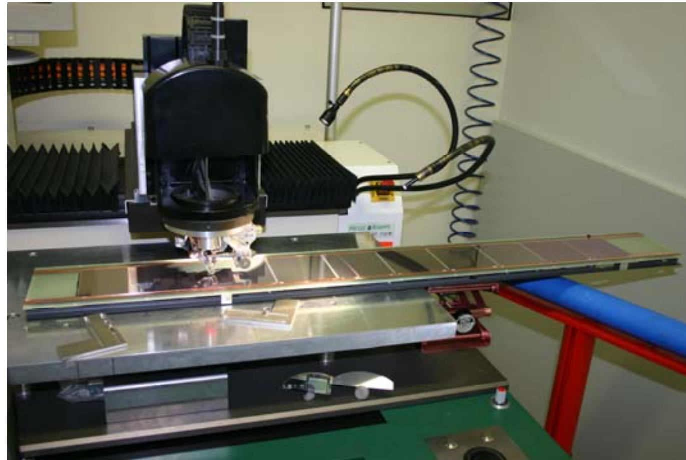
It avoids duplication of efforts and plays a stimulating role in confronting various sensor technologies and achievements. These firms are not all able to ensure large scale production. The present stage is at the R&D level (few sensors for testing novel ideas) or at the level of production of small scale series (for building the various detector prototypes). The transfer of technology is a future step that is will be carefully studied.

II-2-1: The microstrips baseline

For the all silicon solution (SiD) or for the outer silicon envelope (as proposed in LDC), large areas of silicon sensors in the order of a few hundred square meters have to be covered. In contradiction to the LHC experiments for the ILC radiation is no issue, neither is a high occupancy nor a fast readout. On the other hand for ILC excellent position resolution is required. Multiple scattering is the main design constraint and hence the material budget is of outmost importance. There are several strategies under investigation to arrive at a low mass detector: large area sensors, long ladders read out by a single readout unit and thinner than usual sensors.

The main goals of the sensor R&D for the ILC project are the development of larger 8” sensors and the identification and evaluation of a number of reliable companies to mass-produce established 6” sensors. A second priority is to establish a connection scheme to the readout electronics via e.g. bump bonding to strip sensors.

The pictures show a long prototype ladder with 10 sensors connected to one readout hybrid.



The baseline for the ILC silicon strip sensors will be sensors with a thickness in the order of 100 µm to 400 µm from high resistivity floatzone wafers. The final thickness is still depending on the future readout capability to cope with a small signal, the final wafer size and the capability of industry to provide thin sensors. The baseline pitch will be 50 µm without intermediate strips, which are considered as an option only. To cover a large area with silicon sensors the design of these sensors needs to be as simple and robust as possible. To simplify processing and thereby cost a DC only option without a coupling oxide is under consideration. During R&D and evaluation both, AC and DC will be followed. The DC option needs to be especially evaluated, because of the standby feature of the chip during runtime, where a definitive GND is still needed on the strips to guarantee a stable bias on the sensors. Also, no recent large experiment uses DC sensors. The testing of a large number of DC coupled sensors is also an issue of R&D. We consider also for the DC sensors a FOXFET biasing, simplifying testing and operation. In the case of the AC option the biasing will be done by standard polysilicon resistors or by FOXFET structures.

For the lower radii and hence smaller areas double sided thin sensors are foreseen, with a thickness of about 150-200 µm. The availability of qualitatively acceptable double sided sensors in a large quantity is not fully obvious and requires further investigations.

The strip parameters need to be adapted to achieve very low noise levels. Load capacitance needs to be minimized for long ladders, even for the possible long integration time of the ILC. The strip currents need to be very low O(1nA), especially for long ladders and DC coupling. Bias resistors have to be high due to the thermal noise contribution, especially for long ladders, where several are added in parallel.

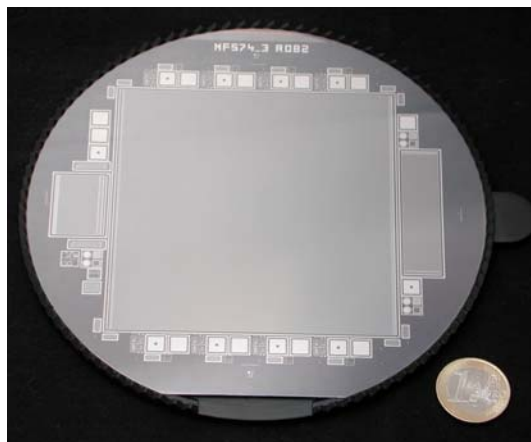
To summarize, the baseline for the large outer layers is a single thin 6”- 8” high resistivity floatzone sensor with DC coupled strips with a pitch in the order of 50µm. The baseline for the inner layers is a double sided 6” high resistivity floatzone sensor with AC coupled strips with a pitch in the order of 50µm.

The development of new radiation hard sensor material, like magnetic Czochralski is not followed by the SiLC collaboration, nor do we need to care about any multiple guard ring feature to guarantee high voltage stability.

From the CMS experience, we learned about the usefulness of standard test structures to have a unified way of quality assurance and process monitoring of the company.

We will implement in each sensor from each supplier at least a full mini sensor, a diode, a MOS structure (V_Flatband measurement), a gate controlled diode (surface current measurement) and structures to measure inter strip capacitance, inter strip resistance, poly resistance, coupling capacitance, Al resistivity, p+ resistivity and oxide breakdown. These structures and their treatment are thoroughly explained in the QA section.

Picture showing a large area sensor for CMS including specially designed test structures.



In the second stage of the R&D connectivity needs to be evaluated to possible steer away from the actual chip on hybrid scheme. A possible additional thick silicon oxide, polyimide or BCB layer with an additional metal routing is under discussion, where the individual strips are routed to an array field of connection pads. This is especially important in view of the chip development with a higher number of channels, where bump bonding even for strip sensors could be an option. Also the silicon on insulator technique will be further observed.

II-2-2: The Korean approach

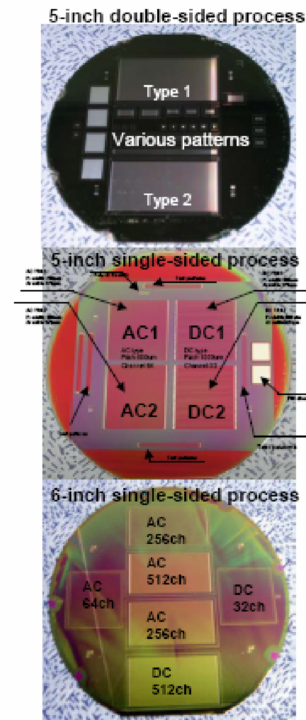
The Korean team is developing since a few years a very interesting and promising line of research in collaboration with ETRI Company. Their main goals are to produce a new generation of Silicon strip sensors that follow our wish list in terms of microstrip sensors for both the single-sided and double-sided alternatives. The present status of the products they are developing with ETRI are summarized in the picture and Tables here below. And for a very enlightening review of this work see the presentation by H. Park at the last SiLC Collaboration Meeting: http://www.cnm.es/projectes/SILC_meeting/ and click on “agenda”)

- yields

type	DC-type	AC-type
single-sided	90%	80%
double-sided	< 30%	N/A

- fabrication line

line	DC-type	AC-type
5 inch	double/single-sided	single-sided
6 inch	single-sided	single-sided (in progress)
8 inch	**thickness (725 um, can be thinned ~500 um)**	



Summary of the present status of the R&D on microstrip sensors achieved by the Korean group in close collaboration with ETRI (Korea)

The Korean team has developed a series of Lab test bench and test beam briefly mentioned in the Lab test bench and Test beam section of this document. This ensures the characterization in realistic conditions of these new products. It is a very interesting example of close collaboration with an Industrial firm.

This work is included in the R&D framework on sensors of the SiLC collaboration and a collaborative effort is launched to include this line of research, in line with the Quality Test Approach task in SiLC. Indeed, the final aim is to have these new sensors ready for equipping detector prototypes for the forthcoming test beams.
ETRI and SiLab (possibly Canberra and Micron) are at the present time the companies that are interested in pursuing the development of the double-sided sensor fab line with 6'' wafers and with which we have contacts through different SiLC Institutes (see flow chart above).

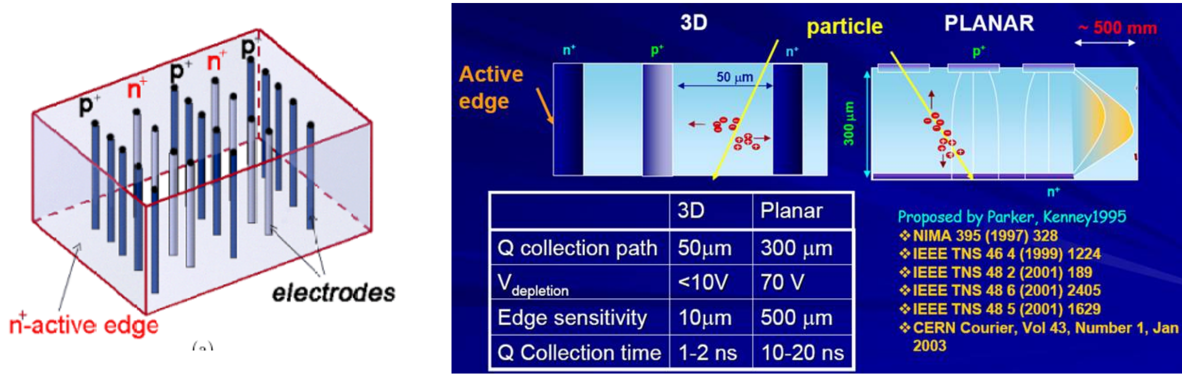
Another option, a new way of edgeless sensors is currently under development; they will be described in the next section.

II-2-3: Novel sensor technologies

Two Laboratories, IMB-CNM/CSIC in Barcelona and HIP together with VTT in Helsinki, are conducting R&D developments on the 3D Silicon detector and via technology that has several interesting applications for SiLC. The use of the 3D planar strip technology is underway at VTT and HIP in order to develop a new line of production for micro strips detector that present several interesting features. The development of 3D detectors at IMB-CNM/CSIC has two aspects, one is the application to new pixel technology the other one is to provide the possibility of wiring on detector the FE chip. Both developments are discussed in this proposal. In this section is described the current status of these developments. These 3D developments are very much indebted to S. Parker who proposed 3-dimensional (3D) detectors in 1995 [[1]] and C. Kenney active edges in 1997 [[2]].

II-2-3-1 Three-dimensional and active edge radiation detectors(VTT and HIP)

This technology, which combines micro-machining and standard VLSI (Very Large Scale Integration) processing, takes full advantage of the development of high precision etching techniques in silicon. Since the publication of the 3D detector idea, several prototypes with different dimensions and electrode configurations have been fabricated and fully characterised [2, 3,4].



	3D	Planar
Q collection path	50µm	300 µm
$V_{depletion}$	<10V	70 V
Edge sensitivity	10µm	500 µm
Q Collection time	1-2 ns	10-20 ns

Fig. 1. *Left:* Sketch of a pure 3D detector where the p^+ and n^+ electrodes are processed inside the silicon bulk. The edges are trench electrodes (active edges) and surround the sides of the 3D device making the active volume sensitive to a few µm from the physical edge. *Right:* Pictures and summarises the major differences between 3D and planar detectors, and shows a typical charge collection of a minimum ionising particle (MIP) [2, 3, 4].

Fig.1 sketches the main features of this novel detector design. Contrary to the standard planar silicon configuration, in the 3D design the electrodes are processed inside the bulk of the silicon wafer instead of being implanted on its surface.

The consequences of this approach are manifold:

1. collection distance as short as 50 µm or less while using the full charge generated by the traversing particle in a thick substrate (normally MIP deposits 80 e^-/µm in silicon);
2. a factor 10 faster pulse speed, due to the shorter drift distances, the higher average field for any given maximum applied field and the small differences in arrival time for the charges arrayed parallel to the electrodes;
3. increased radiation tolerance due to the shortened drift distances and a still moderate full depletion voltage;
4. capability for room temperature operation after heavy irradiation (see Fig. 2)
5. very low depletion voltage in the order of a few volts – compatible with the battery powered operation.
6. sensitivity of the sensor up to the edge: dead space is of O(5µm), rather than O(100µm) for classic structures with guard rings

Several of these features are very attractive to ILC detector designs. For instance, when bonding two (or eventually more) sensors together to form ladder structures, the insensitive area between sensors is significantly reduced. Likewise to assemble the elementary modules one to each other in the overall detector architecture, the edgeless property together with the wiring on detector of the electronics are important features which we are studying.

As charge collection happens along the length of the sensor, rather than its vertical thickness, the sensors can be made very thin, therefore reducing the total material of the tracking detector. This is another attractive feature for the SiLC application.

At present, the charge collection efficiency has been measured to be 60 % for a detector irradiated up to 10^{15} protons/cm^2 with a detector bias of 40 V. The irradiation and the characterisation of some samples have been performed at room temperature. An example of a signal from a minimum ionising particle (MIP) after such fluency is shown in Fig. 2 (left). A full depletion bias voltage of 105 V, in Fig. 2 (right), has been measured for a device irradiated with 10^{15} 55 MeV protons/cm^2, corresponding to 1.8×10^{15} neutrons/cm^2. 3D detectors are expected to resist beyond 5×10^{15} neutrons/cm^2, in particular if oxygen enriched substrates and electron signal readout are employed [2, 3, 4].

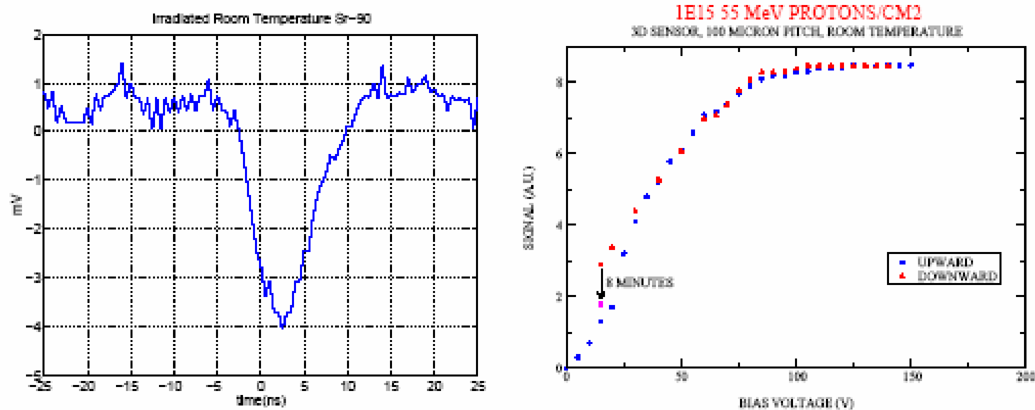


Fig. 2. *Left*: oscilloscope trace of a MIP detected with a 3D detector irradiated to 10^{15} protons/cm^2 and fully reverse annealed. The test was performed at room temperature. *Right:* signal of a 3D device irradiated with 10^{15} 55 MeV protons (equivalent to 1.8×10^{15} neutrons/cm^2) measured at room temperature but stored at low temperature with minimal beneficial and reverse annealing. The 8 min pause at one point was allowed to show the apparent hysteresis due to the time required for (presumably surface) charge settling [5, 6, 7].

- *Active edge detectors*

For planar detectors, shown in Fig. 1. (right), the electric field must be kept away from the saw cuts along the sensor edges, since they are conducting due to numerous unfilled crystal bonds. A large space is needed to keep the field region away from any cracks and chips caused by the sawing. The inactive space can be as large as some tens of microns from the saw edge. Some space must be also left for guard rings, which drop the voltage in a controlled fashion and intercept leakage currents coming from the edge.

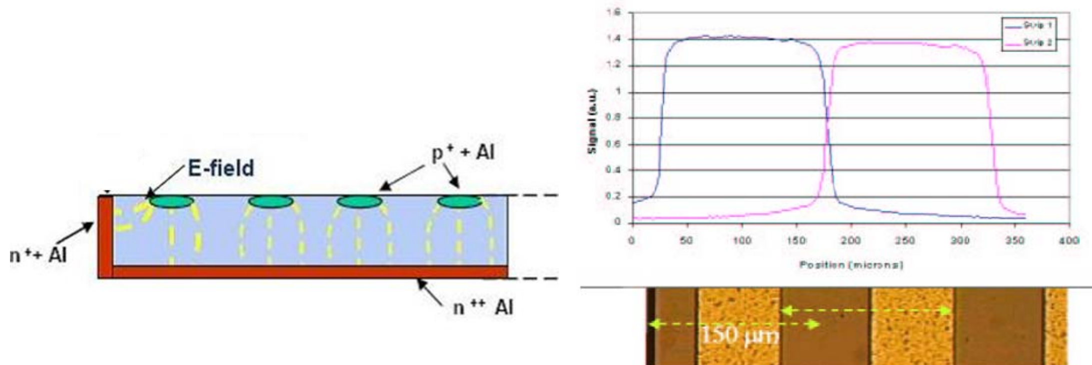


Fig. 3. *Left*: An active edge detector, where the final dicing of the sensor is done by anisotropic etching, avoids the problems seen in Fig. 1. (right). *Right*: Signal from edge and next-to-edge channels as the sensor is scanned across the X-ray micro beam. The rapid turn-on at the left edge is clear [8].

By adding a few 3D process steps into the planar process, the dead space and cracks in the sensor edges of a planar detector can be avoided by using deep-etching, dopant inclusion and diffusion. The final dicing of the sensors is done by etching instead of sawing. In this way the

edges of the sensor become an extension of the backside electrode, as shown schematically in Fig. 3. In the configuration dead space is not needed to avoid extension of the electric field lines to the sawing edge and/or for the guard ring structures. The advantages are that the surface leakage current is suppressed greatly and the dead space is reduced to no more than a few microns as shown in Fig. 3 (right) [8].

For SiLC, HIP and VTT are making R&D on the edgeless thin planar strip detectors. The approach is based on the silicon on insulator (SOI) substrates in order to ensure the mechanical strength during the fabrication. The thinnest active layers of 150 microns are foreseen.

Fig.4. Cross section of the active edge strip detector before the handle wafer removal

In addition to the utilization of the SOI wafer the fabrication and the detector structure contain a few specific features. From the structure point of view we have the front side biasing and the active edge realized with the 3-dimensional (3D) polysilicon technology. In addition to the SOI-substrates and the standard planar strip technology, the fabrication includes thinning and polishing of the active layer to the desired thickness, deep silicon etching, polysilicon fill and planarization for the active edge, separation the detector chips with an etching step (instead of diamond blade) and, finally, the support wafer removal.
At the present the state the substrate fabrication and the structure layout design are carried out.

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II-2-2-2 Three detectors developments at IMB-CNM/CSIC

To avoid the limitations of current silicon and gallium arsenide planar detectors in both X-ray and high energy physics applications, a new detector architecture has been proposed [1]. These detectors have a three-dimensional (3D) array of electrodes that penetrate into the detector bulk, as shown in figure 1.

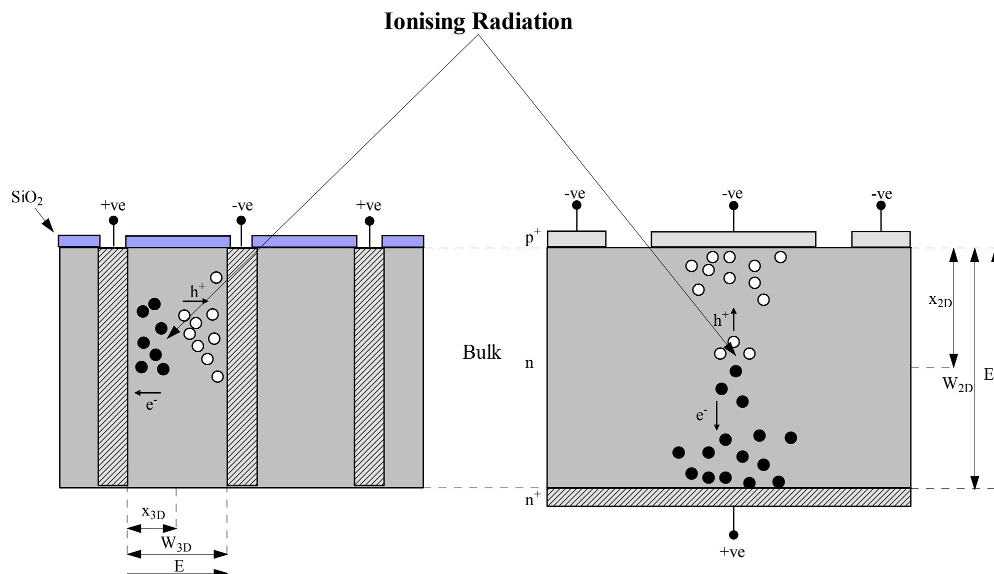

Fig. 1. Cross sections of semiconductor detectors made by standard planar technology (right) and the 3D technique (left).

The electrodes are cylindrical and disposed in a geometry which results in a uniform electric field between the central electrode and the surrounding ones. The electrodes are biased to create an electrical field that sweeps the charge carriers through the bulk parallel to the wafer surface, as shown in figure 1. The electrons and holes are then collected at oppositely biased electrodes. The aim is to set the maximum drift, x, and depletion distance, W, by the electrode spacing rather than by the detector thickness as in the more conventional planar technology.
The advantage of the 3D structure is that the detector has to be depleted only from one column electrode to the adjacent opposite polarity column electrode in order to deplete fully a detector of any thickness. The distance between the two column electrodes is determined by the desired spatial resolution of the detector. With the electrode distance set at 25µm the expected threshold voltage to deplete this distance is below 10 V for Si detectors. This is

much lower than the threshold voltage of 100V which is required for standard Si detectors using a conventional pixel structure.
A further property of the 3D structure is that the active volume of the detector can be increased without increasing the threshold voltage. This is simply done by increasing the substrate thickness. The limit is only given by the attainable aspect ratio of the hole drilling process used to fabricate the electrodes. Hence even materials with low absorption coefficients may become more attractive as X-ray detectors. This can be interesting for silicon, which is usually used for X-ray energies below 20-30 keV. For higher X-ray energies the absorption coefficient of silicon is too low for it to operate efficiently as an X-ray detector. By using the 3D structure, an X-ray detector with high detection efficiency can be constructed with silicon even at high energies.
Another very important property of this type of geometry is that the required lateral depletion is equal to half the pixel pitch for any thickness while in planar detectors the “lateral depletion” is the same as the detector thickness. This means that 3D detectors can be tiled for large areas with negligible dead area between tiles, as the detector cut edge can be very close to the active area. For example, in planar microstrip technology the field must be kept away from the sensor edges since they are conducting and would short it out.
The low depletion voltage and short collection distance for ionising particles make possible with 3D structures an intrinsic resistance to the effect of bulk silicon damage. This will be fundamental for applications of tracking detectors in future very high luminosity colliders that will require semiconductor detectors with substantially improved properties compared to presently available technology. Keeping the electrode spacing small, the ability of silicon detectors to operate in the presence of severe bulk radiation damage should be greatly increased. The charge carriers generated by ionising radiation can be collected within a time smaller than the trapping time of the induced defects. With the electrode spacing set at 25 µm, collection distances and collection times are about one order of magnitude less than those of planar technology, while the depletion voltage is about two orders of magnitude lower. Decreasing the depletion voltage is important to improve the signal-to-noise ratio due to the reduction in the leakage current.
The drawback of this technology is the complexity of the fabrication process and therefore the high cost of the production of a large numbers of devices.

- *Detector Description*

Recently IMB-CNM has proposed [2] a new geometry for 3D detectors which are fabricated in a double-sided configuration, with columns of one doping type etched from the front side of the device, and the other type etched from the back side. Neither set of columns passes through the full thickness of the silicon substrate, as shown in figure 2.

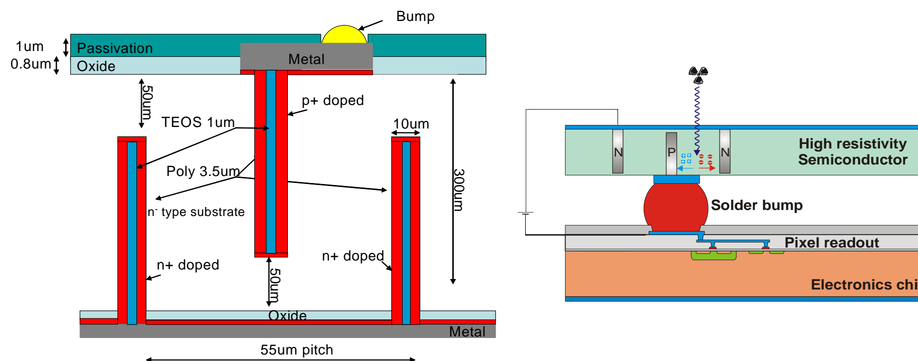

Fig. 2. Layout proposed for the double sided 3D detectors

This structure is similar to a conventional 3D detector, but has a simpler fabrication process because the difficulty of doping the two different kinds of holes on the same side is avoided. In standard 3D detectors very thick layers of polysilicon must be deposited and doped on the same side of the substrate in order to create the p-n junction. By etching the holes on the two sides the photolithographic steps needed to define the electrode contacts is only necessary on the top surface. This simplifies the process and avoids thick layers of poly on the surface which can make it difficult to use bump bonding to connect the electrodes to the pixelated read out chips. Furthermore, the dead area due to the holes is reduced because, as simulation has shown, there is still a high electric field in the volume on the top or the bottom of the holes. Another advantage of this configuration is that it is not necessary to bond the wafer to a "carrier" to avoid wafer breaking.

- *Fabrication technologies*

The main step in the realisation of this type of device is to set up a process to produce holes in the substrate. These holes were etched with Inductively Coupled Plasma (ICP) [3] at the clean room facility at the CNM-IMB. Various hole diameters and thickness are being investigated. Different pitches and geometries have been used to fit the read-out electronics available.
The electrodes within the dry etched holes were formed by filling up the holes with a thick polysilicon layer and doping it with boron and phosphorus to create p-i-n diodes.
Experimental characteristics have been compared to ISE-TCAD software package simulation. Electrical and technological simulations were used to find the optimum parameters for the definition of the detector geometry and fabrication parameters.
A mask set has been designed for the fabrication of 3D detectors with different geometries which includes: test structures; pads diodes; pixel detectors to be coupled to different read out electronics (Medipix2, Atlas and Pilatus chips); short and long strip detectors. The strip detectors will be wire-bonded to LHC readout electronics and tested with radioactive sources to demonstrate the functionality of the 3D strip detector at LHC speeds. At the moment, the fabrication process is going on. All the devices will be tested by measuring their electrical characteristics and charge collection efficiency before and after irradiation with protons and neutrons up to fluences of 1×10^{16} cm^{-2} 1MeV neutron equivalent.
The high aspect ratio holes in the silicon substrate are made using an Inductively Coupled Plasma (ICP) etching process with an Alcatel 601-E machine. The dry etching process follows the patterning of the wafer surface by photolithography. ICP offers a means of transferring patterns with high fidelity onto the surface of a substrate or into the substrate itself. By using an Aluminium mask we obtained 10μm holes with a depth of 250 μm and separated by 45 μm distance. The holes are partially filled with a thick layer of polysilicon

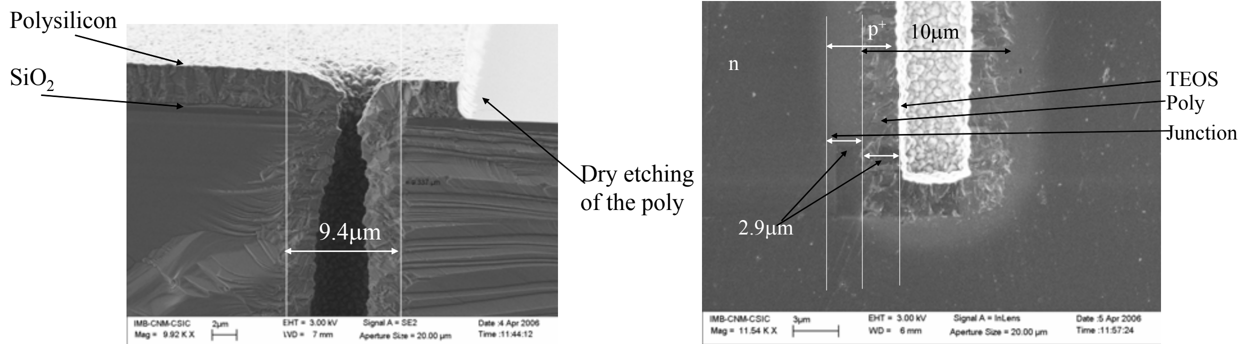

Fig. 3. SEM images of the high aspect ratio holes partially filled with doped polysilicon. The shadow region in the right image is the junction, formed at a depth of 2.9 μm by diffusing the boron inside an n-type silicon substrate.

and then doped from a solid or gaseous source. The p-n junction in the silicon substrate is formed by driving the boron dopants at high temperature during a fixed time. The formation of the junction was proved by spreading resistance measurements and optically by SEM images as shown in figure 3. The contacts are formed by depositing an Al layer on the doped polysilicon layer and different bump bonding techniques will be used to connect the various detector configurations to the corresponding read out chips.
The explained technique of Deep Silicon Etching can also be used to open vias connecting the backside part of the detectors or electronics to the electrically active areas, on the surface. In this way it is possible to make rear connections, simplifying the interconnections. In this case, instead of poly filling, a thick oxide and metal filling is performed.

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II-2-3-3 Infrared transparent strip detectors

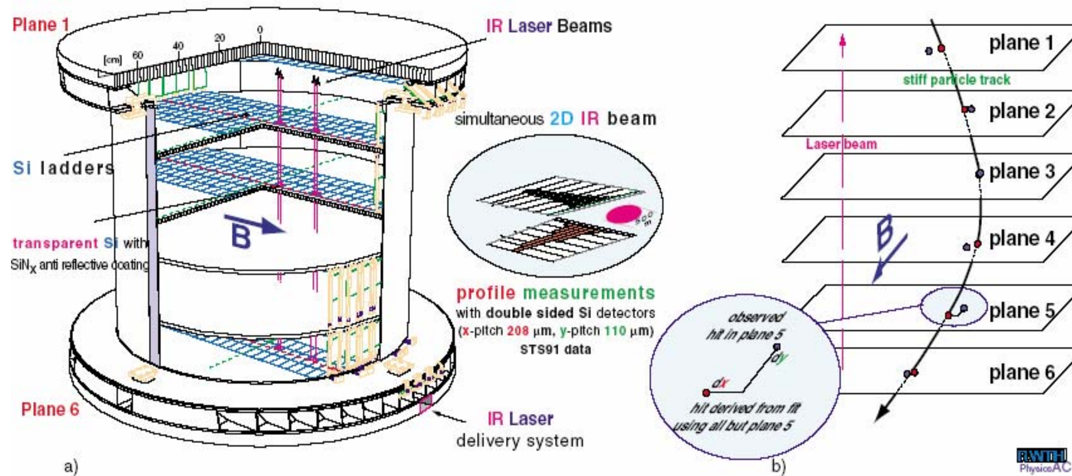
IFCA/CSIC and IMB-CNM/CSIC are involved in the development of a new type of microstrip detectors with infrared transparent electrodes instead of Aluminium. We are moving toward the improvement of microstrips sensors as photodetectors without degrading its particle detector capabilities.

These detectors will allow the usage of collimated laser beams (IR spectrum) going through silicon detector modules. The laser beams would be detected directly in the Si-modules. The main factors limiting the accuracy of a position on opto-mechanical monitoring system are:

- Mechanical transfers (reference the microstrip with respect to fiducial mark monitored by the alignment system.
- non-straight propagation of the reference laser lines.

In this approach, particle tracks and laser beams share the same sensors removing the need of any mechanical transfer. There is minimum interference with silicon support structures and therefore a straightforward DAQ integration. Moreover, the movements interesting for physics are directly monitored. Laser beam as pseudo-tracks may share the same track based alignment software. In measurements taken in AMS experiment resolution better than 2 µm was achieved. In this case uncoated areas in normal detectors were used for IR laser tracks.

This is discussed in details in the subsection on alignment techniques of the Mechanics R&D (see II-1-5 on Hybrid Alignment system)



The technology will be based in transparent electrodes as replacement for standard aluminium layers. TCO (Transparent Conductive Oxide) material as $In_{2-x}Sn_xO_3$ (ITO) or Al doped ZnO will be used to fabricated standard strip detectors. It is important to adjust the optimum thickness to obtain minimum reflective layers for the used wavelength. Also SiO_2 and Si_3N_4 coating layers, used as both as passivation and antirreflective coating will be studied.

The development already started in early 2007, and will address:

- The use of microstrip module as a multilayer media
- Study a few short length microstrip modules with different optical treatments
- Optical characterization: elipsometry, reflectivity, transmitted beam reflection.
- Compare results with very detailed sensor optical simulation.
- Optimize sensor structure and coating for laser detection.

According to IFCA studies, optimum thicknesses of the different layers will be obtained, IMB-CNM will provide strip detectors with the desired layers, and IFCA will make experimental measurements of the suitability of the method.

II-2-4: Pixels

The SiLC collaboration is also interested in studying the use of pixel-like sensors in regions other than those covered by the vertex detector. A number of institutes in the collaboration are already involved in R&D activities on pixel technologies. At the moment the activities are focused on MAPS, DEPFETs and 3D pixel detectors. Particular attention is paid on connectivity issues, of overriding importance in these technologies.

Pixel detectors could be very well used in regions, not covered by the vertex, needing a spatial resolution finer than that provided by strip detectors or to regions in which a smooth transition between pixels and strips is needed to properly resolve ambiguities.

The study reported here below is done in the frame of the LDC concept; it should be noted that it is easy to apply to the other detector concepts. LDC foresees to have two layers of silicon bridging the TPC and the vertex detector: the Silicon Inner Tracker (SIT).

These two layers are very important, in particular for the reconstruction of particles decaying between the vertex and the TPC. Simulations have shown that strip detectors would provide the required performance in momentum determination. However, there is the concern that, given the long distance between the vertex and the first layer of the SIT, and the expected high local occupancies in some topologies with large track density inside the jets, the pattern recognition will have some troubles disentangling ambiguities with the spatial resolution given by this type of sensors. Studies performed with fast simulation (SGV) also show that some improvement in the momentum determination can be obtained having one of the layers made with pixel sensors. For that reason a simulation study has been launched to determine which is the cell size required for the SIT to provide not only the required precision on momentum but also to help the pattern recognition. The outline of this ongoing study is sketched in the next section. It may turn out that at least the first layer of the SIT would need a finer segmentation than that provided by conventional silicon strip detectors.

In the forward/backward region, LDC is planning to have 3 disks on each side made from pixel-like detectors in order to cope with the higher expected occupancies and with the fact that in this region the tracks do not cross the full vertex detector. SiD foresees as well to have 4 disks. The same analysis will be applied in order to determine the optimal pixel area which could be bigger than the required in the vertex detector. In this region one could envisage the use of the same technologies as in the vertex (DEPFET, MAPS, SOI) with coarser pixels whenever feasible. Even if larger pixels could not be build in the different technologies one could find alternative solutions. In the case of the DEPFETs, for example, this could be achieved connecting several pixels in a row. In that case the currents, and therefore the signals, are added with the noise increasing only like $L^{1/2}$, where L is the length of the pseudo strip. For strip detectors the noise would raise like the capacitance, which is proportional to L. The advantage of inheriting technologies from the vertex is that one could have a single line of research, optimizing the resources of the different groups. Alternatively, one could go to more conventional technologies, like the ones employed in BTeV.

The same could be applied on the inner layer, or both, of the intermediate tracker in the barrel region if the analysis shows that better resolution is needed in the z coordinate to resolve the ambiguities in the pattern recognition. The RΦ resolution would remain the same. Depending on the optimal cell size resulting from this analysis one could consider the following options:

- Pixel detectors like the ones in the vertex sub-system with coarser granularity if the technology allows for that. This includes MAPS, DEPFETS, SOI. A program investigating the maximum size that each of the technologies can reliably provide will start soon.
- Macro pixels or short strips: using short strips or long pixels, like envisaged for some of the tracker layers of the tracker in the ATLAS upgrade, could provide enough track separation. Depending on the optimal cell size the length of the strips could vary from 1 to 20 mm

Connectivity is an issue that should be carefully studied for these options. As previously mentioned in section II-2-2, there is progress going on at VTT and CNM-IMB on 3D connectivity with through-hole vias in silicon. They are able to make metal and polysilicon vias filled (See fig.3). Also some work on technologies in the line of Tape Automated Bonding (TAB) have started in some of the institutes (see Fig. 4).

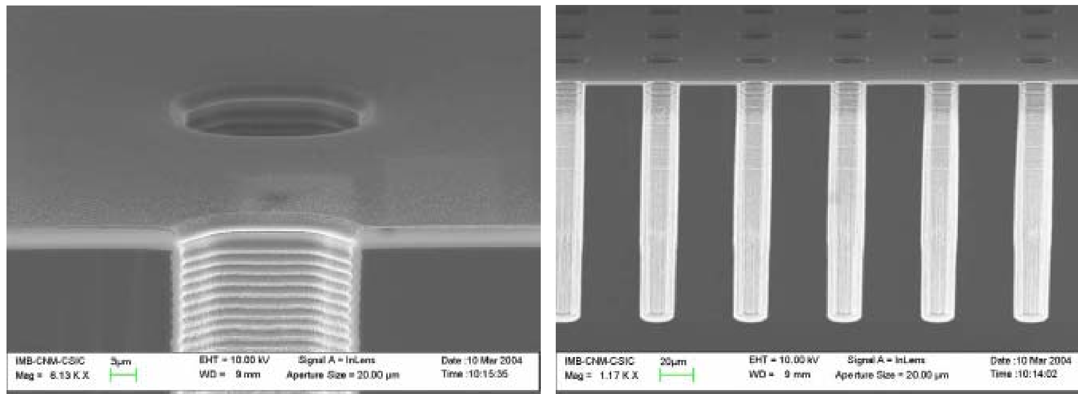


Figure 3. Through hole vias made at CNM-IMB with Deep Rie in silicon

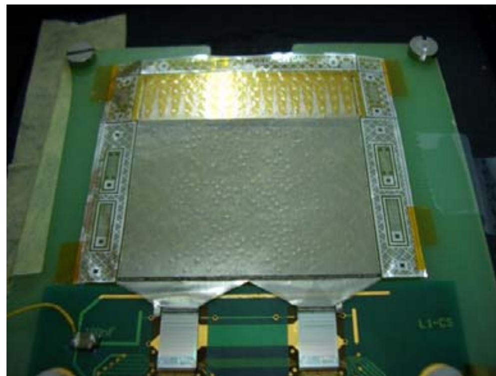


Figure 4. Silicon pad sensor TAB bonded to the readout ASICS. No wire bonds.

- *Pattern recognition study in the inner tracker*

In this section, one very concrete question is discussed, namely "what is the cell size required in the innermost layers to be instrumented by the SiLC collaboration?" While no definitive answer is given in this text, the directions of a specifically conceived study are sketched.

The measurement of the track transverse momentum is the core business of the tracker and the p_T resolution requirement drives the layout design. For a given tracking volume and magnetic field strength, the transverse momentum resolution is essentially a function of the number of hits and the precision of each hit in the plane of curvature (RΦ in the standard configuration with a solenoidal magnetic along the z-axis), leaving very little room for variations of the cell size in that direction. In the following, the cell dimension in the RΦ direction of the layers at intermediate is considered fixed.

The required precision for the measurement of the second coordinate (z in the barrel, R in the end-caps, if measured at all) is a much weaker constraint. Arguments based on track parameter resolution provide little guidance on the optimal cell size in the second coordinate. In this study, the cell dimension in the complementary direction is optimized on the basis of pattern recognition requirements. The performance of the pattern recognition depends critically on the cell occupancy and therefore on its area. The cell dimension in each layer must thus be chosen in agreement with the pattern recognition performance requirement of each layer.

The challenge for pattern recognition – and thus the optimal cell size along z - varies greatly between the different layers of a tracker. High granularity is essential to cope with the dense environment close to the interaction region. Moving further out, the requirement on cell size becomes more and more relaxed in general but, still, one may expect very high track densities in many topologies of interest in physics.

The definition of quantitative specifications for the pattern recognition performance is far from straightforward. High-level reconstruction algorithms and physics analyses rely on high tracking efficiency: the overall tracking efficiency is required to be greater than 99%. Moreover, the rate of fake tracks (more or less random combinations of tracker hits) and distorted tracks (tracks whose parameters are mis-measured as a result of the inclusion of one or more non-related hits in the fit) should be strictly controlled. The total efficiency and fake rate depend on a large number of parameters. Some of these, the fraction of defect component in the installed detector, or the level of sophistication of the track reconstruction software in the first year of running, are quite hard to estimate.

There are a number of quantities that help evaluating and optimizing the quality and performance of the pattern reconstruction that we describe below.

The occupancy: the classical quality marker. The main advantage of this quantity is that it is readily computed. Estimates for all layers and detector technologies are obtained from an analysis of the Mokka simulation result of signal (top pairs) and background (beamstrahlung pair production) events. This is shown in the left plot of Fig. 6. The occupancy there is normalized to an area of a 1 mm^2 and corresponds to the contribution from a single bunch crossing. For a given technology the channel occupancy is obtained by taking into account the number of cells/mm^2, the cluster multiplicity and the time stamp performance of the design.

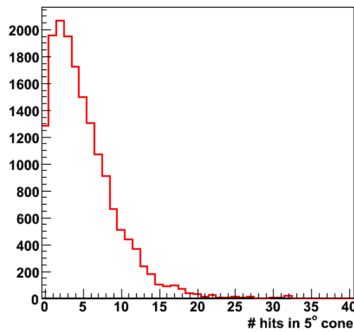


Fig.5. Local occupancy around a given hit showing the number of hits in a 5 degrees cone.

The interpretation of the occupancy is not straight forward. This is especially true in the ILC detectors, where large areas of the detector surface are empty, while several small regions may witness very high density. The non uniform nature of the hit distribution is taken into account by the *local occupancy* that determines the occupancy in the surroundings of the track. In practice the number of hits is counted in a standard solid angle around each hit. The hit in the center of the cone is subtracted. The hit count distributions, like the one in Fig. 5, are quite broad and display a tail towards high occupancies. Finally the result is normalized to the area of the cone projection into the detector surface to produce a figure like the one in the right of Fig. 6. The local occupancy is typically one or two orders of magnitude higher than the average over the whole detector surface.

Search window: In a popular class of pattern recognition algorithms, a seed is created using a sub-set of detector elements with excellent pattern recognition performance. The track is then "grown" by an iterative search for hits in the remaining detector layers. At each step, the track stub is extrapolated to the next detector layer. The uncertainty on the extrapolation defines a search window on the detector surface. The extrapolation error for a given track is determined by the precision of the track stub, the material [for low momentum tracks] and the extrapolation distance.

The elliptical window is convoluted with the detector response to determine the total area in which tracks will leave compatible hits. In the figures below this last step is clarified using two examples. For a single-sided silicon strip the total compatible area (the grey area) is greatly enhanced with respect to the area of the extrapolation error ellipse. For the pixel

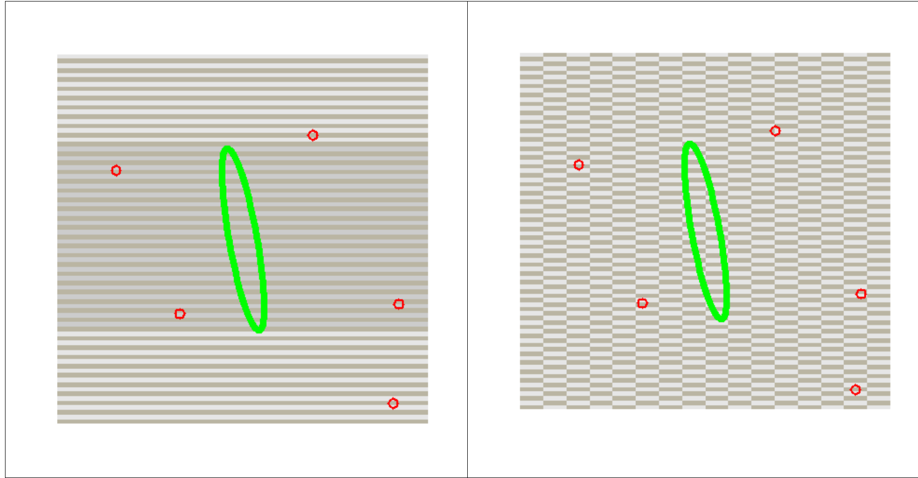


Figure 7: The interplay between the extrapolated search window and the detector technology. The initial search window as obtained from an extrapolation of the trajectory state in the previous layer is represented as a green ellipse. Red circles indicate tracks traversing the layer. The figures correspond to a 1×1 cm^2 area and all objects are drawn to scale. In the two figures, different options for the sensor segmentation are shown. The leftmost figure corresponds to 100 µm pitch single-sided micro-strip detector (1 cm length is represented). The dark-grey shading indicates the region where tracks will produce compatible hits. The rightmost figure represents a 100×500 µm pixel detector. In this case, only tracks that cross the detector plane in pixels that touch the error ellipse yield compatible hits.

detector, only tracks traversing pixels that touch on the error ellipse lead to compatible hits.

Contamination or confusion: the convolution of the occupancy and the search window information allows to determine the contamination, i.e. the number of non-related hits that are found to be compatible with the track. Eventually, this quantity determines the degree of ambiguity or confusion that the pattern recognition should cope with. Thus, pattern recognition "weak spots" may be identified and the relative "strength" of the available technologies can be compared.

Full pattern recognition: Full simulation and reconstruction of several benchmark physics channels is needed to study the impact of the pattern recognition performance on the physics reach and thus to derive meaningful constraints for the above-mentioned quality markers.

- ***Conclusions:***

A study specifically designed to optimize the cell size of the layers immediately beyond the vertex detector on the basis of pattern recognition arguments is being performed. The work program foresees several steps. Only for the first steps preliminary results are appearing. First complete results are expected within six months.
It is also intended to extend this whole study to the other detector concepts in this crucial innermost barrel and forward regions in order to compare concepts and also to propose

solutions. Besides the collaborative contacts with the vertex task force will be further strengthened. It includes the forthcoming test beams (see Part IV)

II-2-5: Characterization and Quality Test Control framework

The large number of silicon sensors needed for the ILC experiments require a sophisticated and well prepared quality assurance program. As an example of such a quality assurance program we consider the work done for the CMS tracker. The tracker of the LHC experiment CMS consists of more than 26.000 silicon sensors and fills up a total area of 200 m^2. The production of these sensors lasted for about four years. The sensors were initially provided by two vendors, later as an outcome of the quality tests, only one vendor produced the majority of the sensors.

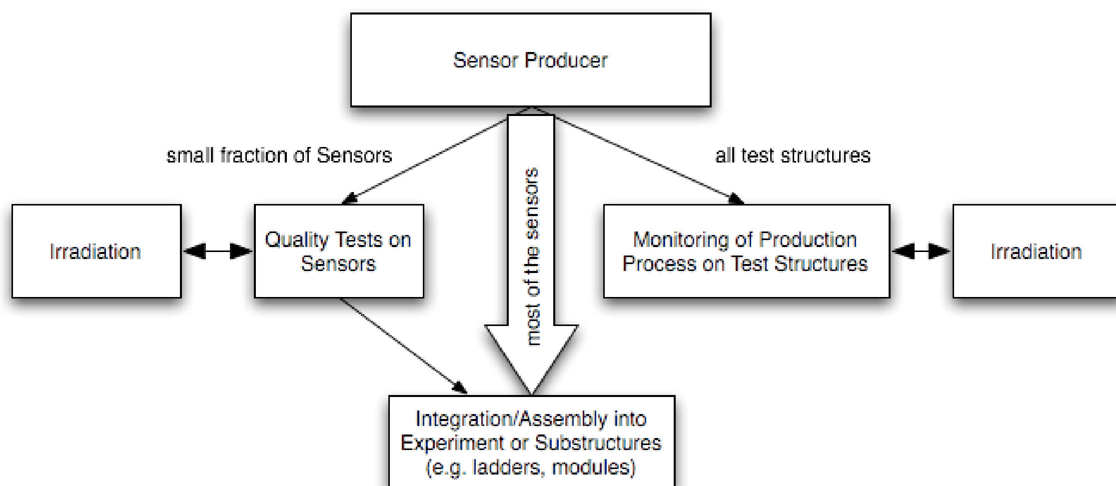
The sensor quality assurance is based on the following strategy. The companies producing the silicon sensors have to perform a very well defined set of measurements and have to provide this data together with additional information related to the production batches and wafer material used.

As the production period will last probably for years stable and reproducible production is mandatory. Therefore it is foreseen to verifying the stability of the production process by measuring characteristic parameters on a large sample of the silicon wafers utilising specially developed test structures. Based on the CMS experience improved test structures are being developed.

On the sensors itself certain measurements are foreseen, e.g. leakage current measurements and capacitance measurements to determine the depletion voltage. Together with these measurements, a strip-by-strip measurement of the sensors is important to have information about the single strip failure rate. Because of the huge sensor quantities, these measurements can only be done on a sample basis. Therefore, the main task for strip-by-strip tests is to verify the measurements of the vendor, which have to been performed on every single sensor.

Additionally, further tests are necessary to prove the functionality of the sensors under the influence of irradiation. This means that all measurements have to be repeated with irradiated sensors. The irradiation dose and particles type should be similar to the irradiation expected in the final experiment.

The diagram below illustrates the complementary measurements required to maintain a constant production quality.



Apart from that, very efficient logistics is necessary to track each sensor on its way between different test setups at various institutes and its final assembly into the experiment. This must

happen fully automatic to avoid human errors. A centralized relational database system, where all measurement results are stored and all logistic steps like shipping are recorded is mandatory and has to be prepared well before the start of the production.

II-2-6 Thinning and other special treatments on sensors:

SiLC is interested, since its beginning, in the possibility of thinning the substrate of larger dimension sensors by a factor 2 or 3. There are also other issues such as the special treatment needed by the sensors used for the hybrid alignment system as developed by IFCA (See sub-sections II-1-5 and II-2-3-3). Other so called special treatments on sensors are induced by the wiring on detector of the FE chips (see sub section III-2-3 on this issue). These different aspects are under investigation and contacts with industrial firms are under exploration or being established, with several possibilities, for instance in France, UK or Russia and including IMB-CNM in Spain.

II-3:Electronics R&D

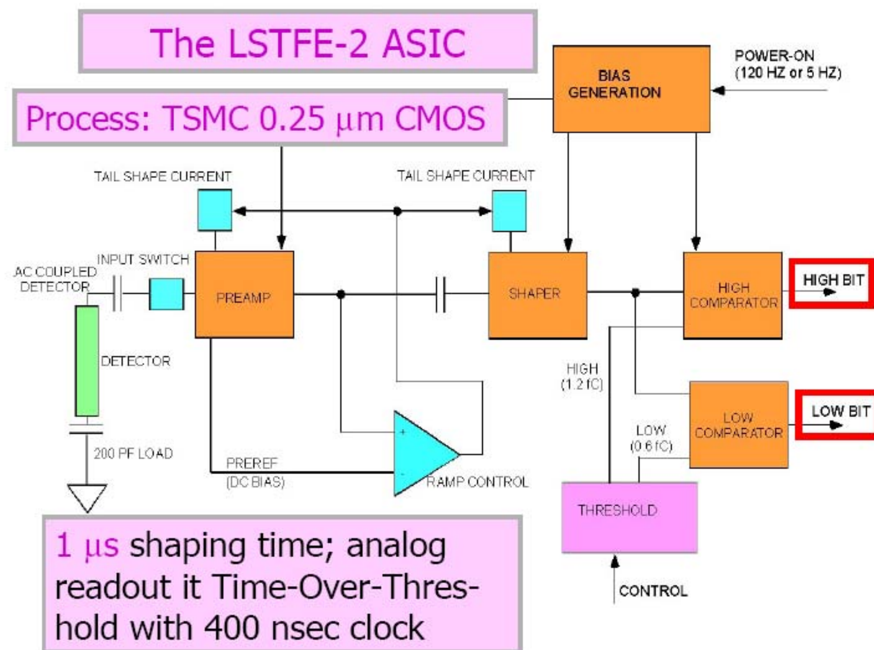
In any detector concept foreseen at the ILC, a front-end readout system for tracking Silicon detectors has to manage millions of channels. Consequently, the amount of material and power per channel has to be carefully optimised keeping noise and readout speed within the constraints of the experiment. It is therefore essential to look for the best integrated technologies available that allow minimizing the amount of material added to the detector, such as connexion capacitances in terms of connectors, hybrid circuits, kaptons, and lead as well to a manageable amount of dissipated power. These technologies allow also implementing efficient data extraction and signal processing techniques such as analogue sampling and on-chip digitisation. As starting examples, CMOS, Bipolar-CMOS and Silicon-Germanium are presently offered in deep-sub micron (250 down to 90nm) at affordable cost through worldwide integrated circuits Multi-Project Wafer Centres. As examples, 180nm and 130nm CMOS readout prototype chips have been designed and tested, and gave satisfactory results in terms of noise and power. Fast timing (sub-nanosecond) is envisaged on some detector layers to get a rough measurement of the coordinate along the strip, using Silicon Germanium chips technology. For designs that covers of the order of 100 square meters and millions of channels, the multiplexing of several tasks such as analogue to digital conversion and zero suppression are mandatory. Power switching at the ILC may reduce thermal dissipation of the Front-end by two orders of magnitude.

II-3-1: FE and readout on-detector electronic chain

The SiLC R&D collaboration is pursuing the development of two Font-End electronics options. The LSTFE design is based on Time-over-Threshold (TOT) and developed by SCIPP and UCSC in Santa Cruz. The second one, ILC-SiTr-180 and ILC-SiTr-130, is developed by LPNHE-Paris with collaboration of LAPP-Annecy. It is a complete FE and readout chain that includes digization. Another important feature of this device is to use Deep-Sub-Micron (DSM) technology. Both developments and present obtained results are described in this section. As discussed in the test beam section, it is foreseen to combine the efforts within the SiLC collaboration and to have the two approaches tested in a joint test beam effort already end of this year.

II-3-1-1 R&D on Time-Over-Threshold Readout (the LSTFE Chip)

The SCIPP LSTFE effort is based on the philosophy of developing an efficient amplification and digitization scheme that provides only the information warranted by the readout of micro-strip sensors employed by an ILC detector. The LSTFE design is rigorously optimized for ILC micro-strip readout, making use of the results from a complete simulation of the collection, amplification, digitization, and reconstruction chain. Following a low noise pre-amplifier and μsec-scale shaper, the signal is evaluated by two comparators – one with a high threshold to suppress noise hits, and the second with a lower threshold to provide pulse-integral information in the region surrounding a high-threshold crossing. The gain of the amplification stages is high, with pulse height (but not integral) saturating between two and four times minimum ionizing. In this way, the application of the high and low thresholds is made insensitive to irreducible channel-to-channel variations. Analogue information (up to over 100 times minimum ionizing) is provided by time-over-threshold from the second comparator – an effectively logarithmic response that emphasizes the minimum-ionizing region for which the reconstruction of an accurate centroid is necessary to provide a point resolution of better than 7 μm. Studies done with the pulse-development and readout simulation suggest that, due to the intrinsic limitations of the charge deposition process, no usable information is lost by this time-over-threshold approach, and the 7 μm goal can be achieved.



Schematic design of the LSTFE Front-End based on Time over Threshold technique

The use of time-over-threshold offers a number of critical advantages over full analogue-to-digital conversion. The chip's proposed digital architecture (currently implemented in basic form on FPGA's at SCIPP) allows for the accumulation of time-over-threshold information in real time, eliminating the need for buffering. Thus, the LSTFE approach will allow for operation at arbitrarily high data rates with close to single-bucket timing, an essential feature for forward-tracking applications. In addition, the dual-comparator time-over-threshold solution is elegant, avoiding a great deal of complexity. As a result, substantial headway has been made with the initial design of the LSTFE, and we appear to be well on our way to

producing a chip that will have all the required functionality needed for the optimal readout of ILC detector microstrips. The relative simplicity of the LSTFE design is also advantageous for the kilo-channel ASIC application envisioned in the SLAC tracker design, for which the issue of channel yield will be of central importance.

For central tracking, the LSTFE approach is applicable to both long- and short-ladder designs (with a minor change in the amplification and shaping parameters). Should the SLAC effort to develop sensors, servicing, and mechanical support for a short-ladder design show that to be an attractive approach, a natural point of collaboration would arise: using the LSTFE channel design in a kilo-channel chip with bump-bond channel contacts, producing an optimized detector/readout module appropriate for any region of the detector. Should long ladders be thought a better option for central tracking, the LSTFE chip will again provide an optimal approach to reading out the sensors.

Initial tests of the LSTFE-1 revealed environmental sensitivity that introduced noise 2-3 times higher than expectations. This additional noise was traced to a sensitivity to power-supply ripple, and has been attenuated using filtering toroids on external power lines. This sensitivity has been modelled in simulation, and eliminated for the LSTFE-2 design by the addition of additional buffering. With the use of toroids for the LSTFE-1 system, measurements of the comparator efficiency as a function of threshold level indicated that the noise at the comparator is Gaussian, as expected from the white noise generated by the preamplifier transistor. Figure 2 shows the measured noise performance as a function of capacitive load for large capacitive load (equivalent to ladders of length greater than 50 cm) applied to the channel input, compared to the expectation (dotted purple line) on which our pulse-development simulation was based. The measured noise performance of

$$\sigma_n = 375 + 8.9*C$$

in equivalent electrons, with the capacitance C in pF, is roughly 20% better than expectations for C = 130 pF, the capacitive load associated with a ladder of 1 meter length.

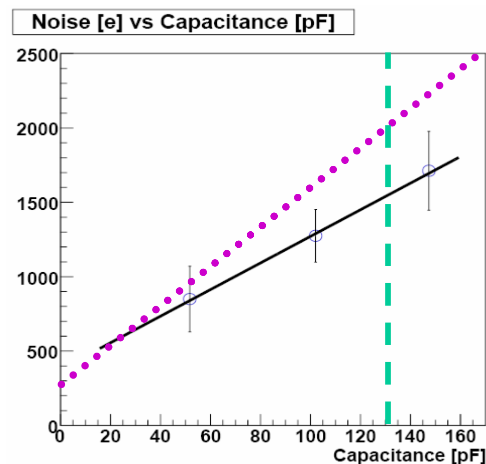


Figure 2: Noise in equivalent electrons vs. load capacitance, as extracted from comparator excitation data. The purple dotted line represents the expectation used in the pulse-development simulation, while the dashed green line represents the load associated with a 100cm ladder. The fit to data (black line) yields $\sigma_n = 375 + 8.9*C$

The dual-comparator channel readout was tested, and the behaviour of the two comparator channels what found to be fully independent, with no discernable cross-talk from the low-threshold comparator into the high-threshold comparator for a given channel. It was possible to run the comparators at levels below 10% of minimum ionizing.

An essential feature of the LSTFE design, necessary to avoid unnecessary power consumption and the need for active cooling of the tracker, is fast power-switching. The approach employed for the LSTFE-1 prototype involved isolating the power-on bias levels during the power-down part of the power cycle, thus reducing to 1 msec or less the time required to restore the power-on bias levels. For the LSTFE-1 prototype, leakage currents (presumably through the protection diodes at each channel's input) compromise this isolation, leading to switch-on times of between 20-40 msec, which would correspond to a 5-10 times power savings for the 5 Hz operation of the ILC. However, the injections of a small (less than 1 nA) current into the front-end can be used to cancel the protection diode leakage, leading to switch-on times of less than 1 msec, and a power savings of 99% (see Figure 4). Excitation of the chip with a minimum-ionizing scale calibration pulse shows that the chip is fully functional at the point at which the shaper response has returned to baseline, approximately 900 μsec after switch-on. Based on these results, the LSTFE-2 design will incorporate a low-power active feedback that maintains the power-on bias levels during the power-off stage, thus achieving the better than 1 msec switch-on time achieved in the test of Figure 3.

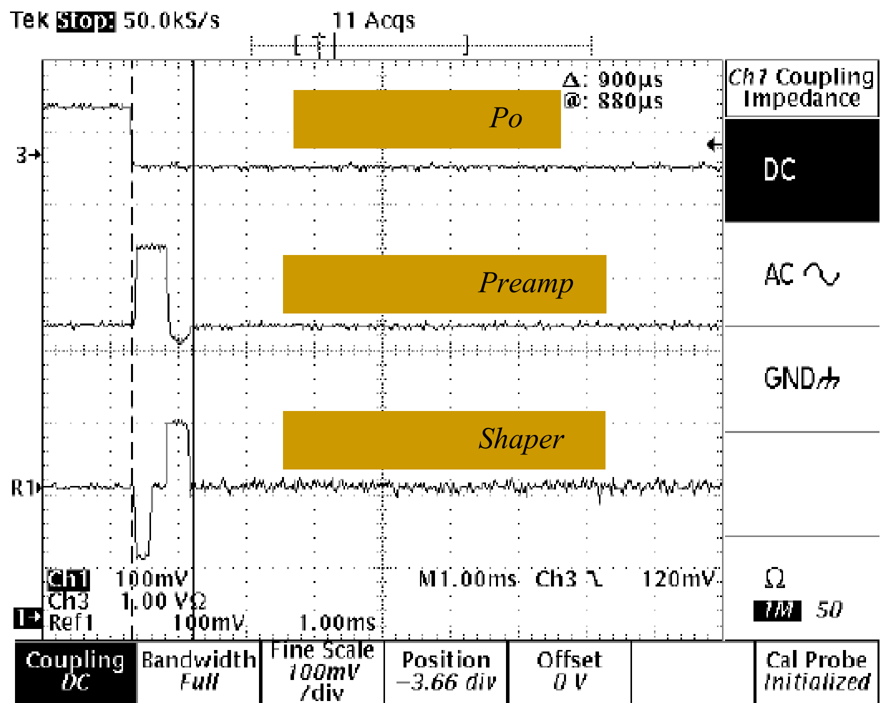


Figure 3: Switch-on time for the preamp and shaper circuitry for case where leakage-cancellation current (approximately 800 pA) is applied to the preamp input. The preamp and shaper are biased, and exhibit full gain, at the point that the traces return to baseline, approximately 900 μs after the downward transition on the control line.

One concern with the progression to ever-smaller feature sizes is the accuracy of channel-to-channel matching, which degrades as surface geometrical tolerances become an ever-larger

fraction of the total component area. Of particular concern to tracking devices, which need to suppress backgrounds to minimum-ionizing signals, is the consistency of the effective comparator threshold from across the channels of the chip. By employing a high gain, the LSTFE design hopes to avoid degradation of the noise-suppression capability of the readout, or the need to develop a system to control individual channel thresholds. Initial studies, with the limited statistics of the outputs of the32 comparators of a two LSTFE chips, show an rms offset variation of less than 10 mV. At a gain of 150 mV/fC, this corresponds to an effective threshold-level variation of better than 6%, or about ¼ of the expected white noise contribution, for a comparator setting of 1.2 fC. This, combined with an observed gain variation of approximately 1% for the same 32 channels, indicates that the current design is in good shape with respect to channel-to-channel matching. Nonetheless, we have identified one or two ideas to explore to further reduce the effective noise contribution from channel-to-channel variation, and are exploring these for the LSTFE-2 submission.

It is foreseen to submit the LSTFE-2 prototype chip in April, and to spend the summer evaluating its properties. We are also in the process of constructing a ladder appropriate for use in a testbeam. Our intent is to join the SiLC testbeam run in late 2007, with the goal of understanding the point-resolution performance of a fine-pitch microstrip system read out by the LSTFE chip. Beyond 2007, our goal would be to perform a small amount of re-optimiziation the LSTFE chip, with the goal of producing an alternative LSTFE chip geared towards use for short strips, and particularly forward tracking, and to test this version in a testbeam run in early 2009.

II-3-1-2 R&D on a FE and readout Deep Sub Micron circuit (SiTr-XXX chips)

For the years to come, Silicon strips detectors will be read using the smallest available integrated technologies for room, transparency, and power considerations. CMOS, Bipolar-CMOS and Silicon-Germanium are presently offered in deep-sub-micron (250 down to 90nm) at affordable cost through worldwide integrated circuits multi-project centres. 180nm as well as 130nm CMOS readout prototype chips have been designed and tested, and give satisfactory results in terms of noise and power [1].

Such Silicon strips exhibit a dominating inter-strip capacitance of the order of 1 pF/cm and strip to substrate capacitance of 0.1 pF/cm. The occupancy at the ILC defined as the percentage of channels hit per beam crossing will be less than 1 % in the outer barrel layers, of the order of a few per cents in the end caps and internal layers. The ILC machine will produce trains of 3000 or 6000 bunches spaced by 150 or 300 ns for 1ms, followed by an idle stage of 200 ms. During trains, in this present scheme, data will be recorded in analogue pipe-lines, then digitised and processed during the idle stage. The overall process will be BCO stamped. The details of data collection and processing are described here below.

- **<u>Detector data</u>**

Pulse height will be recorded and in certain cases, both pulse height and time will be recorded. A resolution transverse to the strip of a few micrometers can be achieved using analogue readout and evaluation of centroids. Two shaping times will be developed, one typically from 500ns to 2 μs on all layers (could be also an even higher one if needed in certain cases ranging from 2 to 5μs), depending mainly on the strip length for beam crossing tagging; The second one, fast shaping of 10-30 ns for some nanosecond timing layer(s)

intended to provide a crude measurement of the impact along the strip with a resolution of a few centimetres as shown below or if for certain cases it is needed to have an accurate time stamping.

The data sketched above can be obtained from the detector with pulse sampling, allowing accurate amplitude and timing measurement. Sparsification is to be performed on the front-end, using thresholds on analogue sums of adjacent channels (See Figure 1). Calibration can also be integrated in the front-end chips using Digital to Analogue Converter and Metal Insulator Metal capacitors of known values as charge reference, together with switches networks.

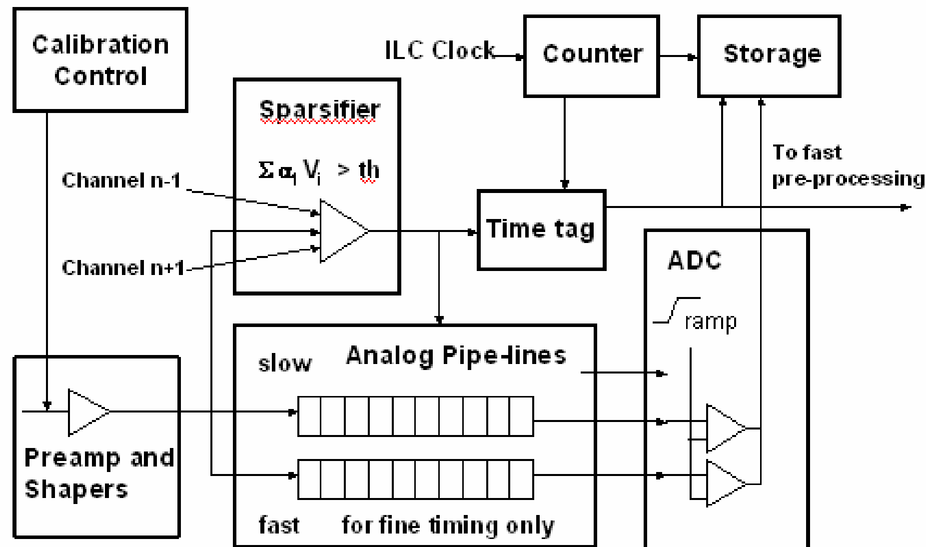


Figure 1 Front-end chips architecture

Coordinate along the strip

Pulse propagation evaluation along the strip using a Spice based linear model and laser diode stimulation measurement show that a current pulse induced in a strips at a given length propagates a voltage step along the strip as in a RLC transmission line with a velocity: $1/\sqrt{LC}$ of the order of c / 5 (~ 6cm/ns), where L and C are the inductance and capacitance of the strip per unit length. Figure 2a and 2b shows the simulated and measured propagation when strips are illuminated with a laser diode light moved along the detector.

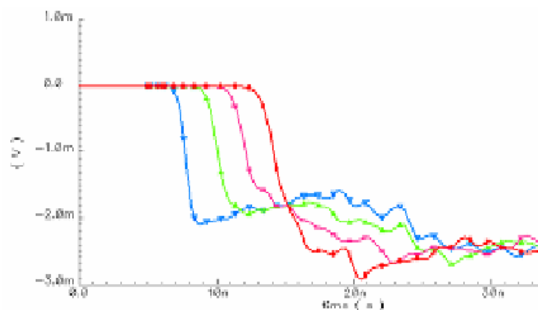


Figure 2a. Simulated propagation along a Silicon strip. Horizontal, ns.
Pulse velocity: 6 cm/ns

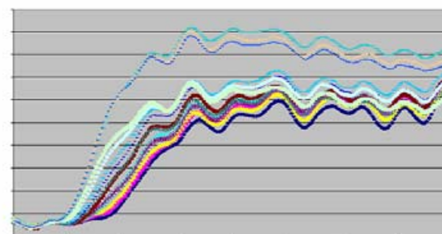


Figure 2b. Measured propagation moving a laser diode along the strip by 24 cm. Horizontal, 10ns.
Pulse velocity: 5.5 cm/ns

The readout electronics system is designed in a way that preserves at best the intrinsic detector performance within the environment of the ILC detectors, making use of the latest technological advances, and matching the following features:

- Comply to the duty cycle of the ILC machine, being presently defined as sequences of one millisecond data taking times of 3246 bunches separated by 308 ns (or 154ns), followed by 199 milliseconds readout times.
- BCO tagging electronics.
- Sparsification and digitization on detector.
- Minimization of power dissipation (less than 1 mW/channel, all included, without power cycling)
- Power cycled front-end electronics
- Ensure an electronics MIP to noise ratio of order 25, for detectors from 10 up to 60 pF capacitance Silicon detector, and accordingly shaping times from 500ns to a few µs.
- Minimize the on-detector total material regarding transparency to radiation.
- Highly multiplexed A/D conversion.
- Provide a continuous stream of digital data at the end of each bunch train. Ensure the reliability, calibration and monitoring of the whole system over the few millions channels.
- Front-end chips mounted closely onto the detector.

➢ **<u>Schematics of the FE, readout and main performance</u>**

❖ *Architecture, FE electronics integration*

During data taking, activity exceeding a given threshold on a few (3-5) adjacent channels will be stored in a 16-deep analogue pipe-line in terms of samples over two shaping times, including pedestal, and digitized after the train in parallel for all channels with a 10-bit on-chip Analogue to Digital Converter. In case a strip is hit several times during a train, an event buffer can record a few tenth sets of samples. The analogue pipe-line has therefore two dimensions, along time sampling and events. Whenever the sum of the charges collected on several neighbour adjacent strips exceeds a given threshold, a time stamp and channel number are recorded, and the analogue pipe-lines continuously running are frozen waiting the end of the data taking stage to be digitised. After two shaping times, the shapers outputs point to the next available analogue pipe-line and are activated again. At the end of the train, analogue pipe lines locations that contain relevant information are digitised, using the multiplexed ADC able to convert one location from all channels at the same time. The global architecture is depicted in Figure 1.

On-detector digital signal processing in the front-end can perform some low level tasks such as centroids, least squares amplitude and time fits, lossless data compression, error correcting codes. Power will be carefully optimized, taking into account the duty cycle of the ILC machine allowing saving at more a factor of 200. On the ILC detector, the voltages supplies will be ramped one by one in a round robin scheme to avoid high current spikes on single spots in the detector.

To summarize, the goal as seen today is to integrate 512 to 1024 channels in the state of the art DSM technology including amplifiers with a 20-30mV/MIP voltage gain over 20-40 MIPs, two pulse shaping options: 500ns-2µs, and 20-50ns for fine timing, zero suppression, pulse sampling, event buffering, highly multiplexed AD conversion, digital pre-processing, calibration and power switching.

❖ *Technologies*

The Silicon detector and VLSI technologies allow today improving both detector and front end integration. Front-end chips implemented in deep sub-micron CMOS technologies allow integrating hundreds if not thousands of channels at a reduced power budget, thanks to the reduction of all wiring capacitors. Silicon-Germanium exhibits less 1/f noise for a bandwidth improved by one order of magnitude, chip thinning, bump bonding and even 3D integration will allow smaller pitch detectors and consequently better position and time resolution, for less on-detector material.

❖ *Low noise design issues in deep sub-micron technology*

Deep sub-micron (< 250nm) CMOS technologies allow to integrate both analogue and digital hardware with increased density, reduced power, at the expense of some loss in dynamic range, dictated by the 1/f noise floor in charge preamplifiers and voltage supply value, under investigation in this R&D work.

❖ *Expected Signal to Noise*

The signal to noise ratio depends upon the total amount of charge collected, and on the total Equivalent Noise Charge proportional to the capacitance of the detector, square root of the leakage current and preamplifier feedback conductance, in a first approximation. The expected signal is therefore 24.000 electrons in 300 μm thick detectors, and current electronic noise typically of the order of 500 electrons + 10 electrons/pF in CMOS deep sub-micron technologies, as it is detailed below.

The best available corresponding Signal/noise ratio is therefore of the order of 20 to 40, depending on the strip length (here up to 60 cm).

❖ *Expected resolutions*

A 50 μm pitch detector read digitally would exhibit ideally a $50/\sqrt{12}$ = 14 μm resolution. However, an analogue readout with centroids should reach of the order of twice better, of the order of 7 μm, for 50 μm pitch strips and incidence below 0.8 radian (see V. Luth, http://www.slac.stanford.edu/cgi-wrap/getdoc/bfac90-015.pdf), depending on the achieved signal/noise ratio on the detector.

A time resolution of 50 nanoseconds should allow identifying the BCO corresponding to a given sampling, even in the case of 150ns BCO intervals.

Concerning fine timing measurements, Figure 3 shows a simulation of the signal processing envisaged, using fast sampling and pulse reconstruction. Resolution is given as a function of the signal/noise ratio and the number of samples taken over two shaping time, under the assumption of a time spread proportional to the derivative of the pulse shape

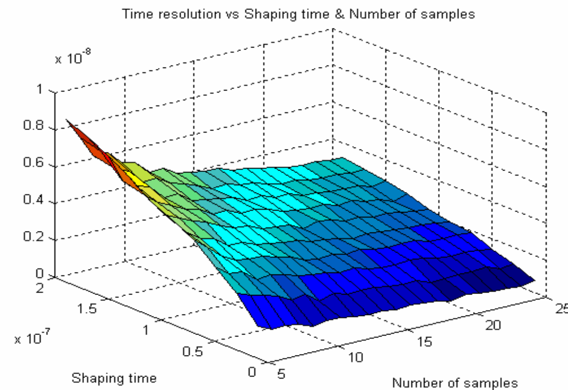


Figure 3. Simulated time resolution as a function of the shaping time, and the number of samples. Signal to noise is set to 25. Least square time estimation using the Cleland and Stern algorithm .

For 16 samples, for instance, taken for two shaping times of 30 µs each, a 1ns rms is obtained, corresponding to an order of 5 cm position resolution if one end is equipped with fast timing, and even less with two ends equipped.

- **Chip designs, schematics and layouts**

  - *CMOS 180 nm Chips: SiTR-180*

A chip was submitted in 180nm CMOS technology, and tested in 2005 (Figure 4). Each channel comprises a preamplifier-shaper, a sample and hold, and a comparator. The 180 nm CMOS technology and tools from United Microelectronics Corporation, Taiwan, were accessed through Europractice at IMEC (Leuven Belgium). The process allows six metal layers, various threshold voltages transistor options with thin oxide C_{ox} at 4.9 mF/m^2, 3.3V transistors, Metal Insulator Metal planar capacitors at 1 fF/µm^2.

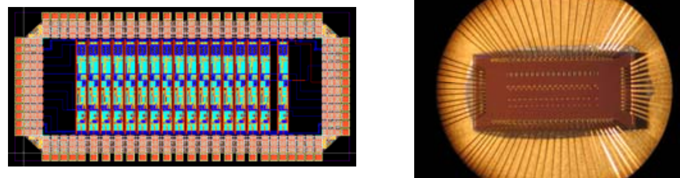


Figure 4. 180nm chip layout and picture.

The preamplifier is a buffered folded cascode structure providing a gain of 8 mV/ MIP, the shaper is an active CR-RC filter using an optimised version of the preamplifier. Power is 210 mW for the preamplifier and shaper. The chip has been extensively tested, process spreads within a wafer have been measured of the order of 3 % (Figure 5)

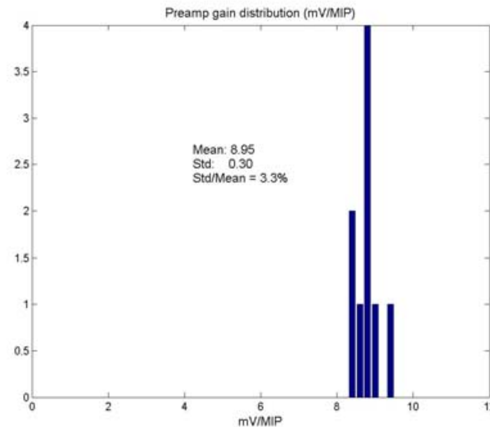


Figure 5. Process spreads (preamplifier gain) across a 180 nm CMOS Multi-project wafer from UMC.

The shaper output noise is shown Figure 6. A total noise of 375 electrons + 10.4 be-/pF is found against 275 + 8.9 predicted by simulations, explained by a small instability of the shaper understood and fixed in the 130nm next version.

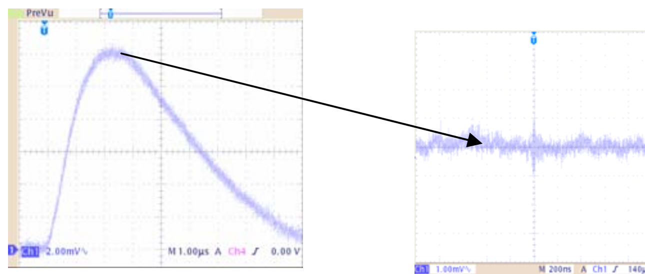


Figure 6. Shaper output. 375 electrons rms noise

As a conclusion, this process appeared to be stable and mature, models being accurate, yield excellent: only one failure found over twelve chips measured. As the 130nm CMOS process from UMC was available beginning 2005, it was decided to implement the next design in this technology.

- *CMOS 130nm Chips: SiTR-130*

The motivations to go to thinner process were the following: chips are smaller, faster, more radiation tolerant, dissipate less power. In addition, support will be given in the next years to these technologies that will be dominant in the industry.

However, some features make designs more constraining such as a reduced voltage swing (to keep the same electric field in the devices), leaks appear under the threshold voltage, as well as tunnel currents across the gates. Models are more complex, somewhat inaccurate in some cases as found later on, since the 130nm process is today less experienced as the 180 nm for which these problems did not show up. Table 1 compares 180 and 130nm technologies.

	180nm	130nm
3.3V transistors	yes	Yes
Logic power supply	1.8V	1.2V
Metal layers	6 Aluminium	8 Copper
MIM capacitors	1fF/ m^2	1.5fF/ m^2
Transistors	Three Vt options	+ Low leakage option

Table1. Comparison with some characteristics parameter of DSM CMOS technologies

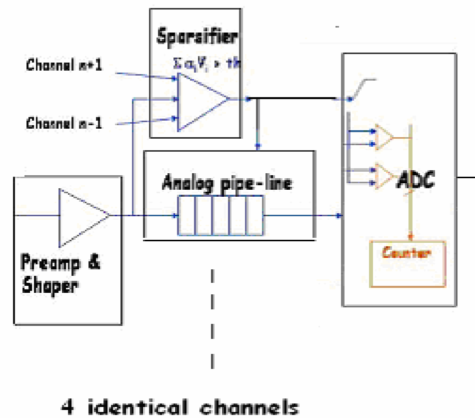


Figure 7. First 130nm prototype chip architecture

❖ *First 130nm Prototype Chip: SiTR-130_1*

The 4-channel chip (Figure 7) was received in end August 2006. Figure 10 shows a simulation of the analogue pipe-line signals and controls. Figure 11 shows layout and picture as well as analogue sections in 180 and 130nm at the same scale. The input stages have been tested and give results detailed below. The pipe-line and ADC are under tests

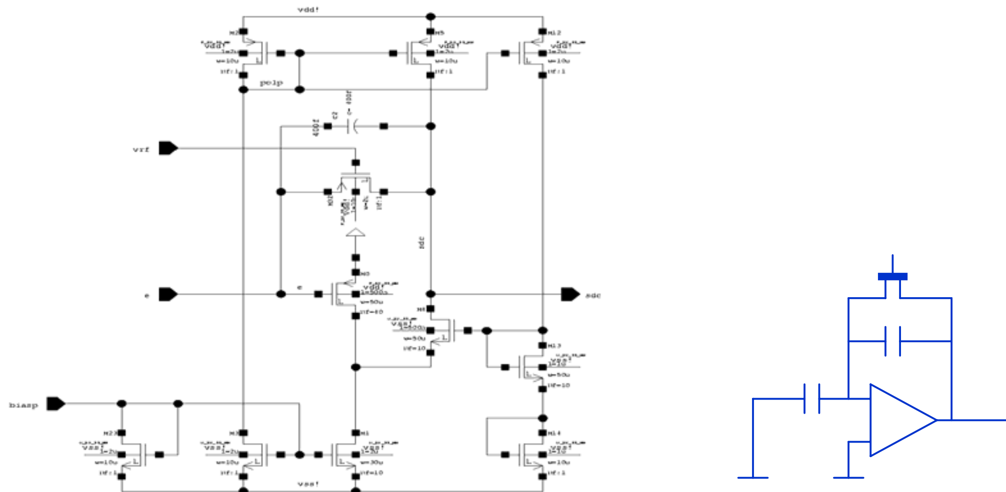


Figure 8. Preamplifier schematics

❖ *Second 130nm Prototype Chip: SiTR-130_2*

A second chip has been sent in October 2006, and received beginning January 2007. An improved version of the analogue pipe-line comprising an output amplifier has been included, as well as a Digital/Analogue Converter having in view the calibration, and the cancellation of some predictable process non-uniformities in a multi-channel version, some basic components for tests such as a calibration capacitor, and a large PMOS transistor. This second chip did not integrate the Analogue to Digital Converter part.

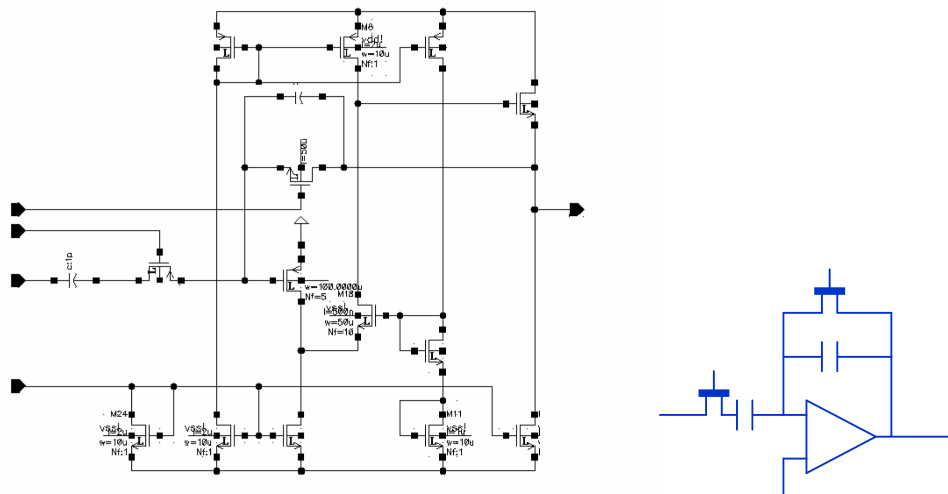


Figure 9 Shaper schematics

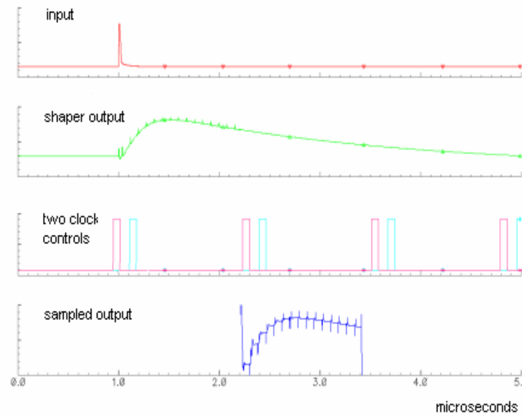


Figure 10 . Simulation of the analogue pipe-line signals and controls.

As an example, during the design of these chips, transistors noise was found much higher in simulations compared to the 180 nm process under the same sizes and trans-conductance conditions, and low V_t transistors somewhat more leaky compared to 180nm technology, as the low leakage option was not used. Verifications were performed using the original package from UMC under Mentor, rather than Cadence.

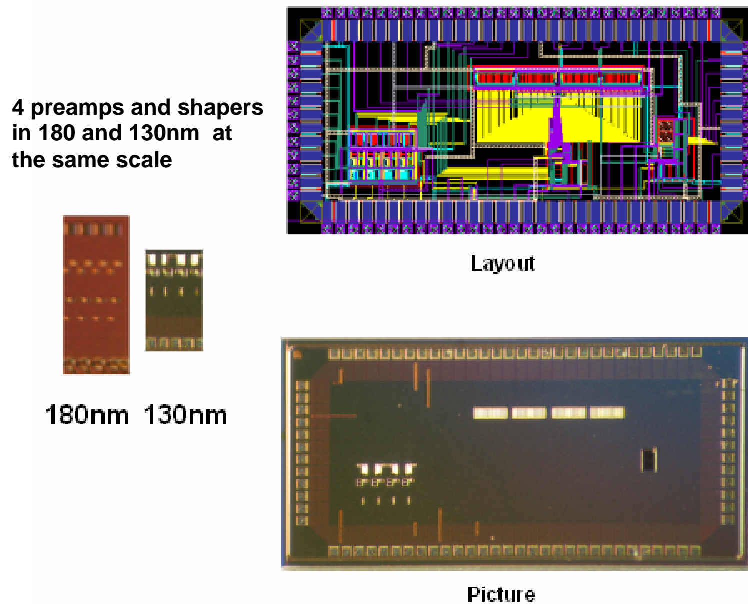


Figure 11. First CMOS 130nm Silicon. Layout and picture.

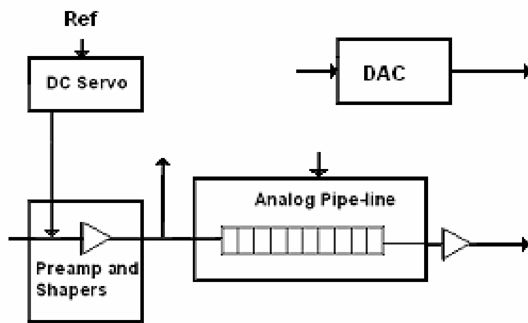


Figure 12. Second 130nm chip architecture

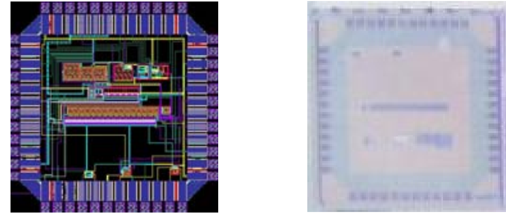


Figure 13. Second 130nm chip layout and picture.

➢ **Currently achieved results on the functionality of those chips**

For the CMOS 180 nm chips, at 3 µs shaping time and 210 µW / channel power the following results were achieved:

Gain:	**8 mV/MIP**
Preamp noise	**500 + 16 e-/pF**
Preamp+Shaper noise:	**375 + 10.5 e-/pF**

The first CMOS 130nm chips are under tests. The measured preamp gain is 32 mV/MIP against 28 simulated, according to an increased value of the feedback capacitor. This is not explained right now, simulations predicted a range of the order of milliseconds.

In the same way, the shaper time constant cannot be made longer than 2 µs, due to similar MOS transistor behaviour when operated under the threshold. Presumably, conduction is this regime is more important than predicted by the model.

The total measured ENC is one fourth of the simulated value. At 0.8 µs shaping time, it is 813 + 15e-/pF at the shaper output. Dynamic range can extend up to 20 MIP at 1% linearity, since 3.3V transistors are used in the analogue sections. At 2 microseconds shaping time, measured ENC is 625 + 9e-/pF.

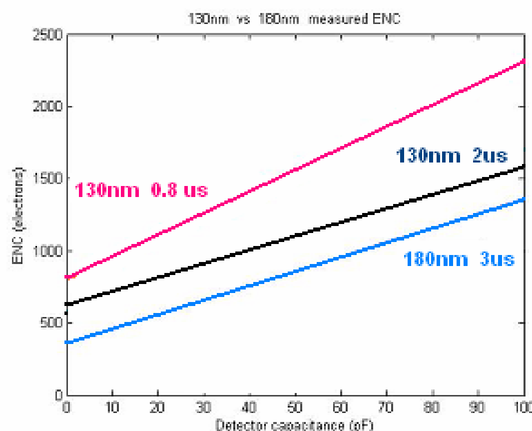
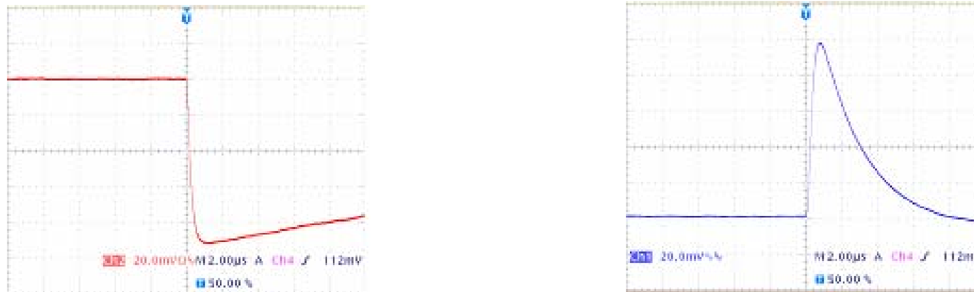


Figure 14. Noise in 180 and 130 nm. Shaping times: 180nm, 3 µs; 130nm, 0.8 µs.

Therefore the 130nm UMC CMOS technology although less mature than the 130nm is giving better results than even anticipated by the simulations. A noise worse by about a factor 2

between 130nm and 180nm UMC cases was anticipated from the simulations. As shown in the Figure 14, reality looks much better. This is quite encouraging.
Figure 15, shows the preamplifier response (left plot) and the shaper response (right plot). The horizontal scale is 2µs/square on both plots.



One should also note that the two submissions: 180nm and 130nm were successful at the first time already. This is indeed the case for the analogue part of the 130nm prototype currently under tests. The Paris team is now testing the analogue sampling part before attacking the digital part. This implies of course quite an amount of work to set the proper test bench and procedure to test these totally new parts.

- *Calibration*

Calibration will make use of on-chip circuitry comprising a precision reference voltage (band-gap), a DAC, and calibration capacitors (the achievable accuracy will be evaluated after measurements of the components laid out in chip 130-2). If the chip to chip spreads or temperature/voltage supply dependence of band-gaps or calibration capacitors values are found out the required specifications (an overall absolute precision of the calibration of 2% should be sufficient for a tracking readout), another strategy will be implemented, having the reference voltage and calibration capacitor still on-detector, but off-chip as discrete components. Current spreads due to process/temperature/supply dependence of integrated components using DSM CMOS technology let think the on-chip strategy is realistic. In any case, a set of on-chip switches network will multiplex the calibration pulse towards the required channel. This addressable switch network will also allow disabling a noisy or faulty channel. It will be implemented in the next 128-channel chip.

- **Pulse reconstruction, Centroids, Time picking.**

Reconstruction of pulses from samples including pedestal can be achieved using robust Minimum Least Square (MLS) algorithms such as developed by W. Cleland [*W.E. Cleland, E.G. Stern, Nucl. Instr. and Meth. A 338 (1994) 467*] for Liquid Argon Calorimetry (Figure 3). The pulse shape has to be known. Components spreads here have still to be known in order to predict the reconstruction accuracy. These algorithms provide both the time and the amplitude of the pulse, and should allow to reach a 5 µm precision for the position transverse to the chip making use of charge centroids, provided a sufficient Signal to Noise ratio is obtained on the detector. Time picking accuracy is estimated to 30ns for a slow sampling at 100ns, a few ns for a fast sampling at 10ns (See Figure 3). This reconstruction could be integrated in the Front-end chips

- On detector data packing.

Data packing will be performed both on-chip and on-detector. On-chip sparsifying will allow to build blocks of 5-byte data including strip address: log2[1024]=10b, charge 10b, and time: log2[3246]=12 b, and one extra byte for redundancy. With an occupancy of 1%, and 3246 bunches/train, each chip data block sent to the detector processor after on the fly AD conversion, would be at more (in the central region) 3246 x 1% x 1024 x 16 samples x 3 x 5 bytes= 8 Mbyte per train, assuming 3 strips hit per track, and 165 Kbyte after pulse reconstruction and centroid estimate with the detector processors.

- Track finding and amplitude/time estimation.

Track finding need to correlate different layers of detectors. On a detector layout such as depicted Figure 14, a combination of programmable logic devices (FPGA) and/or Digital Signal Processing sitting at detectors edges could reduce the dataflow sketched above to a few space points per detected track, to be sent upwards after the train. Fine amplitude and time estimation can be performed also at this level (See section below).

- **Perspectives and final goals**

A set of problems have to be tackled in the very next future, such as power switching, multi-channel design, process uniformity, fast shaping and fast pulse sampling having in view the 2-D readout, production issues for a large set of chips to equip the beam-tests detector prototypes, wiring on detector.

- *Next designs in 130nm (128-channel version)*

This chip will be the first one aiming to equip a full detector element. It will take benefit from the SiTR-180 and SiTR-130_1&2 designs and tests integrating low noise charge amplifier and shaper, zero suppression, sampling, event buffer A/D conversions, calibration and power cycling. Presently, 130nm CMOS technology is foreseen, unless 90nm is proven to be less noisy (some recent measurements indicate 1/f noise could be significantly lower (See *V. Re et al. IEEE Trans. Nucl. Sci. Vol 52, Dec 2005 p 2733*).

- *Design of fast sampling test chip*

A very fast front-end in Silicon-Germanium using bipolar input devices is foreseen to achieve 2D readout detectors, having in view an overall timing precision of the order of one nanosecond [*See M. Friedl et al. 12th LECC Workshop, Time Resolution of a Few Nanoseconds in Silicon Strip Detectors using the APV25 chip, September 25-29th 2006, Valencia Spain*]. The integration of this front-end together with CMOS technology would follow shortly, since this mixed process technology is available today, with the caveat that merging the two processes may alter the performance of each of them. This can be evaluated, at least with simulations.

- **Issues on technology choice**

- *Noise in CMOS DSM*

From the tests of the 130-1 chip, we conclude that the actual 1/f noise dictating the noise floor is of the same order as in 180nm, under the same conditions (Figure 14). 90nm will be investigated

- *Availability of design kits*

Design kits provided by Multi-project international centres as Europractice, CMP-Grenoble, MOSIS, CERN, including digital libraries are not always up to date. Their availability and merging into a Cadence or Mentor mainframe is a criterion of choice for a given technology node. This work made use of the UMC design kit provided by IMEC (Leuven).

It should be pointed out that there is expertise within the SiLC collaboration on various CMOS 130nm technology, namely: UMC (as reported here), ST Microelectronics, and IBM with our close contacts with CERN on this particular topic. This will lead us to compare these technologies in order to make a final choice, at latest by end 2007.

II-3-2: The power switching

The best power switching would reduce to zero the current needed in the analogue front-end chips sections between trains. This has been tried in simulation, and seems realistic, but has not been implemented in Silicon up to now. There are concerns about reliability operating in this way using simple MOS switches that may lead to current and voltages spikes during transients. In addition, the time needed before the front-end is truly active (i.e. able to amplify and pulse-shape is not negligible w.r.t the ILC timing (10-50 microseconds).

A way to overcome these drawbacks is to let flow a small fraction of the nominal biasing current through the input stages, instead of cutting any electrical activity. This can be done using current mirrors, or even switching the current sources used for regular biasing between two values, high and low. Ramping the voltage supplies could reduce greatly internal current or voltages spikes.

As for calibration, these strategies will be evaluated in the next chip design.

- *Zero power option based on SPICE simulations.*

This option basically switches the two voltages supplies from their nominal values (±1.65V) to zero. The simulation below (Figure 16) shows that provided the integrating capacitor of the charge amplifier is reset before power-off and after power-on, taking 5 μs.

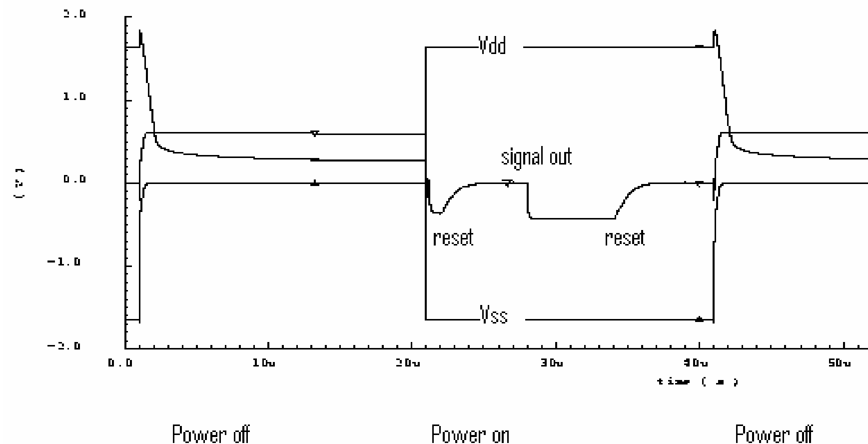


Figure 16. Simulated power switching at zero power-off.

Maximum current spike on the supplies branches is A. Voltages spikes are more difficult to evaluate, at least the simulation does not show any bump at the output of the

preamplifier. Tests using true integrated hardware on a test bench have to be performed. A first test of this option is going to be done on the Electronics Lab test bench with the present SiTR-130_1chip.

- *Some power option*

Another option is to switch the current source feeding both the preamplifier and shaper between two values to be determined by simulation.
In this option, a very small fraction of the order of 0.1% to 1% (to be determined by the simulation studies) of biasing current is held during the « power off ».This can be done in a very simple way by switching one more transistor in the current mirror.

Figure 17 shows the effect on the current in the supplies branches.

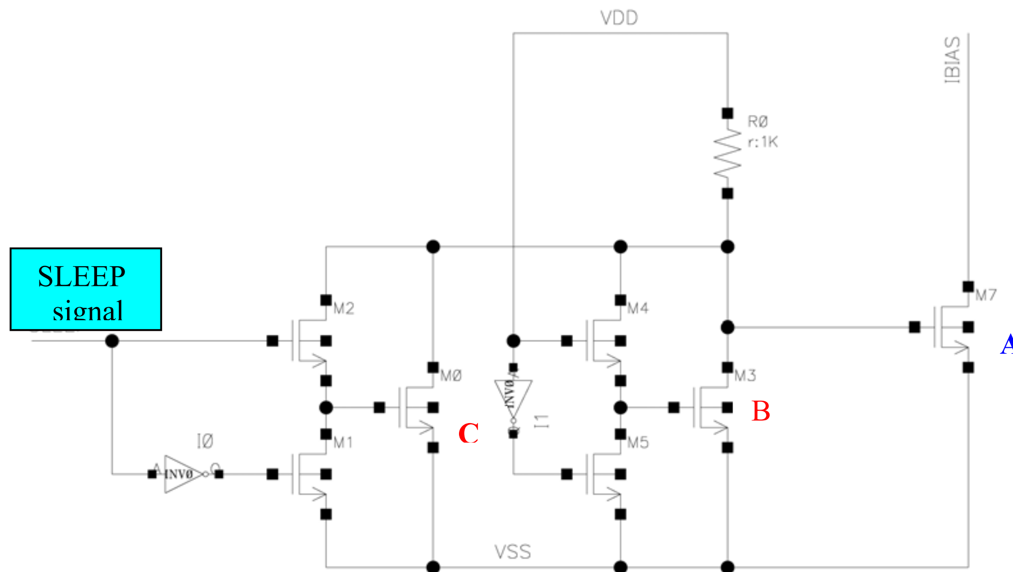


Figure 17: Schema of power switching with some power left

When the « SLEEP » signal is set to low, the value of the bias current is determined by the ratio of the width of transistor A ($\mathbf{w_A}$), over the width of transistor B ($\mathbf{w_B}$), i.e.: $\mathbf{w_A/w_B}$.
When the « SLEEP » signal is set to high, the ratio to be considered is width of A over width of B plus width of C, i.e. $\mathbf{w_A/(w_B + w_C)}$.
The width of transistor C ($\mathbf{w_C}$) determines then the value of the bias current during the sleep mode.
Simulation studies are going to be done to evaluate the optimum value of the sleep bias current.

Whatever the option, the simulation has to take into account the maximum current and voltages transients that may damage the CMOS circuitry. In addition, a recovery time after power-on less than 50 µs should be granted. The power cycling after simulation studies will be included in the next SiTR-130 version

Reference:

[1] J. David, M. Dhellot, S. Fougeron, J-F Genat, R. Hermel, H. Lebbolo, T-H Pham, A. Savoy Navarro, R. Sefri, S. Vilalte, *Front-End Electronics for Silicon Trackers readout in Deep Sub-Micron Technology: The case of Silicon strips at the ILC*, presented by J.F Genat at

the 12th Workshop on Electronics for LHC and Future Experiments, Valencia, Spain, Sept 25-29th 2006, to appear in Proceedings of the Conference.

II-3-3: Wiring on detector and cabling

SILC tracker needs very accurate spatial information. Particle detectors, either strips or pixels, have high integration level and high number of channels per detector. Compared with LHC, the spatial resolution will be better, with a strip pitch in the order of 50 to 80 µm. Readout electronics also have a very high integration level and has to be very close to detector. There is a difficult interconnection due to problems with pitch adaptation between detectors and electronics.

The traditional approach, used in LHC, is to have detectors + pitch adapters + PCBs. Conventional PCB minimum pitch is too big compared to detectors. Next table shows the maximum pitch for inner and outer layers in PCB technology, up to class 6. PCB vendors are currently offering up to 16 layers.

PCB Class	3	4	5	6
Outer layer pitch (µm)	600	400	300	250
Inner layer pitch (µm)	500	300	250	200

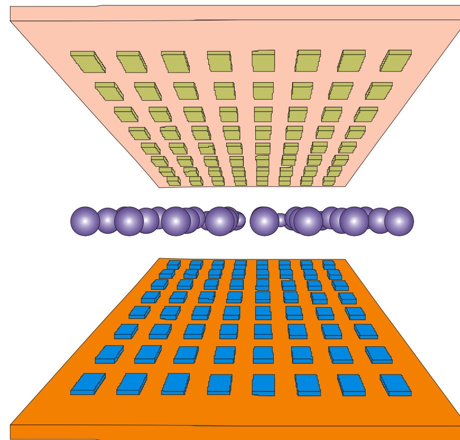
Some companies offer High density Printed Circuit Boards. There are few companies available, for example CICOREL, Switzerland and DYCONEX, France in Europe. The minimum achievable pitch is approaching 60 - 80 µm. They offer up to 8 layers maximum, but not at the minimum pitch. This is not enough for certain applications, is very expensive, and probably not suitable for large PCBs.

As a result of this pitch mismatching, it is necessary to use pitch adaptors. They are usually fabricated using microelectronics technology with metal on glass. This is a reasonable solution, but it requires an extremely high number of wire bonds. For example, each SCT-ATLAS inner module needs 4,722 bonds.

An alternative for wire bonding is flip chip with bump bonding interconnection. Following table offers a comparison between both technologies.

Wire bonding	**Flip-chip**
• Only periphery of chip available for IO connections • Mechanical bonding of one pin at a time (sequential) • Cooling from back of chip • High inductance (~1nH) • Mechanical breakage risk (i.e. CMS, CDF)	• Whole chip area available for IO connections • Automatic alignment • One step process (parallel) • Cooling via balls (front) and back if required • Thermal matching between chip and substrate required • Low inductance (~0.1nH)

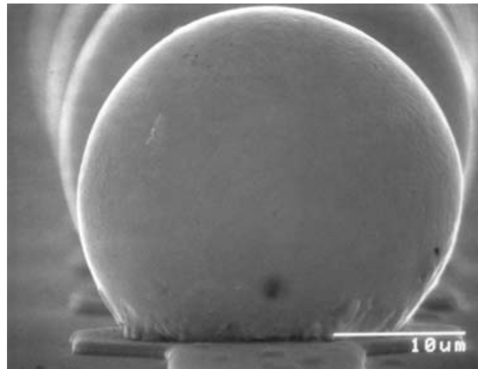
Bump bonding flip chip technology is the electrical connection of chip to substrate or chip to chip face to face (flip chip) using of small (in the range of tens of microns) metal bumps (bump bonding), as sketched in the figure:

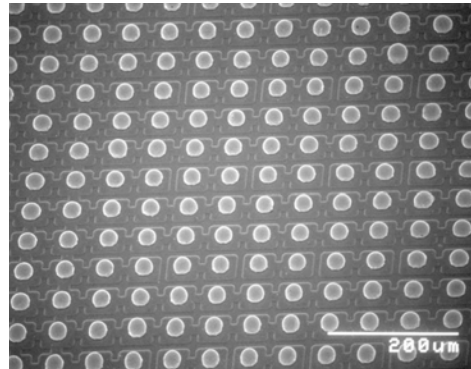


The main process steps are:

1. Pad metal conditioning: Under Bump Metallisation (UBM)
2. Bump growing in one or two of the elements
3. Flip chip and alignment
4. Reflow
5. Optionally underfilling

Next pictures show different views of electrodeposited Sn/Ag bumps manufactured at CNM.





It is an expensive technology, specially for small quantities (as in HEP) because there is a big overhead of NRE costs. Minimal pitch reported in the literature is 18 µm but we can find very few commercial companies for fine pitch applications (< 75 µm).

There are several bumping technologies, the most used are cited here:

- Evaporation through metallic mask
- Evaporation with thick photoresist
- Screen printing
- Stud bumping (SBB)

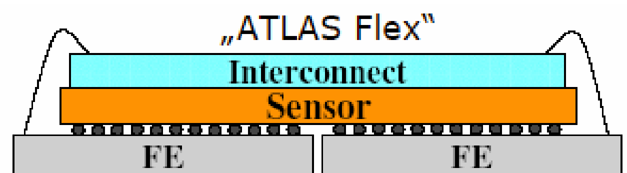
- Electroplating
- Electroless plating
- Conductive Polymer Bumps
- Indium evaporation

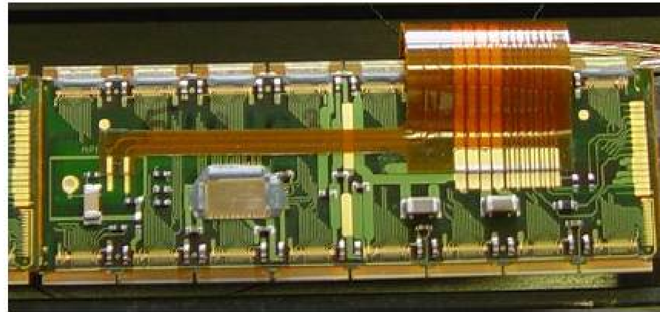
The most interesting for our application are electroplating, electroless plating or indium evaporation, each one with its own advantages and disadvantages. Stud bumping can also be considered for prototyping in the case of small number of bumps, as in strip detectors, but not for pixel detectors.

The most commonly used alloy for bumps is Sn/Pb. Nevertheless Pb is going to be banned in industry due to environmental issues. Moreover there are also potential noise problems as Pb is an alpha emitter, which is bad for particle detectors. Manufacturers are now looking for alternatives to Pb. They are many alternatives, either with lower or higher melting point temperatures. The reflea temperature usually is 40ºC more than the melting point. Next table offer a list of potential alloy replacements, but at this time there is no clear which one is the best one for our application and which ones will be finally choose by industries for mass production.

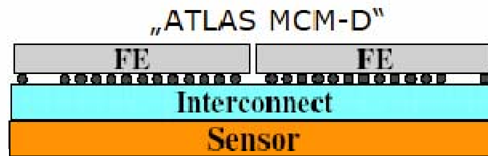
Alloy	Melt.Point(°C)
57Bi 43Sn	139
In	156
62Sn 36Pb 2Ag	179
63Sn 37Pb	**183**
90Sn 9.5Bi 0.5Cu	198
96.5Sn 3Ag 0.5Cu	218
96.3Sn 3.7Ag	221
95Sn 5Sb	236
89Sn 10.5Sb 0.5Cu	247
20Sn 80Au	280

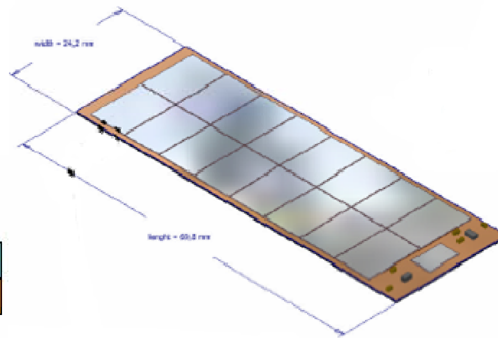
Bump bonding technology is currently used for pixel detectors. There is a "standard" technology, as used in ATLAS pixel modules, combining bump bonding with wire bonding using flexible PCB technology, the interconnect is made via Kapton foils, as shown in next pictures.

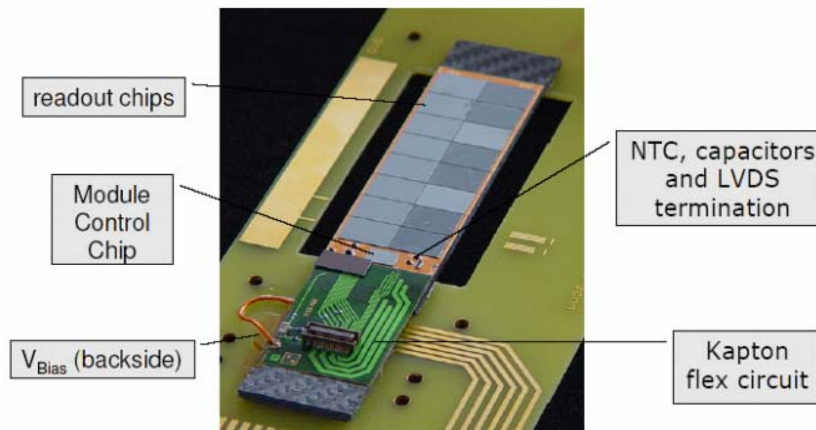




There are still more than 500 wire bonds per module in this "3D" design, and sensor has to cover gaps in electronics. It has been developed at FhG/IZM, Berlin more advanced solutions, based on an MCM-D approach. It allows up to 5 copper layers, with a minimum pitch of 30 µm (15 + 15). The final metal is Cu/Au with a dielectric of spin-on CBC photosensitive polymer with a thickness of 2 to 6 µm. The maximum process temperature is 250ºC and the main advantage is that there is more need for wire bonding. Next images show this technology.





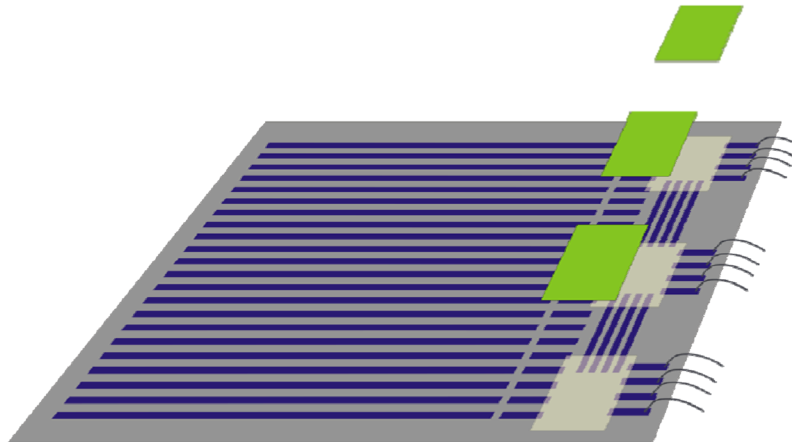


Next table summarizes the pros and cons of conventional versus advanced approaches in detector modules.

Pros	Cons
• Better module handling • Only bump bonding, no wire bonding • Reduced assembly steps • Higher degree of automatization during production	• Increased module size (but reduced height) • More silicon consumption • Lower testability • High complexity of the process • Industrialization: very limited number of companies available

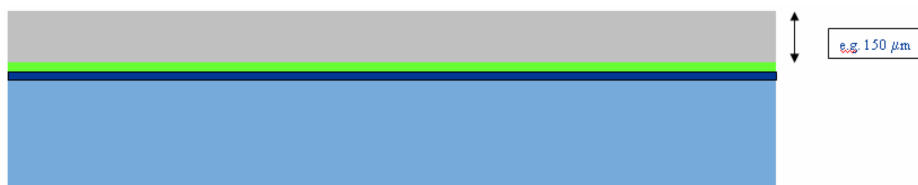
One of the main issues of Multi Chip Modules (MCM) is heat dissipation, but in our proposal, very low consumption electronics is being developed, which is combined with high detector quality with very low leakage currents. Moreover, in Linear Collider there is no much radiation degradation, so no big increases in current are expected. Therefore we think this compact approach can be used with air cooling only.

The same approach of wire bonding elimination can be applied to strip detectors by directly connecting readout chips bump bonded on detectors. Of course, this is made at the expense of an increase in detector area. In a first approach, a minimum number of wires in the detector, not in ROIC, is still used, as shown in the figure below. Nevertheless, they can be replaced by flex ribbon tapes with TAB (Tape Automated Bonding)

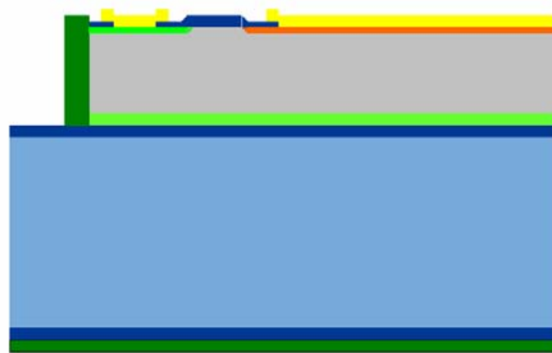


Finally, the combination of wafer bonding techniques with the use of Deep Silicon Etching for vias or active edge formation offers new state-of-art possibilities for detector modules.

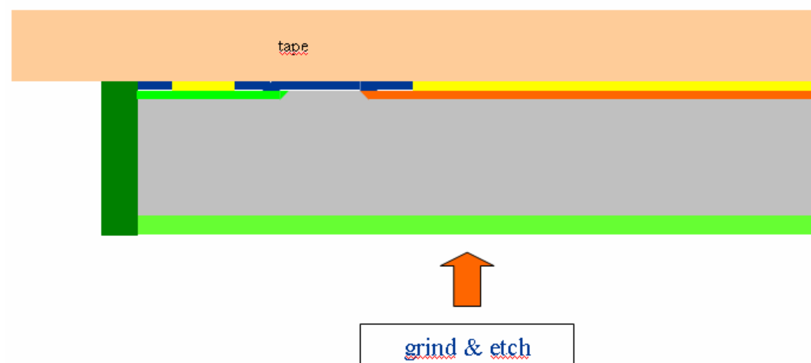
An advanced proposal, is the Edgless Thin Detectors, developed at VTT Finland. The starting point is two wafers bonded, on is thinned, acting as sensor, and the second is only a support structure, released at the end of the fabrication process.



Using deep silicon etching, trenches are made, filled with doped poly and detectors are diced with etching again.



Finally they are bonded to tape and the support wafer released.

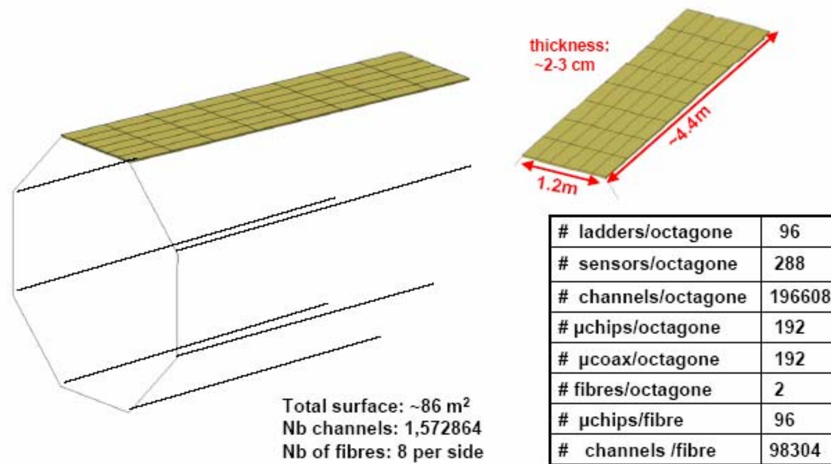


At the end of the process, thin detector are electrically connected without the need of using wire bonding; even the backside contact is made from the front through doped poly (dark green in the figure).

II-3-4: Cabling, Data Flow and Data processing: preliminary thoughts

This is a field that has not been yet tackled by SiLC; there are just preliminary thoughts [1] which are summarized here as an indication of the directions we might go. As an educated guess let's consider the case of the external barrel Silicon layer as proposed for instance in LDC case; it covers the largest surface and represents the largest number of channels.

The central outer barrel layer in this case, comprises eight plans of 4.4m in length, and 1.2m in width, each plane is subdivided in 2 in its medium part. This whole layer represents a total detector area of $86m^2$. It is made of two single-sided layers made of elementary modules built using 20 x 20 cm^2 sensors (if large enough wafers) and assembled in elementary module where 3 such sensors are bonded to each other thus making 60cm long strips. Figure 1 shows this outer layer that would be with an octagonal shape.



# ladders/octagone	96
# sensors/octagone	288
# channels/octagone	196608
# µchips/octagone	192
# µcoax/octagone	192
# fibres/octagone	2
# µchips/fibre	96
# channels /fibre	98304

Figure 1: External barrel layer layout

The present idea is to daisy chain several adjacent front-end chips (in this special case 4) on the two corresponding single-sided layers, of the same octagonal plane, with ***micro coax*** cabling. This would make 6 micro coax cables per octagonal plane read out in parallel by ***digital fibers*** in the considered example. One fiber could serve 2 half octagonal plane.

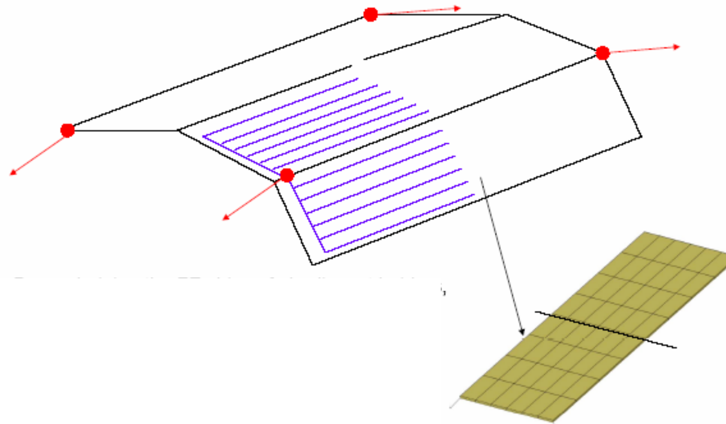


Figure 2. Outer Barrel layer readout schema

Data Flow Transmission: it is presently foreseen to use micro-coax cables of typically one inch diameter, 300 mW power dissipation at 1 GHz and that can be power cycled. Kapton cables are also under consideration. At a later stage in the cabling scheme, i.e. to transmit the information from the edge of the detector to the outside, 6GHz SCM fiber optic links are presently considered. (as sketched in the example in Fig. 2). This is under serious investigation because the following main issues /or concerns:

- Cabling versus and/or fibres: micro coax are making a real comeback
- High multiplexing rate versus redundancy
- Technological field that evolves very rapidly (telecom etc..)

<u>Data processing</u>: As described in the Front-End electronics section, after every bunch train, data is digitized and stored locally after zero-suppression in the front-end chips. Then, correlations between layers, amplitude and fine timing can be computed on-detector using dedicated hardware such FPGAs and/or Digital Signal Processors. These processors implemented as Multi-Chips-modules would represent a very small amount of material, and dissipate almost nothing, as they would be active for a short period. They would sit at the detector edges as shown in red Figure 2.
The following dataflow can be estimated from the assumptions above.
In the considered scenario there are 98,304 channels per fiber. There are 3,246 x 1/200 ms = 16,230 bunch crossings per second, with an occupancy of 1% and 6-byte data, therefore 1% x 98,304 x 3,246 x 5 x 6 = 96 Mbyte/s per fiber.

Besides it could be foreseen to implement at the edge of the detector some FPGAs / DSPs processing just before sending the signal through the fibres. This processing could consist in a centroid evaluation. Just as an educated guess and based on the fact that a centroid on n points requires O(n) multiply/accumulate operations, assuming a correlation over 5 adjacent strips. Time and amplitude reconstruction requires $O([4x(2n^2+4)])$ where m is the number of samples. 856 is obtained with m=10 samples. At a one nanosecond clock rate, the result is obtained in less than one microsecond. With 100 tracks per chip, the space points and time are computed in less than 25 microseconds, assuming a parallelism of 4 DSPs.

It will be a matter of policy of the ILC community and also of the experiments on how they will decide to handle the overall DAQ system, and what is the amount of processing that has to be performed on-detector and out-of-the-detector. SiLC has since the beginning taken part to the R&D activity on the overall DAQ and will follow it closely. The test beams will also be excellent playground to develop and experience ideas.

[1] J.F. Genat and A. Savoy-Navarro, *Preliminary thoughts on the DAQ for the next generation of Silicon Tracking systems,* presented at the DAQ session at LCWS06, in Bangalore (India), March 2006, and to be published in the Proceedings.

<u>Part III: The R&D Tools</u>

<u>III-1: Simulations</u>

Detector simulation is an essential tool in the R&D phase towards an experiment and during the data taking phase. In the R & D, the use is twofold. On the one hand, the simulation is used to perform a detailed analysis of some of the channels that play a central role in the experiment's physics programme. These studies allow establishing the physics requirements on the detector performance and derive the detector specifications. Some examples are given in Part I. On the other hand, “full” simulation provides a detailed estimate of the performance of a given detector solution. Thus, the effect of variations of the layout and technology can reliably be predicted and the performance of different solutions can be compared. Both fast and detailed detector simulations are discussed in the two next sub-sections. This includes the tools that are already available, some of them developed by people in the SiLC collaboration, or tools that are under development. It is important to mention that a real task force is raising in the Collaboration thanks to an increase interest and number of people that are joining the

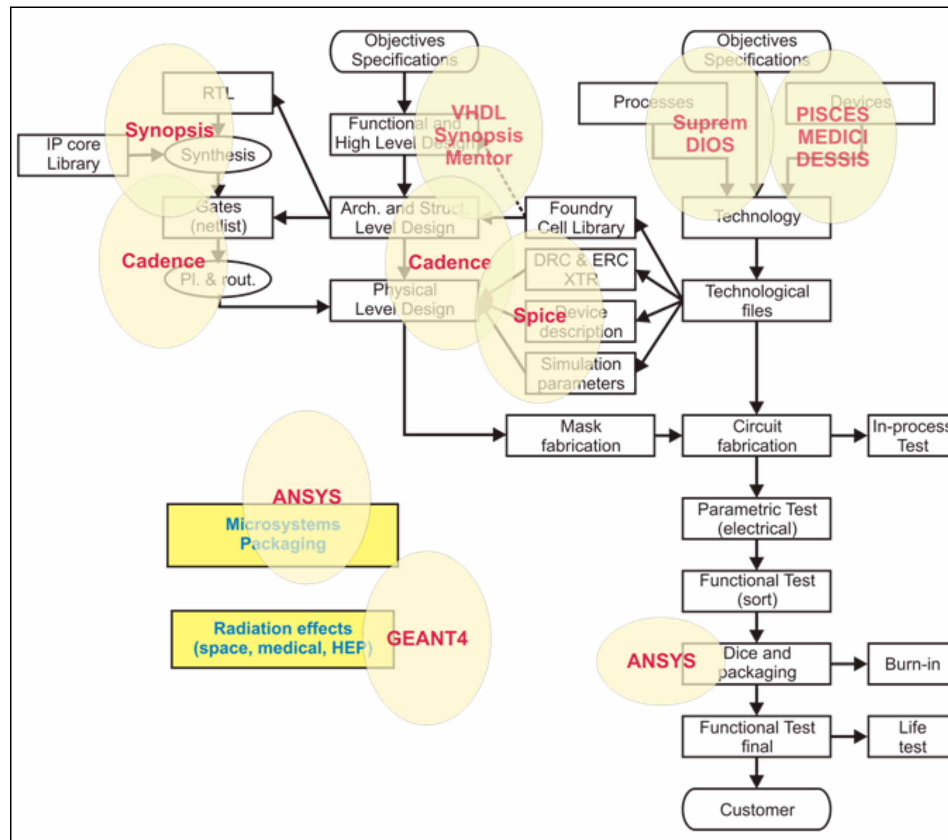
team. This work closely follows and indeed participates to the developments of simulation software occurring in the overall ILC community.

III-1-1: "Microscopic" simulations for studying the sensors and electronics or thermo-mechanical properties

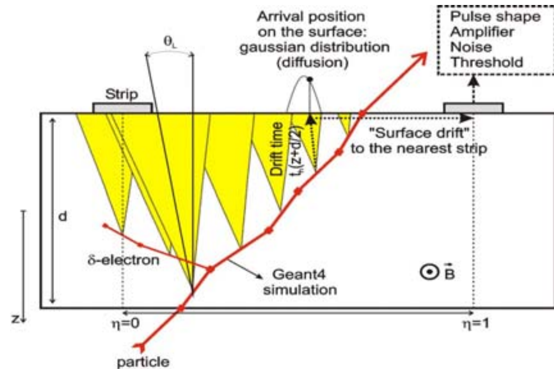
Simulation is a key point in development of detectors. Simulation is used in almost all the steps of development

1. Behavioral models --> Simulink, ADS
2. Functional and System --> Level System Verilog, System C
3. Logical and RTL --> VHDL, Verilog
4. Electrical Circuits --> SPICE, Spectre
5. Microelectronic Processes --> Suprem, Dios
6. Electronic devices --> Pisces, Medici, Atlas, Minimos
7. Mechanical devices --> Ansys, Coventor
8. Radiation behavior --> Geant4

For readout electronics development, simulations in categories 1, 2, 3 and 4 are crucial. Also for detector development, it is important the use of fabrication and electrical simulators, categories 5 and 6, to optimize the sensor design and the fabrication processes. For mechanical design and cooling optimization ANSYS is needed, and finally, to study the overall behavior under radiation conditions, GEANT has to be used. Next picture offers a schematic view of the use of simulators in different aspects of system development.



The SiLC collaboration gathers a variety of expertise on this simulation field. Prague has developed a GEANT4 based tool for this purpose that should be easy to interface with an overall detector simulation (see Figure here below) IMB-CNM/CSIC and HIP plus VTT use commercial software, such as ISE-TCAD or TMA for technology simulation. An example of the use of this simulation is discussed here below for the 3D detector.



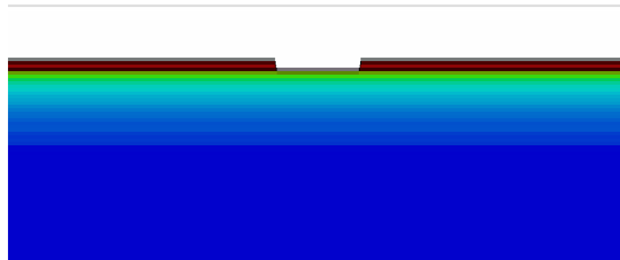
Geant4 simulation in http://www-ucjf.troja.mff.cuni.cz/diploma_theses/reznicek_dipl.pdf

Furthermore a simulation tool, MATLAB-based, is developed at LPNHE. It allows simulating the full signal processing, in a sort of "*fast simulation*" (see application of this tool to the time and pulse height resolution studies, reported in the electronics session). This tool could also be easy to link to the detector simulations that we are discussing now.

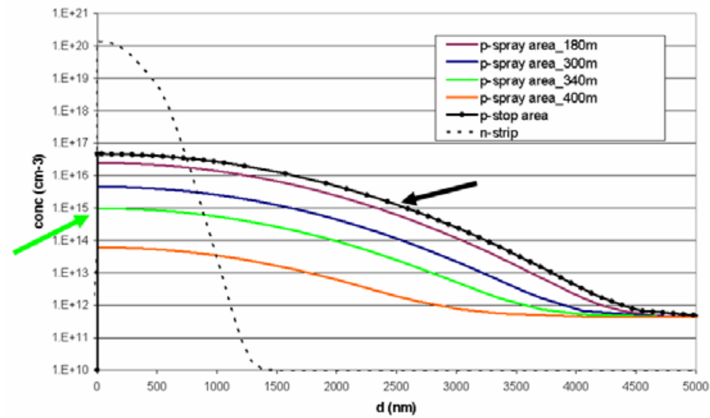
Example 1: Technology simulation to optimize p-spray insulation in p-type detectors

CNM has developed a process to perform insulation for p-type detectors based in moderated p-spray technology, propose by MPI, Munich. The first process steps are common to p-type detector fabrication: oxidation, photolitograpy p-stop regions, partial wet oxide etching, photoresist striping. At this point there are two different oxide thicknesses: thin oxide in the p-stop area and a thicker oxide on the rest of the silicon surface ("p-spray area"). We perform a P-implant (Boron ion, energy 50 keV, dose 10^{13} cm^{-2}). And we finish with the usual fabrication process

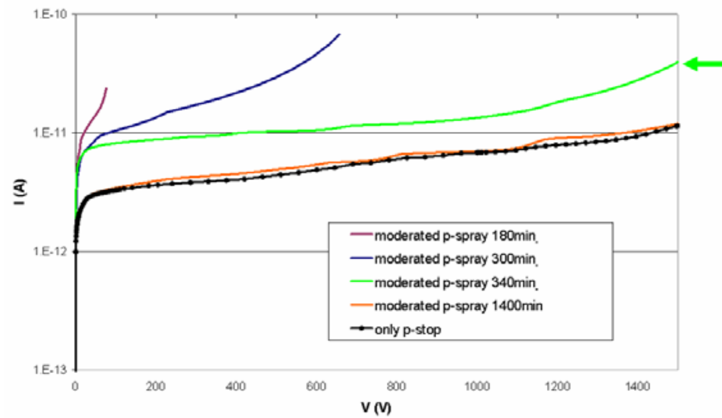
In this case, we have used a 2D process simulation, following figure shows the basic structure simulated.



First we optimize the doping profiles, varying oxide thickness, implant energy and dose, and reflow time and temperature. In next figure it is marked in green the selected profile for the insulation.

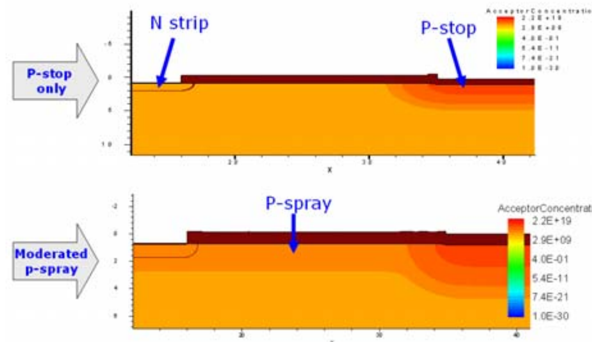


With the simulated profiles, electrical behavior is simulated. In the figure breakdown voltage is shown. In green it is marked the selected profile, corresponding to the conditions shown in the previous figure.

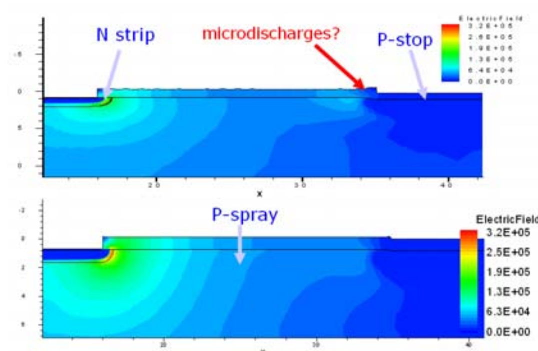


In the next figures we compare the doping profiles and electrical field inside the detectors for simple p-spray insulation and the new moderated p-stop approach. As can be seen the high field area, that is the origin of electrical noise due to microdischarges, close to the p-stop implant has been eliminated.

Example: Doping profile comparison



Example: Electric field comparison



Example 2: the TCAD simulation of semi-3D detector (performed by HIP and VTT)

Device models based on numerical solutions of differential equations were started by H. K. Gummel in 1964 on 1-dimensional steady state analysis of bipolar transistors [1]. In 1969, 2-dimensional models appeared with the analysis of junction field-effect transistor [2]. Also bipolar transistors were simulated in 1- and 2-dimensions by J. W. Slotboom [3]. It took more than a decade until one of the first 3-dimensional models was published in 1981. This model used finite element analysis in 3-dimensions for the study of the basic characteristics of semiconductor devices [4]. Almost simultaneously the first ion-implanted silicon detectors with planar structures on the material surfaces were produced [5]. Since then the detector production technology has developed rapidly and nowadays a great variety of production techniques exists.

Modelling is a very important issue in designing new semiconductor detector structures since many properties of these devices can be studied before manufacturing. It should be noted that the fabrication of high quality semiconductor devices is time consuming and expensive. Using simulations one can try to optimize the detector performance for a variety of different detector structures and even simulate different process techniques. In addition, one can obtain a deeper understanding of device performance, for example by studying the magnitude of leakage current or by defining the breakdown voltage. Until recently, 2-dimensional simulations of planar detector structures sufficed due to the small influence of the third dimension on the detector performance. With the 21st century process technology, the third dimension is becoming more and more important in understanding the performance of 3-dimensional detector structures. An example of this would be a novel structure called "semi 3D detector

structure", whose layout is presented in Fig 1. (left). Fig 1. (right) shows two photographs taken from the semi 3D structures with different electrode diameters and implant sizes [6].

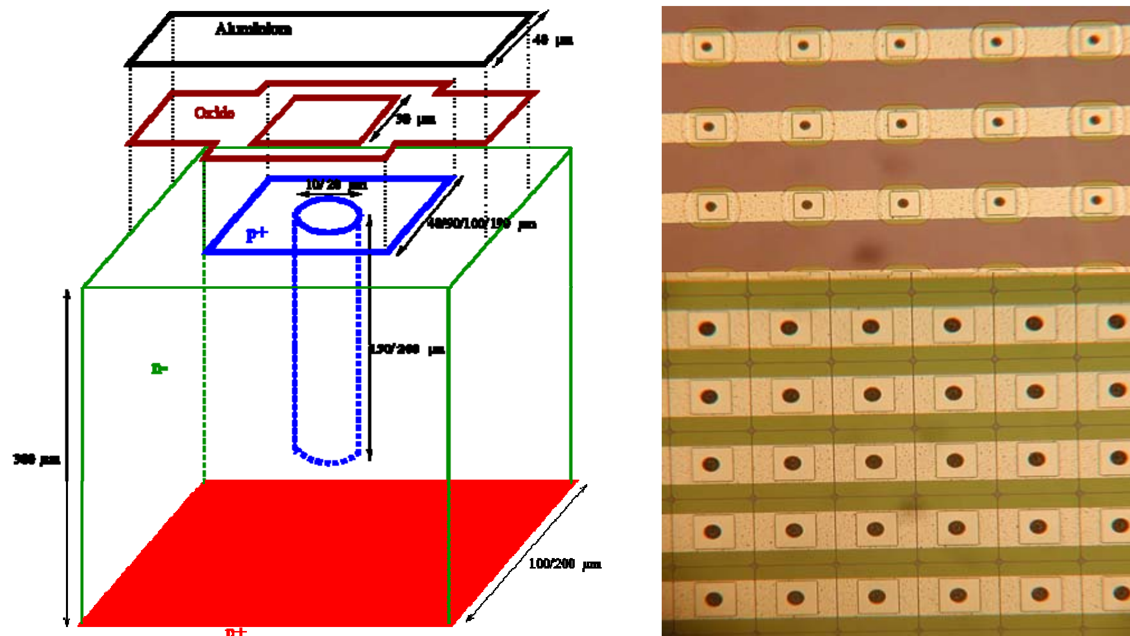


Fig. 1. ***Left:*** **Layout of one pixel of a semi 3D detector structure [vi]. The depth of the p$^+$ electrode is 150 µm or 200 µm corresponding to diameters of 10 µm and 20 µm. The implant size above the p$^+$ electrode is varied from 40 µm to 190 µm depending on the pixel size. The neighboring pixels are connected in series using aluminum strips.** ***Right:*** **Photographs of the fabricated structures. The upper one has the electrode diameter of 10 µm and the implant size of 40 µm, and the lower one has similarly 20 µm and 100 µm, respectively.**

The basic idea of a semi-3D detector design is to increase radiation tolerance, lower power consumption and simplify the 3D fabrication process, while keeping the spatial resolution and radiation attenuation depth similar to the planar or full 3D detectors.

Fig. 2 (left) shows simulation results using a device simulation software ISE-TCAD [7] to investigate the dependence of the zero electric field region (between grounded p$^+$ electrodes) on the implant size [6]. It would be practically impossible to simulate these kinds of characteristics using 2-dimensional simulation tools.

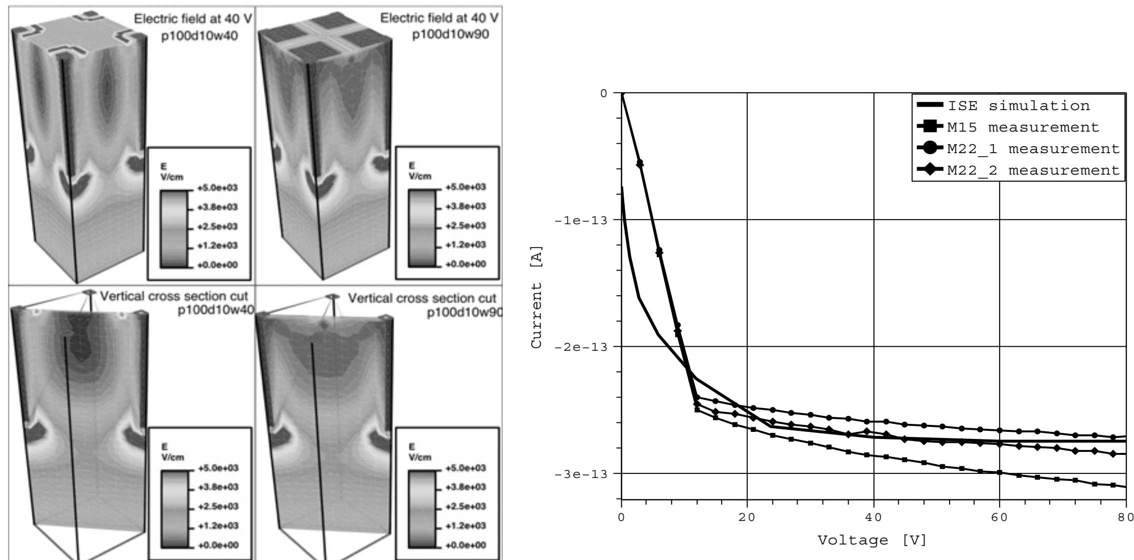


Fig. 4 ***Left:*** **ISE-TCAD simulations of semi 3D detector show the electric field distribution at 40 V with two different implant sizes (40 µm and 90 µm) [viii]. The zero electric field region (dark blue) decreases as the implant size is increased.** ***Right:*** **The measured and simulated leakage currents of semi 3D structure with implant size of 90 µm. The simulations give quite accurately the magnitude of the leakage current but the curve behavior at low voltages is different.**

Fig. 2. (right) depicts a comparison between simulated and measured leakage currents of semi 3D structure. The variation of the measured currents is quite large that is due to the measurement setup. The setup should be improved in order to draw conclusions of the accuracy of the simulations.

The 3-dimensional transient device simulations on the semi-3D detector structures were carried out using the ISE-TCAD software [[8]]. The transient simulation enables the user to define the charge collection characteristics of simulated detector structure. Fig. 3 shows the simulated current response pulses of a minimum ionising particle detected with structures shown in Fig. 2 (left). The minimum ionising particle (a fast proton) creates about 24 000 electron-hole pairs when passing through a 300 µm thick silicon wafer. Fig. 3 shows the leading edge of the current response pulses and charge collection curves of such a particle at 40 V. Fig. 3 (right) is an integral of Fig. 3. (left). It should be noted that the exact number of charge carriers created into the bulk is unknown in this case due to imperfect charge generation in the TCAD software. In the current version of the software the problem is solved. Almost all of the charge is collected in less than 20 ns at 40 V.

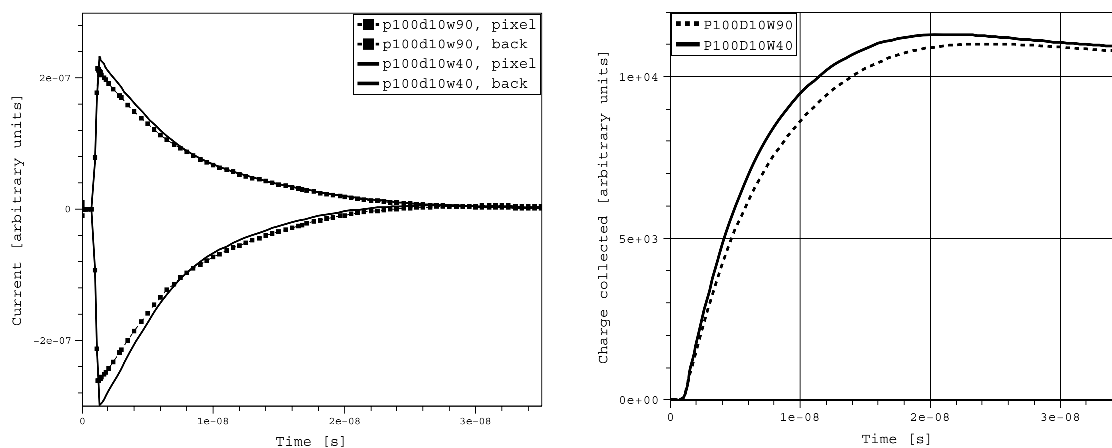


Fig. 3. ***Left:*** **The current response pulses of a proton passing through the simulated 3D detector structure at 1 ns; the effects of the positive surface charge (10^{12} 1/cm^2) and recombination were included in the simulation [8].** ***Right:*** **The charge collection curves of the proton with various reverse bias voltages [8].**

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[7] ISE TCAD Manual, Release 6.1, Integrated Systems Engineering (ISE), (2000)

[8] J. Kalliopuska and S. Eränen: Measurements and simulations of silicon semi 3D radiation detectors, Nuclear Instruments and Methods in Physics Research A 568, (2006), 22-26

III-1-2 “Macroscopic” FAST and FULL detector simulations

Detector simulation is an essential tool in the R&D phase towards an experiment and during the data taking phase. In the R & D, the use is twofold. On the one hand, the simulation is used to perform a detailed analysis of some of the channels that play a central role in the experiment's physics programme. These studies allow establishing the physics requirements on the detector performance and derive the detector specifications. Some examples are given in Part I. On the other hand, “full” simulation provides a detailed estimate of the performance of a given detector solution. Thus, the effect of variations of the layout and technology can

reliably be predicted and the performance of different solutions can be compared. Both fast and detailed detector simulations are discussed in the two next sub-sections. This includes the tools that are already available, some of them developed by people in the SiLC collaboration, or tools that are under development. It is important to mention that a real task force is rising in the Collaboration thanks to an increase interest and number of people that are joining the team. This work closely follows and indeed participates to the developments of simulation software occurring in the overall ILC community.

III-1-2-1 FAST detector simulations

In the "fast" approach the CPU-intensive tracking of the particle through the detailed detector geometry is avoided. Instead, the interaction of the particle with the detector is simulated using a simple model. For tracking detectors, the particle trajectory is typically modelled as a perfect helix. Multiple scattering of the particle in the detector material is parametrized. The position measurements are simulated by smearing the crossing point of the particle and the detector surface by the expected detector resolution. Most packages are moreover able to simulate random layer inefficiencies.

The simulation step is followed by a "dummy" pattern recognition phase. In the case of the two packages used within the SiLC collaboration, tracks are either produced singly or the hits are associated to tracks using the Monte Carlo truth information. No pattern recognition is performed.

Finally, the *found* tracks are fitted and track parameters are extracted. In this step, the fast packages used in SiLC are virtually at the same level of sophistication as the software of any modern spectrometer experiment. The track fit includes material effects. Thus, precise estimates of the resolution can be obtained.

Clearly, the fast simulation approach has its limitations. The measured parameter resolutions provide an "ideal limit". They estimate the performance that can be obtained when the tracks and hits are reasonably well-behaved (i.e. the trajectory closely follows the simplified track model in the simulation, the hit resolution is not affected by emission of a delta-electrons, etc.). And it assumes the pattern recognition phase converged successfully, as only hits (at least partly) due to the simulated particle are used in the track fit.

The enormous gain in speed compared to full simulation is the main asset of the these packages. There are, however, several other – related- advantages. The packages are very easy to install. Setting up of the simulation on a PC takes a few hours. And, last but not least, the packages present a simple interface to introduce modifications in the geometry. Addition or removal of an entire detector layer typically requires editing just one line in the job steering card. Similarly, the material can be doubled or halved at will. Thus, the end user can quickly understand the impact of a design modification.

In the following, two packages that have been developed for or adapted to the ILC, within the SiLC collaboration are described in detail.

Simulation à Grande Vitesse – SGV

(M. Berggren[*)], LPNHE, Paris)

SGV simulates colliding beam detectors in a solenoidal magnetic field.

The detector is described as cylinders with a common axis, parallel to the magnetic field, and as planes perpendicular to the common axis. The cylinders are described by their radius and minimum and maximum extent along this common axis. The planes are described by their position along the axis and their minimum and maximum radius. In addition, the material, the

thickness in radiation lengths, and the type and precision of measurements are also given as attached attributes. Each cylinder or plane can be divided in repeating sectors of measuring and non-measuring parts, so that e.g. blind sector boundaries between detector sectors or overlapping detectors can be simulated.

Cylindrical and plane calorimeters can be specified in a similar fashion. The geometry is given in the same way, while the energy resolution and the shower axis measurement precision are given by parameters.

The geometry is read from a human-readable ASCII file. A simple visualisation of the detector is included. To facilitate detector development studies, it is possible to have up to three detectors can be loaded simultaneously, which will be looped over event by event.

SGV is a machine to calculate covariance matrices: For each charged particle generated by the bare physics simulation (which can be selected at will by the user) which is either stable or decays weakly, SGV calculates which of the tracking detector surfaces the track helix intersects. From the list of those surfaces, the program analytically calculates the precision with which the parameters of the track can be measured. This calculation includes the multiple scattering in the traversed surfaces, and the measurement precision at each surface that measures the track position. It takes the spiraling of low p_T charged tracks in the magnetic field into account, as well as the dependence of the point-resolution on the angle of incidence of the tracks on silicon detectors, and on drift length in long-drift gaseous detectors. Precise formulae for multiple scattering [1)] are used, taking the rest mass of the particles into account. The production vertex can be chosen to be at any position in the detector, and the decay length can also be freely chosen.

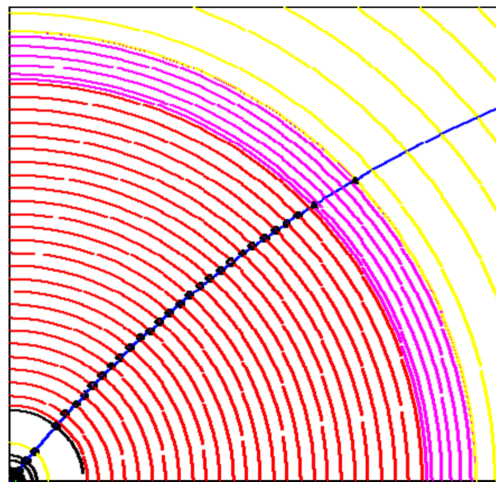

Figure 1: illustration of the simulated points on the cylindrical detector structure in SGV.

SGV will then smear perigee parameters according to the calculated covariance matrix, with Choleski decomposition method. This method takes all correlations into account. In addition, information on the hit pattern is accessible to analysis.

Alternatively, the analysis program can take advantage of the fact that SGV analytically calculates the full covariance matrix for any track it is given on input, and scan the detector with a “ray-gun” – an option included in SGV – thereby producing plots of any element of the covariance matrix versus the scanned property. The plots in this report showing momentum resolution versus momentum or polar angle have been produced in this way.

Each particle (neutral or charged) is also followed to its intersection with the calorimeters. The program determines which one the particle hits first (ignoring electromagnetic calorimeters if the particle is a hadron). From the user-defined properties of the hit calorimeter, SGV decides how the detectors will respond, either giving a MIP signal, an electromagnetic shower, a hadronic shower, or if no signal will be generated (either because the particle is below threshold, or because of inefficiencies). The parameters supplied by the user is then used to simulate the measured energy and the direction of the shower in the detector. Optionally, the program can also merge showers that are so close together, that they would be hard to distinguish in a real detector. As the tracking to and the response of the calorimeters are separate, it is easy to plug in other (more sophisticated) shower simulation code.

Scintillators and taggers are also be simulated much in the same way as calorimeters, except that they do not yield any energy-information, only the information if they were hit or not.

Optionally, the most important electromagnetic interactions in the detector can be generated, ie. bremsstrahlung from electrons and production of e^-e^+ pairs from photons.

The user can supply routines to simulate inefficiencies and particle identification.

To generate the initial event, interfaces to PYTHIA, JETSET and SUSYGEN are included in SGV. Single particle "ray gun" simulation is also included, as is the reading of generated events form an external file [2)].

The data used for analysis is delivered in COMMON blocks as extended 4-vectors, supplemented by track parameters with correlations, calorimetric clusters and hit patterns. When relevant, the corresponding true values are also given. including auxiliary information on particle history. Various global properties are also given.

SGV includes a set of analysis tasks: information on jets, event-shapes, secondary vertices, impact parameters and b-tagging is filled by calls to routines, included in SGV. Access routines give an easy interface to the detector geometry.

In the design of SGV, we kept in mind that the analysis code developed by the user should be easy to transport to an other environment, e.g. the analysis program of the experiment. This was accomplished by sealing of the analysis part of SGV as a separate object, which the rest of SGV need not to know the internal workings of, nor vice versa. Hence, one can develop an analysis "at home", write a small interface routine that reads the experimental data and formats it according to the specifications for the input to this analysis-object, and then use exactly the same analysis code on real data, or on data simulated by the full detector simulation. Such an interface, based on LCIO, has been developed by *B. Jeffery* at Oxford, and will be included in a forthcoming release of SGV. The analysis code needs by no means to be written in the same language as SGV.

In Annex 1, the application of SGV to the study of the Silicon Envelope as proposed in the case of the LDC detector concept is presented. It discussed in details the case for the various components of this Silicon tracking system. It shows how adding these various silicon components around the central TPC improve the performances of this overall tracking system.

[*)] mailto:mikael.berggren@cern.ch

[1)] *G. R. Lynch* and *O. I. Dahl,* Approximations to multiple Coulomb scattering, LBL-28165-rev. (1991).

[2)] Note that this option introduces a fair amount of i/o, and will compromise the real-time performance of SGV. It should only be used during development. In fact, SGV is structured in a way to make it easy to interface to other well-structured generators.

http://delphiwww.cern.ch/~berggren/sgv_ug/sgv_ug.html

The LiC Detector Toy

(M. Regler[*], M. Valentan and R. Frühwirth, HEPHY, Vienna)

This is a mini simulation and track fit program tool for fast and flexible detector optimization studies. A simple but powerful software tool for detector design has been developed for tracking studies at the ILC. It aims at investigating the resolution of reconstructed track parameters in the vertex region for the purpose of comparing and optimizing the track sensitive devices and the material budgets of various detector set-ups. This is achieved by a mini simulation of the set-up yielding the measured coordinates, followed by full single track reconstruction.

The detector model corresponds to a generic collider experiment with a solenoid magnet, and is rotational symmetric w.r.t. the beam axis; the geometric surfaces are either cylinders ("barrel region") or planes ("forward/backward region"). The magnetic field is homogeneous and parallel to the beam axis, thus suggesting a helix track model. Material causing multiple scattering is assumed to be concentrated within thin layers.

The mini simulation generates a charged track from a primary vertex along the beam axis, performs exact helix tracking in a homogeneous magnetic field with inclusion of multiple scattering, and simulates detector measurements including inefficiencies and errors. The basic version supports Si strip detectors (single or double sided, with any stereo angle), pixel detectors and a TPC; systematic and/or stochastic inefficiencies; and uniform or Gaussian measurement errors.

The simulated measurements are then used to reconstruct the track by fitting its 5 parameters and 5x5 covariance matrix at a given reference cylinder, e.g. the inside of the beam tube (they may be converted to a 6-dimensional Cartesian representation). The method used is a Kalman filter, with the linear expansion point being defined by the undisturbed track at that surface.

Subtle tests of goodness of the fits, like chi-square distributions and pull quantities, are standard. An integrated graphics user interface (GUI) is available.

The tool may optionally generate vertices with any desired number of tracks, thus being able to deliver input for a follow-on program studying multiprong vertices, or the separation of primary and secondary vertices; an output module was implemented for interfacing with the RAVE vertex reconstruction toolkit. In addition, it could also supply input for pattern recognition studies, for the development of alignment strategies, or for trigger simulation studies.

The algorithms used in the tool are on a solid mathematical base. The program is written in MatLab®, a high-level language and IDE, and is deliberately kept simple. It can easily be adapted to meet individual needs; for an expert this would take only a couple of hours.

The main purpose, however, is to supply a tool for non-experts, without any knowledge of the Kalman filter method or even a programming language. The program may be installed on a desktop or laptop PC, and used for obtaining quick results, e.g. when discussing detector related problems. Once the "input sheet" describing the detector set-up has been set up (certainly the most demanding part), individual detector layers can be moved, removed or modified within minutes, and the result of these changes can be evaluated after a very short running time. A beta release is available and has been used for the calculation of track and vertex resolutions in a simplified LDC detector set-up.

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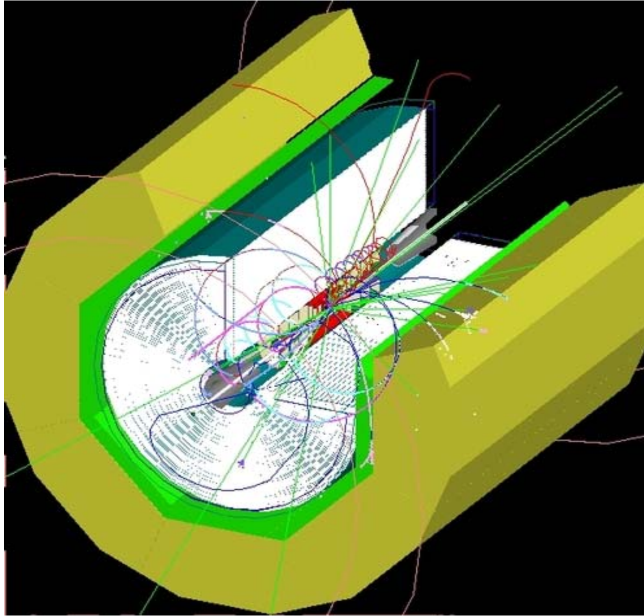
http://wwwhephy.oeaw.ac.at/p3w/ilc/talks/06_SiLC_Barcel/MK_LiCToy.ppt
http://wwwhephy.oeaw.ac.at/p3w/ilc/reports/LiC_Det_Toy/UserGuide.pdf

III-1-2-2: Full (GEANT based) simulations

To study the performance of the detector in all its detail "full" simulation studies are performed. The simulation package parses a detailed geometry description, containing geometry and material properties of all detector elements up to the most insignificant nut and bold. Realistic event topologies are produced using the well-known event generators. The generated particles are followed on their journey through the detector, where all interaction with the detector material are carefully simulated.



To convert the GEANT4 result (energy deposits in the active detector elements) into a realistic detector response, the signal collection and the subsequent processing by the Front End electronics is modelled in the digitization step. Provided all data formats are defined, the output of this step can in principle be made indistinguishable from a real event in the detector. Thus, all reconstruction software can be tested extensively on simulated events.

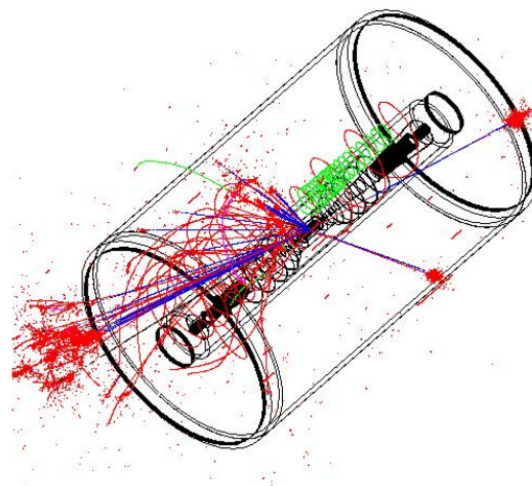
The final step of the "full" simulation is the reconstruction of the event. For the tracker this implies, reconstruction of position measurements and errors (hits) from the detector "digits", seed finding, pattern recognition and finally a track fit that returns a measurement of the particle four-vector. Tracks form the input to a large number of higher-level algorithms: vertex reconstruction, tagging of heavy flavour jets and hadronically decaying t-leptons, jet reconstruction, etc.

While a systematic and uniform "full" simulation framework and implementation are not yet available, significant progress is being made towards this goal in the ILC community.

The HepEVT standard essentially enables the use of all popular generators on the market.

Several packages for the central "full" simulation step, all based on GEANT4 [1], are available within the ILC community. The C++ package Mokka [2] mostly caters the European LDC studies. The Java-based SLIC [3] fulfils a similar role in the American simulation studies for SiD.

As "full" simulation is CPU intensive, sample production is necessarily a centralized activity. Low-statistics samples corresponding to different topologies, various detector layouts are available on Storage Elements in the world-wide computing grid. The use of a standard format for persistency storage, LCIO [4], throughout the three continents and four detector concepts greatly facilitates access to "full" simulation studies for individual students or institutes. The results from several studies



into machine-related backgrounds (most notably pair production due to beamstrahlung) are also available.

In the following the main achievements and shortcomings of the full simulation support for SiLC-like silicon sensors are listed:

- The geometry of two the silicon layers in the Large Detector Concept (LDC) has been implemented in the Mokka framework, as well as the all-silicon SiD tracker (*Valeri Saveliev*). For the LDC, moderate statistics samples of key physics processes, including pair background from beamstrahlung, are available.
- The SiD geometry has furthermore been simulated extensively in the the SLIC framework. Multiple samples for different physics topologies are available.
- A suite of digitization packages for the several detector designs is still largely lacking. As the designs takes shape and test bench and beam test characterisations become available.
- The final step of the “full” simulation – reconstruction of the events – is where most effort is required. Whereas in recent times two frameworks for reconstruction, MarlinReco [5] and org.lcsim [6], have seen the light, only a very limited number of algorithms is available. Recent times have seen the creation of several high-level algorithms like flavour tagging and particle flow algorithms. However, most of these algorithms rely on Monte Carlo truth information for the central underlying reconstruction steps. Systematic application of a full-blown track reconstruction algorithm to a large range of event topologies and detector geometries largely remains to be done.

In the following, a series of full simulation and reconstruction studies is described in some detail. A second example is found in Annex 1 on optimization of the pixel cell size.

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[1] http://geant4.web.cern.ch/geant4/

[2] http://www-flc.desy.de/ilcsoft/ilcsoftware/Mokka/

[3] http://www.lcsim.org/software/slic/

[4] http://lcio.desy.de/

[5] http://www-flc.desy.de/ilcsoft/ilcsoftware/MarlinReco/

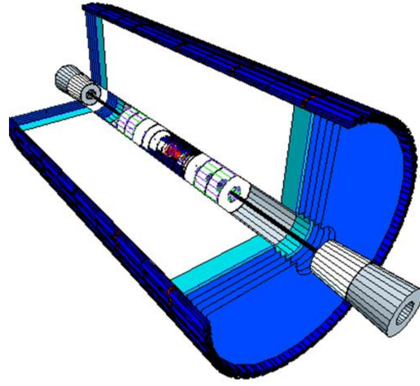
[6] http://www.lcsim.org/software/lcsim/

Geometry Implementation

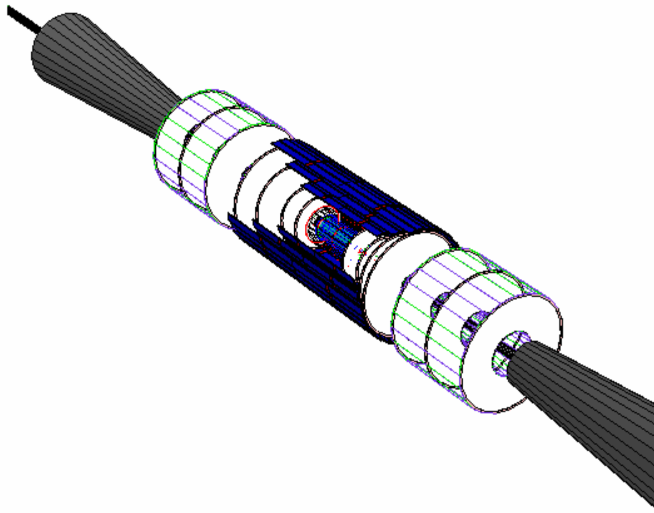
Full Monte Carlo simulations of the silicon tracking subdetectors in ILC experiments rely on two main frameworks, both based on GEANT4: the European framework Mokka, and the American framework SLIC. For Mokka, the geometry description is implemented in a MySQL database (supported by a lightweight toolkit, Gear); for SLIC, the geometry description is by XML-based GDML. A common geometry description toolkit (LCGO) is currently being developed by the SLAC software group.

In the LDC design, the silicon tracking system includes the Silicon Internal Tracker (SIT), the Forward Tracking Detector (FTD), the End Cap Tracker (ECT), and the Silicon External Tracker (SET) – together forming the so-called the “Silicon Envelope” to the TPC. As an illustration, the following three figures show (a) the overall silicon tracking components (the Si Envelope); (b) the details of the innermost components (SIT and FTD, together called “Inner Tracker”) together with the silicon vertex detector; and (c) the SET, consisting of one layer surrounding the TPC in the barrel region:

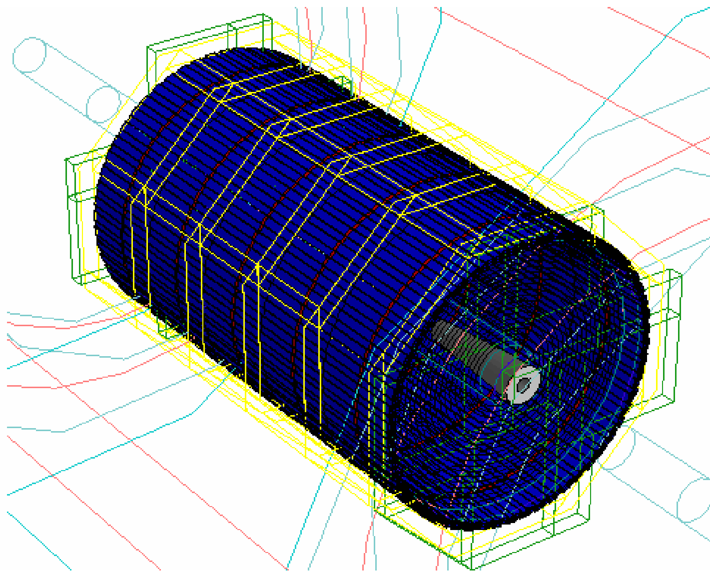
The SiD geometry was also implemented in the same framework (see as an example the fully simulated 6 jets event in the event plots next sub section).



(a) The Si Envelope (SIT, FTD, ECT and SET)



(b) Inner Tracker (SIT and FTD) and Si Vertex Detector



(c) The Silicon External Tracker (SET)

Reconstruction and Analysis

The reconstruction and analysis framework MARLIN is under development as a common effort of the LDC community; its track search and fit algorithms are derived from those of the DELPHI experiment at LEP. Studies in this framework on the silicon tracking performance are in progress. Below are given some preliminary results on event reconstruction in both the LDC and SiD detector concepts, and estimates of the occupancy in the various layers of the silicon envelope in the LDC concept.

One of the main physics channel for studying the overall tracking performance is Higgs-strahlung, because the goal is to get the intrinsic resolution of the Z^0 in order to study the Higgs bosons by the recoil mass method. This benchmark physics process is already included in the simulation framework.

Figs. 1a and 1b below show a fully simulated event of the Standard Model Higgsstrahlung process $e^-e^+ \rightarrow ZH \rightarrow l^-l^+$b-bbar. The event was generated with Pythia 6.2. The important initial state radiation (ISR) was simulated within Pythia, and the beamstrahlung was taken into account by the CIRCE simulation program:

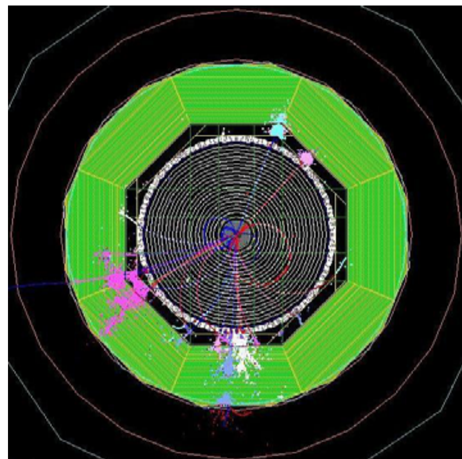


Fig. 1a: Mokka event display of a fully simulated Higgsstrahlung process in LDC

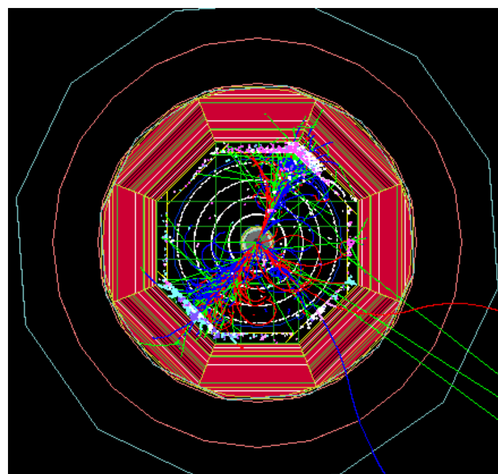
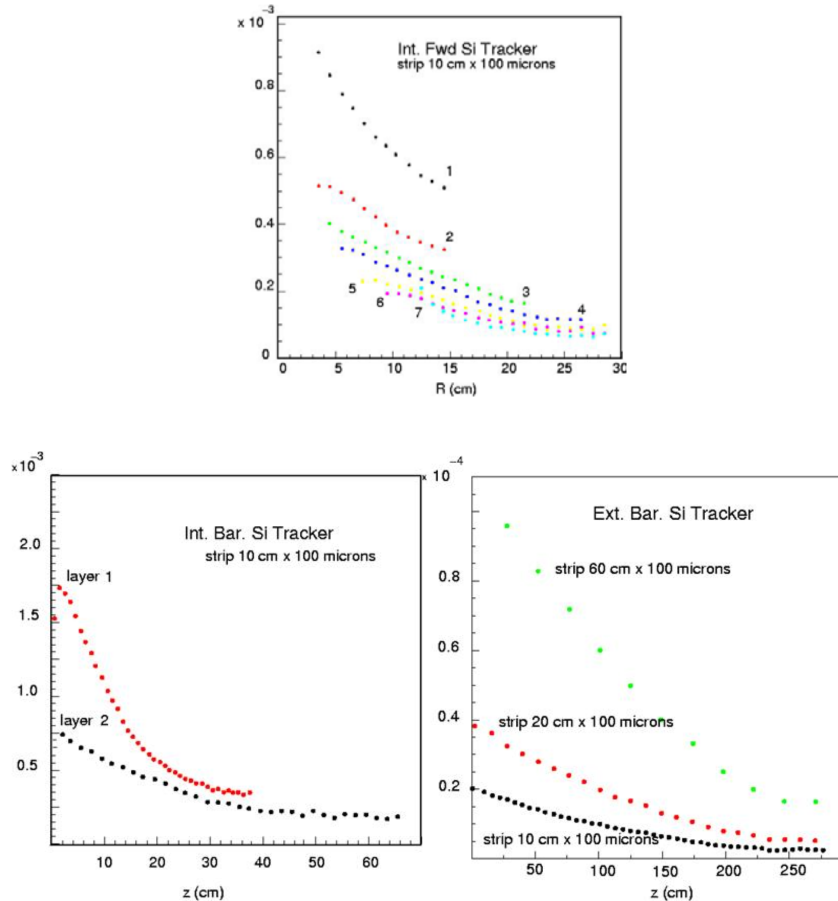


Fig. 1b: Mokka event display of a fully simulated 6-jet process in SiD

Other physics processes sensitive to the tracking system performance are under study and will be included in our strategies of investigation.

The plots below show the results of studies on the occupancy expected for Si strips of 100 μm pitch and 10 cm length in the forward disks (FTD), and in the two innermost barrel layers of the SIT. Also shown is the occupancy in the external barrel layer (SET) for strip lengths of 10, 20 and 60 cm, respectively.



At present, major efforts are devoted on the reconstruction framework, and on optimization duties of the sub-detectors in the full simulation and reconstruction environments for both the LDC (TPC and Si tracker) and the SiD (all-silicon) concepts.

The tracking environment

(M. Vos, IFIC, Valencia)

The tracking environment – most notably the density of tracks – is an important consideration for the design.

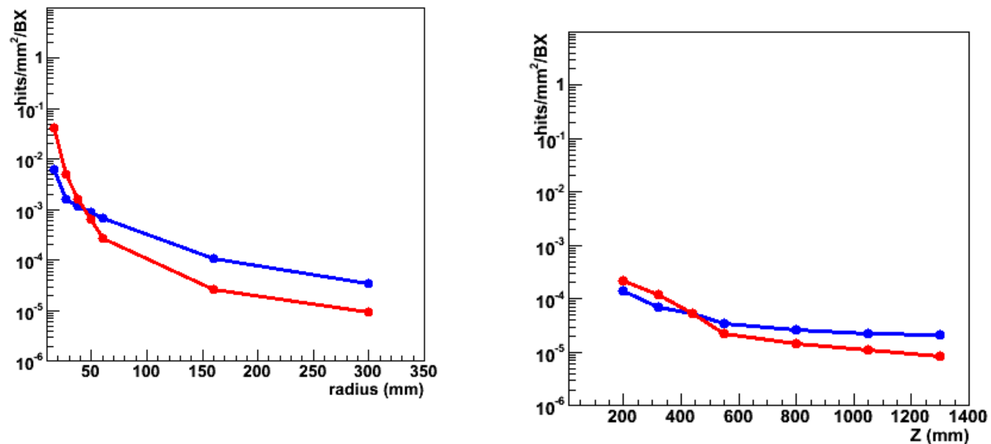
Full simulation results for the hit occupancy in top pair events and the contribution from the pair background due to beamstrahlung are shown in the figures below. The occupancy is presented normalized to an area of a 1 mm^2 and corresponds to the contribution from a single bunch crossing. Thus, these results are strictly the product of the layout and essentially independent of the detector technology. The pair background is the dominant source of hits in the vertex detector. In the innermost tracker layers, the contribution from the pair background

is quite similar to the occupancy generated by dense physics topologies like the top pairs simulated here.

To obtain the channel occupancy for a given technology the results should be convoluted with their specific response:

- cell area;
- the average cluster multiplicity;
- for the background contribution one should furthermore multiply by the number of bunch crossings that the read-out integrates.

The average occupancy as a function of distance of the layer from the origin is shown in the Figure here below:



The left figure represents the LDC barrel layers, including the vertex detector; the points at radii of 160 and 300 mm correpond to the intermediate SIT layers envisaged in the design. The right figure shows the same results for the end-caps with the geometry corresponding to the baseline FTD layout. The two curves indicate the contributions from a high-multiplicity signal topology (top pairs, blue), and the background due to beamstrahlung (red), respectively; the latter are obtained from the Guinea Pig generator and subsequent full Mokka simulation (courtesy of *A. Vogel*, Desy).

Naturally, the cell area has an important impact on the channel occupancy. In the vertex detector pixel sizes of 20 x 20 $\mu m^2 = 4*10^{-4}$ mm^2 are envisaged. A single-sided microstrip detector with a pitch of 50 µm and a strip length of 10 cm yields a cell area of 5 mm^2. Depending on the incidence angle and the characteristics of the technology used, each energy deposition by a minimum ionizing particle may result in a varying number of channels containing a signal above threshold. For microstrip detectors, this number is rarely much larger than 2 or 3, but the average multiplicity can be as large as 10 for certain vertex detector technologies. At last, the speed of the front-end electronics determines the relevance of the pair background. Therefore, a technology which can provide bunch crossing identification is inherently less sensitive to the pair background.

Full reconstruction studies for the SiD

(*B. Schumm, UCSC-SCIPP, Santa Cruz)*

The SiD baseline design incorporates a five-layer central tracker, extending from approximately 20 cm to 125 cm in radius, composed entirely of axial microstrip sensors.

Such a design raises a number of questions that can be addressed with simulation: what resolution can be aachieved with such a design; the capability of the detector to do pattern recognition in dense ILC jets, particularly for tracks that originate outside of the first few layers of the vertex detector; the degree of z-segmentation required of the tracker; and whether five is the optimal number of layers for such a design.

In 2005, the SCIPP group explored the capabilities of the VXDBasedReco algorithm (written by Nick Sinev, University of Oregon) to reconstruct tracks in the SiD detector. A sample of q-qbar events at E_{cms} = 500 GeV, with no machine backgrounds, was generated, and the reconstruction efficiency for tracks in the central detector was explored as a function of the angle α between the event thrust axis and the candidate track. The results of this study are shown in Figure 1: the efficiency is independent of α, but only about 94% integrated over all values of α.

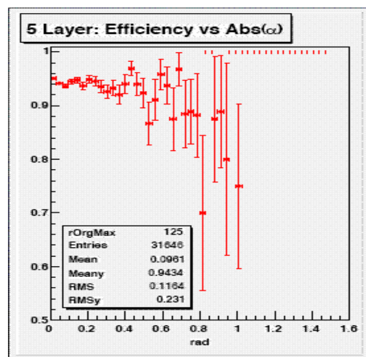


Fig. 1: SiD/VXDBasedReco track reconstruction efficiency as a function of angle from the jet core, for q-qbar events at √s = 500 GeV

In fact, VXDBasedReco requires vertex detector segments to seed tracks for the reconstruction, and so it is unable to reconstruct tracks that originate beyond the second layer of the vertex detector. Fig. 2 shows the efficiency vs. α strictly for tracks that originate within 1 cm (radially) of the origin. Again, the efficency is independent of α, but for this sample of prompt tracks, the average efficiency is 99%. Thus, it appears that the challenge for the SiD tracker is to reconstruct non-prompt tracks.

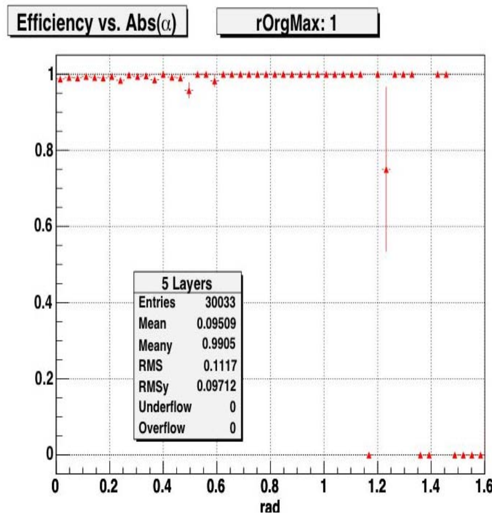


Fig. 2: SiD/VXDBasedReco track reconstruction efficiency as a function of angle from the jet core, for q-qbar events at √s = 500 GeV for prompt tracks (tracks originating within 1cm of the origin).

More recently, SCIPP has adapted a stand-alone reconstruction algorithm (AxialBarrelTracker, written by *Tim Nelson*, SLAC), originally intended to find tracks in the absence of the vertex detector, to find non-prompt tracks among the hits remaining after the reconstruction of prompt tracks. The SCIPP studies began with a characterization of the central tracker hits remaining after the elimination of hits due to prompt tracks.

Hits were assigned to one of four categories: "good", "looper", "knock-on", and "other", based on the characteristics of the track from which they were associated. "Good" hits are those from tracks with a total momentum is greater than or equal to 1 GeV. "Looper" hits are those from tracks with total momentum greater than 10 MeV but less than 1 GeV, and greater than six hits. "Knock-on" hits are from tracks with total momentum less than or equal to 10 MeV, regardless of the number of hits. "Other" hits are from tracks with the same total momentum as looper tracks, but with six or fewer hits per track. The following tables show the breakdown of tracks and hits within these categories About 6% of remaining hits come from tracks with sufficient momentum that make a single pass through the detector, while almost half (44%) of hits come from non-prompt looping tracks. An additional third (36%) come from very low momentum tracks that are presumably generated by material interactions.

Total tracks:	**6712**	**100%**
Good tracks:	445	6.6%
Looper tracks:	459	6.8%
Knock-on tracks:	3303	49.2%
Other tracks:	2505	37.3%

Total hits:	**30510**	**100%**
Good hits:	1754	5.7%
Looper hits:	13546	44.4%
Knock-on hits:	10821	35.5%
Other hits:	4389	14.4%

It's also of interest to explore the radial origin of the tracks that produce the remaining hits. From Figure 3, we see that the majority of "good" tracks have the profile of physics-generated tracks, while the remaining three categories, including "loopers", are dominated by material interactions.

Of great interest, of course, is the percentage of "good" tracks that can be reconstructed. We have explored the efficiency for reconstructing such tracks in the SiD detector with the adapted version of AxialBarrelTracker. In this study, we have assumed only two z segments in each layer, i.e. that each detector layer is compsed of two ladders, each of which runs half the length of the layer.

For this study, we have refined the definition of "good" track somewhat, defining a class of "findable" non-prompt particles with the requirements that (1) the particle be charged, and not originate from a material interaction ("backscatter") in the calorimeter; (2) the particle have a radius of origin between 2 cm and 40 cm of the beamline; (3) the paricle have a transverse momentum of greater than 0.75 GeV and a pathlength in the detector of at least 50cm; and (4)

the particle have a polar angle θ within |cos(θ)| < 0.8. In a modest sample of Z^0 –> b-bbar events in SiD, a total of 378 "findable" non-prompt tracks were identified, with an average frequency of roughly two per event, or about 4% of all tracks.

Reconstructed AxialBarrelTracker tracks, which are required to have at least four hits (but can have no more than five hits), were associated with "findable" particles as follows. The "findable" particle that contributed the most hits to the reconstructed track was identified. If the track had four hits, and at least three of these came from the majority "findable" particle, or if the track had five hits, with at least four coming from the majority particle, the "findable" particle was labeled as "found". Any reconstructed track not labeled in this way as "found" was given the label "fake"

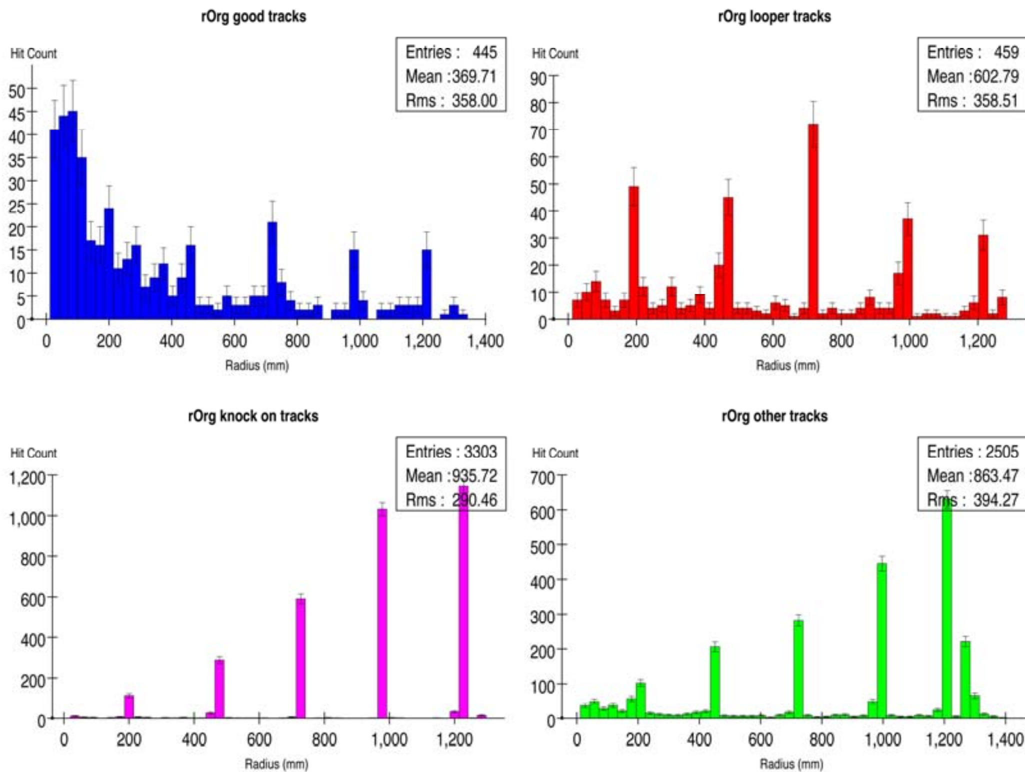


Fig. 3: Radial origin of non-prompt tracks. The upper plots, left and right, are for "good" and "looper" tracks, respectively. The lower plots, left and right, are for "knock-on" and "other" tracks, respectively. See the text for a definition of the four categories.

Of the 378 "findable" tracks, a total of 115 (30%) are "found" with five hits, while another 88 (23%) are found with four hits, for a total reconstruction efficiency of 53%. At the same time, though, 327 fake tracks are found, for a total purity of 203/(203+327) = 38%. However, all but one of the fake tracks has four hits. Thus, if "found" tracks are required to have exactly five hits, the purity becomes 99%, although the efficiency drops to 30%.

These results are quite preliminary, and there are a number of reasons to expect that they can be significantly improved. Although the SCIPP group adapted AxialBarrelTracker for this second-pass tracking, it has not optimized the routine, and there are a number of ideas that we will explore that we expect will improve the efficiency for finding five-hit tracks. In addition,

we will explore the addition of finer (10 cm) z segmentation, as well as the inclusion of additional layers.

III-1-2-3: Concluding remarks

In this still preliminary phase of the overall detailed simulation framework, the SiLC simulation effort should mainly aim to provide guidance, in the form of performance estimates for different designs, to the detector R&D.

The main available tools have been discussed above in this section. They comprise two fast simulation packages to estimate the track parameter resolution performance. A toolkit able to study the vertex reconstruction performance is being released. The flexible steering and fast execution times of these packages allow understanding the impact of design variations in a matter of hours.

The fast packages should be complemented by full simulation of several key layouts. Apart from corroborating the fast simulation results on the expected precision of the parameter estimate, these detailed studies can address the pattern recognition performance of the design. A detailed description of the LDC, containing all the silicon tracking components, is available in the Mokka GEANT4 simulation framework. The SiD layout is available in Mokka and lcsim.org. Several samples of key physics processes, including pair backgrounds, are available.

As the design becomes more and more concrete, and test bench and beam test results become available, a detailed digitization suite will be mandatory.

Detailed reconstruction studies are starting to take shape. There is an urgent need for a truly general track reconstruction software to be shared between different sub-detectors, and for different detector concepts.

The Valencia group is developing a toolkit (based on full simulation and a full-blown Kalman filter track fitter) to study the **pattern recognition** performance; the aim is to quantitatively evaluate the impact on the pattern recognition of several parameter. The development of a general **track reconstruction** toolkit has started recently (*N. Graf,* SLAC).

The Vienna group is developing a detector-independent toolkit for **vertex reconstruction** (RAVE). It deals both with “finding” (pattern recognition of track bundles) and with “fitting” (estimation of vertex position and track momenta). The algorithms used so far include robust adaptive filters, and are derived from the CMS experiment at LHC; further contributions (e.g. ZvTop) are considered as well. The toolkit is supplemented by a standalone framework (VERTIGO) for testing, analyzing and debugging. Tools include visualisation, histro-gramming, artificial event generation (“vertex gun”), an LCIO interface, and flexible I/O (“data harvester & seeder”). Emulation of various detector set-ups is supported by a flexible “skin concept”. Main design goals have been ease of use, high integrability into existing software environments, extensibility and general openness. The toolkit and framework are coded in C++, with interfaces for other languages (Java, Python). Embedding RAVE into MarlinReco and org.lcsim is under way; a beta release is available.

Last but not least, as mentioned at the beginning of this section the SiLC collaboration has recently launched a simulation task force thanks a dedicated team that now has reached a critical mass in terms of expertise and of manpower.

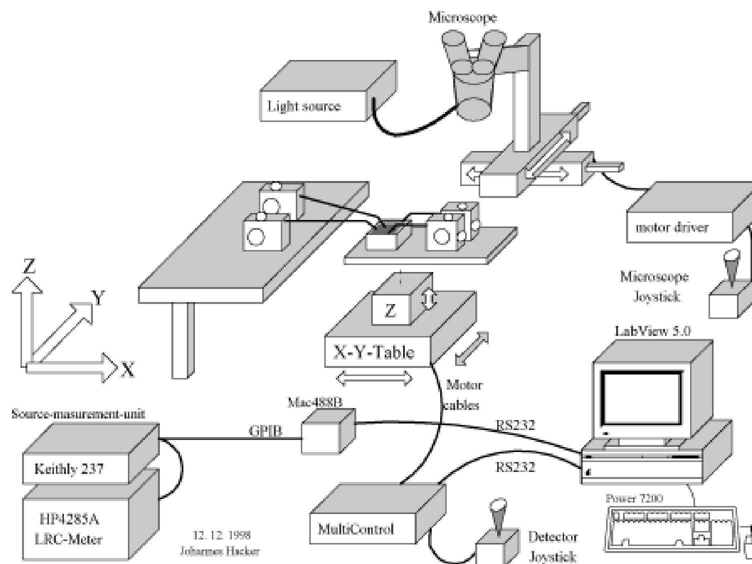
III-2: Lab test benches , description and present results

Different kinds of Lab test bench were already developed from previous experiments or ongoing construction of Silicon devices. New ones are being developed in certain Labs not yet equipped with the requested facilities. In both cases the Lab test benches will need continuous upgrade to evolve with the technological developments we are undertaking.

III-2-1: Lab test benches for sensors quality test and characterization

1. Strip-by-Strip Test System

The sensors for future high-energy experiments will have many strips to achieve a high spatial resolution. An automated test system is necessary if the measurement of the electrical parameters of each single strip is required. A schematic overview of the setup described below can be seen in the following drawing and picture of the real setup.



Semi-automatic probe station - System overview

The mechanical set-up of this system consists of a vacuum support carrying the sensor. This support is moved by a motorised XYZ-table together with a micro positioner holding two needles that are in permanent contact with the detector's bias line. This arrangement allows the spatial movement of the sensor while the bias voltage is always applied. Two additional micropositioners are located on a separate support and probe the individual strips. These two probes contact both the DC and the AC pad of each strip. The sensor is moved by the XYZ-table in a way that the strips are located sequentially underneath the stationary probe needles. The system is controlled by a computer running a LabVIEW measurement program and communicates with the motor controller and the instruments via an IEEE488 interface bus.

Once the sensor is placed onto the vacuum chuck, the system has to be aligned. Three reference points on the sensor are located so that the program can determine the orientation of the sensor and the pad positions. The pad layout of the sensor is loaded from a configuration file and, therefore, this system can measure different sensor layouts without hardware modifications.

The electrical circuit of the system is designed for high voltages up to 1000 V and very low currents in the range of a few pA. Therefore, HV isolation and shielding of all cables are crucial items. Two source measure units, a LCR-Meter and an electrometer are connected to the sensor pads via a cross point switching matrix, depending on what electrical parameter is measured: The strip leakage current I_{strip}, the poly-silicon resistor R_{poly}, the coupling capacitance C and the dielectric current I_{diel} values are measured for each strip. The instruments can also be configured in a way to measure the total leakage current (IV) and the total capacity (CV) of the sensor versus the reverse bias voltage. Both quantities are measured during a single bias voltage ramp.

Once the strip scan is finished, the strip parameters are compared against the required values defined in a text file. All channels, which are not within the specifications, are flagged and this information is stored in an XML file together with all the measurement results. This file is uploaded into a relational database system to allow a central storage of all measurements.

In this setup, the sequence of switching the switching matrix contacts between the instruments is a crucial point, since both the sensor and the instruments can be damaged if there are just minor inconsistencies in the switching sequence defined in the Labview software. The software has to be flexible in the measurement procedure while maintaining a high level of security against any kind of damages.

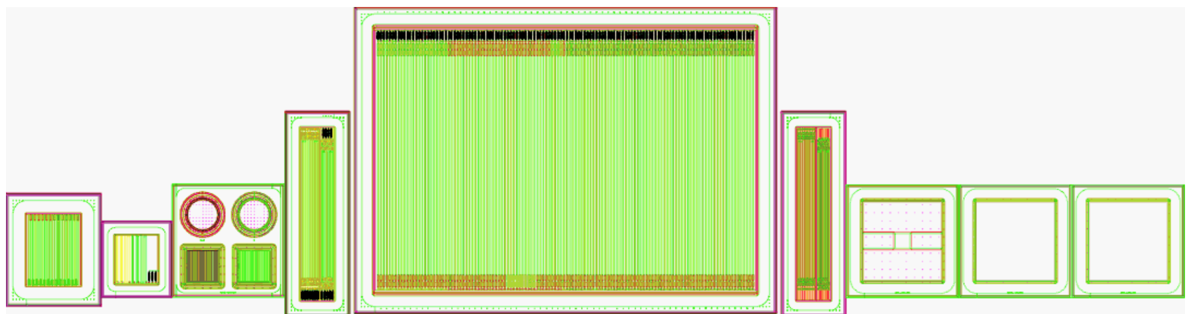
2. Monitoring of the manufacturing process

Each wafer should host additional devices beyond the sensor, designed to monitor the stability of the manufacturing process. Since these test structures were processed on the same wafer as the sensor, we can assume that both, the sensor and the test structures perform identical or exhibit the same weaknesses. A standardized set of nine test structures is under definition. This set consists of the following structures:

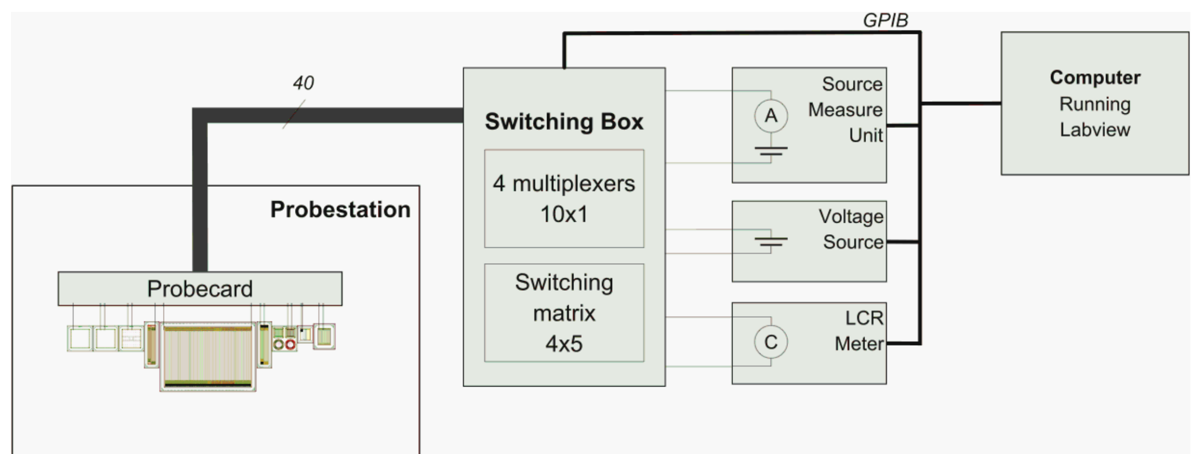
- Array of 26 strips directly connected to bias ring without bias resistor, used to measure the dielectric breakdown voltage and the capacitance of the dielectric oxide underneath the AC strips.
- A structure to measure the resistivity of aluminium, implant and polysilicon layers by applying a voltage to long lines of each type and measure the current.

- A gate controlled diode used to measure the surface current in the Si/SiO2 interface.
- A structure dedicated to measure the inter-strip capacitance.
- A similar structure but without polysilicon bias resistors to measure the inter-strip resistance.
- A structure called “baby sensor” which is a small replica of the main sensor. It is used to measure the bulk breakdown voltage and the bulk dark current at a certain voltage.
- A rectangular diode to measure the depletion voltage of the bulk material to determine the bulk resistivity.
- Two MOS structures used to measure the flatband voltage and to determine the oxide charge in both, the thick interstrip oxide and the thin readout oxide.

An illustration of these test structures can be seen in the following drawing.

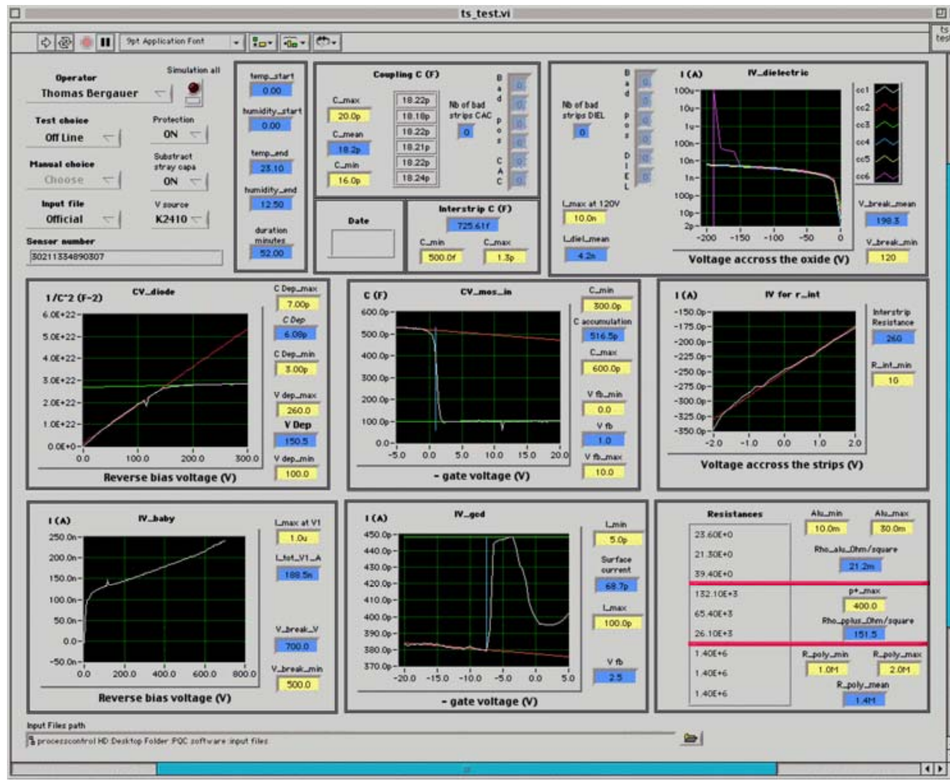


The setup to perform the measurements on the test structures is based on a probe card contacting all pads of the test structures with a set of 50 needles. A PC running Labview is connected to the instruments via the IEEE488 interface bus to control the instruments and the cross point switching matrix, which is used similarly to the strip-by-strip setup: It connects the instruments to the different needles that are contacting the corresponding pads of the test structures. A schematic overview of the setup is drawn below.



After the manual alignment of the needles of the probe card in respect to the pads in XY direction, the probe card must be lowered in Z direction to establish electrical contact of the needles. A measurement routine is started on the PC that performs the measurements on all structures automatically in a sequential order. After the measurements are finished, the software applies linear fits to the recorded IV and CV curves to deduce the interesting parameter of each curve. These results are again compared against predefined cuts and an

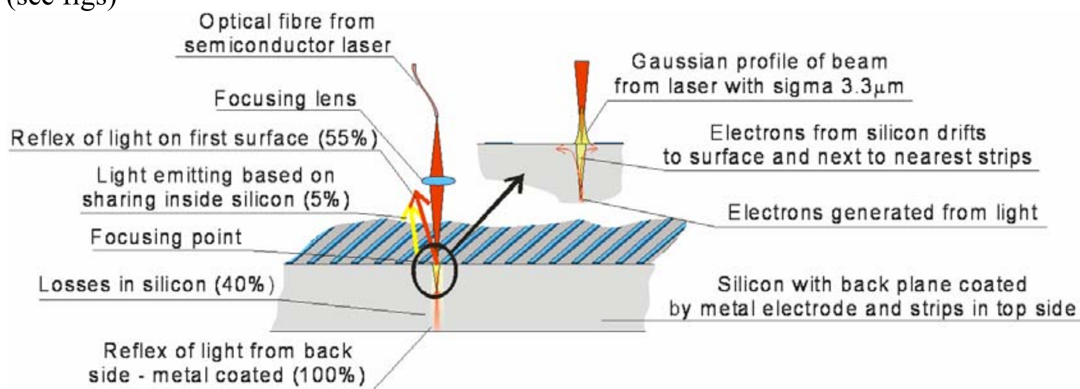
OK/not OK decision is stored together with all measurement data in a central relational database. A screenshot of the acquisition software is shown below.



The setup with the probe card does not allow a flexible layout of the test structures. For the R&D phase a more flexible system of individual micro positioners is developed to enable the testing of structures with different design from different suppliers.

- Laser test bench

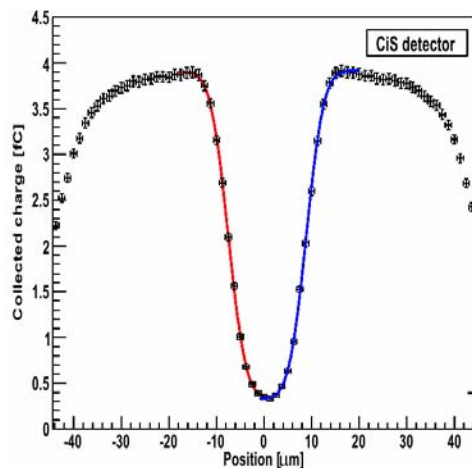
A system to evaluate the response of silicon strip detector to laser illumination exists in several laboratories. The ionisation characteristics of the laser light are different from a m.i.p., (see figs)

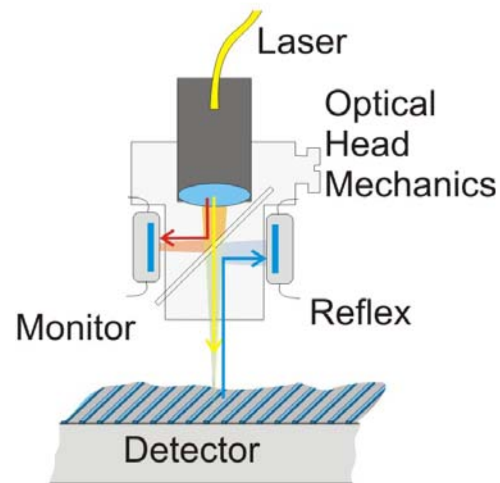


In particular:

1. The semiconductor laser beam has nonzero rise edge (nanoseconds), a finite size beam profile (sigma more 1 μm) and a minimum pulse duration of 3ns
2. the light is reflected by metal layers and at the various interfaces (Si, SiO_2, poly etc.).

3. Interference effects can be originated by reflections
The results are very sensitive to the optimal focus distance; therefore a sophisticated focusing procedure was developed. The system can be cooled down to –20°C in dry atmosphere in order to study the property of irradiated devices. The time resolution and the spatial resolution of the system are 1ns and 3μm, respectively. The example of a fine scan over a strip edge is displayed at Fig:
The amplitude measurements are subject to more difficulties. In principle, the narrow laser amplitude spread results in an output signal very sensitive to sensor and electronics operating parameters (in contrast to the broad Landau spectrum). However the amount of light penetrating to the silicon bulk and converting into e-h pairs is strongly dependent on the optical properties of top and bottom surfaces, on the angle, etc.
Measured data of reflectivity and refractivity at the infrared range are very scarce, so a direct reflection monitoring was developed (see Fig.).
Further details are available at [Z. Dolezal et al., Laser tests of silicon detectors, Nucl. Inst.Meth A, doi:10.1016/j.nima.2006.10.].





- Lab test bench for detector characterization includes both characterizations with laser diode as here above and with a radioactive source. This is the last step before the full realistic test in a test beam. Many Institutes in the SiLC collaboration are equipped with such facilities and examples and results of the ongoing work on Lab test bench in SiLC are given in III-2-4.

III-2-2: Electronics Lab test benches

1. Electronics functionality and parametric tests

Chips are characterized after measuring the following parameters, on as many samples as possible, after wiring straight on PCBs and insertion in a Faraday cage:

- DC Power vs biasing
- Gain (preamp, shaper)
- Noise (without and with input load between 1 and 100 pF)
- Linearity, dynamic range (preamp, shaper)

These measurements provide an electronics signal to noise floor, and dynamic range for a given accuracy, then other parameters such as:

- Pulse shapes and peaking times (shaper mainly)

- Power supplies rejection
- Process spreads
- Temperature dependence

are measured.

For the next chips to come, the Analogue pipe-lines and Analogue to Digital converters part are going to be evaluated in order to determine mainly the ENOBs and maximum speed performance, as well as the full chain behaviour with respect to noise, power and accuracy. This quite a new field for us and a fair amount of test tools both hardware and software are needed in order to be able to achieve this work. It is just starting now with the first 130nm UMC prototype.

2. Next comes the prototyped chips are fully characterized first at the Lab test bench, with the chip linked to a real detector that it read out when the detector is excited with both a laser diode and a radioactive source.
3. Then the chip is tested in even more realistic conditions i.e. in a test beam.

The SiLC collaboration is following this sequence of tests with the 180nm chip. And preliminary results are reported here below in subsection III-2-4.

III-2-3: Mechanical Lab test benches

There are in the collaboration several types of dedicated test benches already installed ot that are under development on the Mechanics R&D side, such as:

- For developing the alignment system (ex: IFCA)
- For developing the cooling system (ex: LPNHE)
- For developing the tools for various mechanical purposes & studies (several Institutes)

More will have to be developed as SiLC is starting the construction of prototypes for the forthcoming test beams.

III-2-4: Lab test benches for complete characterization of the detectors and associated electronics: Present results.

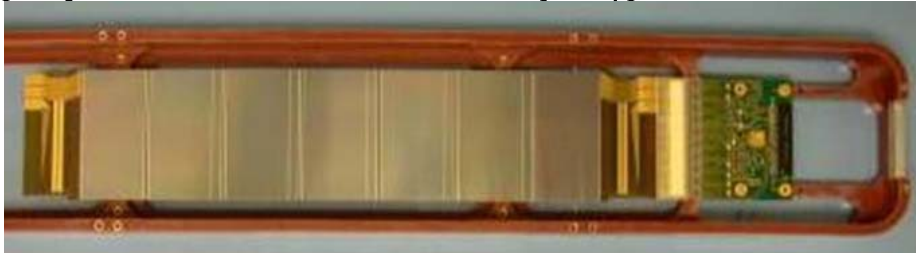
- ***Characterization of strips of various lengths and of the new FE chips: SiTR-180.***

An automated test bench is set up at LPNHE; it is LabView based. The detector to be tested is sitting on a 3D motorized table in a Faraday cage. The LabView programme allows to automatically move the table in all 3 dimensions with a 5µ step precision. An FPGA card is programmed in order to pilot the data taking and to set the parameters needed for the functioning of each type of FE chip. The FE chips of the VA series produced by IDEAS are used to read out the detectors and also as “reference” to compare with the obtained results when the detectors are read out by the new FE chips developed at the Lab. Up to now only analogue FE chips, i.e. VA chips and the SiTR_180 chip are used, thus the digitization is performed with a 14 bit, 100 MHz A/D card NI 5122 from National Instrument. For the test with the SiTR_130 the DAQ will be changed as A/D conversion is included in the chip.
Three detector modules have been so far tested in this Lab test bench

- *First prototype tests: S/N as function of strip length*

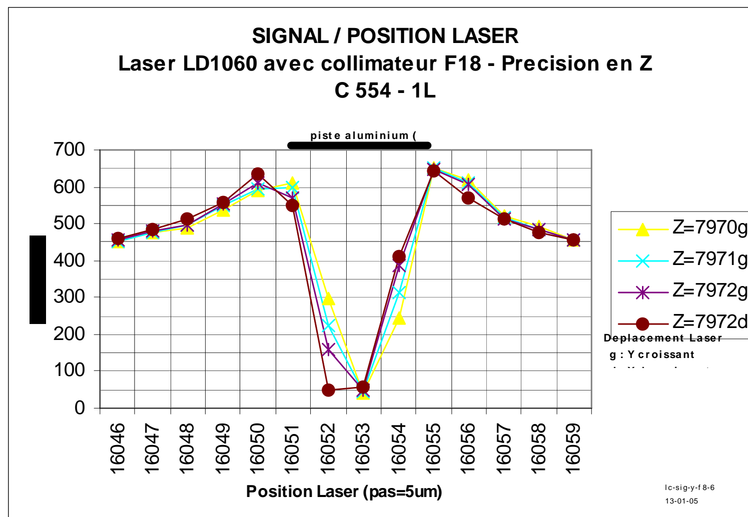
A first detector prototype was built with sensors from AMS experiment and using the AMS technique to bond 7 such sensors to each other such to have a ladder with 28 cm long strips (See figure here below). The prototype was read out with VA-64 hdr FE chip produced by IDEAS for AMS. This is a long shaping device, with a shaping time of 3.7 µs adapted for long strip length. Besides a series of strips in the detector were daisy-chained in a serpentine

way in order to get strips with respectively: 56, 112 and up to 224cm length. Therefore we had 4 strip lengths available for measurements in this prototype.



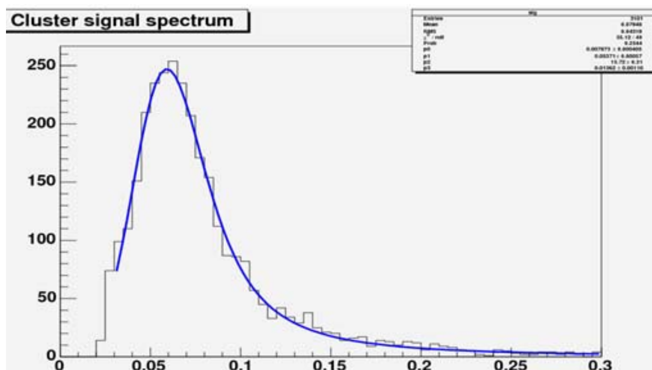
Photograph of the first detector prototype with variable length strips and VA_64hdr readout chips from IDEAS for AMS.

The detector module was excited by a well focused laser diode LD1060nm and submitted to a detailed characterization. As an example the plot here below show the results of a scan with a 5µm step from one strip to another.



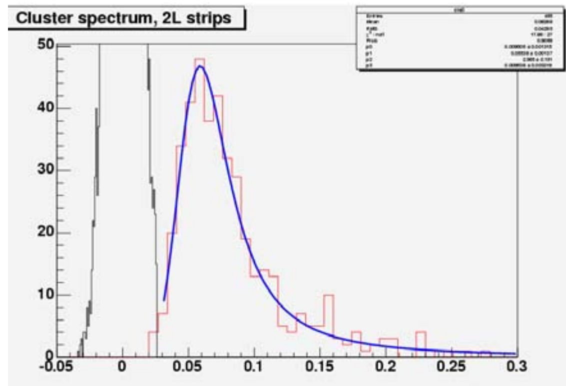
Plot of the scan of the transverse structure of the sensor along the strips by step of 5µm

The detector module was also excited with a radioactive SR90 source and the Signal-to-Noise ratio was measured for different strip lengths after common mode and pedestal subtraction. Both the Maximum Probable Value (MPV) and the Mean value were computed. The results are presented in the plots here below.



S/N for 28cm strip long:

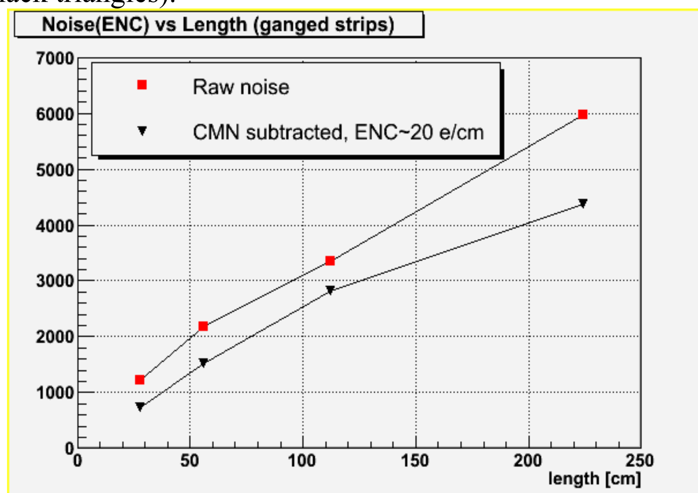
S/N=20 (MPV) or 30 (Mean)



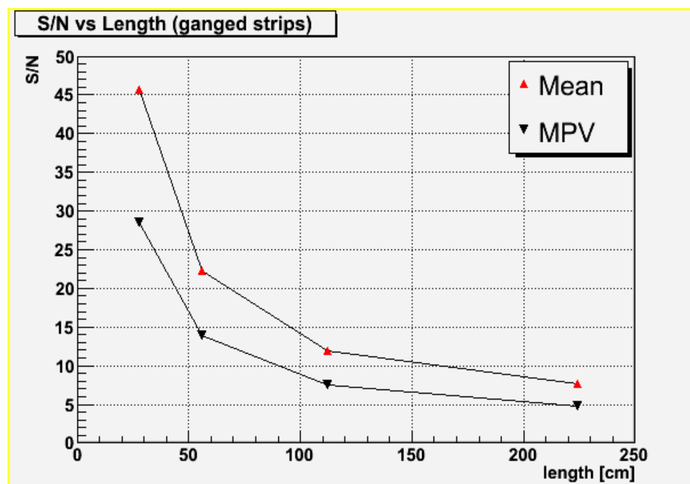
S/N for 56 cm strip long:

MPV:55 mV;Mean:83 mV;Noise:4.6 mV
Thus:
S/N=12(MPV) or 18(Mean)

The plot here below summarizes the obtained results in terms of the Noise in ENC versus the length of the strip both for the raw noise (red squares) and the with the common noise subtracted (black triangles).



The plot here below summarizes the obtained results in terms of the Signal-to-Noise ratio versus the length of the strips: the ratio is computed both with the Mean and the Maximum Probable Value.



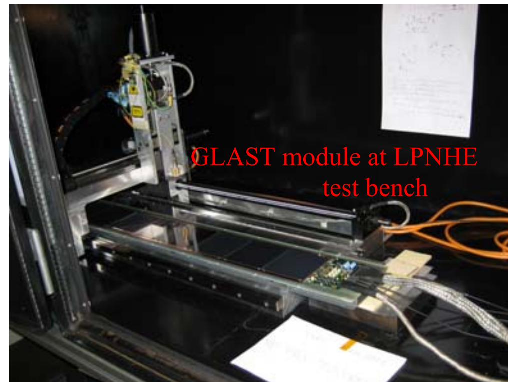
This is quite a unique measurement for strips over such a strip length range.

❖ *Second series of tests in preparation and in complement to the DESY test beam*

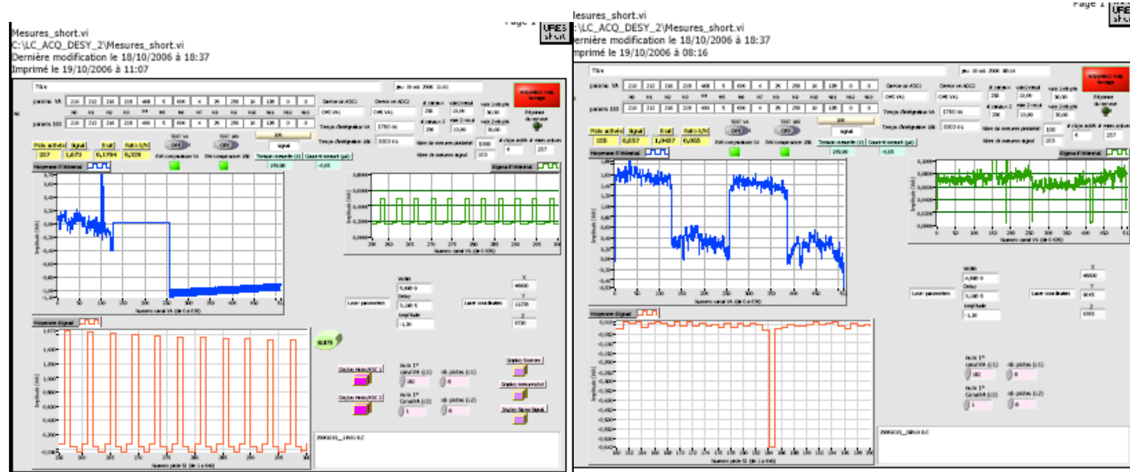
A series of measurements were performed in 2006 in preparation for the test beam in DESY to qualify the new modules and the new readout electronics as well as the associated upgrade of the overall Lab test bench.

Two types of detector modules were built for these tests. One module, made by IEKP Karlsruhe, was a long ladder made of ten 9x9 cm^2 single sided 6” new sensors made by Hamamatsu HKP for GLAST; these sensors were bonded making this way, 90 cm long strips. They are 228 µm readout pitch and 400µm thick. The two other modules made by LPNHE-Paris with collaboration of CERN for the bonding, were made each of 3 sensors of 9.45 x 9.45 cm^2 thus making 28.5 cm long strips. These strips were 183 µm readout pitch and 500 µm thick. The long ladder and one of the other two modules were read out by a VA1 chip on 128 channels and 4 other channels were read out by the new 180nm readout chip prototype. The other short module was read out by 4 VA1 readout chips therefore all the channels of this module were read and this module with its related electronics is used as reference for testing both the modules and the new readout chip. The VA1 and new chips were installed on a Front End board designed by this LPNHE to process the signals from the detector modules (see photograph here below on the right).

Photograph of the 2 modules with CMS sensors and 4VA1 &1VA1+4SiTR_180ch. chips



The Photograph on top right shows the module made of 10 GLAST sensors sitting at the Lab test bench in Paris.



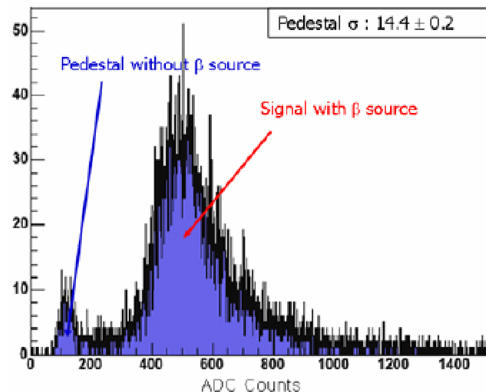
The plots here above shows the online displays indicating that the signal from LD1060 excitation is well read out by the SiTR_180 hit channel in the GLAST module (on the left) And similarly for the CMS module read out with the 4 VA1 chips (on the right).

All the newly developed DAQ hardware and software, the 3 new modules equipped with new FE electronics were the send to DESY for the first test beam session of SiLC (See III-2-3)

The full characterization of the new SiTR-180 chip is being achieved now at the Paris Lab Test bench, after the tests in DESY and to complement them. The tests are underway and we expect to have preliminary results to present at the Beijing Workshop.

- *Characterization of new sensors at the Korean Lab test bench*

This Lab test bench is based on a similar set-up to the one described in the previous case and it allows performing measurements of the Signal/Noise of various new sensor prototypes as developed by ETRI with new single-sided and double-sided sensors. The sensors are read out by VA1 chips from Ideas. As an example the Figure here below shows a nice result: the Signal-to-noise ratio is measured to be 25.0 for this sensor (see Figure on the left).



Started since already a few years in some Labs part of the SiLC collaboration, the Lab test bench activity has increased significantly over this last 18 months. It is expected to increase even still much more now and to still expand in a variety of different domains according to development of the various R&D facets.

As shown here, the Lab test bench for testing detector prototypes (new sensors) and new FE electronics chips is a crucial tool closely related to the test beams.

III-3: Test beams

An active program of test beams was launched at the end of 2006 and took a lot of work during the overall last year. It will proceed on, these next years essentially following the E.U. EUDET framework and programme of work. Despite being a European project, it should be pointed out that the facilities and all the infrastructures are also available for all the SiLC partners included the non European ones.

III-3-1: Motivations

The Lab test benches of different types are a first approach towards experiencing in more realistic ways various real life conditions. The test beams are their indispensable continuation and extension to ensure that the device will satisfy the requirements and/or verify how much it satisfies them.

The test beams allow identifying new problems, not yet anticipated even at Lab test bench.

The test beams allow combining several sub detectors.

Apart from the preliminary characterization tests that we started in 2006 on sensor and on chip Signal-to-Noise ratio evaluation, the test beams give a huge potential for developing the R&D on detectors. The beam allows to study in real conditions the full performances of a tracking device including the track reconstruction and combination with other tracking devices (especially the vertex detector prototypes and also the combination with a TPC and all the related issues).

Besides the combined beam with the calorimeter prototype will be a first complete test of the particle flow. Furthermore the test beams allow experiencing the cooling and alignment issues.

III-3-2: DESY test beam

During October and November 2006, the first SiLC test beam took place at DESY. Here 3 prototype modules were tested in a beam of 1-6 GeV electrons.
In the following text beam test setup will be described as well as basic results.

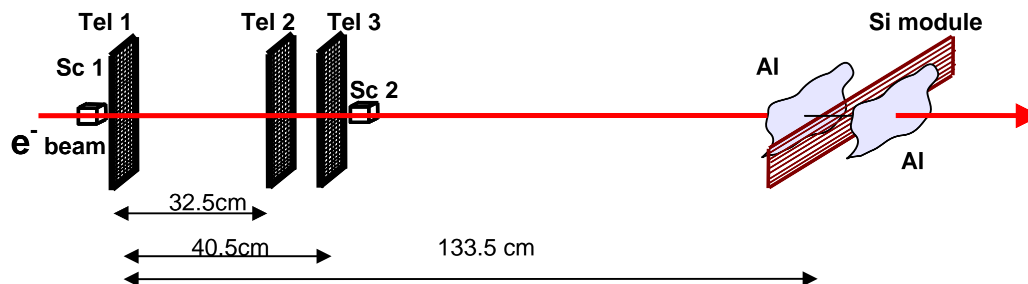
Module prototypes

Notation	sensor	pitch [μm]	total length [mm]	FE electronics
A	GLAST	228	900	228 nm + VA1
B	CMS	183	283.5	180 nm + VA1
C	CMS	183	283.5	VA1 (reference)

Table 1 Characteristics of the module prototypes and their associated F.E. electronics}

- *Mechanical arrangement*

Sketch of the mechanical arrangement is displayed at Fig[mechanicsTB]. The incoming beam was detected by 3 trigger scintillators and its position measured by 3 telescopes. Then a Faraday cage with the measured prototypes was placed. It was fixed to a motion stage so various positions on sensors could be tested.



- *Telescopes*

In order to define the beam position 3 beam telescopes were used. These were kindly made available to us by DESY ZEUS group[7]. The set consisted of three trigger scintillators and photomultipliers defining an area of 9x9 mm^2 triggering the readout of the three telescope units and of the Silicon module prototypes.
The telescopes consisted of three modules with crossed sensors of about 3x3 cm^2; diode pitch 25 micron, readout pitch 50 micron. They were read out using set of VME modules (CAEN module V550 and V551). The final precision obtained is below 10 microns. The set of telescopes and scintillators is displayed at Figure here above

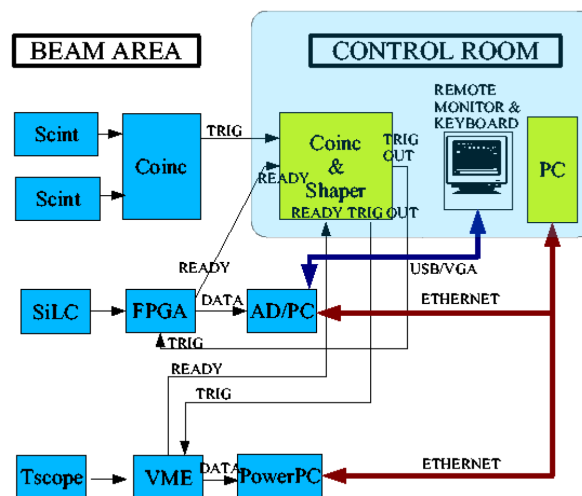
[7] We are grateful to T. Haas, N. Meyners, J. Sztuk and U. Koetz, as well as to DESY and EUDET for the financial support of 3600 Eur (travel expenses of 6 participants) and 2 weeks of beam time.

Photograph showing the telescope arrangement at the DESY test beam

Photographs showing the test beam in DESY: on the left the 2 CMS modules installed in their Faraday box and similarly on the right the long ladder installed in its insulating box.

- *Data acquisition*

The data taken from the telescopes were acquired by DESY software. Here program running on VME Power PC under Lynx OS communicated with the two CAEN modules and stored data at the linked hard disc at the Linux machine in the control room.
The Silicon module prototypes used software written in Paris for lab bench tests.
Hence a synchronisation of the two systems was necessary to obtain correlated events taken by both systems.
The logic from trigger signals and BUSY flags from both system was built (see schematics in Figure here below).
The problem was further complicated by the different dead time of both systems: while DESY VME software was able to take data virtually on all triggers (tested to the maximal rate of 300 Hz), the LabView based system of SiLC had lower throughput (max 50 Hz). This led to 0.1% discrepancy in number of taken events. To facilitate off-line matching of the two files, dual scaler Canberra was implemented to the system and read out via serial interface. Here events (BUSY signals) from both systems were counted.



Schema of the Trigger, Telescopes and detector prototype DAQ logics

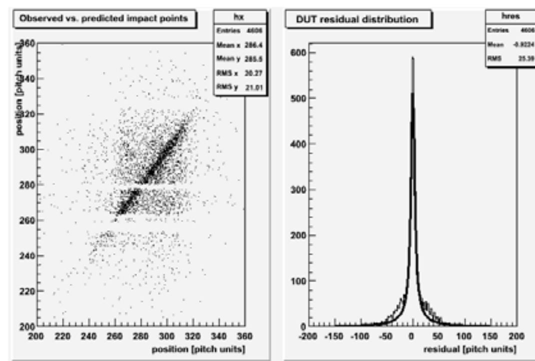
➢ *Analysis*

The data taken were analysed using standard beam test analysis chain.

1. The telescope alignment
   The alignment constants were found and tracks parameters for each event were determined
2. Track projection onto the prototype plane
3. Pedestal and common mode subtraction of the prototype data
4. Noise determination
5. Cluster finding
6. Signal amplitude spectrum, S/N
7. Alignment with the track parameters
8. Residuals, position precision

➢ *Data taken*

Due to the technical problems with modules and necessary time needed to built and debug the whole data taking system reasonable data from one module only have been taken.
These data however served as a perfect test bed for whole data analysis chain. The resulting plots show correlation between predicted track position versus detected position by the Silicon module C, a clear signal that the events taken were well synchronised.

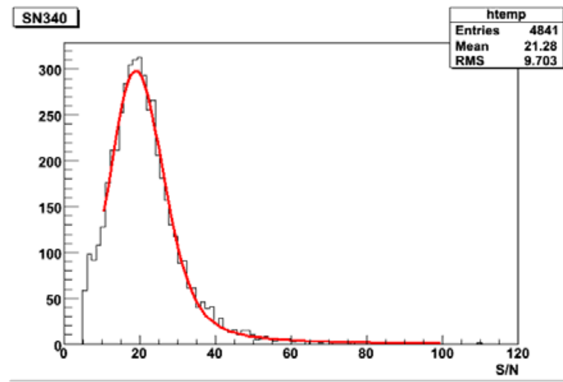


Correlation between the predicted track position versus detected position by the detector prototype

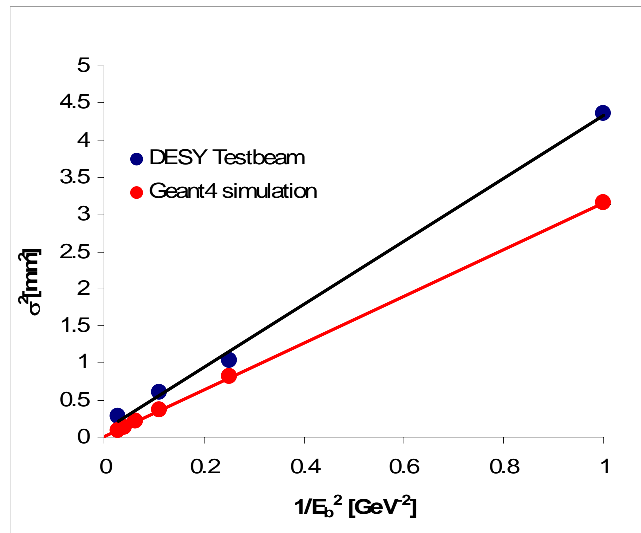
Bias voltage	S/N (MPV)
200	13.62 +/- 0.33
260	15.79 +/- 0.29
299	15.70 +/- 0.25
350	16.52 +/- 0.73

Table showing the Signal/Noise ratio as a function of the applied bias voltage

The maximum was 16.5 for 28.5 cm strip long read out by the VA1 chip.



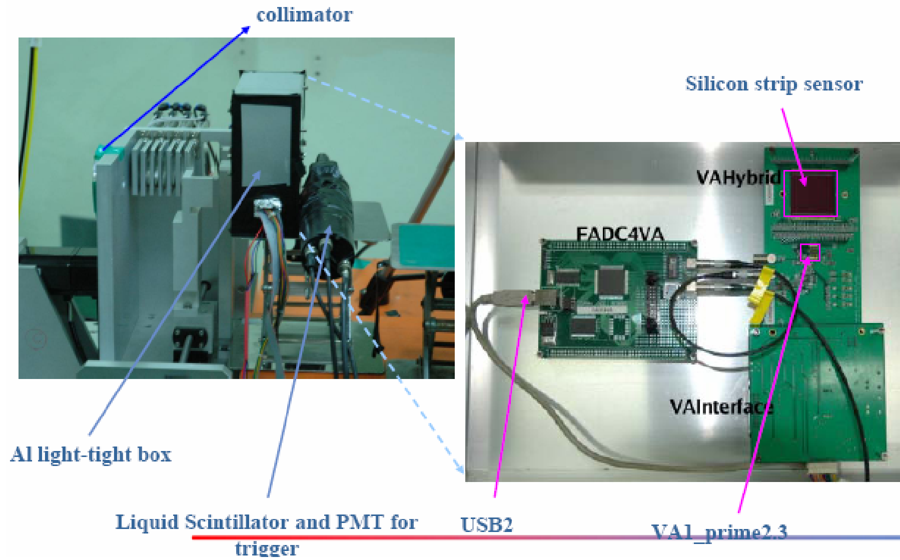
The spatial resolution achieved at the DESY beam test as a function of beam energy is shown in the usual plot of σ^2 versus $1/E_b^2$ in Figure here below. In this plot, results from the GEANT4 simulations are shown as well. The resolution is clearly driven by multiple scattering, particularly severe at the arrangement of the measurement (the detector prototype was positioned at about 1 m after the telescope set). The linearity of the plot allows predicting extrapolated resolution at the infinite energy (resulting in 300 microns)



Plot giving the spatial resolution achieved at the DESY test beam as a function of the beam energy, E_b

For the next test beam we try to work in a more suitable arrangement with the detector prototype installed in between the telescopes. For this geometry simulated precision is around 15 microns.

The Korean team is also involved in test beam using the facility at the Korea Institute of Radiological and Medical Science, providing a proton beam of energy between 35 and 45 MeV. The photograph here below shows part of the experiment test beam set-up. A smaller module being tested it allows to put it very close to the beam telescope as shown in the photograph here below on the left.

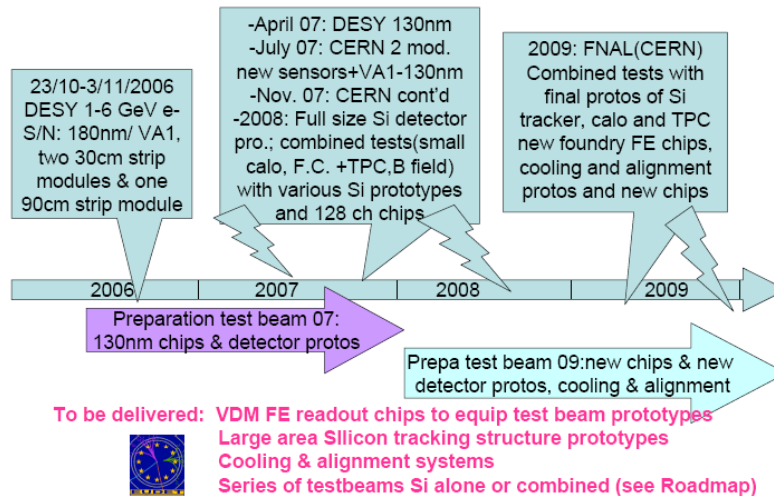


This test beam activity is in order to fully characterize, under realistic conditions, the new sensors developed by ETRI. It is foreseen to have the Korean team joining the test beam at CERN in 2007.

III-3-3: Test beams at CERN and FNAL

The next steps in test beam program addresses test beams at higher intensities and higher energy beams as those available at CERN (SPS) or FNAL Laboratories.

The roadmap of the foreseen program of tests also part of the EUDET EU overall project has been presented at the ILC Test Beam Workshop at FNAL 17-19 January [1] and it is reminded here below with a sketch of the main foreseen steps. This roadmap will be of course also very much dependent of the success and advances of the various R&D activities to which it is closely related (see tentative milestones and schedule table in IV-3).



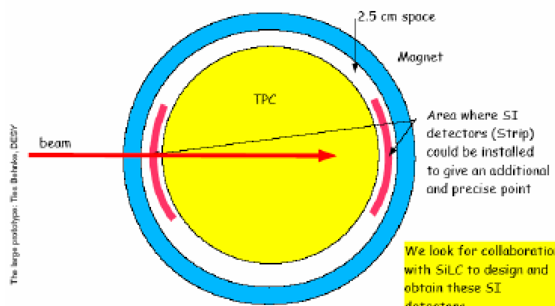
In 2007, the main steps are a test beam around April-May to fully characterize the SiTR-130_1 chip prototype, which is currently under functionality tests. This will be achieved with the modules that were already used for the test beam in 2006, changing the readout board.

Besides a beam request was sent at the end of 2006 to the SPS coordinator and as SiLC is requesting more than one week of beam in 2007, we were asked to present a written full proposal to the SPSC Committee at CERN. This proposal is being sent. These test aims to test new sensors and to start with a larger prototype that will only be partially equip with sensors and electronics (both standard and the SiTR-130_1 prototypes). Besides the first alignment system based on the "hybrid" solution should also be available for these tests.

SiLC also intends to send a proposal for test beam in 2008, to FNAL. It is quite clear from the workshop at FNAL few days ago, that CERN will not be available for test beams starting November 12, 2007 and for a large fraction if not all the year 2008. This makes even more obvious the choice of FNAL as the only available place for high energy and high intensity tests.
It should be noted that it may appear interesting for some dedicated tests to apply for a test beam at SLAC in 2008, on a small prototype, in order to test in real beam conditions the power cycling scheme.

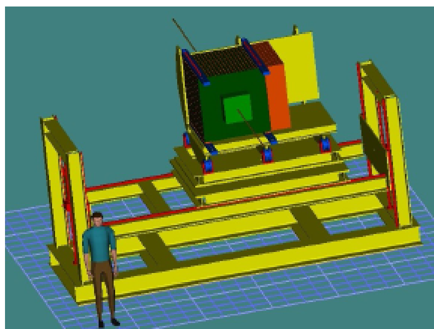
Another important issue are the combined test beam. Following the proposition of the LCTPC collaboration to join them for a combined test beam in 2008, with the prototype of the field cage, we are starting the discussion to develop a cylindrical layer prototype that will surround the field cage as schematized in the Figure here below (top left). In addition the different series of test beams that will proceed starting 2008 and extending beyond 2009, are summarized in the picture here below.

2008 & beyond: combined test beams

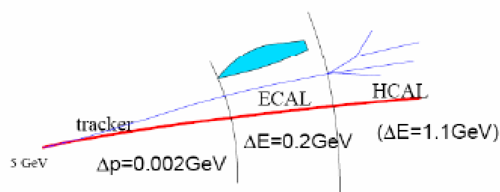


Testbeam with TPC Field Cage & strip layer surrounding it: SET(LDC)

Test beam with pixel detectors: tests on internal tracking region & Vertex + Silicon tracker



Testbeam with Si-W calorimeter & few Silicon strip layers in front: experience particle flow



A. Savoy-Navarro, TBILCW'hp, FNAL, 011807

Reference:
[1] See htpp:// https://conferences.fnal.gov/idtb07/ and look in the "Scientific Program", talk on: ***Silicon Main Tracker R&D: Test beam present status and perspectives***, by A. Savoy-Navarro on behalf of the SiLC Collaboration and of the SiD detector Concept.

PART IV: R&D Organization, Milestones and Resources

The organization of the overall R&D collaboration in terms of definition of tasks, of responsibility or sharing of resources and of defining milestones has made major progress these last two years. This was driven by the increase in interests of new teams to join the effort and by the increase in amplitude and challenges of our R&D activities.
Despite the lack of means, the Collaboration has set up starting at the ECFA Vienna meeting in November 2005, a series of Collaboration meetings that occurred about each 4 months in different Labs part of SiLC. There were up to now 4 Collaboration meetings at: Vienna (Austria) in November 18 2005 organized by HEPHY-Vienna, Paris in the Campus of the University Pierre et Marie Curie where is located the LPNHE, February 2-3 2006, Liverpool in the Campus of the University, organized June 13-14 2006 and in Barcelona, December 18-21 2006, organized by the team from IBM-CNM/CSIC at their place in the Campus of the IFAE-Bellaterra.

The attendance was between 30 and 40 people at each event and the programs are accessible in:

http://www.cnm.es/projectes/SILC_meeting

This site has a link to the Websites and agendas of each of these meetings.
Our collaboration meetings are also an occasion to review what other experiments are doing in the field (especially the LHC experiments: ATLAS, CMS, LHCb and ALICE). People from other sub detectors are also invited to attend and we started with the TPC group in Barcelona. These exchanges are going to be pursued and extended to other sub detectors especially the Vertex and the calorimeter.

IV-1: The sharing of tasks

ITEMS	Involved Institutions
Sensor R&D	
Overall QTC	IEKP, HEPHY-Vienna
Strips (new sensors, thinning)	Korean Group, MSU & SiLAB, OSU, Liverpool, LPNHE, HEPHY-Vienna, IMB-CNM/CSIC
Pixels (different technologies)	IFIC, UB, Liverpool, IMB-CNM/CSIC
3D technology	IMB-CNM/CSIC, HIP & VTT
Test bench characterization	IFIC, Korean Group, HEPHY-Vienna, LPNHE, UCSC, IMB-CNM/CSIC

Electronics R&D

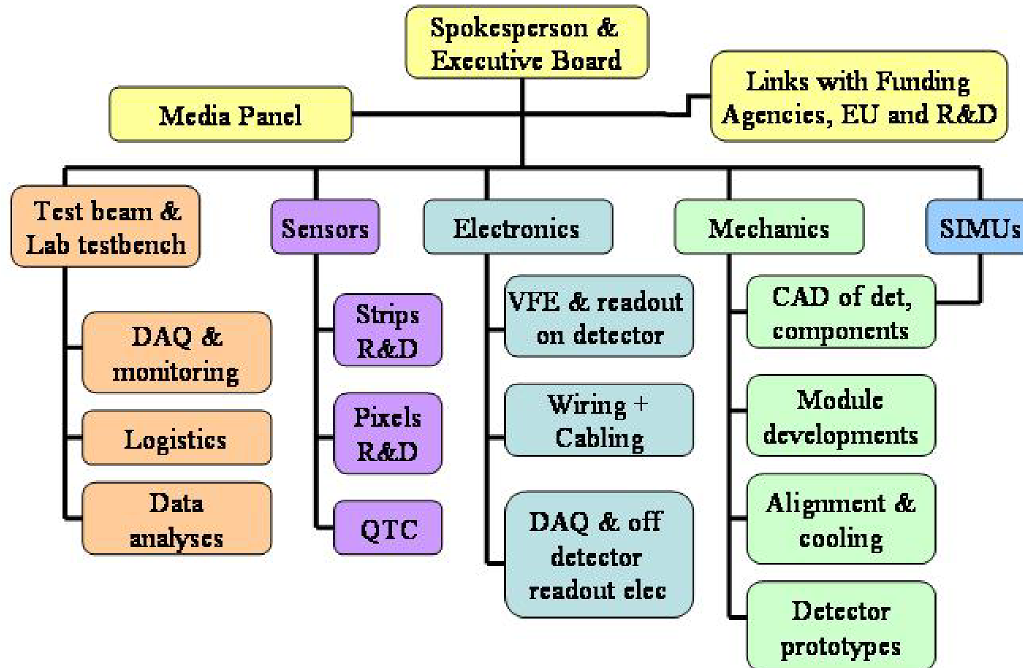
VFE & readout on detector: chip design & development	LAPP, LPNHE, SCIPP&UCSC, UB, IFCA
Characterization with detector on Lab test bench	LPNHE, SCIPP&UCSC
F.E board developments for test	Korean Group, LPNHE, UCSC

beam & lab test bench	
Wiring on detector (novel technologies)	IMB-CNM, LPNHE + industrial firms
Cabling and services	CU Prague
DAQ electronics	Korean Group, LPNHE, UCSC
Mechanics R&D and related issues	
CAD for various components	IFIC, Liverpool, LPNHE, Torino
Modules developments	IFIC, IEKP, UCSC, LPNHE, Liverpool,
Detector prototypes design and construction for test beam	IFIC, Liverpool, Torino, IEKP, HIP, LPNHE, MSU and OSU, UCSC-SCIPP
Cooling system	IFIC, Liverpool, Torino, IEKP, HIP, LPNHE
Positioning, alignment system	IFCA, University of Michigan
Software tools	
DAQ software for test beam	IFCA, HIP, LPNHE, Korean Group, UCSC, CU Prague
Simulation	IFIC, HEPHY-Vienna, OSU, CU-Prague, Korean Group, LPNHE, U. of Michigan, UCSC
Analyses packages	CU Prague, IFCA, LPNHE and all…
Website dev. & maintenance	
Test beam running (DESY, CERN, FNAL)	
Logistics	Contacts = Lab based people
Installation & running	All

Table 1: Group involvement in the prototype and R&D work

IV-2: MOU under elaboration

A Memorandum of Understanding is under preparation within the SiLC collaboration. It was first discussed during the last collaboration meeting in Barcelona at the end of December. A preliminary draft was circulated among the collaboration mid January and should be submitted to the signatures of the authorized persons in each Institutes by mid/end February.
It defines the organizational aspects of the collaboration as roughly and very preliminary described in the schema here below. The distribution of tasks and of responsibility is underway. The tasks distribution as of today is given in Table 1 (see previous subsection).
A policy for publications, talks given at workshops and conferences, proceedings, authors list is also defined in this document. An Annex on resources in FTE and funds is also included and the Tables 2 and 3 are parts of this Annex. Last but not least the document also tackles the aspects in terms of *Intellectual Property* and on *Non Disclosure Agreements* that may be objects of contracts between two or more partners in the Collaboration or with Industrial Firms with whom SiLC partners are collaborating on R&D issues.



IV-3: Milestones and schedules

The milestones and schedules that are presented in the Table here below are very tentative and should be taken with great caution. They are strongly dependent on the development of novel technologies, on our ability to best use them, without speaking of the need for means. This makes that the proposed schedule may easily shift by 6 to even 12 months. There is also the need to keep less risky and/or conservative solution as back-up.

items	2007	2008	2009
Electronics (FEE)	130 Full characterization (*including test beam*) Des.128ch+pw-cy Si Ge design Exploring	Tests & prod for eq. Proto MergeSiGe+cmos ≤90nm *design 512 best dsm*	Equip. protos *characterization* *tests and launch production*
Sensors µstrips + thining 3D-planar Pixels Wiring-on-detector	*initiate 8" ssd* *Exploring* *µseries/ test* *1st protos* *tests* *Studies* *define specs* *Bump bonding explor* *3D wiring exploration*	*Mini series equip proto* *first protos & tests* *1st proto* *prod. µserie*	
Mechanics Elementary module Prototype construction Alignment Cooling	*Construction follows* *1st proto* *1st proto*	*evolution and success in ap* *test beam proto & keep* *test beam proto & keep*	*plying related technologies* *evolving the techno* *evolving the techno*
Test beams **Simus**	*Modules + 1st larger proto* *Pattern recognition &full Reconstruction by end 07*	*Large proto & combined t.b.* *Continue developing simus*	*Combined t.b, cont'd* *& performance studies*

The milestones of the SiLC R&D are following the current ILC schedule and milestones and also the milestones of the EUDET E.U. project that in many ways closely follows the overall ILC program.
We are defining a roadmap for the period of time that goes from 2006 to 2010 and that is schematized here below. It gives the main milestones in order to achieve the main goals of this R&D, but this will be carefully readjusted year to year and even 6 months per 6 months in order to cope with various important issues still unknown. This flexibility is mandatory because the R&D tackles high tech issues and because of the possible changes in the ILC overall schedule in these next years and up to 2010.

IV-4: Resources

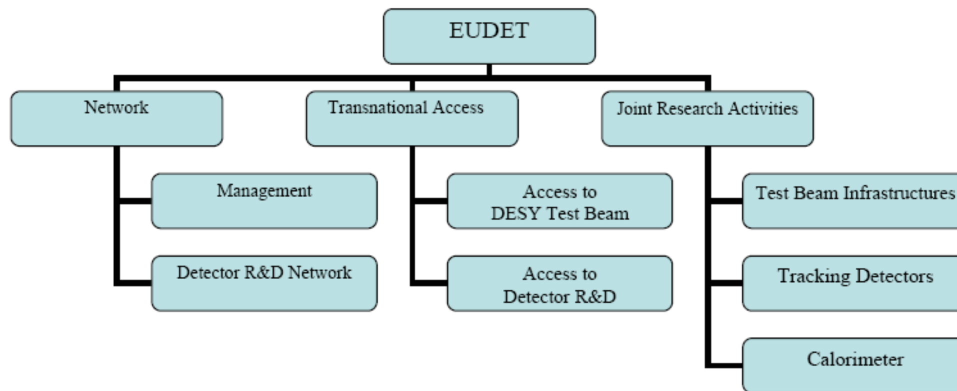
Resources are the "*nerfs de la guerre*" and therefore SiLC is paying a great deal of attention to this fundamental aspect, by evaluating carefully the needed means in persons, in funds and also in avoiding duplication of efforts, but letting at the same time enough flexibility in the developments of various solutions to be developed in parallel. We are still at the detector concept level and not yet building a definite experiment. Besides technologies will evolve very rapidly in many aspects of this R&D and thus we have to keep an eye opened and not to freeze too quickly solutions that will be obsolete already at the start of the detector construction.

IV-4-1: EUDET

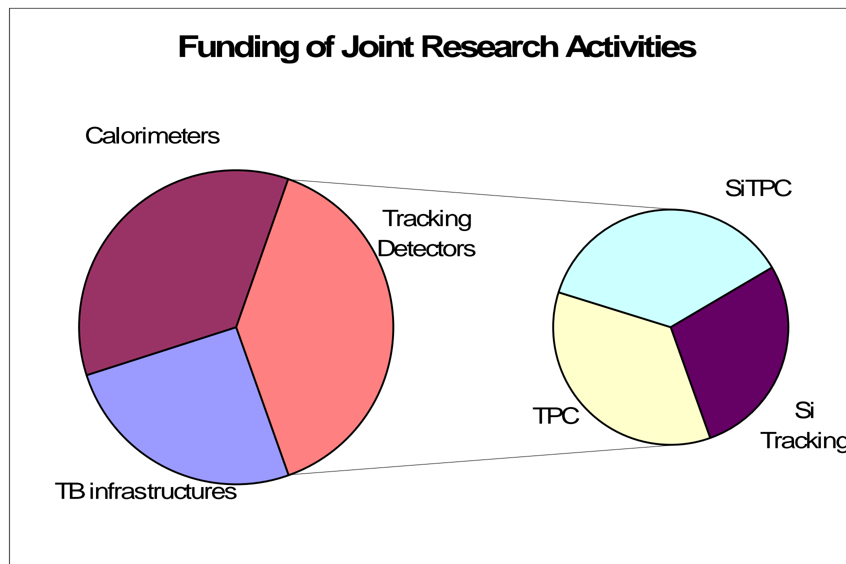
Besides resources obtained from national funding agencies and institutes SiLC can benefit from a support of the Commission of the European Communities under the 6th Framework Programme "Structuring the European Research Area", contract number RII3-026126 (EUDET – www.eudet.org) from 2006 to 2009.
This project aims at creating a coordinated European effort towards research and development for the next generation of large-scale particle detectors. Thus the goal is to establish a common European infrastructure for the research on advanced detector concepts for the ILC and to foster collaboration between European partners and associated institutes.
The project is structured into three types of actions:
Four SiLC institutes

> The establishment of a **European detector development network** will improve communication and interaction between groups involved in detector R&D.
> The establishment of three dedicated **Joint Research Activities (JRA)**with specific actions will coordinate and improve existing infrastructures.
> The instrument of **Transnational Access** is used to grant interested groups access to the different infrastructures provided through this initiative.

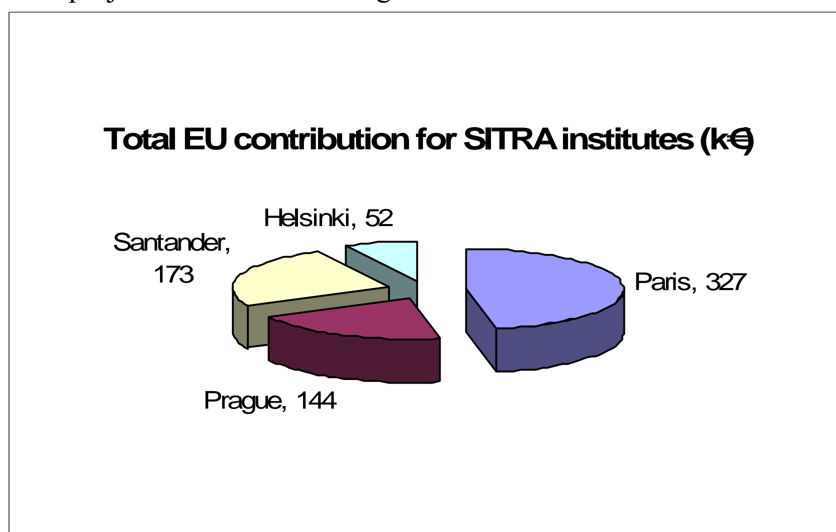
The organisation of the project is displayed at the figure. Each of the JRA's are further subdivided into individual tasks. In the case of tracking detectors (JRA2) these are TPC, Silicon readout TPC and Silicon Tracking.



Four SiLC institutes are members of EUDET: HIP, University of Helsinki (Finland), LPNHE, UPMC and IN2P3/CNRS (France), Charles University in Prague (Czech Republic), IFCA-CSIC and University of Cantabria (Spain). Moreover there are six associated institutions: IMB-CNM/CSIC in Barcelona (Spain), IEKP-University of Karslruhe (Germany), Liverpool University (United Kingdom), Moscow State University and Obninsk State University (Russia) and IFIC/CSIC and University of Valencia (Spain).There are several modes of support from EUDET. The members as well as the associated institutions receive money for the networking (travel costs for meetings). The significant fraction of the support is in the form of direct funding of hired postdocs (3 persons), and consumables (contribution to the purchase of the readout electronics, alignment system).
Another important way of support is enabled access to the infrastructure of EUDET members. Here mainly access to the test beam of DESY and CERN is of great importance for SiLC. During first beam test in 2006 SiLC obtained beam time, telescopes, computing facilities and local support form mechanics and other issues from DESY within the Transnational access task of EUDET. In addition, travel costs of 6 persons were also reimbursed by DESY from this project.
The total EU contribution for this project is 7 M€. The sharing of funds between individual activities is displayed at Fig.



The silicon tracking (SITRA) task of JRA2 was allocated with almost 700 k€ during 4 years of the project. Its division among 4 SITRA institute can be seen at the Figure.



After one year of EUDET one can already see the positive impact on the infrastructure for the ILC detector development and on the collaborative efforts of both member and associated institutions.

IV-4-2: Table of resources in financial means and FTE from funding agencies

It should be noted that all the numbers quoted here in funds and in FTE, starting this year 2007, are subject to approval from the funding agencies and therefore should not be taken as granted.

Institutions	Equipment funds (KEuros)	Travel funds (KEuros)	Effort (FTE)
HEPHY-Vienna	8	7	1
CU Prague	10	8	3
HIP-Helsinki	*Not given yet*	*Not given yet*	*Not given yet*
LAPP-Annecy	6	1	1
LPNHE-France	80	35	9
IEKP-Karlsruhe	10	3	3
Torino U.	5	2	1
Korea Group	205	34	6.2
OSU & MSU	*Not given yet*	*Not given yet*	*Not given yet*
IMB-CNM/CSIC	1	3	0.5
IFCA/CSIC-Unican		10	2
IFIC/CSIC-Valencia	30	14	4
Liverpool U.			0.1
U. of Michigan	*Not given yet*	*Not given yet*	*Not given yet*
UCSC-SCIPP	52(32+17[P])		2

Hamamatsu	15		
EUDET	144[P]		2(CU & IFCA)

Table 1: <u>Funding and effort investment in 2006</u>

Institutions	Equipment funds (KEuros)	Travel funds (KEuros)	Effort (FTE)
HEPHY-Vienna	21	7	1.3
CU Prague	10	10	3
HIP-Helsinki			
LAPP-Annecy	8	2	1,5
LPNHE-France	92	45	10
IEKP-Karlsruhe	10	3	3
Torino U.	6	2	1.2
Korean Group *=confirmed (): will be requested and start on April if approved	55* (+130)	34* (+15)	
OSU & MSU	Not yet		
IMB-CNM/CSIC	10	5	1.5
IFCA/CSIC-Unican	136(64+72[P])	34	≥3
IFIC/CSIC-Valencia	30	14	4
UB/URL	5	5	1[1]
Liverpool Univ.		5	0.5
UCSC-SCIPP	45(35+10[P])	7	2.5
Hamamatsu			
EUDET	213[P]		3(CU & IFCA & LPNHE)

Table 2: <u>Provisional funding and effort investment in 2007</u>

Note [1]: The FTE effort will vary and increase significantly during the year dur to effect of the LHCb commissioning, it will start with 0.5 FTE but after the summer it will increase, reaching probably 4 FTE at the end of the year. Funding will increase (especially in equipment in 2008)
Note [P]: Indicated with an exponent P is the amount of funds that will be devoted to salaries (whenever known). Otherwise the numbers on the first column do not include salaries, these are only funds dedicated to equipment.

IV-4-3: Other contracts or resources

Many of the R&D activities that are needed for developing the Silicon tracking system for the ILC are demanding high technologies in fields that require relatively large amount of funding

- for the equipment of the Laboratories (new laboratories or upgrade of the existing ones in order to maintain them at the needed level)
- for triggering the collaborative efforts with industrial partners
- for buying material (mechanics, microelectronics, boards fabrication etc…) corresponding to relatively small orders and therefore relatively high cost per unit. This is needed in particular for the construction of prototypes.

It is therefore quite obvious that most (if not all) our funding agencies cannot provide with all the needed money for this R&D.

The SiLC collaboration has thus, since its beginning, been actively looking for other sources of additional funds. Our participation to the EUDET E.U. project is a successful example of it. But besides this, the various partners of this collaboration are exploiting other possible resources, at the national (local) level and also at the international level. Because of its international character, the SiLC partners are applying for collaboration programs that are set up by Ministries of Sciences or of External Matters from different countries in the world. This allows *exchanging* or *longer term visits* which are essential for improving the collaborative efforts between Institutes in many ways. Collaborative contacts are also established between Institutes and Industrial Firms and again are extended to the benefit of all the other members of the collaboration. Many members of the SiLC collaboration have a long history of collaborative efforts with the Laboratories such CERN, DESY, FNAL, KEK and SLAC. It proves to be very useful when installing or running test beams for instance. Again this is benefiting to all the SiLC collaborators.

It is intended to pursue all these ways to get more funds and also to strengthen even more the collaborative spirit already quite good in the SiLC collaboration which is a key of success of this enterprise.

Concluding remarks

Over the last year and a half, the SiLC R&D collaboration has achieved in many ways an impressive step forward. Advances in various fronts such as:

- first detector module prototypes built and tested in Lab test bench and test beam;
- first FE and readout chips in deep sub micron CMOS technology were layout and proven to be successfully functioning already in their first submission;
- launching of a real task force on the simulation front, that is manifesting in gathering forces and expertise from various Labs in a coherent way;
- launching of the test beam activities;
- building up the collaborative framework with regular collaboration meetings in different places that are real forums and at the same time allow to know each other and our different expertise and capabilities; definition of tasks and responsibilities (MoA in progress);
- Enlargement of the collaboration with new groups joining (the spanish teams that are bringing a very valuable expertise), and other collaborators especially from Asia (under discussion)
- The teams still heavily involved in the LHC construction have already started this year to give valuable contributions and it is expected that this is going to grow up by the end of the year. At the same time the synergy between ILC and LHC will also operate to the benefit of LHC upgrades as it is already appearing quite clearly, given us an additional asset.

But in order to allow us pursuing successfully our R&D program it is essential that we get the needed means in terms of funds and persons, in particular physicists (there is (will be) a natural attraction for appealing running experiments especially LHC). The full support of this panel is therefore crucial to allow us going ahead.

ANNEX 1:

The SGV Studies on the Silicon Envelope in the LDC detector concept

Introduction

The performance of the ensemble of tracking detectors has been evaluated analytically, using the SGV code. A large number of configurations - more than 100 - of the silicon envelope of the TPC were studied. This section is an account of the conclusions.

Basic Formulae

The tracking system directly measures is curvature(ρ = 1/R), or more precisely the sagita (S) over the length of the coda (L). If multiple scattering is neglected, the error can be calculated analytically:

$$S = L/2\rho = 2S/\left[(L/2)^2 + S^2\right] \Rightarrow \sigma(\rho) = \sigma(S)/L^2 * 8 \left| \frac{1 - 8(S/L)^2}{[1 + 4(S/L)^2]^2} \right|$$

If S«L, $\sigma(S) \approx 8\,\sigma(S)/L^2$ but if, S=L/2, $\sigma(S) = 2\sigma(S)/L^2$ (ie. if the track turns back). For three evenly spaced points the error on the sagita is:

$$\sigma(S) = \sqrt{(\sigma_{start}/2)^2 + (\sigma_{end}/2)^2 + \sigma_{mid}^2}$$

Since:

$$p\sin\theta = p_{\perp} = 0.003B/\rho$$

i.e. $1/p=330 \sin\theta\rho/B$, it follows that $\sigma(1/p)=(330/B) \sin\theta\sigma(\rho)$, (or $\sigma(p)=(330/B)p^2 \sin\theta\sigma(\rho)$)
Hence, at high momentum, $\sigma(1/p)=(8*330/B) \sin\theta\sigma(S)/L^2$.
The error on the sagita, $\sigma(S)$, can be calculated in several cases, as a function of the point errors, σ_{point}:

- Three points, all with the same error: $\sigma(S)=\sigma_{point}\sqrt{6}/2$
- Three points, first point ``fixed'' (i.e. with a negligible error compared to the other points): $\sigma(S)=\sigma_{point}\sqrt{5}/2$
- Three points, first and last point ``fixed'': $\sigma(S)=\sigma_{point}$

In the case of many points, all with the same error, a simple approximation can be used: Group the points in the first, second and third thirds of the measuring range. Then use the first expression above, to arrive at $\sigma(S) \approx (\sigma_{point}/\sqrt{n/3})\sqrt{6}/2$. In this case, L should be reduced by one third since the first point is in the middle of the first third of the measuring range, the last in the middle of the last third. Comparison with detailed calculations shows that this approximation is good to $\sim$30 %.

Designing the silicon envelope

As a starting-point of our studies, we investigated a tracker made only of a TPC. We used the TESLA TDR TPC as an example: R_{inner} = 36.2 cm, R_{outer} = 168.2cm, (i.e. L=132cm), Z_{max}=250 cm, B=4Teslas, σ_{point} = 180μ, 225 layers. In such a detector, one expects $\sigma(1/P)$ proportional to $\sin\theta/L^2$ in the barrel, and proportional to $\sin\theta/(\tan^{5/2}\theta - (Z_{max}/R_{inner})$ in the forward. The extra $1/\sqrt{\tan\theta}$, because in the forward region, n_{points} is proportional to L. At $90°$, the approximation gives 35 % more than the exact result from SGV. In figure 1 - where the exact calculation from SGV is overlayed by the approximate formula above - one notes that the formula for the resolution perfectly describes the result of the detailed calculation, once

the an over-all factor has been tuned to give agreement at the highest momentum. One also notes that multiple-scattering gives a negligible contribution beyond 10 GeV, that indeed the resolution (multiple scattering neglected) at the point where the track turns back is four times as good as at high momentum, and that below this momentum, the deterioration of the resolution by purely geometric effects is much faster than that due to multiple scattering. The latter has as a consequence that the multiple scattering contribution is quite small also for very low momenta (below 0.5 GeV).

The formula also gives a good description of the detailed result as a function of polar angle (figure 1, right). One notes the disastrously fast deterioration of the resolution as the polar angle diminishes. The reason for this is the triple effect of the larger longitudinal component of the momentum, the shortened lever-arm, and the decreased number of measured points. The last two of these effects can be alleviated by adding discs inside the TPC, and fitting such detector elements indeed has a dramatic effect: with the discs, $\sigma(1/P)$ prop to $\sin\theta/(\tan^2\theta)$, i.e. the term Z_{max}/R_{inner} above vanishes (figure 2). Hence, already at this preliminary stage, the necessity of the FTD is established.

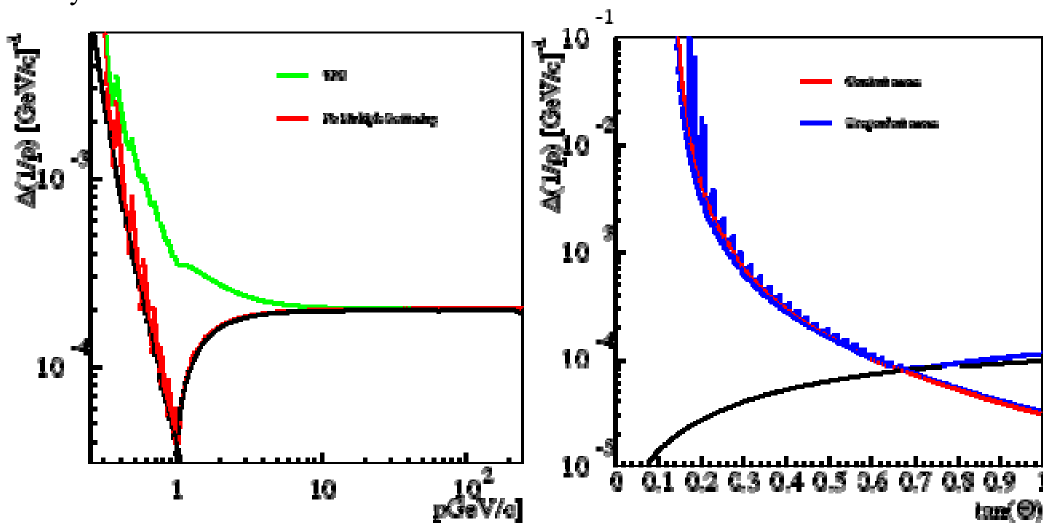


Figure 1: Resolution-curves of the TPC alone

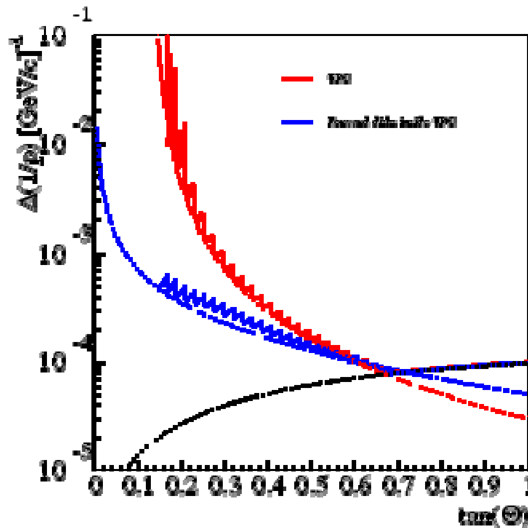


Figure 2: Resolution-curves of the TPC combined with the FTD

We further investigated the amelioration of the system by sequentially adding the other silicon elements of the tracking system. By adding the vertex detector and SIT to the track fit, the effective L increases from 88 cm to 146 cm, ie $1/L^2$ decreases by a factor 2.8. The start-point of the measuring range is ``fixed'', due to the very small point-error of the silicon elements, so σ(S) decreases by 10 %. Hence, an overall amelioration by a factor 3 is observed (figure 3). Adding the SET further increases the effective L from 146 to 170 cm, and σ(S) decreases by 10 %. The expected 35% amelioration is indeed observed. Finally, the addition of the ECT has an effect similar to that of the SET. For reference, the TESLA ``TDR'' augmented by the SET and ECT is also shown in figure 3. It differs by the geometry of the FTD, where the last disk was approximatively at the middle of the TPC.

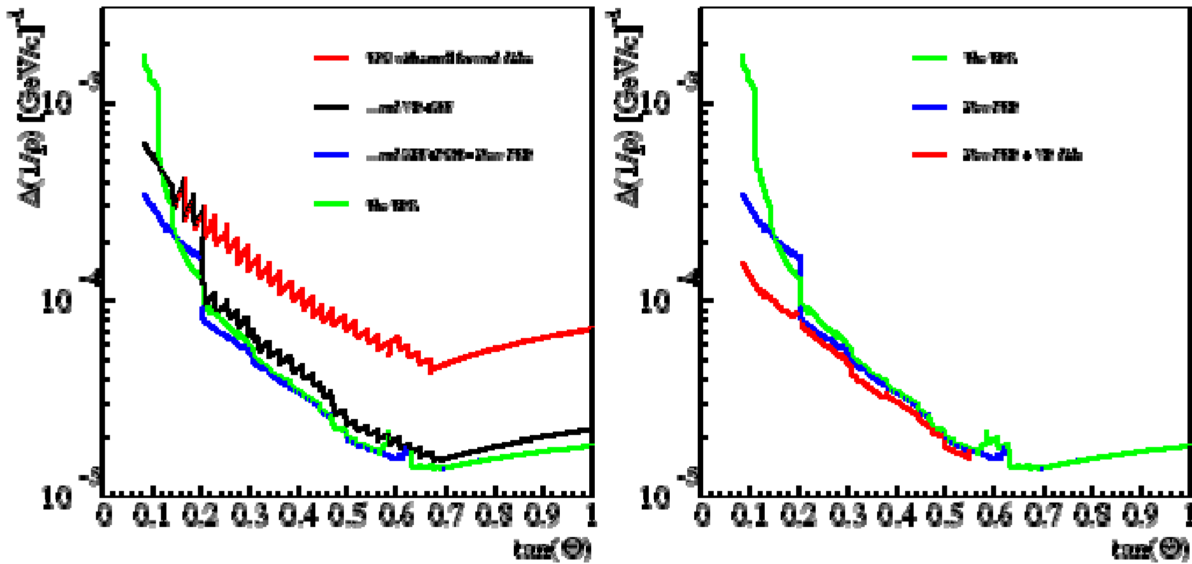


Figure 3: Resolution-curves of the full tracking system

One can note the divergence at low angles in the TDR case, explained by the shorter FTD. One also notes a sharp step at the angle where the tracks no longer pass the vertex detector. This can be remedied by adding a pixel disk with $\sigma_{\mathbf{point}}$ = 4µ just outside the vertex detector, as can be

Detailed study of the silicon sub-detectors

ECT

The optimisation of the ECT was studied by moving it by the 30 cm available between the TPC and the forward calorimeter. It was placed either as close as possible to interaction point, as far as possible, or evenly spaced. Furthermore, the effect of thickness of the TPC end-plate was also studied.

A 30 cm change of the position corresponds to a change of L^2 by 25 %, which is indeed observed for particles with high momentum (figure 4). At such high momenta, the best position is at the maximum distance, but the difference between the different options is quite marginal. Some effect of the scattering in the end-plate is visible even at this momentum. At lower momentum (25 GeV), scattering dominates, and the best position is at minimal distance. The effect of the end-plate is clearly visible. Hence, if the end-plate remains as thick as in the TDR (30 % X^0), it is best to place the ECT as close as possible. However, a definite answer to this issue cannot be given until a final design of the TPC end-plate is at hand.

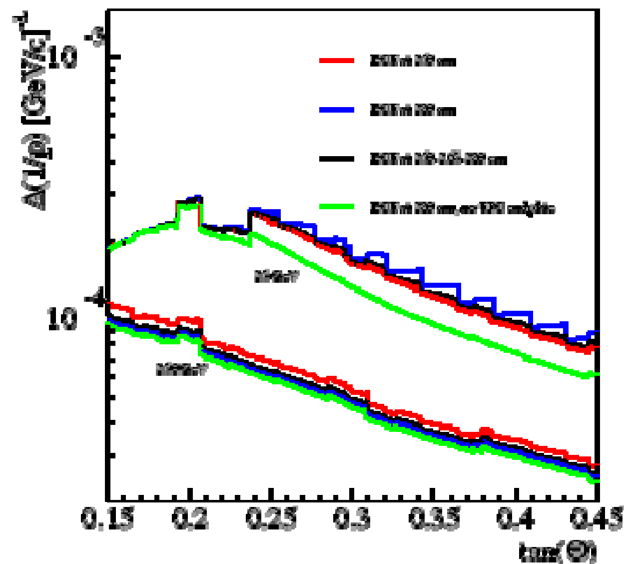


Figure 4: Resolution-curves for different ECT designs

SIT

We studied whether adding a third layer to the SIT and/or if layers with different point-resolution would substantially ameliorate the performance. We found that adding a third, intermediate, layer had a very marginal impact, but that doubling the point resolution, in particular in the outer layer could yield an substantial gain, see figure 5 .

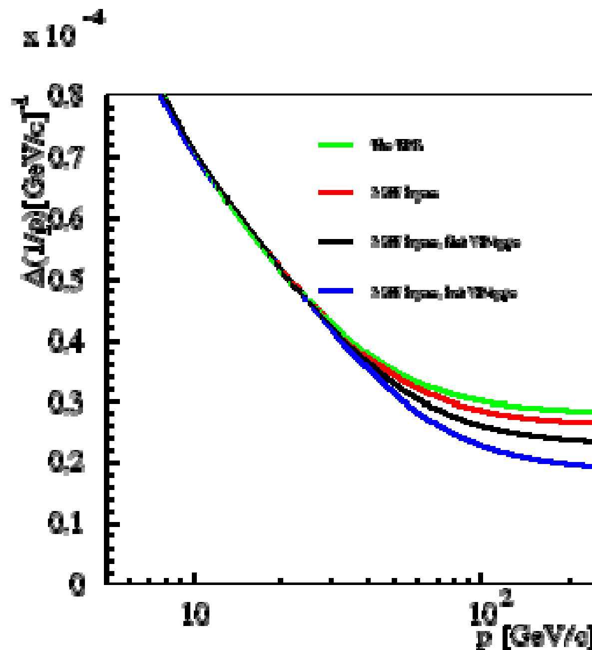


Figure 5: Resolution-curves for different SIT designs

SET

The optimal disposition of the layers of the SET was investigated by varying various aspects of the layout. It was found that the best option was to make the SET as thin as possible, ie. a single layer, and the effort should be focused at attaining the best possible point resolution (figure 6) . This is due to the fact that while the same precision at high momentum could be attained either by one maximally precise layer or a stack of less precise ones, the latter necessarily would take more radial space. This would compromise the resolution at lower momenta by reducing the lever-arm of the TPC. The ``thin SET'' option is also preferable at

high momenta, because the average radial distance of the SET-point - and hence the lever arm - is larger for this layout. On the other hand, the lower material budget of the ``thin SET'' is without importance for the tracking, as the SET is the last point of the measuring range.
The potential advantages of the ``thick SET'' is that it could detect and measure electrons from photons converted in the outer field-cage of the TPC, and could ameliorate the angular precision of the track-extrapolation to the calorimeter. However, it was estimated that neither of these properties were strong enough to endorse such a choice: at most a few percent of the photons convert in the outer field-cage, and only those with energy below 4 GeV would be better measured by a SET with a lever-arm of 10 cm than they would be by the calorimeter. The amelioration of the direction of the extrapolation of charged tracks is important (a factor 2), but the precision is already much better than that of the calorimeter, so a further increase is of little use.

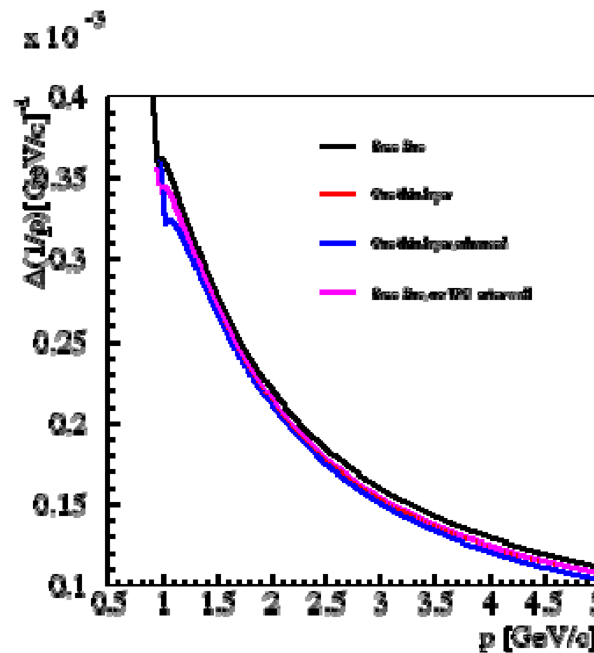


Figure 6: Resolution-curves for different SET designs

<u>The interplay of the tracking detectors in the barrel</u>

Figure 7 shows the momentum resolution for tracks at 90°, with various detector-components active.

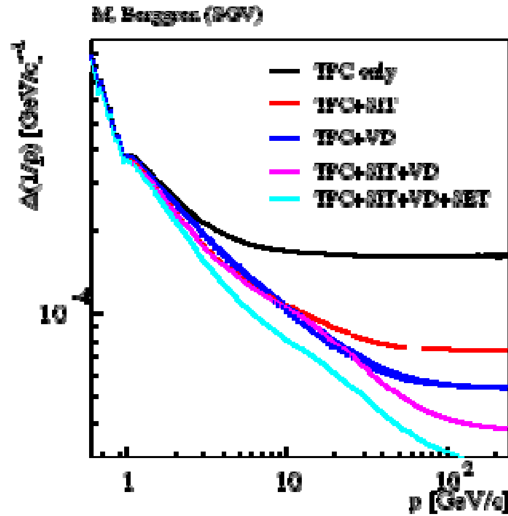


Figure 7: Resolution-curves for different combinations of elements. (The blue dashed line corresponds to the case with no SIT at all, while the blue solid line corresponds to the SIT material being present, but the SIT measurement not being used)

The dependence on momentum is clearly non-trivial, and one can in particular note the region between 8 to 25 GeV, where the resolution of TPC+SIT+VD is actually worse than for TPC+VD only, while it is better both for higher and lower momenta. The explanation of this feature is as follows: At low momentum the SIT gives a better first point compared to the TPC alone. The VD has too much material, and is to far away to add information. At 8 GeV, the extrapolation from the VD to the outer SIT layer is better than the SIT-point itself, and here the SIT adds no more information. Finally, at 15 GeV, the multiple scattering in the inner field-cage of the TPC becomes sufficiently small, so that the VD+SIT ensemble contributes both with position and angle. Note that the SET is insensitive to these kind of effects, as it gives the last point in the measuring range, and is placed just outside the outer field-cage. Therefore the SET tends to ameliorate the resolution more or less uniformly at all momenta.
A study was also made to evaluate the effect of the resolution of the TPC at long drift-distances, notably the effect of replacing the ``TDR'' gas (Ar-CH4-CO2 (93/5/2)) by the P5 gas. These two gases yield quite similar results at short drift-distances, but the P5 gas has a much lower transverse diffusion coefficient, essentially resulting in a point-resolution independent of drift-distance. The results of this study are shown in figure 8.
One notes that, as expected, the difference in the forward region is modest (left-hand plot). There is an important amelioration for tracks at 90°, but the relative amelioration by adding the silicon elements remains important (right-hand plot).

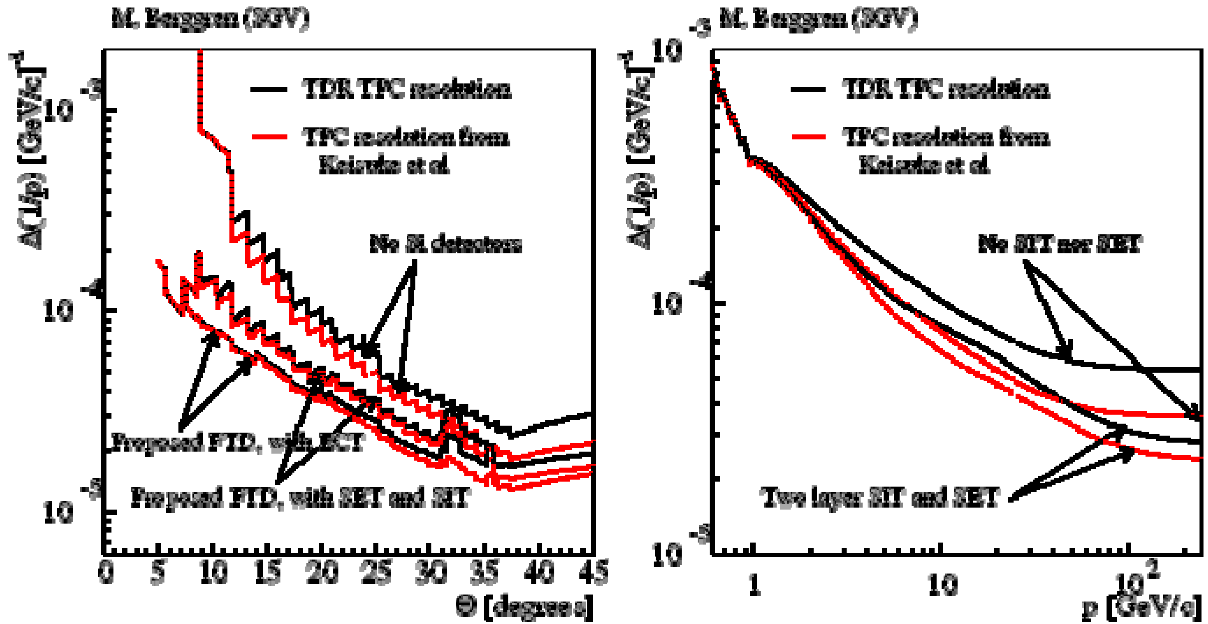


Figure 8: Effect of modified transverse diffusion in the TPC

Hit densities

Elsewhere in this report, the hit densities induced by background has been presented. It is also important to study the densities expected from physics events, as such hits are correlated in space. In order to do so, three cases were studied, using SGV to generate events:

Highest possible total multiplicity: $t\bar{t}$

Highest possible collimation: τ+τ-

Probable worst case: light quark antiquark

Three detector locations studied: SET, the inner layer of the SIT (R=16 cm), and the ECT (z=273 cm).

Two aspects are important: The number of hits per module, important for double-sided detectors, since there will be N! possible combinations of the two sides,and the probability to have two hits on the same or neighbouring strips.

For the SET, no problems are expected: any track-track correlations over the size of a SET ladder are washed out by scattering and bending in the B-field.

Hit densities in the SIT

For this study, it was assumed that the inner layer of the SIT was made of ladders half the length of the layer.

For $t\bar{t}$ events (figure 9, left), we find that there is on average 10 hits in most hit module, and that it can be above 20, ie. with 20! = 2.4×10^{18} possible combinations. We also find that in every $t\bar{t}$ event, there will at least be one module with 5 hits, 5!=120. There is a 3 % probability that a given track will have another track within 100 μm. Note that the distance-distribution is best described by a compound Poisson law, showing that the correlation is of the type clusters-of-clusters, presumably jets containing particles that decay. Both features are visible on the scale of a module.

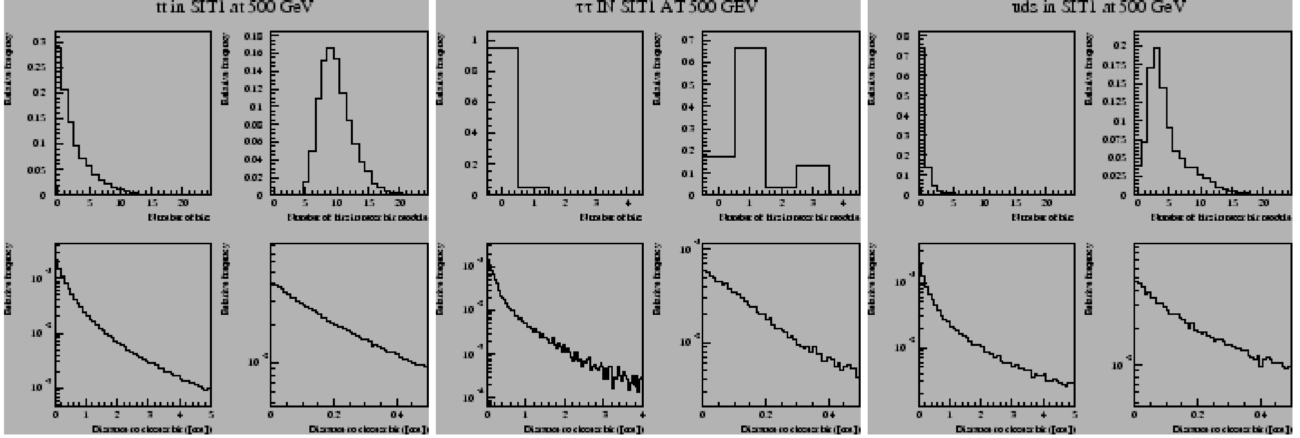


Figure 9: Hit densities in the SIT

For $\tau^+\tau^-$ events (figure 9, middle), the entire decay is usually in one module, so the number of hits is equally the topological branching ratio of τ decays. Furthermore, 18 % of the $\tau^+\tau^-$ events give no tracks at all in the SIT, and there is a 5 % probability that any given track will have another track within 100 µm. There is some tendency to see the effect of the sweeping out of the tracks by the B-field (in conjunction with charge conservation), since the probability to get two tracks very close is lower than that having a neighbour at a distance corresponding to the typical separation given by the field.

Finally, for q qqbar events (figure 9, right), there is on average 4 hits in most hit module, and there might be as many as 15 (15! = 6.5×10^{11}). There is a low probability (3.5 %) that a light q qqbar events give no tracks in the SIT, and there is a 3 % probability that any given track will have another track within 100 µm The deviation from the exponential shape is more pronounced in this case compared to the $t\bar{t}$ events - it is visible on the millimetre-scale - so the clusters-of-clusters type of correlation is present also for light quarks.

Hit densities in the ECT

In the ECT, we study the RΦ distance to other tracks in the event. We restrict to 8 "rings" in R: first ring has extends from R=32 to 39.4 cm, the following are all 14.8 cm wide, and we generate $t\bar{t}$ and light q qqbar events. It is important to note that γγ events are abundant at low angles. At the ILC, the integrated luminosity per train is of the order of 1 nb^{-1}, and the cross-section for $\gamma\gamma \rightarrow e^+e^- l^+l^-$, with one charged track above 10 degrees is 150 nb (bdk/bdkrc simulation), so a detector that can't separate wagons within the train will have of the order of 100 overlaid tracks.

For $t\bar{t}$ events (figure 10), we find that the track-density in RΦ is around 0.05 per cm, and that the distribution is flat on the scale of one module (10 cm). The average number of hits in a module can be estimated from the number of rings that would be read out together times the RΦ width of the module times the track-density in RΦ. Typically, this would amount to a few hits per module.

As the TPC end-plate represents 30 % X^0, it is important to generate γ -conversions, as can be seen in by comparing the left-hand and right-hand plots in figure 10, corresponding to γ -conversions in SGV being switched on or off, respectively.

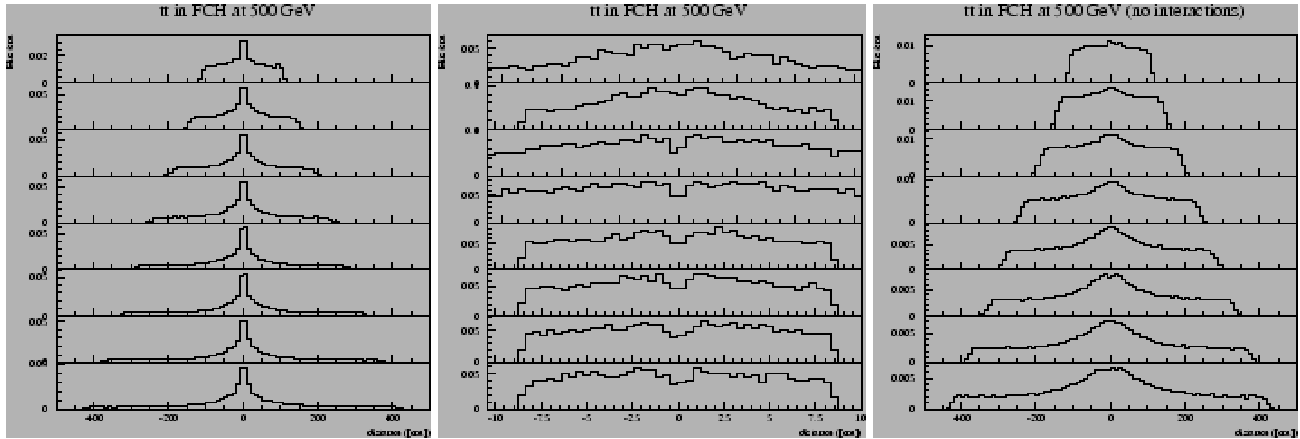


Figure: Hit densities in the ECT for $t\bar{t}$ events. The left and middle plot shows the same distribution, on different scales. The right plot shows the distribution if γ-conversions are switched off.

Similarly, for q qqbar events (figure 11), we find that the peak track density in RΦ is around 0.25 per cm. At the lower radii, contrary to the $t\bar{t}$ case, the jets are visible on the scale of a module. Hence, the density is not flat on this scale and therefore the exact layout of the module will be important. One can also observe the effect of the radiative return process (with the ISR in the beam-pipe), in that there is an accumulation of tracks at the opposite side of the detector, corresponding to the two jets being observed in the same end-cap but back-to-back in the RΦ projection.

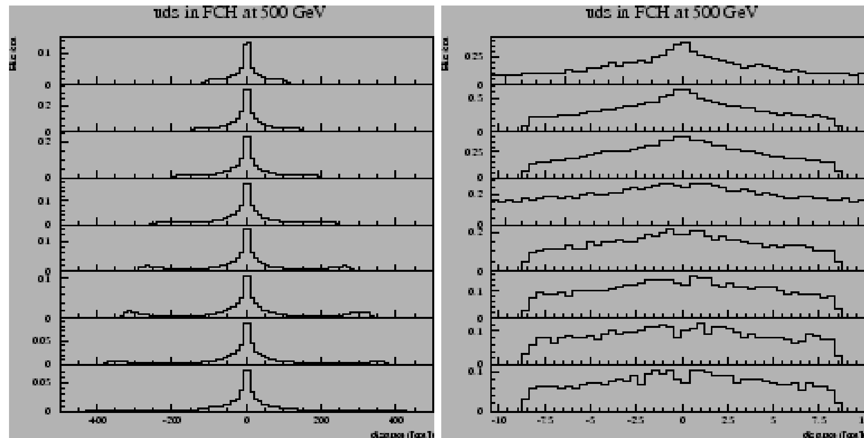


Figure: Hit densities in the ECT for q qqbar events