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Project: *CMOS sensor based Vertex Detector for the ILC*
Status Report

Development of Swift and Slim CMOS Sensors for a Vertex Detector at the International Linear Collider

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Abstract

CMOS sensors offer appealing vertexing performances. They are being developed for their application at the ILC since almost ten years and have reached a matureness allowing to use for them for short and mid-term applications in sub-atomic physics. This report provides an overview of the status of the developement of sensors of the MIMOSA[1] series, and outlines the next importants steps of the R&D.

The report also addresses studies performed to optimise the geometry of a high precision vertex detector best adapted to the running conditions near the ILC interaction point, keeping in mind that the dominant beam background (due to beamstrahlung) is subject to large uncertainties. Overall, the ambitionned performances of the detector should allow to cope with a background rate exceeding substantially the Monte-Carlo predictions. The results of the studies indicate that fast CMOS sensors are within reach, which could compose a vertex detector satisfying these particularly severe requirements.

[1] standing for Minimum Ionising MOS Active pixel sensor.

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1 Introduction

The ILC physics programme requires an extensive knowledge of the quantum numbers describing most of the final states observed. This goal sets a new standard in vertexing requirements, as it will be necessary to unravel the flavour of nearly every jet in final states often composed of several b, c an τ jets. Detection technologies used in previous occasions (e.g. CCDs in SLD) or developed for the LHC experiments (e.g. Hybrid Pixel Sensors) are far from being adequate. They require substantial performance improvements which necessitate a considerable R&D effort, and are exposed to several show stoppers. This observation is at the origin of the developement of a novel, alternative, pixel technology at IPHC-Strasbourg in the late nineties, called Monolithic Active Pixel Sensors (MAPS) or, more simply, CMOS sensors. These devices had never been used in particle tracking, but were progressively replacing CCDs in commercial cameras. The developement pioneered at IPHC consisted first in developing exploratory pixel matrices, which would depart from the commercial visible light imagers, which were too slow, exhibited poor detection efficiency and were radiation soft.

Since the start of the project, most of the R&D effort is invested in the sensor design, including both the detection system and integrated signal processing micro-circuits, and into the characterisation of sensor prototypes. These activities are sustained by detailed studies aiming to fine tune the requirements a vertex detector at the ILC has to fullfil, and to optimise its parameters when composed of CMOS sensors. Finally, studies are made to settle reliable and cost effective thinning procedures in industry or in academic laboratories.

Several research teams have joined the R&D effort since its start, and taken over some of its major tasks. Moreover, the latter are carried out within a network of teams developing CMOS sensors in Europe and the US, which allows to share efficiently the progress made in each team.

Since this sensor technology was never used for particle tracking previously, an essential issue of the developement consisted in demonstrating that a detector made of CMOS sensors could be operated in a subatomic physics experiment with satisfactory results. Meanwhile, the performances achieved, though not yet meeting all the ILC requirements, became already sufficient for particle tracking applications which are less demanding than the ILC ones. The sensor R&D programme for the ILC is therefore based on intermediate calendar and performance milestones, where the sensors will be used in subatomic physics experiments for vertexing (or tracking) purposes. The benefit from this organisation of the R&D is multifold: it allows to address major material budget, integration and engineering issues, to operate simultaneously hundreds of sensors, to investigate their performance in charm tagging in real experimental conditions (e.g. operating temperature, radiation tolerance) and to share the R&D effort.

The detection performance goals of the R&D programme are quite diverse. They concern generic parameters (granularity, material budget, read-out speed, radiation tolerance, power dissipation), as well as some others which are specific to the technology (fabrication processes, integration issues, etc.). Moreover, several of these issues rely on doping details of the sensor fabrication process which cannot be known with the necessary accuracy to simulate the functionning of the sensors. Finally, since the signal processing micro-circuits are integrated on the same substrate as the detecting elements, these two parts of the sensor need a simultaneous, coherent, optimisation. In ordre to progress in sink on all these different fronts, the R&D needs to lean back on numerous prototypes, each addressing specific issues, and providing the necessary information to optimise the performances of the analog part of the sensor.

Some of the vertex detector requirements are still not well established. This statement applies to parameters driving the impact parameter resolution, such as the material budget. It applies

also to those driven by the running conditions, such as the read-out speed and the radiation tolerance. Some of these parameters may actually remain poorly known until the start up of the collider. For these particular parameters, the sensor performance goals were assessed with sizeable safety margins, which translate into more ambitious requirements for the CMOS sensors described in this document, called MIMOSA, than those usually considered in other sensor R&D programmes.

The document is organised as follows. It starts with a short reminder on the principle of operation and specific technical and industrial aspects of CMOS sensors. The next two sections (i.e. 3 and 4) review the performances achieved up to now with the MIMOSA sensors. Two classes of performances are considered: those driven by the physics goals (directly connected to flavour tagging capabilities) and those imposed by the running conditions (reflecting the IP environment). The latter are recalled, highlighting those requirements which are imposed to be more constraining as usually accounted for. Section 5 describes vertex detector design studies which aim to optimise the detector performances by exploiting specific advantages of CMOS sensors. The main steps of the sensor R&D foreseen until 2009/2010 are summarised in section 6. Integration issues, which complement the sensor R&D activites, are overviewed in section 7. The summary (section 8) is followed by two appendices providing a minimal set of details of the different chips fabricated since the end of 2003 and foreseen to be fabricated until 2009/2010.

The physics goals motivating the R&D are not covered in this document, since - up to recently - they were only poorly addressed by the research teams involved in the CMOS sensor development described hereafter.

2 Main characteristics of CMOS sensors

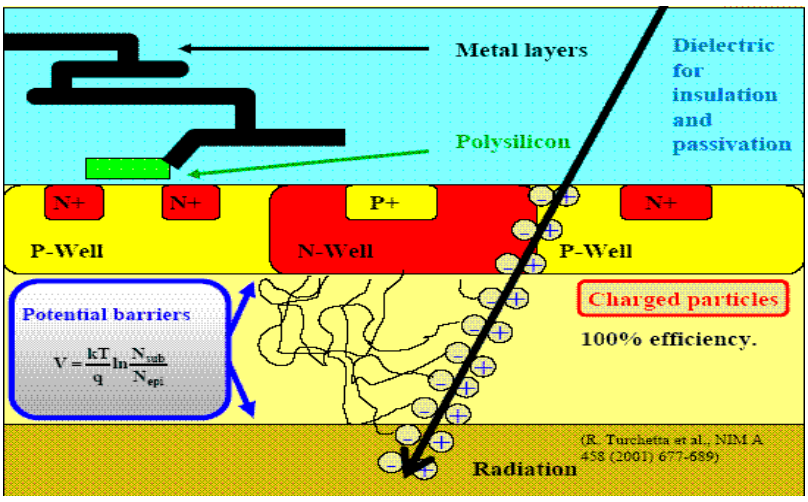


Figure 1: Principle of operation of CMOS sensors.

CMOS sensors allow to detect charged particles by collecting the charge they liberate when traversing the thin, almost undepleted, epitaxial layer, buried underneath the read-out electronics. The carriers of the signal charge (electrons) diffuse thermally in the layer and are collected

by sensing elements formed by regularly implanted n-wells in direct contact with the (p-type) epitaxial layer [1]. Since minimum ionising particle generate typically $\sim$ 80 electron-hole pairs per micrometer in the $\sim$ 5 - 15 μm thick epitaxial layer, the signal charge ranges from a few hundreds to $\sim$ 1000 e^-. The principle of operation of these sensors is illustrated in figure 1.

In its simplest version, each pixel is equipped with three transistors: one for resetting the sensing diode voltage, one connected to a source follower which integrates the charge collected and one for adressing the pixel for the read-out and signal transfer. This architecture does not include yet any signal processing.

The early stage of the development was dominated by the need to validate the technology for charged particle tracking [1]. The adequacy of CMOS sensors for this application is now well established, as shown in the next section, and the R&D goals have moved to topics focussed on the specific features of the technology in order to push its performances at the level required by future vertex detectors where existing technologies would not be satisfactory. At present, the main R&D activities consist in the following:

- develop signal processing micro-circuits integrated on the sensor substrate, which provide fast, low noise and low power signal processing;
- explore the characteristics of fabrication processes in order to find those best adapted to charged particle tracking;
- push the radiation tolerance at its best possible, especially at room temperature;
- find industrial procedures which allow to thin the sensors very close to the epitaxial layer without degrading their mechanical (and electrical) properties.

The exploration of fabrication processes is specific to the CMOS sensor technology because several basic manufacturing parameters, such as the thickness of the epitaxial layer (which determines the signal magnitude), are fixed by the manufacturer and are quite often not known reliably. Exploring fabrication processes is therefore of prime importance for the development of high performance sensors.

It is worth noticing that the progress made during the last few years in the developement of these sensors for particle tracking has benefitted from the fact that the manufacturing technology is a world wide standard, meaning that the prototype fabrications are cheap and that their turn over is fast.

3 Physics driven performances

3.1 Introduction

As pointed out above, the charged particle detection performances of the sensors are largely influenced by basic manufacturing parameters. An essential parameter is the thickness of the epitaxial layer, which needs to be effective over $\gtrsim 10\ \mu m$ in ordre to ensure enough signal charge. Several other parameters are also to be considered, such as the doping profile, leakage current, depth of the n- and p-wells, oxide thickness, transistor feature size, number of metal layers, a.s.o.. Most of these parametres may vary substantially from one fabrication process to another, with very limited possibilities for HEP customers to influence the parameter settings. Finding well adapted fabrication processes is therefore of crucial importance.

More than 20 different MIMOSA sensors were designed, fabricated and tested up to now, in 7 different manufacturing processes, as summarised below:

- AMS-0.6 μm: MIMOSA-1, MIMOSA-5
- AMS-0.35 μm without epitaxial layer: MIMOSA-4, -12 and -13
- AMS-0.35 μm OPTO with epitaxial layer: MIMOSA-9, -11, -14, -15, -16, -17, -18, -19 and -20.
- MIETEC-0.35 μm (which became AMI-0.35 μm more recently): MIMOSA-2 and -6
- TSMC-0.25 μm: MIMOSA-8 and -10
- IBM-0.25 μm: MIMOSA-3
- STM-0.25 μm: MIMOSA-21

Technical details on most of the chips fabricated since the end of 2003 are provided in Appendix A.

The most satisfactory technology characterised so far is the AMS-0.35 OPTO process. Excellent tracking performances were obtained with 4 consecutive small prototypes fabricated via multi-project runs from 2003 to 2006. Several larger chips (i.e. from $\sim$ 5x5 to 10x20 mm^2 wide) were fabricated in 2006 and 2007 within an engineering run. Their preliminary test results confirm the good performances obtained with the small prototypes.

The AMS-0.35 OPTO process became therefore the baseline for the sensor generic R&D and for their short and mid-term tracking applications (STAR HFT, EUDET beam telescope, demonstrator for the CBM vertex detector[2]). This process provides also a relatively economical framework when prototyping sensors for the ILC vertex detector. It is nevertheless unlikely to be used for the fabrication of the final ILC sensors. This has several reasons:

- the availability of the process in the next decade;
- the too restricted number of metal layers (only 4, while at least 6 are needed);
- the relatively large feature size.

Mainly for the first reason mentioned above, the search for new, better suited, manufacturing technologies is part of the R&D activities.

3.2 Basic detection performances

The m.i.p. detection performances were studied with the sensors being mounted on a beam telescope made of of 8 planes of silicon micro-strips, installed on $\sim$ 100 - 200 GeV particle beams delivered by the CERN-SPS. The telescope resolution is about 2 μm per plane, which translates into an accuracy on the extrapolated impact position of about 1 μm.

The response of the sensors to the beam particles is illustrated by figure 2, which shows the charge collected by the seed pixel and by clusters of 3x3 and 5x5 pixels centered on the seed pixel. It also displays the pixel noise, the seed pixel signal-to-noise ratio (SNR) and the mean total charged collected in a cluster as a function of the number of pixels included in it.

In summary, the pixel noise amounts to $\lesssim 9$ e$^-$ENC, the seed pixel SNR most probable value (MPV) is $\gtrsim 25$ and the cluster multiplicity is around 10 - 15, with $\sim$ 90 % of the total charge collected in a 3x3 pixel cluster centered on the seed pixel. The corresponding m.i.p. detection efficiency was 100 % for this specific run (with a statistical accuracy of 0.02 %).

The dependence of the detection efficiency on the pixel pitch (varied from 20 to 40 μm) and the operation temperature is shown in figure 3. One observes that the detection efficiency

[2]Cold Baryonic Matter experiment at FAIR, GSI (Darmstadt)

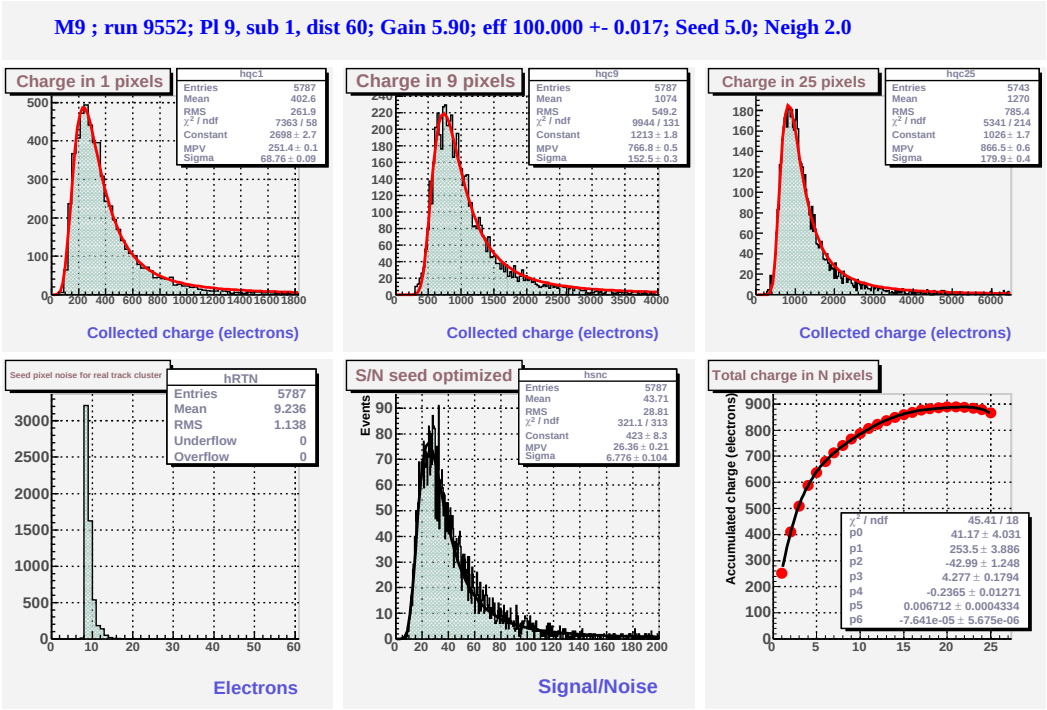


Figure 2: MIMOSA-9 (20 μm pitch) beam tests results at an operating temperature of 20° : seed pixel charge (top left), 3x3 cluster charge (top center), 5x5 cluster charge (top right), pixel noise (bottom left), seed pixel SNR (bottom center) and cluster charge versus cluster multiplicity (bottom right).

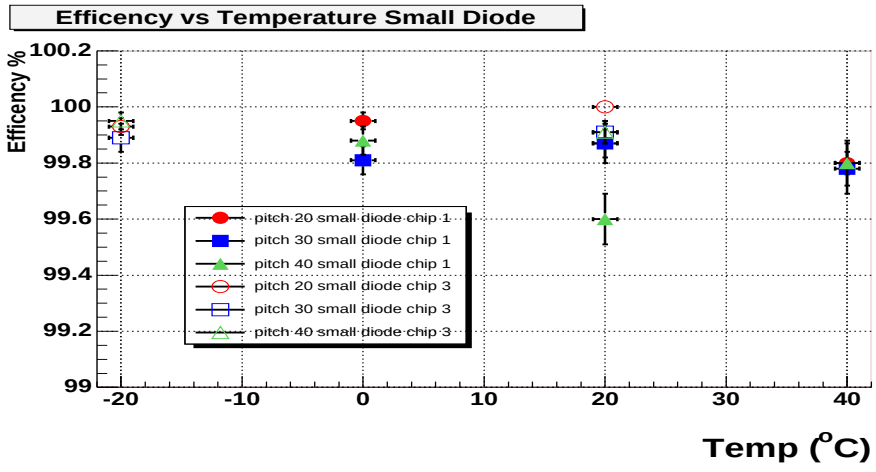


Figure 3: Data collected at DESY (few GeV electrons) with two MIMOSA-9 sensors mounted on a Si-strip telescope. The detection efficiency for beam electrons is displayed as a function of the coolant temperature for pitch values of 20, 30 and 40 μm.

remains essentially $\gtrsim$ 99.8 % at all temperatures and for all pitch values, the best performances being obtained with the smallest pitch (20 μm) and below 40°.

In summary, the results shown so far demonstrate that a pixel detector providing a 20 – 40 μm pitch with a useful thickness of $\sim$ 30 μm[3] can be operated at room temperature with close to 100 % detection efficiency.

These very encouraging results deserve however some caveates, because they were derived from measurements which do not include all relevant features expressing the operation of the final sensors, i.e.:

- final sensors will cover much larger surfaces and will be numerous. The homogeneity of the pixel performances needs to be assessed, as well as the fabrication yield;
- in ordre to achieve data sparsification, the final pixel design will incorporate signal processing micro-circuits (e.g. for CDS[4]) running at high clock frequencies. The design of the pixel and read-out architectures has to maintain an acceptable pixel noise as well as to garantee a signal amplification sufficient to minimise the influence of the noise generated by the read-out chain;
- the pixel noise and the signal charge collection efficiency may degrade after some exposure to beamstrahlung electrons, especialy at room temperature. Special care has to be taken in ordre to minimise their impact.

All these aspects were already addressed by the R&D in some extend. They are treated later in this report.

3.3 Spatial resolution

3.3.1 Required resolution

Requirements on the resolution to be provided by the vertex detector at the ILC are difficult to assess at this stage of the ILC project: they depend on the arrangement and performances of other sub-detectors and require mature software tools for event reconstruction. The impact of various options of the vertex detector on the physics performance of the whole apparatus is therefore still under study. Meanwhile, a target value on the impact parameter resolution is being used, which is provided in the TESLA TDR, i.e.: $\sigma_{IP} \leq a \oplus b/p \cdot sin^{3/2}\theta$, with a $\leq$ 5 μm and b $\leq$ 10 μm. These upper limits on a and b translate into stringent limits on the inner most layer of the vertex detector: a sensor single point resolution typically $\lesssim$ 3 μm and a material budget for the layer corresponding to $\lesssim$ 0.2 % of radiation length.

To evaluate the challenge, one may compare the values of a and b to the best values ever obtained before (i.e. with the SLD microvertex detector): a $\sim$ 8 μm and b $\sim$ 33 μm. The gap between these previous best performances and those aimed at the ILC is thus substantial, in particular at low momentum. The groups developing MIMOSA sensors did not yet much involve themselves in physics studies allowing to fine tune these target values. This situation will change: a study based on the Higgstrahlung process is getting started, which is aiming to provide an outcome within one year or so.

[3] one can envisage thinning down CMOS sensors to such a thickness without any signal loss.

[4] Correlated Double Sampling

3.3.2 Measured single point resolution

CMOS sensors offre very high resolution as a direct consequence of one of their basic operation principles. Since the charges liberated when a m.i.p. traverses the epitaxial layer diffuse thermally and get distributed over a several pixels, the resulting charge sharing allows to reconstruct hit positions with a spatial resolution much better than the binary resolution associated to the pixel pitch (i.e. pitch / $\sqrt{12}$).

Besides the prominent influence of the pixel pitch on the spatial resolution, there are several other critical parameters entering the spatial resolution. Some of the most important ones are listed below:

- the epitaxial layer thickness because of its influence on the signal charge;
- the epitaxial layer doping and the collecting diode characteristics because of their influence on the charge collection efficiency, and thus on the signal magnitude;
- the operating temperature, because of its influence on the charge collection efficiency, i.e. the signal magnitude;
- the electronic noise because of its influence on the SNR;
- the clustering algorithm, which influences the pixel multiplicity in the clusters, and therefore the possibility to compute a barycentre of the charge distribution.

The spatial resolution of the sensors was evaluated at the CERN-SPS with numerous different prototypes mounted on the silicon strip telescope mentionned in section 3.2. The sensor resolution was derived from the residue between the extrapolated impact position and the position reconstructed in the CMOS sensor. The values extracted from the MIMOSA-9 data are summarised on figure 4.

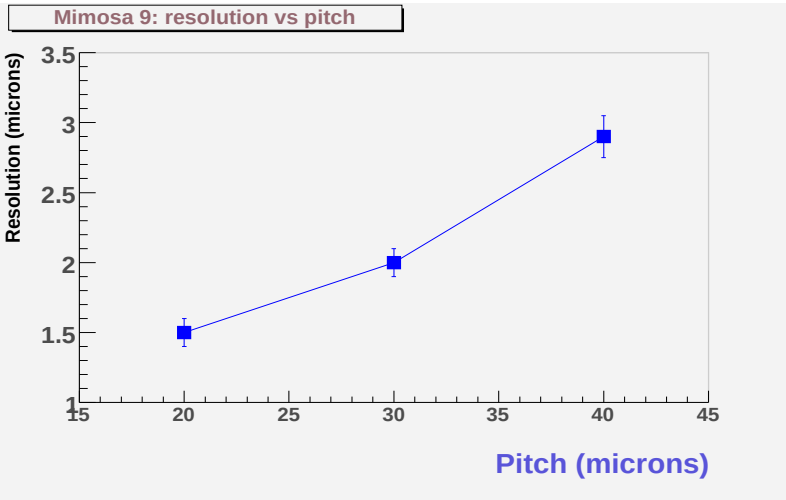


Figure 4: MIMOSA-9 beam tests results: single point resolution as a function of the pixel pitch.

The resolution obtained amounts to $\sim$ 1.5, 2 and 3 μm for a pixel pitch of 20, 30 and 40 μm respectively. The 20 μm and 30 μm wide pixels provide values which are much better than the minimal performances required. Since the results were obtained with charges encoded on 12-bit ADCs, there is room left to encode the charges on a much less granular (and thus

very compact and fast) ADC. Studies were made in order to evaluate how much the single point resolution degrades as one reduces the number of ADC bits on which the charge is encoded. The study was performed with the real (MIMOSA-9) data used in figure 4, simulating the encoding on 3, 4 and 5 bits. For a 20 μm pitch, resolutions of about 2.1, 1.9 and 1.7 $\pm$ 0.1 μm were achieved, respectively. Equipping the sensors with ADCs featuring at least 3 (real) bits looks therefore sufficient to provide a resolution close to 2 μm. This developement is described in section 4.3.1.D.

3.4 Rate of noisy pixels

The least significant bit of the ADCs integrated in the sensors will be used to select those pixels which were hit by a particle, and suppress all other signals. This is mandatory to keep the data rate delivered by the sensors compatible with the data acquisition system. The optimal value of the threshold is to be found, which is sufficiently low to preserve the detection efficiency and high enough to reject efficiently noisy pixels.

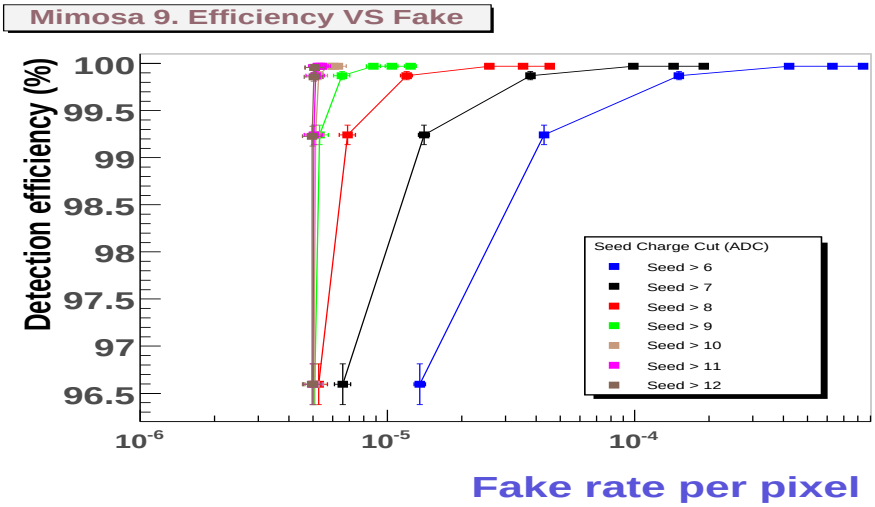


Figure 5: MIMOSA-9 beam test data. Correlation between the detection efficiency and the noisy pixel rate as a function of cluster charge threshold. Clusters are selected by applying separately a cut on the seed pixel charge and on the total charge of the 8 pixels surrounding the seed pixel. The former cut is varied from 6 ADC units (equivalent to $\sim$ 4 times the pixel noise) to 12 units by steps of 1 unit. Fore each of these 7 cut values, 6 different values of the cut on the crown charge are considered, amounting to to 0, 3, 4, 9, 13 and 17 ADC units (from right to left along each series of measured points). The lowest value of the "fake rate" is saturated due to the limited sensitivity of the measurements.

The effect of noisy pixels was investigated with the beam test data collected with MIMOSA-9 at DESY. One of the motivations of the study was to find out whether the data flow of future sensors equipped with zero suppression micro-circuits would be influenced by noisy pixels delivering a fake signal above the discriminating threshold integrated at the column ends.

The results are illustrated by figure 5. It displays the detection efficiency as a function of the fraction of pixels delivering a fake signal coming from the electronic noise. The correlation

between both parameters is displayed for various values of the cluster selection parameters. The latter are the seed charge and the sum of the charges of the crown of pixels surrounding the seed pixel. Measurements performed with the same cut value on the seed charge (varied from 6 to 12 ADC units) are connected with a line. They differ by the cut on the crown charge, varied from 0 to 17 ADC units.

One observes that a detection efficiency of $\gtrsim 99.9$ % is rather easily obtained without letting the fake rate exceed $\sim 10^{-4}$. Since the beamstrahlung rate is expected to fire a fraction of the pixels ranging from $\sim 10^{-3}$ to several per-cent (depending on the layer), one can conclude that noisy pixels should not increase significantly the data flow delivered by the sensors in any of the detector layers. The results need, of course, to be confirmed with the final sensors integrating all signal processing micro-circuits (with the corresponding noise) and fabricated within their own industrial process.

3.5 Assessing performances of real size sensors

Mainly for financial reasons, most of the R&D steps are based on small prototypes made of a few thousands of pixels covering typically a surface of O(10) mm^2 or even less. Demonstrating that satisfactory performances obtained with such small prototypes can be reproduced with real scale ones is an important step of the R&D programme. Investigating the detection performances with sensors made of $\sim 10^5$ to 10^6 pixels and covering a surface in the ordre of a centimetre squared allows to evaluate the uniformity of the pixel response accross the sensor surface as well as the uniformity of the sensor response across each reticle, each wafer or from wafer to wafer.

The first real size sensor (MIMOSA-5) was fabricated in 2001/2002. It featured ~ 1 million pixels (17 μm pitch) and a total active surface of $\gtrsim 3$ cm^2. Fabricated in the AMS-0.6 μm technology, its frame read-out frequency was a few tens of Hz. Its detection performances reproduced quite well those obtained with the small prototype MIMOSA-1. The fabrication yield was found to be ~ 30 - 40 %, a typical value for CMOS industry.

The evaluation of the response uniformity and of the fabrication yield of the present baseline manufacturing process, AMS-0.35 OPTO, became necessary for the developement of sensors adapted to STAR an EUDET. An engineering run was ordered in 2006 in ordre to manufacture several real size sensors (i.e. ~ 0.5 - 2. cm^2 large), in perspective of their use as detector demonstrators.

One of the goals of this run was to assess the fabrication yield; another objective was to characterise a new option of the process, featuring a thicker epitaxial layer (called "20 μm" epitaxy).

The engineering run provided more than 50 copies (reticles) per wafer of each different sensor hosted on the reticle. This new generation of large sensors differs from the previous one (MIMOSA-5) mainly on the following aspects :

- its read-out frequency is one or two orders of magnitude higher (typically thousand frames per second);
- the sensors can be operated at room temperature (no cooling required);

Some of these real size sensors (MIMOSA-17 and -18) were mounted together in ordre to build a telescope made of 3 or 4 planes of CMOS pixel arrays, called TAPI[5]. The telescope was commissionned in June 2007 on a few GeV electron beam at DESY, and operated at the CERN-SPS in Septembre 2007.

[5]standing for *Telescope A Pixels de l'IPHC*

Beam test data are still being analysed. Preliminary results show that the MIMOSA-18 sensors (made of 512 x 512 pixels featuring a 10 μm pitch) are working well: the residual noise is found to be $\sim$ 10 e$^-$ENC and the SNR amounts to $\sim$ 30 at room temperature. This is illustrated by figure 6.

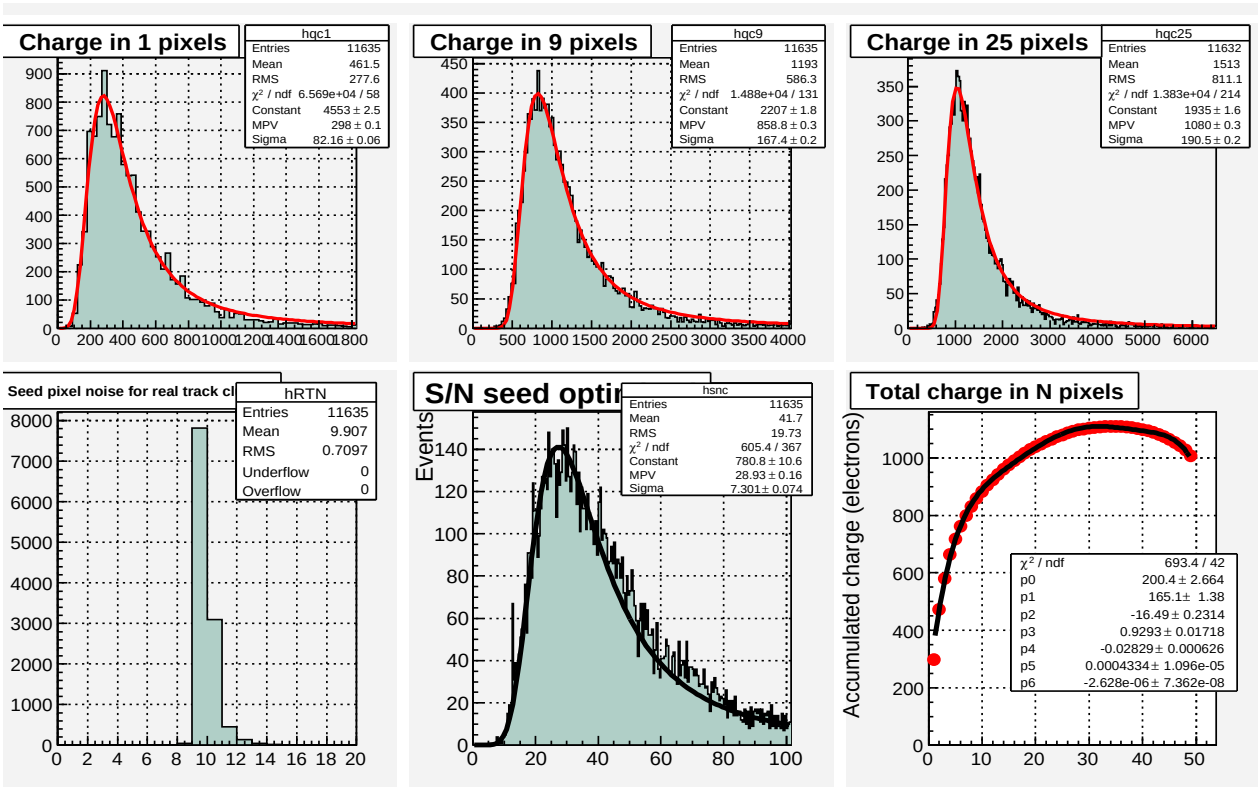


Figure 6: MIMOSA-18 (10 μm pitch) beam test (5 GeV electrons at DESY) results at an operating temperature of 20° : seed pixel charge (top left), 3x3 cluster charge (top center), 5x5 cluster charge (top right), pixel noise (bottom left), seed pixel SNR (bottom center) and cluster charge versus cluster multiplicity (bottom right).

Several MIMOSA-17 sensors (256 x 256 pixels of 30 μm pitch) were used to equip the demonstrator of the EUDET telescope. The latter was commissionned in Spring and Summer 2007 at DESY, and operated for the first time at the CERN-SPS in Septembre 2007. The data collected are still being analysed, but the satisfactory functionning of the sensors is already established.

Recently, several wafers of the AMS-0.35 OPTO engineering run were analysed with a probe station in ordre to estimate the fabrication yield. The study concentrates on the largest chip of the reticle, i.e. MIMOSA-20, which takes half of its surface. It is not yet completed, but its first results indicate that the fabrication yield varies from $\lesssim$ 40 % to $\gtrsim$ 80 %, depending on the wafer. This substantial dispersion between wafers is currently being scrutinised.

3.6 Thinning

3.6.1 General remarks

The single point resolution offered by the sensors and their very thin "useful" thickness (typically 30 μm overall) provide strong motivations to thin them down to $\sim$ 50 μm or less. Establishing a reliable thinning procedure encompasses a series of crucial points listed hereafter:

- the rate of broken or chipped sensors should remain marginal;
- thinning procedures applicable to complete wafers are ususally considered as more reliable than those applied to individual sensors. However, the latter offers the advantage of being more cost effective, especially during R&D. Both types of procedures may therefore be investigated;
- the release of mechanical stress consecutive to the thinning will bend the sensor. It should however remain possible to manipulate and bond it on a support;
- the thinning procedure may generate additionnal noise (consequence of micro-cracks, etc.). The SNR performance of the sensors should essentially remain unaffected.

Thinning trials were made at various places and with sensors of various sizes, either by thinning entire wafers or individual sensors to typically 50 μm. Studies of thinned sensors were performed in several laboratories, in particular at LBNL for STAR experiment. Their outcome is still based on a few tens of sensors only, and addresses mainly mechanical issues. The preliminary, partial, conclusions which can already be drawn are encouraging:

- the sensors can be thinned to $\sim$ 50 $\pm$ 5 μm without significant loss (broken of chipped sensors);
- despite the fragility of the thinned sensors and the bending resulting from the mechanical stress release, they can be glued on a flex cable, a mechanical support or on interface boards and bonded to their steering and read-out peripheral electronics;
- preliminary noise measurements of a few sensors (e.g. of $\sim$ 6 x 5 mm^2 large MIMOSA-18 chip) indicate a potential noise increase of $\sim$ 5 e$^-$ ENC. This result, which is not really worrying, needs to be substantiated with additionnal investigations.

In conclusion, the goal of thinning the sensors down to $\sim$ 50 μm seems realistic. There are still several pending questions, concerning functionnal aspects rather than mechanical ones. Studies are progressing, which should clarify most of the topics by the end of 2008. Moreover, a more agressive target value, such as $\gtrsim$ 30 μm, may be achievable on the mid-term.

4 Performances driven by running conditions

4.1 General remarks

The ILC running conditions, though much less constraining than at LHC, represent a major obstacle for the achievement of a high precision vertex detector suited to the physics goals. The dominant constraints originate from e$^\pm$ created through beam-beam synchrotron radiation (i.e. beamstrahlung). The rate of beamstrahlung electrons traversing the innermost detector layer dictates the sensor occupancy as well as the integrated radiation doses it has to withstand. These constraints have major consequences on the R&D programme of the MIMOSA sensors. The achieved performances and the next steps of the developement addressing the constraints coming from the running conditions are summarised in this section.

4.2 Radiation tolerance

The integrated radiation dose which the sensors are required to tolerate is almost fully determined by the rate of beamstrahlung $e^{\pm}_{BS}$. This statement is definitely true for ionising radiation; it applies also in a large extend to non-ionising radiation, as the fluence related to the neutron gas propagating inside the apparatus is at least one ordre of magnitude below the fluence associated to the beamstrahlung $e^{\pm}$ in the innermost layer.

High radiation doses have generally two kinds of consequences on the sensor performances: first, they tend to increase the leakage current, which enhances the noise (depending on temperature and integration time); second, they introduce intersticial traps, and thus reduce the charge collection efficiency due to electron-hole recombination. The increase of noise may be marginal for the short read-out times relevant for the ILC (i.e. 25 - 100 μs), but a cautious pixel design may still be useful as it may allow running at room temperature, a condition which allows for reduced material budget. The appearance of traps can be more disturbing, especially for CMOS sensors, where the signal electrons diffuse thermally in the epitaxial layer until reaching a sensing diode. Running at a temperature close to 0°C is known to improve substantially the sensor tolerance, but it may conflict with the goal to squeeze the material budget. The goal of the study in this case thus concentrates on demonstrating that the sensors work efficiently at room temperature for the expected fluence.

4.2.1 Ionising radiation

The ionising radiation dose which the sensors are supposed to tolerate has been estimated to O(100) kRad per year, accounting for the effect of the experimental magnetic field and multiplying the Monte-Carlo outcome based on the GUINEAPIG generator with a safety factor of 3 [4].

The typical energy of beamstrahlung electrons in a 4T magnetic field at 15 mm from the beam lines is $\sim$ 10 MeV. The genuine tolerance of sensors to such electrons was studied for the first time in Spring 2005, with a low energy (9.4 MeV) electron beam. The chips could be irradiated while being operated.

MIMOSA-9 and -5 sensors were exposed to this electron beam. The chips received integrated doses of $3{\cdot}10^{12}e^{-}{\cdot}cm^{-2}$ and $1{\cdot}10^{13}e^{-}{\cdot}cm^{-2}$. The latter value corresponds to the maximal dose expected in the inner most layer after more than 5 years of operation. The test results of the MIMOSA-9 chip (20 μm pitch, 3.4x4.3 μm^2 diode) exposed to an integrated flux of $1{\cdot}10^{13}e^{-}{\cdot}cm^{-2}$, show that (at a temperature of -20°C), the SNR value is still high ($\sim$ 23 instead of $\sim$ 28 before irradiation), and that the detection efficiency, which amounts still to 99.3 $\pm$ 0.1 %, exhibits only a modest change. The question remains however how this performance may deteriorate when running at room temperature.

In ordre to tolerate high radiation doses at room temperature, the pixel design was revisited in ordre to contain the increase of the leakage current consecutive to large integrated dose exposures. Arrays of MIMOSA-11 and -15 were designed for this purpose with pixels where the thick oxide near the sensing diode was removed and a P+ guard ring was implemented around the diode. The tolerance of MIMOSA-11 was studied in Spring 2005 with an ^{55}Fe source for values of the integrated dose delivered by a 10 keV X-Ray source ranging up to 1 MRad.

Figure 8 shows how the residual noise, measured with standard pixels and with radiation tolerant ones, varies as a function of the integration time at different temperatures, after exposure to an integrated dose of 500 kRad (i.e. several times the upper limit on the yearly dose mentioned

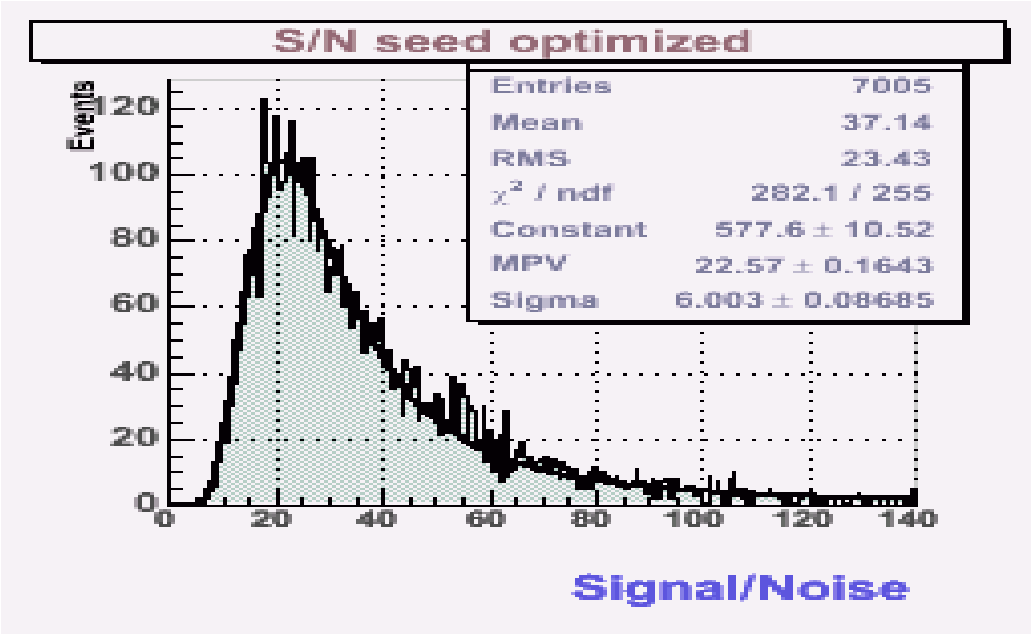


Figure 7: SNR distribution of a MIMOSA-9 sensor (20 μm pitch, 3.4x4.3 μm^2 diodes) irradiated with 9.4 MeV electrons. The integrated dose amounts to $1{\cdot}10^{13} e^-/cm^2$. The distributions were measured at an operating temperature of -20°.

above).

One observes that, contrary to the standard pixel, the radiation tolerant structure stands 500 kRad at room temperature (i.e. the noise remains well below 20 e^-ENC) for the range of integration time values foreseen at the ILC (typically 25 to 100 μs).

These radiation tolerance studies were extended with the prototype MIMOSA-15, which features pixels designed with the same architecture modifications as MIMOSA-11, slightly optimised in terms of noise and charge collection efficiency (CCE). The radiation tolerance of MIMOSA-15 sensors was assessed in 2006 on a $\sim$ 5 GeV/c e^- beam at DESY. One among the chips tested had been exposed to an integrated dose of $\sim$ 1 MRad (obtained with a 10 keV X-Ray source). The results of the measurement are summarised in table 1.

Integrated Dose	Noise	SNR (MPV)	Detection Efficiency
0	9.0 ± 1.1	27.8 ± 0.5	100 %
1 MRad	10.7 ± 0.9	19.5 ± 0.2	99.96 ± 0.04 %

Table 1: Tests of MIMOSA-15 (30 μm pitch) with a $\sim$ 5 GeV e^- beam at DESY. Noise, SNR and detection efficiency are displayed for a non-irradiated sensor and for another one irradiated with 1 MRad of 10 keV X-Rays. The coolant temperature was -20°C.

The irradiated sensor still exhibits a SNR of $\sim$ 19, to be compared to $\sim$ 28 before irradiation, and a detection efficiency of $\sim$ 99.9 % at a coolant temperature of -20°C (with 180 μs integra-

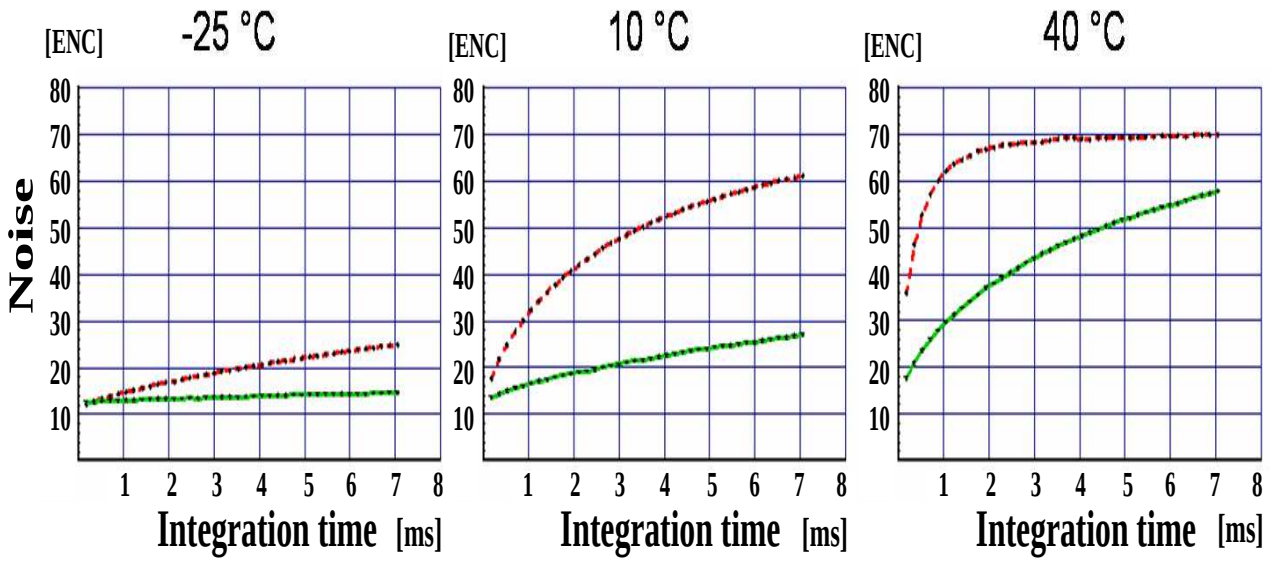


Figure 8: MIMOSA-11 tests with an ^{55}Fe source after exposure to an integrated dose of 500 kRad. The residual noise is shown as a function of the integration time for pixels designed without special care w.r.t. radiation damage (upper dotted line) and for radiation tolerant pixels (lower dotted line). The measurements are displayed for three different coolant temperatures (- 25°C, + 10°C, + 40°C).

tion time). These performances validate the pixel architecture implemented against parasitic leakage current generated by ionising radiation. The results need still to be confirmed at room temperature, with $\sim$ 10 MeV electrons and with the final pixel architecture, but no substantial change is expected for the short integration times under consideration.

4.2.2 Non-ionising radiation

Bulk damage is expected to come mainly from the neutron gas and from the beamstrahlung $e^{\pm}$. While the fluence corresponding to the neutron gas rate is $\lesssim 10^{10}$ n_{eq} /cm^2, that due to beamstrahlung is about one ordre of magnitude more (assuming a NIEL factor of 1/30 for the $e^{\pm}$ in the relevant energy range). As a consequence, one may consider a fluence of $\lesssim 10^{12}$ n_{eq} /cm^2 as a safe requirement for the sensor tolerance.

The radiation tolerance may be quite different from one fabrication process to another. The first sensor fabricated in the AMS-0.35 OPTO technology to be tested against non-ionising radiation was MIMOSA-9, which was exposed to $\sim$ 1 MeV neutrons in Dubna, and consecutively tested on the DESY electron beam. It was observed that even for a fluence of $\sim 10^{12} n_{eq}/cm^2$, the sensor still exhibited a SNR of $\sim$ 19, and a detection efficiency of $\sim$ 99.5 % at a coolant temperature of -20°C [2].

The study was completed with the MIMOSA-15 prototype, which was exposed to fluences of up to $\sim 6{\cdot}10^{12} n_{eq}/cm^2$. Figure 9 summarises the results. It shows the detection efficiency as a function of the fluence. One observes that a sensor exposed to $\sim 2{\cdot}10^{12} n_{eq}/cm^2$ still exhibits a detection efficiency above 99 % at a coolant temperature of -20°C. For a fluence of $\sim 6{\cdot}10^{12} n_{eq}/cm^2$, the detection efficiency drops to $\sim$ 80 %. The next steps of this study will consist in assessing the sensor performances at room temperature.

Beyond the tests of sensors with analog output and no signal conditionning in the pixels,

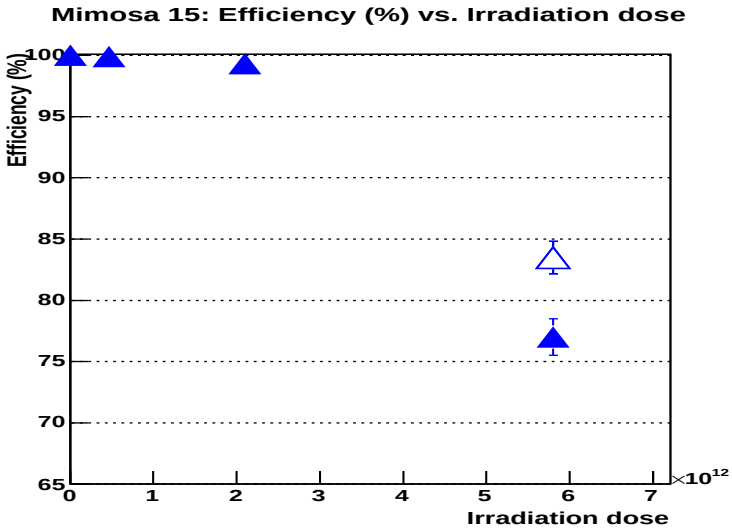


Figure 9: Tests of MIMOSA-15 with a $\sim$ 5 GeV e^- beam at DESY. Preliminary values of the detection efficiency of sensors exposed to various values of the fluence.

it is foreseen to also test the sensors providing a digital output. In this case, the noise before irradiation is slightly larger (12 - 15 e^- ENC). The study needs therefore to show up to which fluence the SNR is still high enough, for various operating temperatures.

4.2.3 Summary on the radiation tolerance

The radiation tolerance studies performed in the last two years have established quite reliably that CMOS sensors can stand the ionising and non-ionising radiation doses to which the vertex detector is going to be exposed at the ILC, even if these doses come out to be much higher than the present Monte-Carlo predictions. In this latter case however, it may be necessary to cool the sensors slightly.

The sensitivity of the sensors may strongly depend on details of the fabrication process. Each of them needs therefore to be carefuly evaluated in terms of tolerance to bulk damage and ionising radiation effects. It is also of interest to continue investigating the role of temperature (and time) in recovery procedures.

4.3 Sensors with integrated fast read-out architecture

The rate of beamstrahlung electrons will determine the occupancy in all layers of the vertex detector, with particularly demanding constraints on the two inner ones [4]. Some azimuthal sectors in the other layers may also be exposed at high rates due to electrons backscattered from final focus components.

In order to cope with the high rate expected in the two inner layers, the ambitionned frame read-out time was set to 25 (respectively 50) μs in the inner most (respectively second) layer. These target values, which are more ambitious than those indicated in the TESLA TDR, should allow for nominal impact parameter resolution even if the background rates come out to be a factor of 3 to 5 above the value derived from present Monte-Carlo simulations (i.e. up to 15 or

20 $e^{\pm}/cm^2/BX$).

In ordre to achieve the short read-out times ambitionned, the sensors are subdivided into columns of pixels read out in parallel. Inside each column, the pixels are read out sequentially. The pixel read-out frequency foreseen is 10 MHz (typically 16 clock cycles at 160 MHz inside each pixel). The two inner most layers would host sensors with columns made of $\gtrsim 256$ and 512 pixels, translating into read-out times of ~ 26 and 51 μs respectively.

The development of the sensors is based on three work packages addressed in parallel, and sharing the analog, mixed and digital parts of the sensors:

- WP-1: development of a fast, column parallel, architecture, which encompasses the sensing elements, the analog micro-circuits integrated in the pixel and at the column end, as well as the discriminating logic ending each column;
- WP-2: development of a 4-5 bit ADC foreseen to be integrated at the end of each column (replacing the discriminator developed in WP-1);
- WP-3: development of sparsification micro-circuits to be integrated on the chip periphery, and complemented with output memories.

4.3.1 WP-1: Development of a fast column parallel architecture

A – The MIMOSA-8 prototype

a) Main features of the sensor: The R&D effort addressing the read-out speed and the related integrated data flow reduction micro-circuits has already generated two successful prototype pixel arryas delivering discriminated signals.

MIMOSA-8 is the first of these prototypes. Fabricated in TSMC-0.25μm technology, it features 32 columns of 128 pixels (25 μm pitch) read out in parallel. 24 columns are equipped with an integrated discriminator, while the remaining 8 columns deliver an analog output (for test purposes). Pedestal subtraction is performed before discriminating the signals with the help of correlated-double-sampling (CDS) micro-circuits integrated in each pixel, complemented with double sampling (Fixed Pattern Noise subtraction) at the end of each column [9]. Some main features of this prototype are summarised in Table 2.

Fabrication technology	TSMC-0.25
Thickness of epitaxial layer:	$\lesssim 7$ μm
Nb of columns:	32, out of which 24 equipped with discriminator
Nb of pixels per column:	128 (= number of rows)
Pixel pitch:	25 μm
Nb of sub-arrays:	4 (32 rows each)
Specificity of sub-array 1:	sensing diode of 1.2x1.2 μm^2, clamping architecture
Specificity of sub-array 2:	sensing diode of 1.7x1.7 μm^2, clamping architecture
Specificity of sub-array 3:	sensing diode of 2.4x2.4 μm^2, clamping architecture
Specificity of sub-array 4:	alternative amplification architecture
Read-out clock frequency:	nominal value 100 MHz
Row read-out frequency:	nominal value ~ 6 MHz

Table 2: Prominent features of the MIMOSA-8 sensor.

b) Laboratory tests results: Several sensors were tested and calibrated with an ^{55}Fe source. Besides determining the charge-to-voltage conversion gain, a major goal of these tests consisted in assessing the operation of the 24 integrated discriminators. This was performed by looking at the sensor outputs while varying the discriminator thresholds. This test was repeated with and without illuminating the sensor. The results are shown in figure 10.

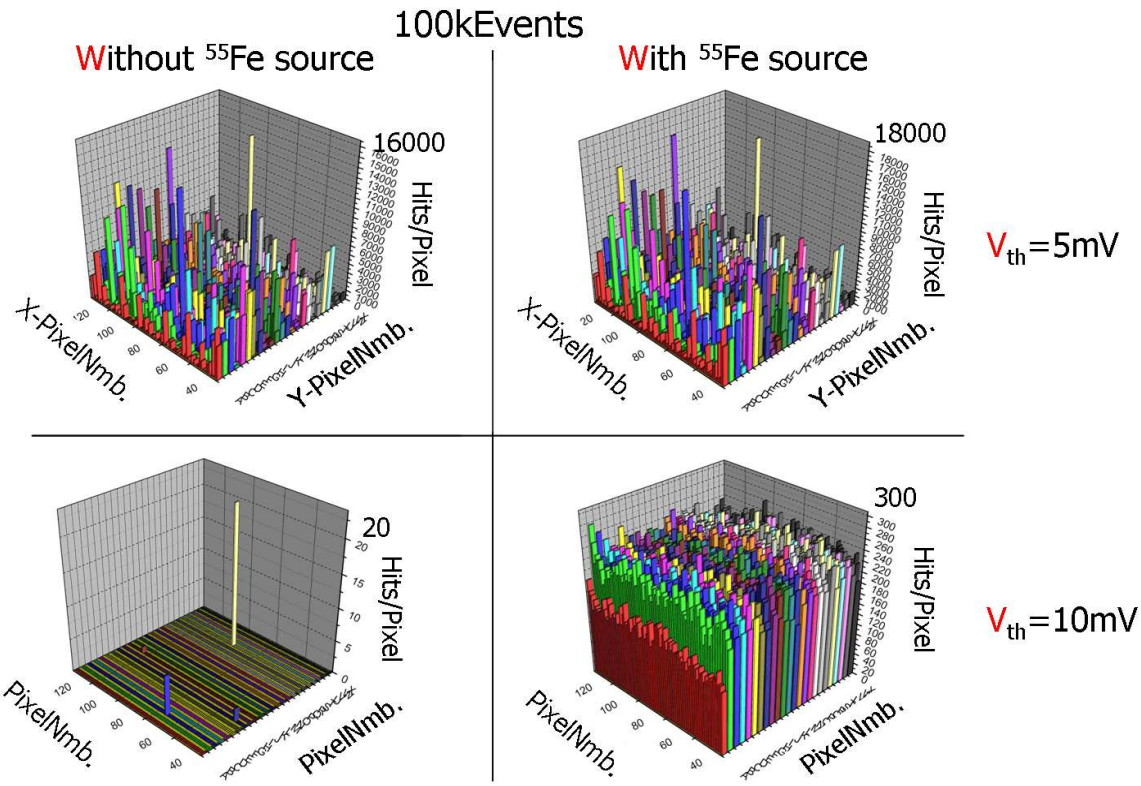


Figure 10: MIMOSA-8 tests with ^{55}Fe source: variation of the number of pixels passing the discriminator threshold over the array of 24 columns (each made of 128 pixels), for two different values of the discriminator threshold voltage (top: 5 mV ; bottom: 10 mV). Figures on the left hand side were obtained without illuminating the sensor, while those on the right show how the sensor behaves when being illuminated.

One observes that all pixels fire when the discriminator threshold is set to 5 mV, whether illuminated with the source or not. Once the threshold is ramped up to 10 mV, very few, isolated, (i.e. noisy) pixels still pass the threshold in absence of the source, while all pixels continue firing when the source illuminates the sensor. The chip is thus working as expected. Moreover, the uniformity of the 24 thresholds was evaluated. It corresponds to less than 1 mV noise, and affects therefore only marginally the signal discrimination, which is typically set at a few millivolts.

c) Beam tests results: Next, some sensors were mounted on the beam telescope made of 4 pairs of Si-strip detectors already mentioned in this report, and installed on a ~ 5 GeV e^- beam at DESY. The operation of the sensor on beam could only be verified up to a row read-out frequency $\gtrsim 2.5$ MHz (i.e. about a quarter of the target value) because of data acquisition

limitations.

The noise of the signal after CDS was measured to be less than 15 e^-ENC. The detection efficiency derived from the discriminated data collected with the telescope amounts to 99.3 $\pm$ 0.1 % for an average discriminator threshold equivalent to slightly more than 3 times the noise. The corresponding fake hit rate was found to be $\sim 10^{-3}$ only (see figure 11). This achievement can be considered as a breakthrough, especially whith regard to the relatively thin epitaxial layer ($< 7\ \mu m$) inherent to the TSMC-0.25 technology.

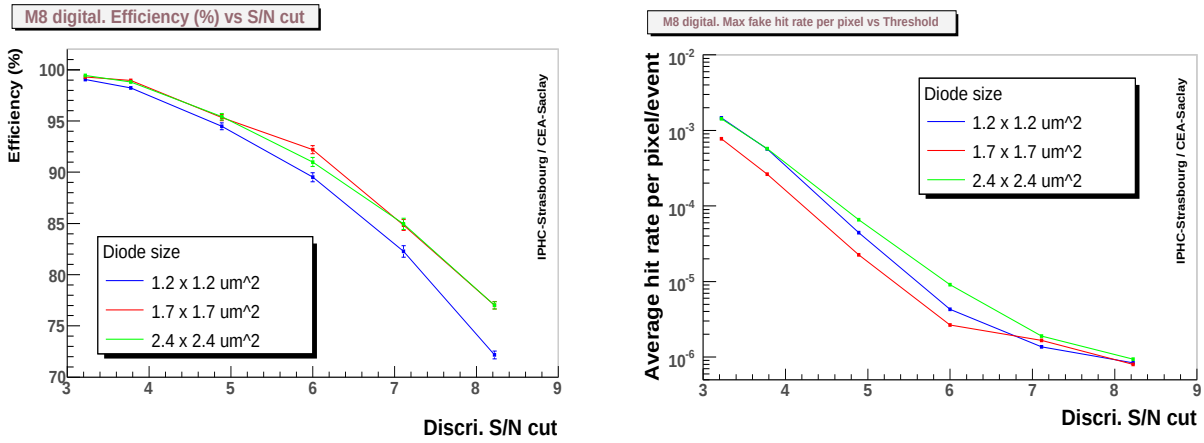


Figure 11: MIMOSA-8 beam tests ($\sim$ 5 GeV electrons): detection efficiency (left) and fake hit rate (right) as a function of the discriminator threshold, expressed in terms of SNR, for 3 different sensing diode sizes (1.2x1.2, 1.7x1.7, 2.4x2.4 μm^2). The row read-out frequency is 2.5 MHz (equivalent to a clock frequency of 40 MHz).

The single point resolution of the sensor was evaluated in Summer 2006 at the CERN-SPS, with the Si-strip beam telescope mentionned above. A resolution of $\sim$ 7 - 8 μm was found, i.e. about the intrinsic resolution ($\sim$ 7.2 μm) reflecting the pixel pitch (25 μm). This result indicates that the replacement of the discriminators with ADCs featuring very few bits will be sufficient to satisfy the requirements of the ILC vertex detector (typically $\lesssim 3\ \mu m$ single point resolution in the inner most layer), keeping in mind that the pixel pitch will also be slightly reduced, to $\sim$ 20 μm.

Overall, these tests demonstrate that the chip architecture performs very well and can be extended by replacing each discriminator with a 4-5 bits ADC. On the other hand, the chip should be manufactured in a technology offering a thicker epitaxial layer, in order to ensure a higher SNR. The AMS 0.35 OPTO technology was the natural candidate, based on th test results of MIMOSA-9, -11 and -14 (see section 3).

B – Translation of MIMOSA-8 pixels in AMS-0.35: MIMOSA-15 The first step consisted in translating the MIMOSA-8 pixels with integrated CDS (but not yet its columns ended with discriminators) from the TSMC to the AMS technology in order to investigate potential differences in the manufacturing parameters, such as those influencing the residual noise.

The study was performed with the pixels of sub-arrays 2 and 3. The prototype, called MIMOSA-15, was fabricated in Summer 2005 and consecutively tested with an ^{55}Fe source. The

observed noise was close to 10 e^-ENC, showing that the pixel design was translated successfuly.

The only unexpected result concerned the charge collection efficiency (CCE), which came out to be extremely poor with the smallest diodes (i.e. 1.7x1.7μm^2) and was still rather modest for the larger (2.4x2.4 μm^2) ones. In this case the CCE was actually found to be $\sim$ 10 % in the seed pixel (while $\gtrsim$ 20 % were expected) and the 3x3 clusters centered on the seed pixel collected only $\sim$ 30 % of the cluster charge (while $\gtrsim$ 70 % were expected).

This is to be compared to the previous sensors (MIMOSA-9, -11, -14) fabricated in the same technology, which did not exhibit a particularly low CCE. Since the sensing diodes integrated in these prototypes were typically 3.4x4.3 μm^2 large, there is a strong suspicion that the P+ doping in the neighbourhood of the sensing N-well diffuses towards the latter and may screen partly the contact surface between the N-well and the P- epitaxial layer. Since the CCE is strongly depending on this surface, small diodes may be much affected by this effect, which may only marginally modify the CCE of larger sensing diodes.

C – Translation of the full MIMOSA-8 sensor in AMS-0.35: MIMOSA-16

a) Main features of the sensor: The translation of the complete MIMOSA-8 design in the AMS-0.35 OPTO technology was achieved in 2006. Some of the main features of this new prototype, called MIMOSA-16, are listed in Table 3. Three modifications were introduced w.r.t. MIMOSA-8:

- the smallest sensing diode (1.2x1.2 μm^2) was abandonned;
- the pixels of the sub-array composed of 2.4x2.4 μm^2 sensing diodes were modified in order to improve their tolerance to ionising radiation;
- the architecture of sub-array 4 was replaced by a new one, featuring 4.5x4.5 μm^2 sensing diodes and a new amplification design.

Fabrication technology:	AMS-0.35 OPTO
Thickness of epitaxial layer:	$\sim$ 11 μm ("14 μm" option) or $\gtrsim$ 15 μm ("20 μm" option)
Nb of columns:	32, out of which 24 equipped with discriminator
Nb of pixels per column:	128 (= number of rows)
Pixel pitch:	25 μm
Nb of sub-arrays:	4 (32 rows each)
Specificity of sub-array 1:	1.7x1.7 μm^2 sensing diode, clamping architecture
Specificity of sub-array 2:	2.4x2.4 μm^2 sensing diode, clamping architecture
Specificity of sub-array 3:	like sub-array 2 but with radiation tolerant sensing diode
Specificity of sub-array 4:	4.5x4.5 μm^2 sensing diode, alternative amplification architecture
Read-out clock frequency:	nominal value 100 MHz
Row read-out frequency:	nominal value $\sim$ 6 MHz

Table 3: Prominent features of the MIMOSA-16 sensor.

Figure 12 displays the layout of the sensor, with a zoom on the column bottoms hosting the 24 integrated discriminators.

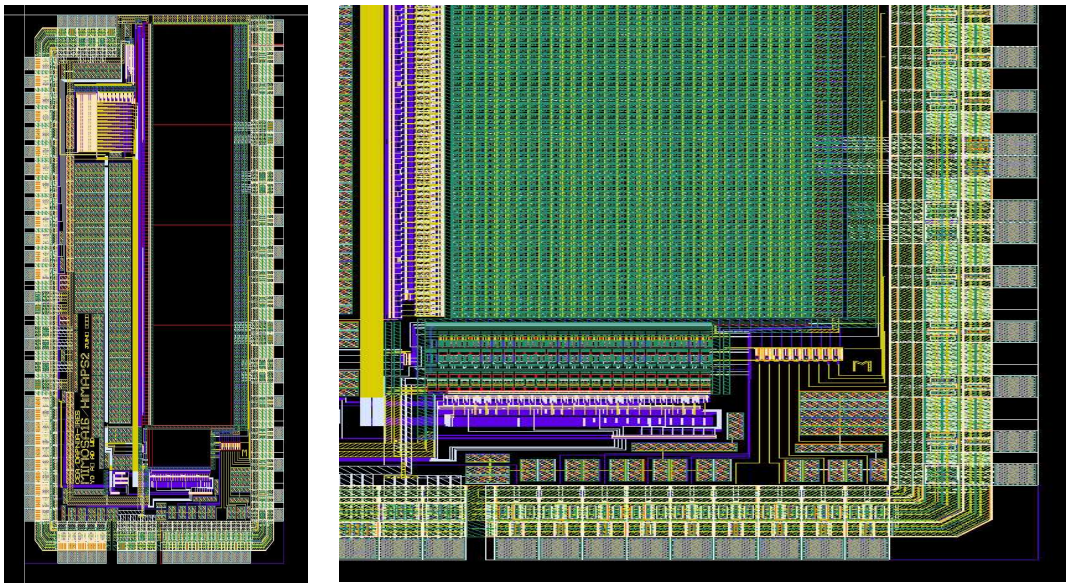


Figure 12: **Left:** Layout of MIMOSA-16 showing the 32 parallel columns, out of which 24 are ended with a comparator, while the other 8 provide an analog output. **Right:** Zoom on the column ends where the 24 discriminators are integrated.

b) Laboratory tests results: The tests of the sensors fabricated with the so-called "20 μm" option started by the end of 2006. They were performed with an ^{55}Fe source, using the signals of the 8 columns with analog output.

Several parameters were measured as a function of the read-out clock frequency, which was varied from 1 to 150 MHz. The tests were first performed with the sensors fabricated with the "20 μm" epitaxy option. Figure 13 displays the pixel noise, the fixed pattern noise, the pedestal averaged over the columns and the charge collection efficiency (CCE) as a function of the frequency. The CCE is obtained by dividing the total charge collected in a cluster made of 3x3 pixels by the charge accumulated in a single pixel when a 5.9 keV X-Ray hits its depleted volume (it corresponds then to $\sim$ 1640 electrons).

One observes that the pixel noise (top-left) lies within the range expected up to the highest clock frequency values [6]. The fixed pattern noise (top-right) adds very little to the pixel noise, as required. The mean pedestal of the columns (bottom-left) does not exhibit any significant feature as a function of the frequency. The situation is less satisfactory as far as the CCE is concerned (bottom-right). It amounts to less than 10 % for sub-array 1 and less than 30 % for sub-arrays 2 and 3. Its value is only acceptable for sub-array 4.

More recent measurements, performed with sensors featuring a "14 μm" epitaxial layer, exhibit a CCE drop which is less pronounced than with the "20 μm" epitaxy. More about this feature may be found in [3].

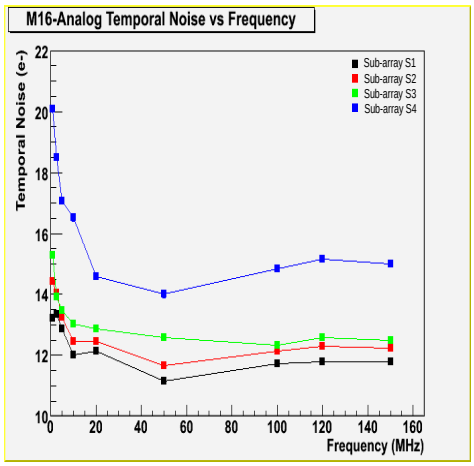
Overall, the conclusion of these measurements is that the next steps of the R&D should be based on the "14 μm" epitaxy rather than the "20 μm" option. Moreover, the dimensions of the sensing diode should be at least $\sim$ 3x3 μm^2.

[6] The raise at low frequency reflects the usual domination of leakage current induced noise consecutive to long integration times.

Temporal noise vs Frequency

Chip#0 (old mezzanine board)

Columns 28-31

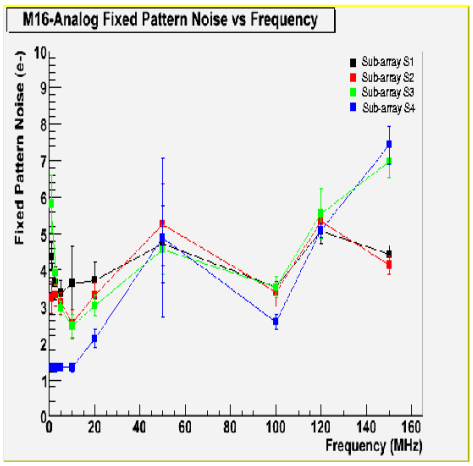


08/01/07 Résumé résultats Mimosa-16 chip#0 2

FPN (dispersion of pedestal) vs Frequency

Chip#0 (old mezzanine board)

Columns 28-31

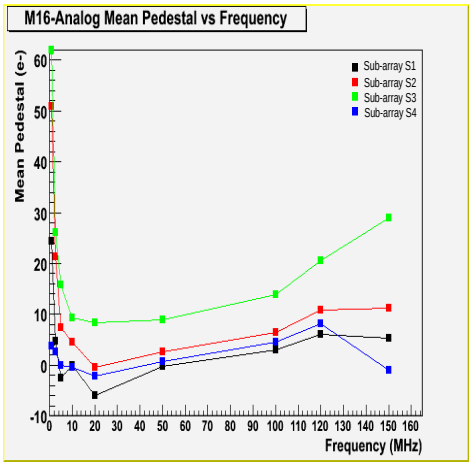


08/01/07 Résumé résultats Mimosa-16 chip#0 1

Pedestal Mean vs Frequency

Chip#0 (old mezzanine board)

Columns 28-31

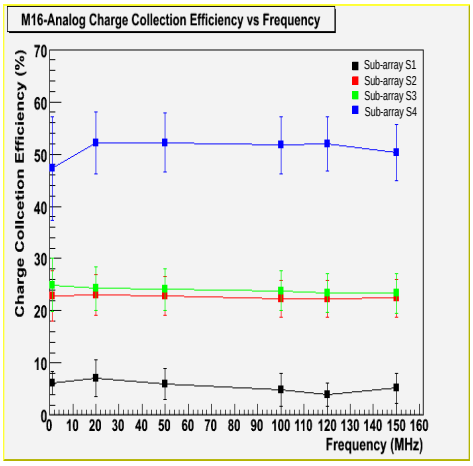


08/01/07 Résumé résultats Mimosa-16 chip#0 3

Charge Collection Efficiency vs Frequency

Chip#0 (old mezzanine board)

Columns 28-31



08/01/07 Résumé résultats Mimosa-16 chip#0 4

Figure 13: MIMOSA-16 analog output measurements with a ^{55}Fe source, displayed as a function of the read-out clock frequency: pixel noise (top-left), fixed pattern noise (top-right), mean pesdestal (bottom-left) and charge collection efficiency (bottom-right). The sensors were manufactured with the "20 μm" epitaxy option of the AMS-0.35 OPTO process.

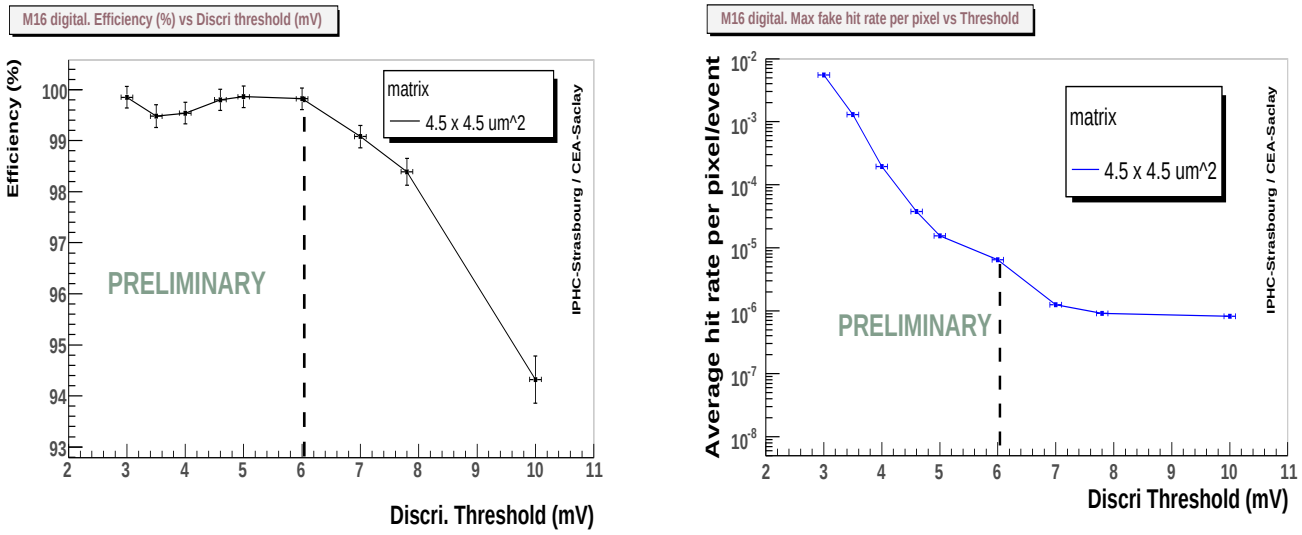


Figure 14: MIMOSA-16 digital output **preliminary** beam test results from data collected in Septembre 2007 at the CERN-SPS ($\sim$ 180 GeV particle beam). The detection efficiency (left) and the fake hit rate (right) are displayed for sub-array S4 (4.5x4.5 μm^2 diode) as a function of the discriminator threshold value. The full line is supposed to guide the eye. The vertical dashed line indicates a typical threshold value for running the sensor.

c) Beam test results:

Several sensors were mounted on the usual Si-strip beam telescope and installed in Septembre 2007 on a 180 GeV charged particle beam delivered by the CERN-SPS.

Some preliminary test results are displayed in figure 14. The latter shows the detection efficiency (left) and the fake hit rate (right) as a function of the discriminator threshold values. The data were collected at a coolant temperature of 20 °C with a row read-out frequency of 2.5 MHz (i.e. 40 MHz clock frequency), which translates into a frame read-out time of 51 μs. The results shown are restricted to one of the four sub-arrays (i.e. S4) and are still exposed to biasses reflecting the early stage of the alignement.

At present, the main message of the study is that the detection efficiency is very close to 100 %, even for a high value of the discriminator thresholds. For instance, a threshold of 6 mV (dashed line on figure 14) translates into a detection efficiency of 99.80 $\pm$ 0.08 (stat) $\pm$ 0.20 (prelim) %, where the second uncertainty reflects the preliminary stage of the analysis. The corresponding fake rate is below 10^{-5}.

The single point resolution is also being evaluated. The preliminary outcome of the analysis is that, due to the high SNR, the single resolution amounts to $\sim$ 5 – 6 μm, i.e. significantly better the binary resolution associated to the 25 μm pitch of the pixels.

4.3.2 WP-2: Development of fast, low granularity, ADCs

To achieve the required resolution on the impact parameter, the pixels of the inner most layer should provide a single point resolution of $\lesssim$ 3 μm. Charge sharing among the CMOS pixels belonging to the same cluster provides a powerful tool to derive a single point resolution much

better the digital value associated to the pixel pitch, as already mentioned in section 3.3. Equipping the sensors with ADCs featuring at least 3 (real) bits looks therefore sufficient to provide a resolution close to 2 μm. Accounting for the ADC noise in a conservative way, it was decided to develop 4-bit ADCs to be integrated at the end of each column of the sensor. The overload due to 5-bit ADCs was also assessed.

The developement strategy consists in developing the ADCs independently of the sensors until they are mature enough to replace the discriminators equipping presently the column ends.

Since the ADCs needed for the sensors are very unsual, their design could not be derived from existing - similar - devices. The design requires finding a compromise between a minimal number of (real) bits, an unfriendly aspect ratio ($\sim$ 20x500-1000 μm^2), a high clock frequency (10 MHz) and very limited power dissipation ($\lesssim$ 500 μW). It should allow discriminating those pixels which deliver a signal above a given threshold. In order to maximise the chances to achieve a well performing ADC within reasonable time, the developement was started in 2005 in 4 different laboratories (Clermont-Ferrand, Grenoble, Saclay and Strasbourg), which explored the potential of different ADC architectures: flash, pipe-line, successive approximations (SAR) and Wilkinson.

These different architectures differ mostly in terms of speed versus power dissipation. For instance, a flash or a pipe-line ADC is fast enough to process signals coming from two neighbour columns. Flash ADCs have the tendency to be power consuming, while Wilkinson ADCs consume much less. On the other hand, the latter, just as SAR ADCs, tend to be slow. The architectures developed in each laboratory are summarised below:

- LPSC (Grenoble): amplifier + semi-flash (pipe-line) 5- and 4-bit ADC for a pair of columns (width: 40 μm instead of 20 μm; frequency: 25 MHz instead of 10 MHz);
- LPCC (Clermont): flash 4+1.5-bit ADC for a pair of columns
- DAPNIA (Saclay): amplifier + SAR (4- and) 5-bit ADC
- IPHC (Strasbourg): SAR 4-bit and Wilkinson 4-bit ADCs

The status of each developement is summarised in table 4.3.2.

Lab	proto.	phase	bits	chan.	$F_{r.o.}$(MHz)	dim. (μm^2)	P_{diss} (μW)	eff. bits	Problems
LPSC	ADC1	tested	5	8	15-25	43x1500	1700	4	Offset & N
	ADC2	testing	4	8	25	40x943	800		
	ADC3	fab	4	> 8	25				
LPCC	ADC1	tested	5.5	1	5(T)–10(S)	230x400	20 000	2.5	P_{diss} & bits
	ADC2	testing	5.5	1	10	40x1100	1000		
DAPNIA	ADC1	tested	5	4	4	25x1000	300	$\gtrsim 2$	Missing bits
	ADC2	tested	5	4	4	25x1000	300		
IPHC	ADC1	testing	4	16	10	25x1385	660		
	ADC2	testing	4	16	10	25x1540	545		

Table 4: Summary of the characteristics and status of the different ADCs developed to equip the column ends of MIMOSA sensors. The parameters displayed include the number of bits, the number of channels, the power dissipation per channel, the clock frequency, the effective number of bits and the type of problem encountered during tests.

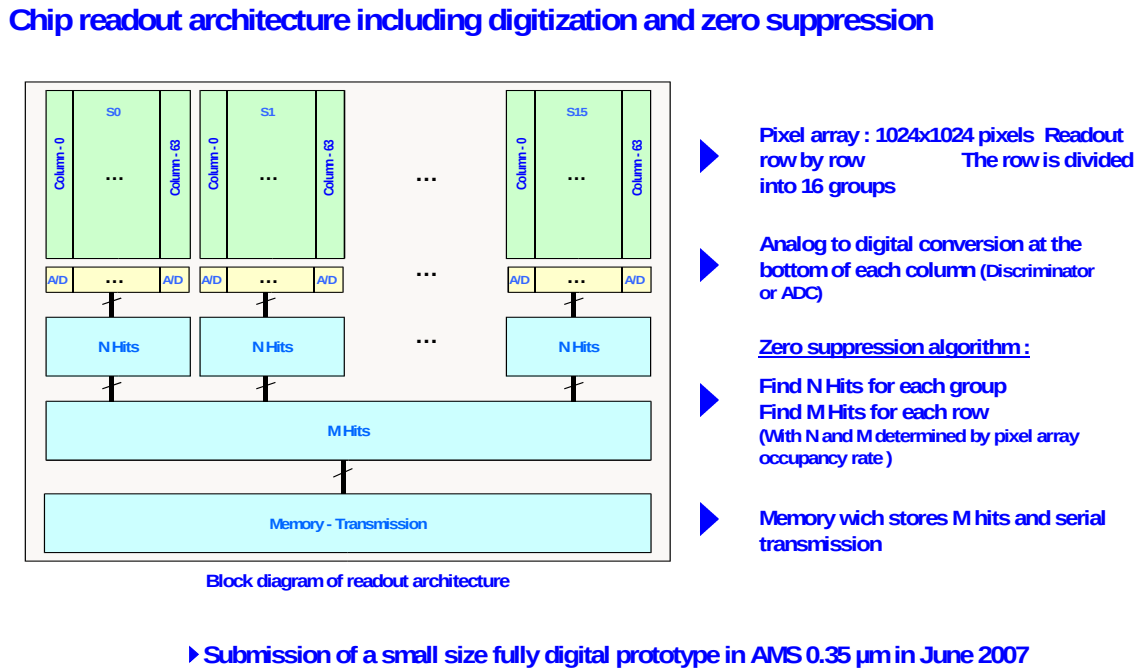


Figure 15: Block diagramme of the zero suppressing SUZE chip.

The most advanced design is the one of the semi-flash/pipe-line ADC developed at LPSC (Grenoble). It is close to match the most demanding requirements: 10 MHz clock frequency per column (twice as much for two columns), $\lesssim 500\ \mu W$ power dissipation per column, dimensions of 20 x 500-1000 μm^2 per column. This architecture is expected to translate into a first mature design before Summer 2008. It may then be integrated in a sensor (see section 6).

4.3.3 WP-3: Development of data compression micro-circuits

The drawback of developing fast sensors adapted to the running conditions close to the interaction point is the high genuine data flow one has to cope with. The read-out rate of the vertex detector generates a raw data flow in the order of 100 Gbits per cm^2 of sensor. It is therefore mandatory to implement signal filtering functionnalities as close as possible to the sensitive area. CMOS sensors are particularly well suited to this type of requirement, as they allow to integrate the necessary sparsification micro-circuits on the sensor itself.

The design of a zero suppression micro-circuit has only started in 2007. The first prototype (called SUZE-01) is based on a logic adapted to less demanding requirements than those of the ILC vertex detector. It actually fits to those of the beam telescope developed for the E.U. F.P.6 programme EUDET, as well as to those of the Heavy Flavour Tagger (HFT) of the STAR experiment at RHIC (BNL).

The block diagramme of the zero suppression architecture is displayed on figure 15. Its logic consists in filtering pixels which deliver a signal charge above the threshold set in the

discriminators. For those selected pixels, it memorises the address of the pixel and transmits it to output memories.

The filtering logic is applied in two steps. The first step addresses groups of 64 columns. Inside each group, the logic scans the row currently being read out, relying on a *token ring* provided by those discriminators where the threshold was passed by a signal. The corresponding pixel gets then flagged with its address inside the row (typically 10 bits), and the number of adjacent pixels with signal above threshold is counted. Up to 4 adjacent pixels can be flagged in this way (on 2 bits). The logic thus provides series of 12-bit words, where the first 10 contain the address of the first pixel of a series, and the 2 remaining bits tell how many adjacent pixels delivered a signal above threshold. This is to minimise the size of the information transmitted, accounting for the fact that the signal is configurated in clusters of several pixels. The logic accepts up to 6 series of pixels inside each group of 64 columns.

The second step of the logic, which treats globally the outputs of all groups of columns, combines the information at the edges of contiguous groups, and keeps up to 9 series of adjacent pixels for the full row. This information is then written in memories, which will consecutively be read out from the external logic steering the detector.

The chip has been submitted for fabrication by the end of July 2007. Its performances should be well suited to the EUDET telescope and STAR-HFT requirements, but not yet to the ILC ones, which are more demanding. Its test results, late in 2007, will settle the ground for an architecture suite to the ILC running conditions, which may be investigated in 2008.

5 Detector design studies

The detector concept taking best advantage of the CMOS sensor peculiarities in order to provide the required performances, is likely to rely on a geometry similar to the one described in the TESLA TDR (based on CCDs). It consists of 5 cylindrical layers with radii ranging from 15 to 60 mm. Depending on the layer, the polar angle coverage extends to $|\cos\theta| \sim 0.90 - 0.95$.

5.1 Geometry and read-out considerations

Some of the prominent characteristics of the detector are summarised in Table 5.

An overview of the detector geometry is shown in Fig. 5.1. Sketch views including or perpendicular to the beam axes are shown in Fig. 17.

Some main differences with the TESLA TDR geometry are:

- a faster read-out (and thus a larger number of ladders equipping the inner layers),
- a variable pixel pitch (and therefore a smaller total number of pixels: 330 millions instead of 800 millions), translating into a reduced data flux and power dissipation,
- less material at small polar angle,
- the absence of a cryostat (room temperature operation).

The number of ladders in the 2 inner layers follows from the ambitionned read-out speed and granularity (i.e. pixel pitch), the ladder width being dictated by the number of pixels per column. This is illustrated on Fig. 18, which displays a sketch view of a ladder from the inner most layer.

It is (at least) 100 mm long. Its width amounts typically to 7 mm, out of which 5 mm are equipped with 20 μm pitch pixels, while 2 mm are reserved for the mixed and digital parts of

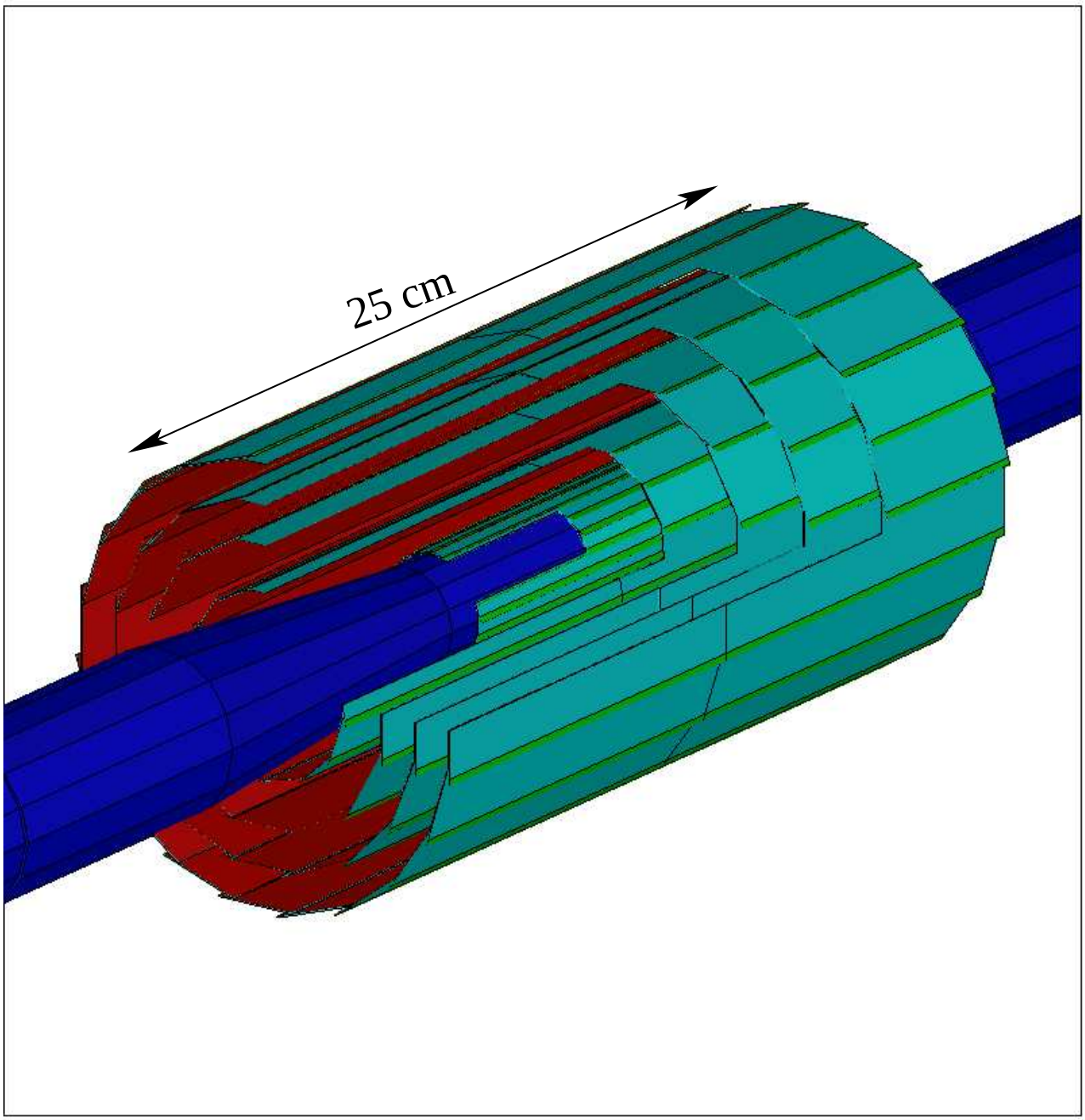


Figure 16: Overview of the detector geometry.

Layer	**Radius**	**Pitch**	$\mathbf{t}_{r.o.}$	$\mathbf{W}_{lad}$	$\mathbf{N}_{lad}$	$\mathbf{N}_{pix}$	$\mathbf{P}_{diss}^{inst}$	$\mathbf{P}_{diss}^{mean}$
L0	15 mm	20 μm	25 μs	7 mm	20	25 M	<100 W	<5 W
L1	25 mm	25 μm	50 μs	15 mm	26	65 M	<130 W	<7 W
L2	37 mm	33 μm	$\sim$ 100 μs	24 mm	24	50 M	<90 W	<5 W
L3	48 mm	33 μm	$\sim$ 100 μs	24 mm	32	80 M	<120 W	<6 W
L4	60 mm	33 μm	$\sim$ 100 μs	24 mm	40	100 M	<150 W	<8 W
Total					142	330 M	<600 W	<30 W

Table 5: Prominent features of the detector concept based on CMOS sensors. For each layer, the table indicates the layer radius, the pixel pitch, the read-out time ($t_{r.o.}$), the ladder width (W_{lad}) and number (N_{lad}), the number of pixels (N_{pix}), as well as the instantaneous (P_{diss}^{inst}) and average (P_{diss}^{mean}) power dissipations. The average dissipation is based on a detector duty cycle of 5 %. The usually assumed duty cycle of 1/200 would lead to a 10 times smaller value.

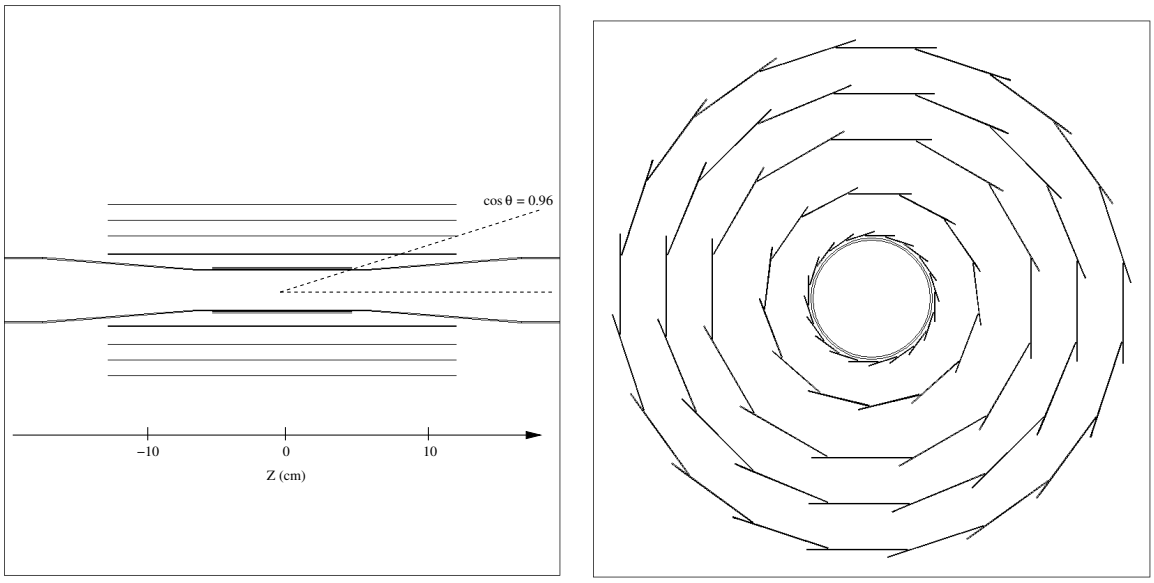
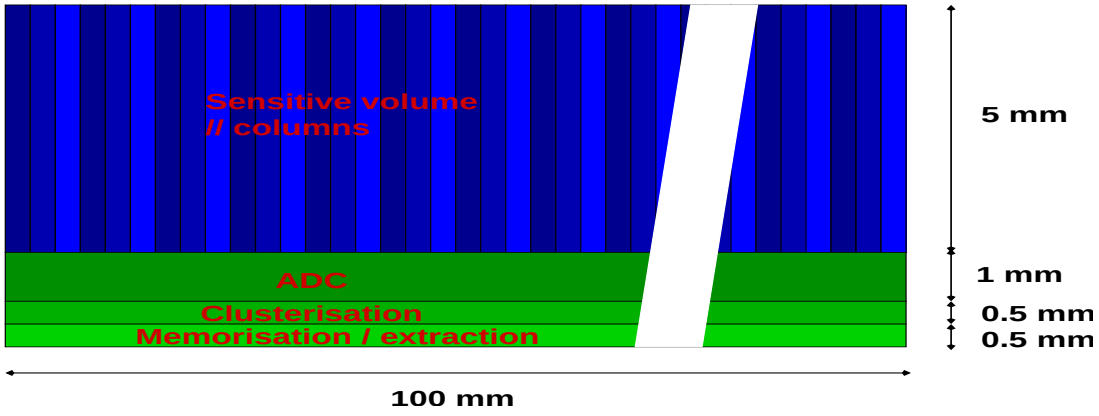


Figure 17: Side views of the detector geometry including the beam axes (left) and transverse to them (right).



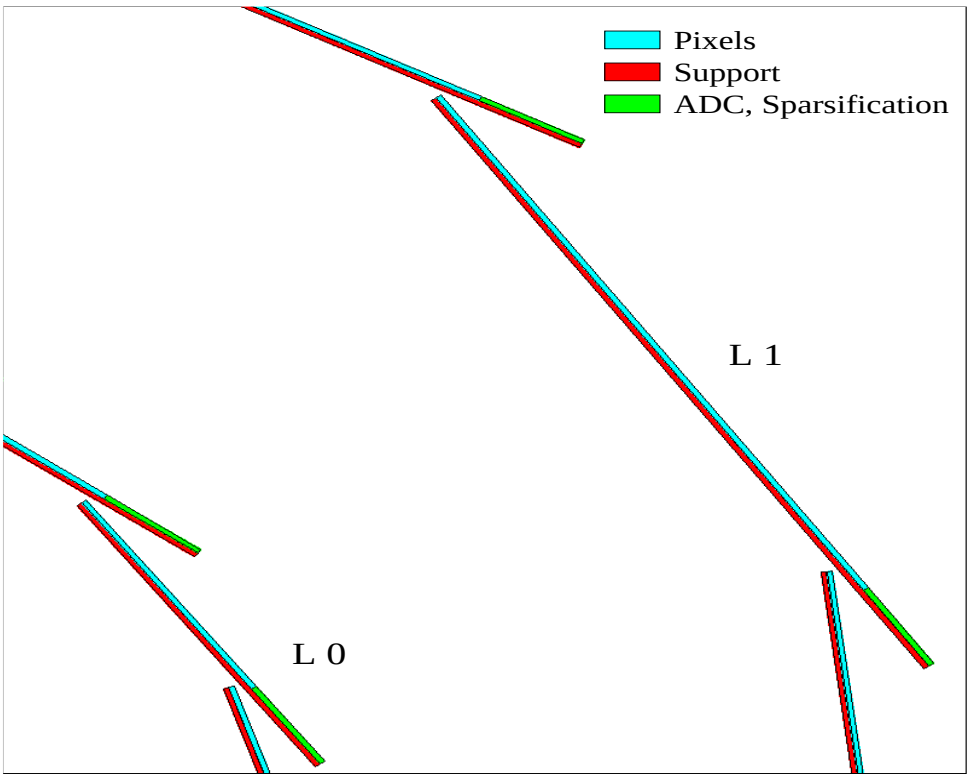


Figure 18: Top: Sketch view of a ladder equipping the inner most layer. Bottom: zoom on a section of the two inner layers, distinguishing the support (red), the part of the sensors made of pixels (blue) and the side band reserved to mixed and digital electronics (green).

the signal processing micro-circuits. The pixels are grouped in columns of 256 units, oriented perpendicular to the beam lines and read out in parallel at an effective clock frequency of $\sim$ 10 MHz, which translates into a column read-out time of $\sim$ 25 μs. While all functionalities of the signal processing chain up to the CDS are integrated in the pixels, the analog-to-digital conversion, data sparsification and signal transfer electronics are integrated in the 2 mm wide side band.

The second layer is equipped with pairs of 125 mm long ladders, stitched near the vertical to the interaction point. The ladder width amounts to 15 mm, shared between $\sim$ 13 mm long columns, perpendicular to the beam lines, and a 2 mm wide side band hosting the mixed and digital electronics. The columns are made of 512 pixels of 25 μm pitch. They are read out in parallel with an effective pixel read-out frequency of $\sim$ 10 MHz, which translates into a ladder read-out time close to 50 μs.

The 3 other layers are also composed of pairs of 125 mm long ladders. They are $\sim$ 24 mm wide ($\sim$ reticle width). Each column is made of 640 pixels with 33 μm pitch. In ordre to squeeze the power consumption, the sensors are ran at $\sim$ 6 MHz read-out frequency (instead of 10 MHz for the inner layers), which still allows for a read-out time of $\sim$ 100 μs.

The choice of the pitch value in each layer is based on the measured single point resolution summarised in section 3.3 and relies on the studies, made with these data, demonstrating that a 4-bit ADC would allow to get $\sim$ 2 μm single point resolution with a 20 μm pitch.

Overall, the total surface of the detector is $\sim$ 3000 cm^2, covered by a total number of pixels of $\sim$ 300 millions (like the SLD vertex detector).

5.2 Comments on power dissipation

The total instantaneous power dissipated by each column is estimated to $\lesssim$ 1 mW, based on the fast sensor prototypes already fabricated. The sensor design is therefore optimised for a minimal number of columns in order to keep the power dissipated as low as possible. This pleads for the largest possible pixel pitch and for the longest possible columns (with the largest possible number of pixels per column). Increasing the pitch deteriorates the single point resolution and increasing the number of pixels per column slows down the read-out speed. The design studies show that an acceptable compromise can be found, which table 5 summarises in its present, still preliminary, version.

For the whole detector, the expected instantaneous power dissipation would amount to $\lesssim$ 600 W, a value which would still require substantial cooling. As for any of the technologies envisaged for the vertex detector, the crucial question arises on how well the beam time structure can be exploited to switch off (most of) the detector inbetween trains, or nearly so. It is usually assumed that the ILC duty cycle (expected to be close to the 1/200 proportion of the TESLA design) can be fully exploited. In this extreme case, the total average power dissipated would amount to $\lesssim$ 3 W. The possibility to switch on and off all sensors at the required frequency is however still among the tasks of the R&D programme which remain to be done. Moreover, the final beam time structure of the ILC, which doesn't need to be identical to the TESLA project one, is still to be defined. Meanwhile, a conservative approach was prefered for the present estimates, which assumes that the detector can be switched off (or nearly so) for at least 95 % of the time, an hypothesis which translates into an average dissipation of $\lesssim$ 30 W. This value is still considered as being compatible with a light cooling system.

Investigations of the possibility to switch on and off repeatidly a sensor have started with the MIMOSA-5 prototype, which features $\sim$ 1 million pixels covering $\sim$ 3 cm^2. This sensor was

fabricated several years ago and was not aimed to run at high frequency. It is therefore not at all optimised for such an exercise, but should nevertheless allow to spot fundamental difficulties in cycling a sensor at the relevant frequencies.

The measurements performed show that 1.2 ms after having turned on the power of the output buffers, the performance of the sensor has already come back to a stable behaviour. The consequence was a reduction of the total sensor power dissipation by a factor of 8, assuming a machine duty cycle of 1/200.

Future sensor designs will include power saving features which are expected to still allow improving the reduction factor above by an ordre of magnitude. It remains now to prove that the functionnalities of the sensors remain unaffected by the alternate switching mode, i.e. that no reprogramming of the sensors will be required within short periods.

5.3 Achievable impact parameter resolution

The resolution on the impact parametre achievable with the detecor geometry summarised in table 5 has been studied with several of its variants. Some of the most representative detector variants considered are liste below:

- **G1:** single point resolution varied from 2 μm in the inner most layer to 4 μm in the outer one, by steps of 0.5 μm per layer;
- **G2:** single point resolution varied from 2.5 μm in the inner most layer to 5 μm in the outer one, by steps of $\sim$ 0.6 μm per layer;
- **G3:** same as G2, but with double material budget: 0.2 % X_0/layer instead of 0.1 %;
- **G4:** single point resolution of 2.2 μm in the two inner layers and 3.3 μm in the outer ones.

The result of the study is summarised in table 6. The values shown are those obtained for the parameters a and b entering the usual expression of the impact parameter resolution[7]. They were fitted to the momentum resolution reconstructed for each scenario. Also shown are the values obtained with the geometry of the TESLA TDR and a single point resolution of 2.5 μm in each layer (made of 0.1 % X_0 equivalent material). This latter case is a reference to which the performances obtained with the CMOS sensor based geometry should be compared.

Scenario	S1	S2	S3	S4	TDR
a (μm)	2.89 $\pm$ 0.02	3.59 $\pm$ 0.02	3.62 $\pm$ 0.02	3.23 $\pm$ 0.02	3.40 $\pm$ 0.02
b (μm)	8.7 $\pm$ 0.1	8.8 $\pm$ 0.1	10.4 $\pm$ 0.1	8.7 $\pm$ 0.1	8.5 $\pm$ 0.1

Table 6: Values of the parameters a and b entering the expression of the impact parameter resolution, for various values of the pixel pitch (and two different layer thicknesses). The column called "TDR" stands for the TESLA TDR geometry with a constant single point resolution of 2.5 μm in each layer.

One observes that the resolutions obtained with the CMOS sensor based geometries compare very well with the reference one. Actually the study also showed that doubling the pitch in the outer layer increases the value of "a" only by about 5 % (scenario G2 compared to TDR).

As far as the material budget is concerned, considering 0.2 % X_0/layer instead of 0.1 % was motivated by the difference in challenge between the two target values. One observes that,

[7] $\sigma_{sp} = a \oplus b/(p \cdot sin^{3/2}\theta)$, with the following requirements: a < 5 μm and b < 10 μm.

even if the material budget happened to be 0.2 % X_0, the parameter "b" would not degrade dramatically, despite its increase by $\sim$ 20 % (assuming a 400 μm thick beryllium beam pipe). On the other hand, one should not allow for thicker layers.

The fact that the columns are oriented perpendicular to the beam lines allows to make them short enough to garantee a swift read-out of the layers most exposed to the beamstrahlung electrons, even if their rate happens to be significantly higher than predicted by present simulations. Since all signal processing functionalities cannot be integrated inside the pixels, the drawback is a narrow side band hosting integrated mixed and digital micro-circuits. This band, which is expected to be $\sim$ 2 mm wide, adds material inside the fiducial volume of the detector (see Fig. 18).

This situation is particular to the CMOS sensor based vertex detector. The alternative technological solutions (e.g. CCD, DEPFET) rely on columns parallel to the beam axes, making it significantly more difficult to achieve read-out times $\lesssim$ 50 μs. Moreover, the read-out electronics is concentrated at the ladder edges, where its material affects the very forward tracking in a narrow angular range.

The consequence of the material budget excess due to the 2 mm side band, specific to the design presented here, was estimated. The loss in resolution on the impact parameter derived from the study is modest: overall, the parameter b, entering the canonical expression of the impact parameter resolution ($\sigma_{IP} = a \oplus b/p \cdot sin^{3/2}\theta$), increases by $\sim$ 5-10 %, depending on assumptions made on the thickness of the sensors and of the mechanical support and cooling system. The effect is mild essentially because of two reasons: i) the material of the beam pipe (500 μm of beryllium, i.e. 0.14 % of the radiation length) governs the multiple scattering parameter b, ii) b grows essentially like the square root of the fraction of radiation length.

In comparison, the benefit in read-out time is rather significant. It can be illustrated by comparing the radii of the inner most layer which provide the same occupancy for two different read-out times: 50 and 25 μs. This study was performed and showed that shortening the read-out time from 50 of 25 μs allows to reduce the radius of the inner most layer by $\sim$ 15-20 %. Since b is proportional to this radius, it improves by the same amount.

6 Plans until 2009-2010

The next steps of the R&D will aim for real size sensors with digital output and integrated data compression logic. These are a 1x2 cm^2 pixel matrix with $\lesssim$ 100 μs read-out time for the EUDET telescope, and a 2x2 cm^2 sensor with $\lesssim$ 200 μs read-out time for the STAR HFT. Both sensors should be fabricated by 2009. They will however not incorporate ADCs because the required single point resolution ($\lesssim$ 5 - 8 μm) can be accommodated with a binary encoding of the charge (i.e. raw discriminator output). The pixel pitch adapted to these goals is 18.4 μm for EUDET and 30 μm for STAR.

These sensors will thus not yet integrate all the functionnalities needed for running at the ILC. They will however provide important milestones on the way to their achievement. Among the most significant obstacles these two sensors offer to overcome, there are several aspects of a fast running architecture over a large area, based on a large number of rows and columns (switches). Moreover, the sensors will be operated in real experimental conditions, which is expected to be very useful for this new technology. In particular, several issues related to system integration will be addressed within these projects.

6.1 Milestones until the final sensor

The milestones bridging the gap between the present most mature prototype (i.e. MIMOSA-16) and the final sensors for EUDET and STAR are summarised hereafter:

- Pixel design:
  - adapt the existing pixel architectures to a smaller pitch ($\sim 18\ \mu m$ instead of $25\ \mu m$);
  - optimise the sensing diode dimensions in ordre to obtain simultaneously sufficient CCE (which calls for a large diode) and sufficient gain (which calls for a small diode).
- Column read-out architecture:
  - adapt the existing discriminating logic to the smaller pitch;
  - integrate data compression micro-circuits and output memories.
- Row and pixel steering (consequence of a large active area):
  - adapt the pixel steering inside columns to the required read-out speed by reducing the capacitance loading due to the large number of switches inside each column;
  - adapt the row steering to their length (~ 2 cm).
- Sensor autonomy and testability:
  - integrate a programmable JTAG steering logic and bias DACs;
  - integrate the necessary DC voltage sources to emulate the column's output for independent mixed and digital logic testing (e.g. discriminators and zero suppression micro-circuits).

The R&D for the ILC requires some additionnal milestones, which reflect the more demanding requirements in terms of read-out speed, spatial resolution and the different time scale:

- replace the discriminators by ADCs at the column's ends;
- adapt the data compression logic to the higher data rate (for the inner layers mainly);
- adapt the pixel and column architectures to the pixel pitch of the inner layers ($\gtrsim 20\ \mu m$) and of the outer ones ($\gtrsim 30\ \mu m$);
- find and assess a fabrication process with a feature size $< 0.2\ \mu m$.

6.2 Chip fabrication schedule

The strategy followed to address the milestones listed in the previous section for EUDET and STAR relies essentially on two prototypes, called MIMOSA-22 and (provisionally) MIMOSA-22+. Their main features are summarised hereafter.

6.2.1 Main features of MIMOSA-22

The pitch retained for EUDET is $18.4\ \mu m$, in order to meet the spatial resolution requirements with binary charge encoding (i.e. no ADC) of the EUDET telescope.

MIMOSA-22 will address the question of adapting the architecture of MIMOSA-16 to the $18.4\ \mu m$ pitch. It will also deal with the optimisation of the sensing diode surface ($\sim$ 10–15 μm^2), and with the problem of steering long columns ($\gtrsim 1$ cm) at high speed. It will be composed of 128 columns with digital output and 8 columns with analog output (for test purposes). The number of rows will be 576 (i.e. 10.6 mm long columns). The active surface will be subdivided

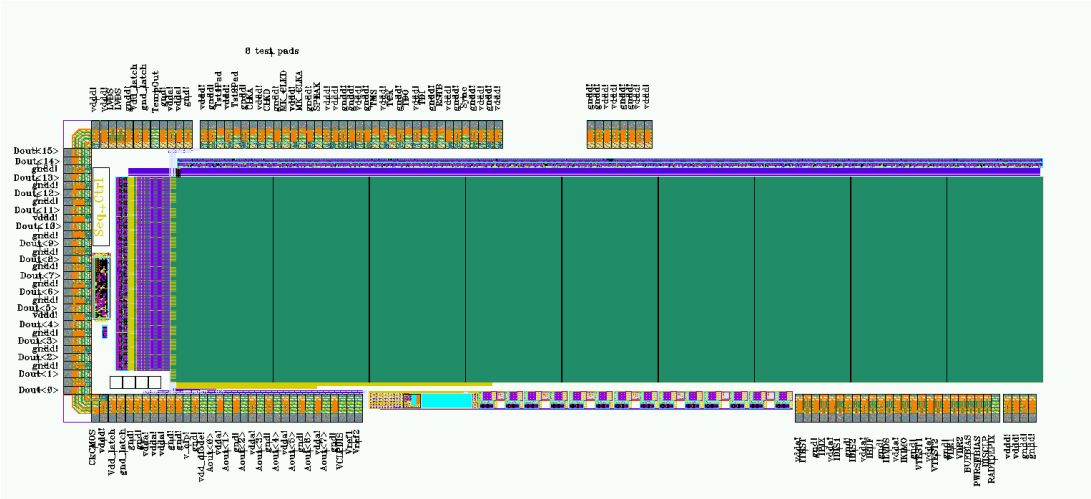


Figure 19: Layout of MIMOSA-22 showing the 136 parallel columns, out of which 128 are ended with a comparator, while the other 8 provide an analog output for test purposes. The active surface is subdivided in 9 sub-arrays of 64 rows, each featuring a slightly different pixel design.

in 9 sub-arrays of 64 rows, each featuring different pixels. The ambitionned read-out speed is the nominal value of $\sim 100\ \mu s$.

Figure 19 displays the - still not finalised - layout of the sensor. The design of the prototype is being completed and its submission date is fixed ot the 27th of Octobre 2007.

6.2.2 MIMOSA-22 extension for the STAR demonstrator: sensor PHASE-1

The first sensor, called PHASE-1, foreseen to equip the STAR HFT should allow to commission the detector. The corresponding sensors are therefore going to be fabricated by Summer 2008.

Their architecture is simialr to the MIMOSA-22 one. The pixel pitch will be 30 μm in ordre to minimise power dissipation. The sensor itself ($\sim$ 2 x2 cm^2 large) will be composed of 640 columns, each made of 640 pixels. The columns being read out in parallel at a row frequency of $\sim$ 5 MHz, the frame read-out time will be $\lesssim 150\ \mu s$.

6.2.3 MIMOSA-22+: the final EUDET sensor

The main motivation for MIMOSA-22+ is to complement MIMOSA-22 with the integrated zero suppression logic developed through the SUZE prototype (see section 4.3.3). It will therefore serve as final EUDET sensor. The 1x2 cm^2 array will host 1088 columns with digital output (i.e. 17 blocks of 64 columns). Based on the test results of MIMOSA-22 (and PHASE-1), the sensor will host the pixel architecture best suited to the EUDET running conditions. The side opposite to the digital outputs will host a compact micro-circuit allowing to investigate the analog part of the sensor in case of problematic pixels.

This final EUDET sensor will be fabricated by the end of 2008.

6.2.4 Additionnal prototyping for the ILC

While developing the sensors for EUDET and STAR, the ADC needed for the ILC will mature through additionnal tests and prototypes fabricated in 2007/2008. It is likely that the first ADC matching all requirements will be ready early in 2008. The data compression logic of the SUZE prototype will also be adapted to higher data flow with a new prototype (SUZE-02) in 2008.

The next step will consist in adapting MIMOSA-16 to the pitch of the inner most layer (20 – 22 μm) and in replacing the discriminators ending the columns with ADCs. The design of this prototype could be ready for fabrication by end of Spring 2008. In case of success, the development could carry on with a new prototype integrating the data compression logic of SUZE-02 and featuring the number of rows foreseen in the inner most layer (between 256 and 320) and at least 128 columns.

In this scenario, the final prototype could be fabricated by 2010. Meanwhile however, a new fabrication technology should come up, which would need some additionnal prototyping.

7 Integration issues

Since the developement of the sensors required all the available means, integration issues were not yet addressed intensely. Some studies were however performed, which are summarised hereafter.

7.1 Ladder mechanical support

The mechanical support needs to be adapted to the sensors having their outputs inside the fiducial volume, distributed along the ladder edge. This has major implications on the organisation of the sensor steering and read-out.

Since these questions have to be answered for the STAR HFT, the plan is to extend the research performed at LBNL for STAR. This activity is actually followed closely by the LBNL group involved in the ILC vertex detector (M.Battaglia et al.). At present the total material budget of an HFT ladder is $\lesssim 0.3$ % X_0, a value which does not look far from the $\lesssim 0.2$ % X_0 ambitionned at the ILC. The task needs however substantial experienced manpower to progress at the right speed, which is not identified yet.

More recently, the IPHC group has started a common project with a Fraunhofer institute and an industrial diamond fabricant, aiming to realise ladders made of an aluminised, $\lesssim 100$ μm thin, diamond support on which the sensors, thinned to ~ 50 μm, are mounted and connected. First results of these investigations, which will also involve the CBM collaboration, are expected by Summer 2008.

7.2 Sensor stitching

Another important question is whether the sensors should be provided in a stitched form, i.e. in slabs as long as the ladders, or whether they should be mounted individually. Though industrial stitching is available, it can only be envisaged if the sensor fabrication yield is well above 90 %. Since the present situation is far from this goal, the baseline approach consists in assuming that the sensors will be mounted individually on the ladders. Investigations have started in ordre to settle a dicing method which minimises the dead zones around the sensors consecutive to dicing. It appeared recently that a residual width of ~ 20 μm seem achievable via plasma dicing.

7.3 Data flow

A major concern is the handling of the data flow coming out from the sensors at the ladder level. Whether the flow will be manageable or not will depend on the actual beamstrahung hit rate. A study has shown that, for a hit rate of $\sim$ 3-4 times the Monte-Carlo prediction in the inner most layer, the rate would be $\sim$ 200 Bytes per row integrated over 25 μs. This requires an architecture able to handle 5 times $\sim$ 10 GBytes/s for each inner most ladder, which seems a real challenge. More effort is needed to study this issue, but manpower is missing to do the necessary investigations.

8 Summary

CMOS sensors of the MIMOSA series have now been developed for more than 8 years, accumulating convincing experience that this technology is indeed adequate for particle tracking. Excellent detection performances (SNR, detection efficiency, single point resolution) were obtained with numerous prototypes, mostly operated at room temperature. Moreover, the radiation tolerance of the sensors, though no yet fully assessed at room temperature, is also satisfactory for the running conditions at the ILC. This statement is likely to hold even if the beam background happens to be much larger than predicted by present Monte-carlo simulations. Finally, industrial thinning of the sensors to $\lesssim$ 50 μm has been validated at a degree where little doubt remains on its viability.

A large majority of these results were obtained with sensors featuring analog outputs, limited to frame read-out frequencies in the ordre of 1 kHz. They are thus not suited to the fast read-out required to cope with the occupancy induced by beam backgrounds. Most of the R&D effort is therefore invested in the achievement of a fast signal processing architecture integrated in the sensor, which introduces minimal material and power consumption. Prototyping of this architecture is already well advanced: the fast column parallel architecture with integrated CDS and signal discrimination is operationnal and is expected to lead to a real scale chip (1x2 cm^2) featuring integrated data sparsification by the end of 2008. It will equip 6 planes of the EUDET telescope. 2x2 cm^2 sensors providing discriminated outputs are also going to be fabricated for the STAR HFT in Summer 2008.

In ordre to adapt these first generation sensors to the ILC requirements, various fast and compact ADCs are being developed, with a first mature design expected in 2008. The read-out speed needed for the ILC vertex detector (inner layers) seems also achievable. Real scale sensors adapted to the ILC requirements are therefore expected to be fabricated by 2010, incorporating feed-back from the sensor operation in the EUDET telescope and the STAR HFT.

Based on the achieved performances and on the perspectives they allow, the design of a vertex detector taking best advantage of the CMOS sensor technology is being studied. It assumes that sensors are composed of pixels grouped in short columns perpendicular to the beam lines in ordre to maximise the frame read-out speed, and allows for a variable pixel pitch in ordre to minimise the power dissipated. With $\lesssim$ 330 million pixels distributed over 5 cylindrical layers, the expected performances can be summarised with the following benchmarks:

- impact parametre resolution corresponding to $a \sim$ 3.–3.5 μm and $b \sim$ 8.5–10.5 μm;
- frame read-out time: 25, 50 and 100 μs in the innermost, second and outer layers respectively;
- power dissipated: 3 - 30 W, depending on the power cycling performance.

Physics studies based on the Higgstrahlung process have started, which are expected to assess the physics potential associated to these performances and to guide further optimisation.

In summary, the R&D programme seems quite well advanced and progressing well. There are however still potential showstoppers until its completion. One of them is related to the (unpredictable) evolution of CMOS industry, and its consequences on fabrication parametres which influence the sensor detection performances or radiation tolerance. Other potential obstacles, though probably less critical, concern integration issues. For instance, the data flow at the sensor level may be extremely high in case of large beam background, and a ladder material budget below 0.2 % X_0 may be out of reach. More effort should actually be devoted to integration issues which are specific to the detector design exposed in this paper. They are however unlikely to be found inside the teams developing the sensors. This situation needs to evolve within relatively short time if a complete prototype ladder has to be fabricated by $\sim$ 2010.

For the sake of completion, it is worth mentioning that the activities related to the R&D on MIMOSA sensors also encompass more futuristic technologies, which may provide adequate replies to the potential showstoppers or obstacles mentioned above. A specific R&D project has started, which aims at using aluminised industrial diamond slabs as mechanical supports and thermal extractor. More generally, the evolution of 3D integration technologies is followed in contact with some of its main industrial expert companies and high-tech laboratories. CMOS sensors are indeed expected to profit a lot from the spin-offs of the main trends of these technologies, as they may allow to combine the technology best suited the detection functionnalities (e.g. doping profile) of the sensors with those best suited to the analog and the digital parts (feature size, number of metal layers, leakage current, etc.) of the signal processing micro-circuits. Major progress is expected from industry by 2010, which may open the door to a new scale of performances for CMOS sensors.

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APPENDIX A: Summary of fabricated MIMOSA sensors mentionned in the report

MIMOSA-8	fabrication	2003 - TSMC-0.25 techno. - epitaxy thickness $< 7\ \mu m$
	geometry	25 μm pitch - 128 rows - 24/8 col. with digital/analog output - 4 sub-arrays with different pixels
	features	column parallel read-out - clock frequency $\geq$ 100 MHz - row read-out frequency $\sim$ 6 MHz
MIMOSA-9	fabrication	2003 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim 11\ \mu m$ (also with "high-res" substrate without epitaxy)
	geometry	20, 30 & 40 μm pitch - various pixel architectures
	features	technology exploration - analog output - serial read-out
MIMOSA-11	fabrication	2005 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim 11\ \mu m$
	geometry	20 & 30 μm pitch - 106x106 pixels - 4 sub-arrays
	features	analog output - serial read-out
MIMOSA-14	fabrication	2005 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim 11\ \mu m$
	geometry	30 μm pitch - 2 groups of 64x128 pixels
	features	STAR prototype - ionising rad. tol. pixels - analog output - serial read-out
MIMOSA-15	fabrication	2005 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim 11\ \mu m$
	geometry	20 & 30 μm pitch - 4 sub-arrays with various pixels
	features	non-ionising rad.tol. pixels - analog output - serial read-out
MIMOSA-16	fabrication	2006/7 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 & 15 μm
	geometry	25 μm pitch - 128 rows - 24/8 col. with digital/analog output - 4 sub-arrays with different pixels
	features	column parallel read-out - clock frequency $\geq$ 100 MHz - row read-out frequency $\gtrsim$ 6 MHz
MIMOSA-17	fabrication	2006/7 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 & 15 μm
	geometry	30 μm pitch - 4 groups of 64x256 pixels
	features	EUDET demonstrator - 4 analog outputs - serial read-out inside each group
MIMOSA-18	fabrication	2006/7 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 & 15 μm
	geometry	10 μm pitch - 512x512 pixels
	features	EUDET sensor - sub-micron resolution - analog output - serial read-out inside each group
MIMOSA-20	fabrication	2006/7 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 & 15 μm
	geometry	30 μm pitch - ionising rad.tol.pixels - 640x640 pixels
	features	STAR demonstrator (final prototype) - 2 analog outputs - serial read-out inside each group
MIMOSA-21	fabrication	2006 - STM-0.25 BICMOS techno. - sensitive volume includes "high-res" substrate
	geometry	128x192 pixels with 10 μm pitch - 64x96 pixels with 20 μm pitch
	features	beta-imager - analog outputs - serial read-out

APPENDIX B: Sensors and micro-circuits to be fabricated $\leq$ 2010

MIMOSA-22	fabrication	2007 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for EUDET	geometry	18 μm pitch - 576 rows - 128/8 col. with digital/analog output - 9 sub-arrays with different pixels
and STAR)	features	col. parallel read-out - clock frequency $\geq$ 100 MHz - row read-out frequency $\sim$ 6 MHz
SUZE-01	fabrication	2007 - AMS-0.35 OPTO techno. - no epitaxy
(for EUDET & STAR)	features	zero suppression logic & memories - specific to EUDET & STAR
MIMOSA-2X	fabrication	Summer 2008 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for STAR)	geometry	30 μm pitch - 640 rows - $\geq$ 640 col. with digital output - $\leq$ 2 sub-arrays with different pixels
	features	col. parallel read-out - clock frequency $\geq$ 100 MHz - final sensor (called PHASE-1) for the HFT demonstrator
MIMOSA-22+E	fabrication	Fall 2008 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for EUDET)	geometry	18 μm pitch - 544-576 rows - 1088 col. with digital output
	features	final chip equipping EUDET telescope - col. parallel read-out with integ. zero suppression - read-out time $\sim$ 100 μs
MIMOSA-22+S	fabrication	2009 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for STAR)	geometry	30 μm pitch ? - 640 rows ? - 640 col. ? with digital output
	features	large prototype of final chip for HFT col. parallel read-out with integ. 0 supp. - read-out time $\lesssim$ 200 μs
ADC	fabrication	2007/2008 - AMS-0.35 OPTO techno. - no epitaxy
(for ILC)	features	various architectures - 4 or 5 bits - $\geq$ 8 channels - specif. for EUDET & STAR
MIMOSA16+	fabrication	2008 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for ILC)	geometry	20-22 μm pitch - 256-320 rows - $\geq$ 64 col. with digital output - $\geq$ 2 sub-arrays with different pixels
	features	col. parallel read-out with integ. ADC
SUZE-02	fabrication	2008 - AMS-0.35 OPTO techno. - no epitaxy
(for ILC)	features	0 suppression micro-circuits & memories - specific to ILC
MIMOSA-X	fabrication	2008/2009 - various technologies with $<$ 0.2 μm feature size
ADC-X	fabrication	2008/2009 - various technologies with $<$ 0.2 μm feature size
SUZE-X	fabrication	2008/2009 - selected technology with $<$ 0.2 μm feature size
MIMOSA16++	fabrication	2009 - AMS-0.35 OPTO techno.? - epitaxy thickness $\sim$ 11 μm ?
(for ILC)	geometry	20-22 μm pitch - 256-320 rows - $\geq$ 256 col. with digital output - $\leq$ 2 sub-arrays with different pixels
	features	col. parallel read-out with integ. ADC & zero suppression
MIMOSA16+++	fabrication	2010 - technology ?
(for ILC)	geometry	20-22 μm pitch - 256-320 rows - $\geq$ 256 col. with digital output - $\leq$ 2 sub-arrays with different pixels
	features	final sensor - col. parallel read-out with integ. ADC & 0 suppression