Design of the front-end digitization electronics for a G-APD-based Cherenkov telescope camera

V. Commichau[1], L. Djambazov[1], O. Grimm[1,*], H.P. von Gunten[1], B. Krumm[2], W. Lustermann[1], D. Neise[2], M. Ribordy[3], U. Röser[1], J. Schneider[1], P. Vogler[1], K. Warda[2], Q. Weitzel[1]
– for the FACT collaboration –

[1]ETH Zürich, Institute for Particle Physics, Schafmattstrasse 20, 8093 Zurich, Switzerland
[2]Universität Dortmund, Experimental Physics 5, Otto-Hahn-Str. 4, 44221 Dortmund, Germany
[3]École Polytechnique Fédérale de Lausanne, Laboratory for High Energy Physics, 1015 Lausanne, Switzerland

FACT – Overview

First G-APD Cherenkov Telescope

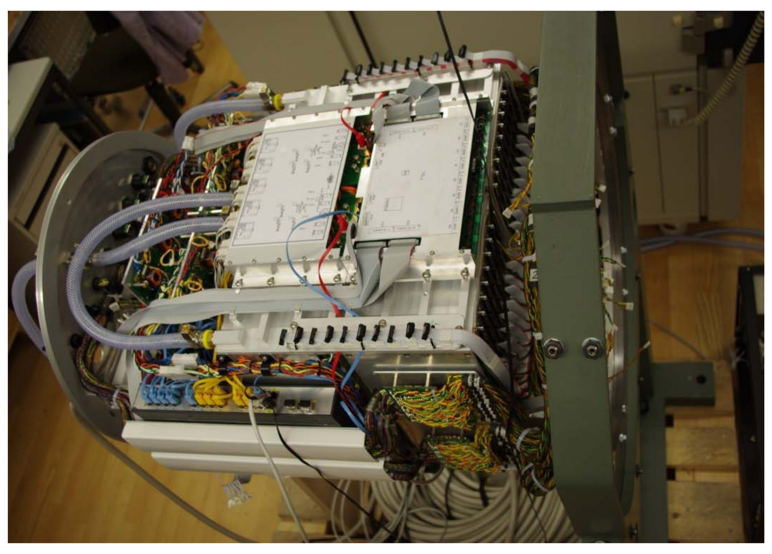
Full-scale camera for long-term monitoring of variable Gamma-ray sources and technology demonstration

4.5° field-of-view (0.11° per pixel), 1440 pixels
Operation also under twilight/moon (background rate up to 5 GHz per pixel)
Power consumption ≈1 kW
Gain stabilization to ≈5% with feedback
Installation on former HEGRA CT3 telescope at La Palma (9.2 m² mirror)

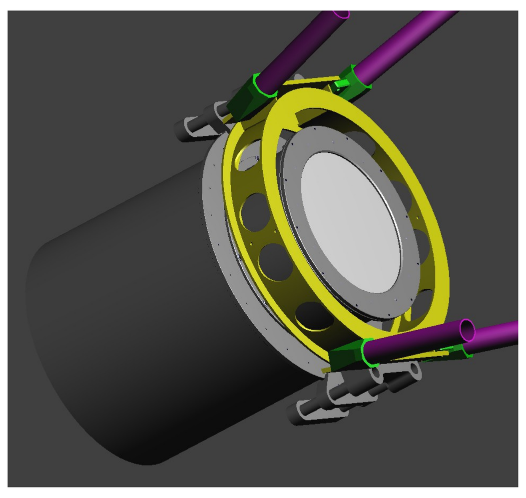
Solid light concentrators

Digitization and triggering integrated in camera

DRS4 analog pipeline chip (PSI development)
Timing better than 300 ps (rms)
Data transfer via Ethernet
Majority-trigger logic of non-overlapping patches



Electronics on 12-layer boards for thermal design reasons.
Boards mounted to custom-build water cooled crates.



Fast digital signals routed via Cat.6 Ethernet cables
Thermal interface uses Calmark Card-Loks

Imaging Air Cherenkov Telescopes

No photons from space with wavelength shorter than UV reach ground

Direct detection only in space or on high-altitude balloons
Cost implies size and weight limit
Event rate very low above ≈50 GeV (Crab nebula >30 GeV: ~0.2 photons/cm²/year)

Above ≈60 GeV: resulting air showers attain detectable size

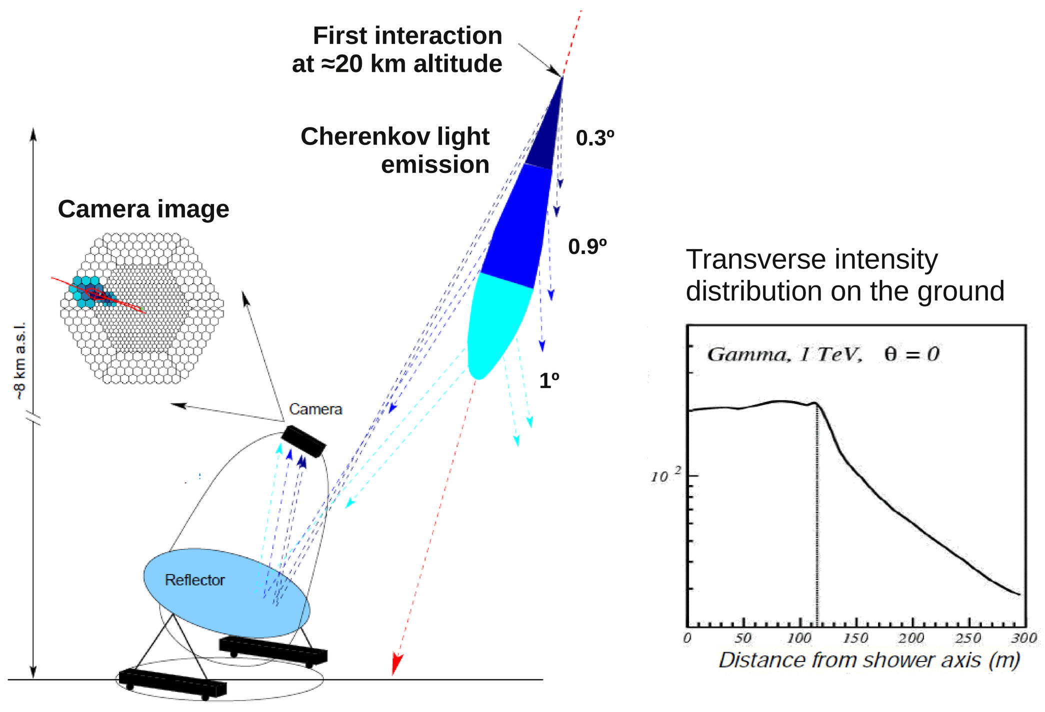
Detection through emitted Cherenkov light
Atmosphere behaves as 27 radiation length deep calorimeter
Challenge is discrimination against hadronic showers (γ/p ratio <10⁻⁴) and muons

Statistical analysis of image parameters

Gamma/hadron separation
benefits from sub-ns time resolution

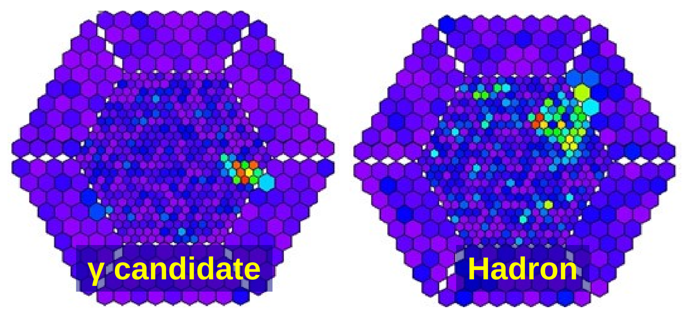
γ-ray energy
≈15% resolution for large telescope

Arrival direction (source location)
≈10 arcmin resolution



from: S. Commichau, PhD thesis, ETH Zürich (2007)

Typical camera images (MAGIC)



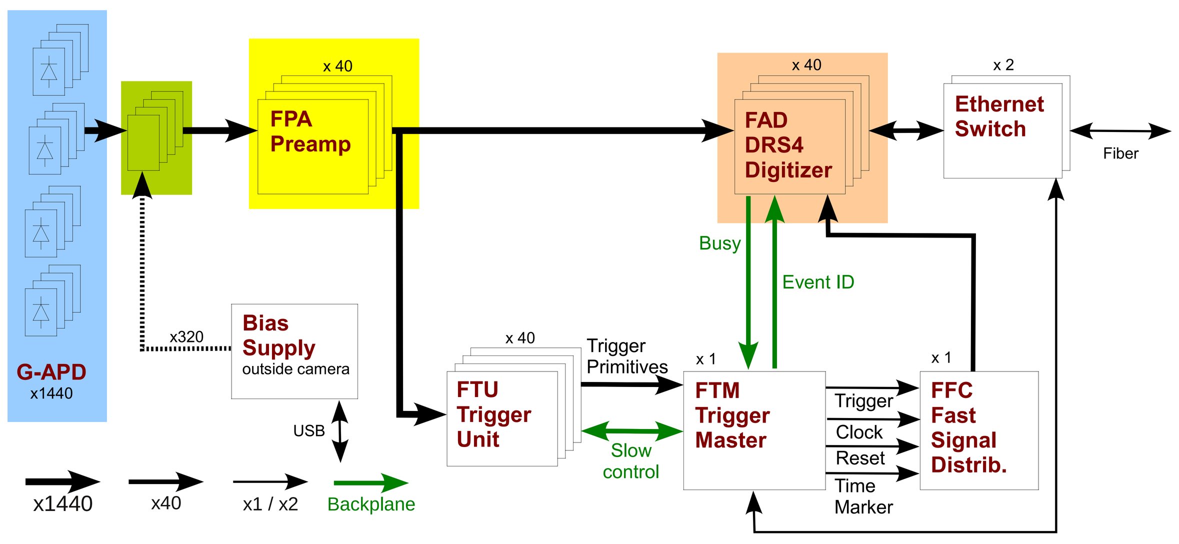
Science targets

Source discovery

Accelerating mechanisms in pulsars and AGN

Signatures of new particles

Electronics Block Diagram

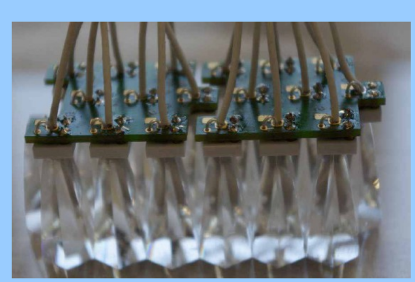


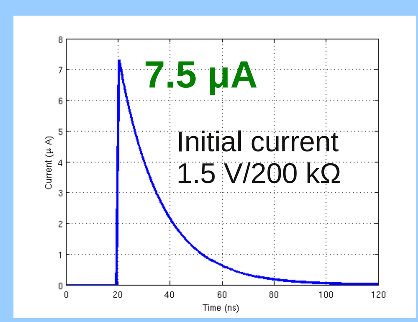
Light Sensor

Geiger-mode Avalanche Photo-diode

Hamamatsu S10362-33-50C MPPC

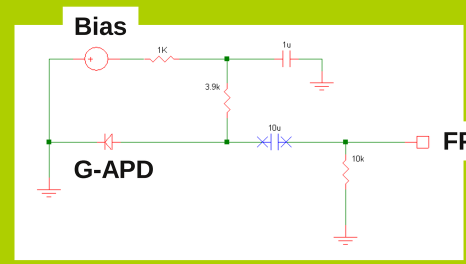
3x3 mm area, 50x50 μm pixel, gain 7.5x10⁵
$U_{operation}$ = 70V, C_{total} = 320 pF
R_{quench} ~200 kΩ, C_{cell} ~ 80 fC → $\tau_{recharge}$ = 16 ns
Nominal over-voltage U_{over} ~7.5x10⁵ e-/C_{cell}=1.5 V





Single avalanche pulse shape

Sensor Bias



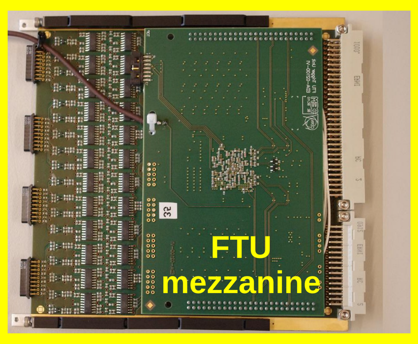
Circuit for bias input and signal out-coupling

320 channel bias supply
0-90 V
USB interface
Custom developed

FPA - Amplifier

Trigger from FTU to FTM

4x9 channel input



Midplane connector

- Signals to FAD
- RS-485 to FTM
- Power supply

Amplification before summing

Output impedance of operational amplifier at signal frequencies ~10 Ω

Resistor network between stages results in signal attenuation by ~1/5.4

Current-to voltage conversion

Transistor in base configuration as current buffer
Conversion to voltage over two parallel 390 Ω resistors

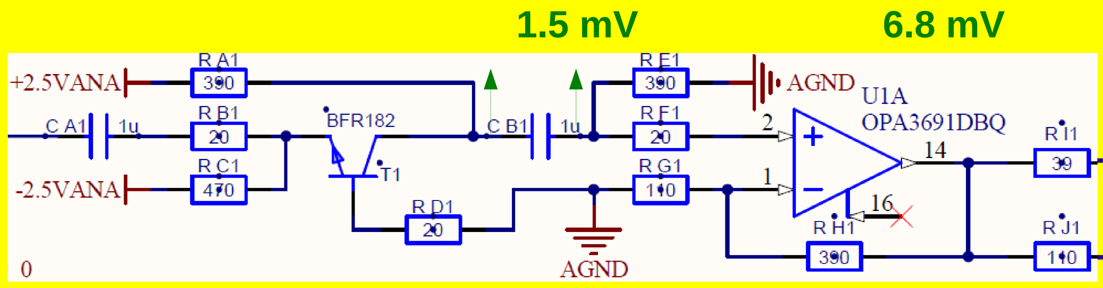
Peak current of single avalanche

7.5 μA

1.5 mV

6.8 mV

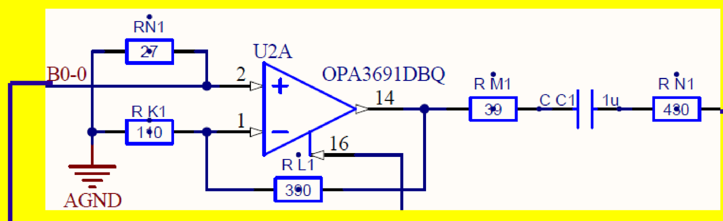
to FAD



x1 x390 Ω/2 x4.5

1.3 mV

5.9 mV



x1/5.4 x4.5

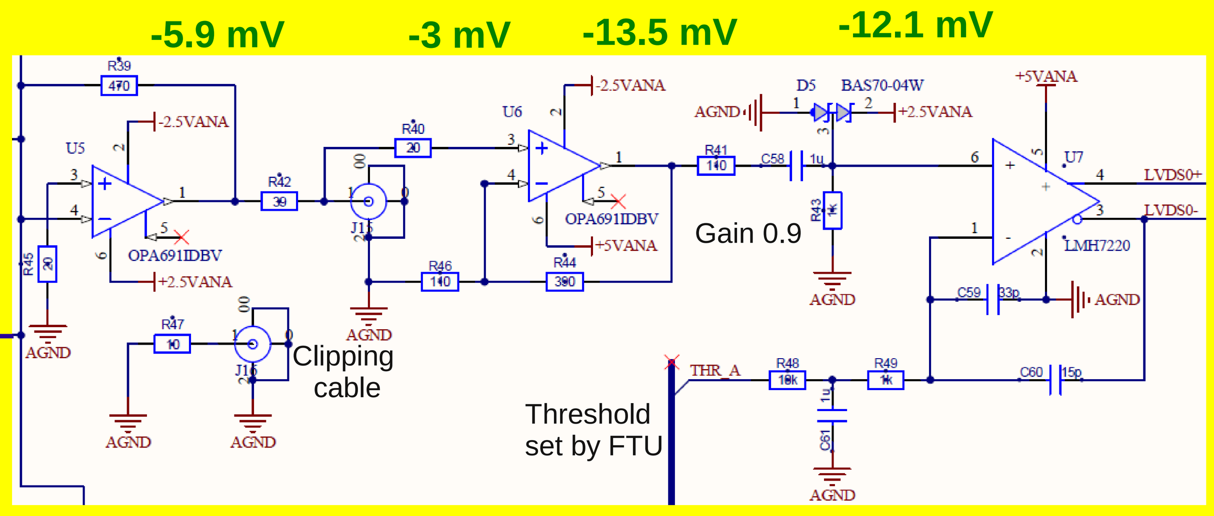
Enable from FTU

Summing for trigger generation

Analog signals from 9 channels summed and clipped by cable reflection
Total gain for trigger 1.6 mV/μA

Trigger decision reported over LVDS to FTU (trigger front-end)

-5.9 mV -3 mV -13.5 mV -12.1 mV



x-1 x1/2 X4.5 X0.9

FAD - Digitization

Single-ended to differential conversion

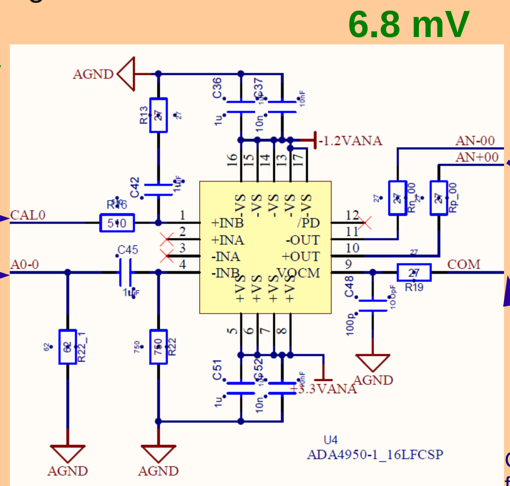
Signal attenuated by resistors and input/output impedance between FPA and FAD by ~0.5
Converter set to gain 2

3.4 mV

6.8 mV

Calibration voltage from DAC on FAD

from FPA

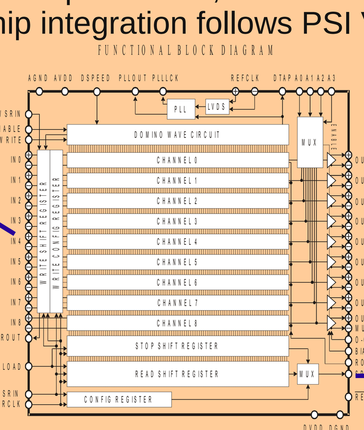


Common mode from DAC on FAD

x2

DRS4 analog pipeline chip

Developed at PSI, Switzerland (http://drs.web.psi.ch/).
Chip integration follows PSI VME mezzanine design



x2

13.6 mV

Total gain
1.8 mV/μA

Sampling frequency 2 GHz
Reference clock from FTM)

ADC
AD9238BSTZ-40

12 bit, 2 V range

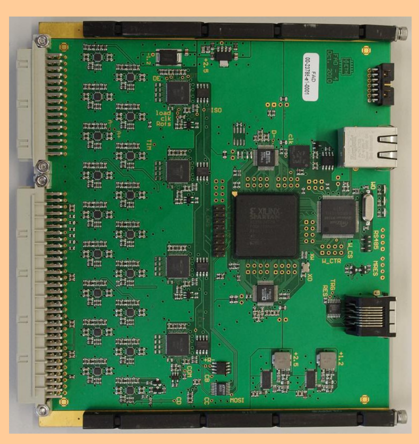
Digital control

FPGA Xilinx XC3SD3400A-4FGG676C

50 MHz frequency
Stops DRS sampling when triggered
Informs trigger master (FTM) when unable to accept triggers
Controls DRS4 and ADC (generates clocks)
Sets DAC on FAD (input common mode, calibration, output offset)
Receives event number over RS485 from FTM
Interfaces with Wiznet chip
Measures reference clock
Reads temperature sensors

Midplane connector

- Signals from FPA
- RS-485 to FTM
- Power supply



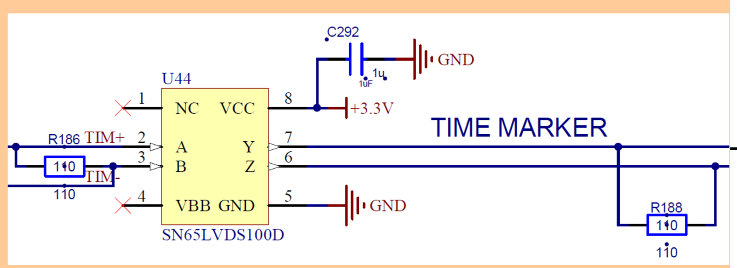
J-TAG

Ethernet

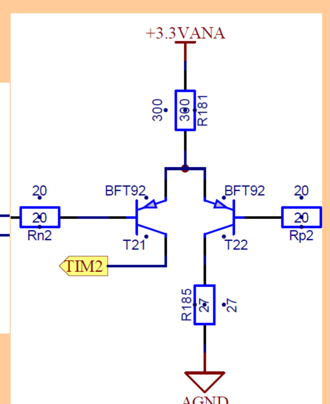
Fast digital signals

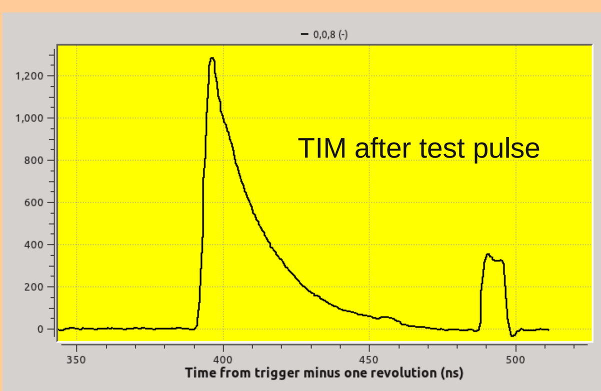
High precision time marker

Time marker (TIM) generated by FTM, transported differentially over category 6 Ethernet cables
Backup in case of problems with DRS phase locked loop



LVDS Repeater
<65 ps jitter





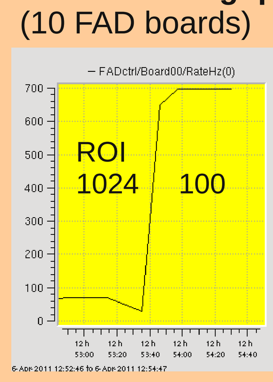
Data transfer

Ethernet interface with Wiznet W5300 chip (100 Mbit/s)

8 TCP/IP sockets used cyclically for sending event data
Socket 0 for receiving command

FAD boards connected to two Gigabit switches (D-Link DGS-1224T), data transfer to counting house over fibers (Huber+Suhner MO104)

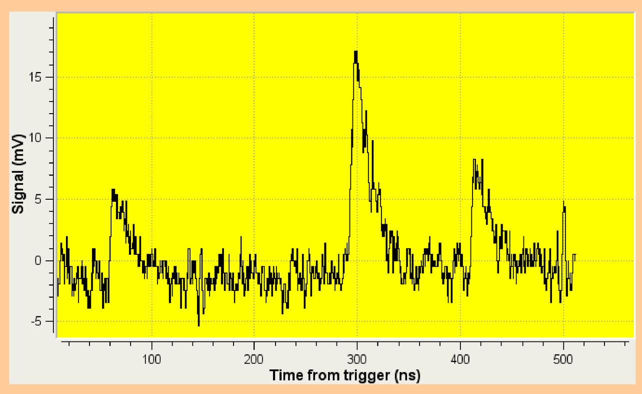
Measured throughput
(10 FAD boards)



~60 MByte/sec
Trigger rate with 100 bins region-of-interest ~700 Hz

G-APD dark counts digitized with FAD

Double avalanche generated by optical cross-talk
Noise after DRS4 calibration 1.5-2 mV rms



*Corresponding author, email oliver.grimm@phys.ethz.ch