CMOS sensors with high resistivity epitaxial layer

State of the art

STAR – Ultimate sensor

ALICE/ CBM

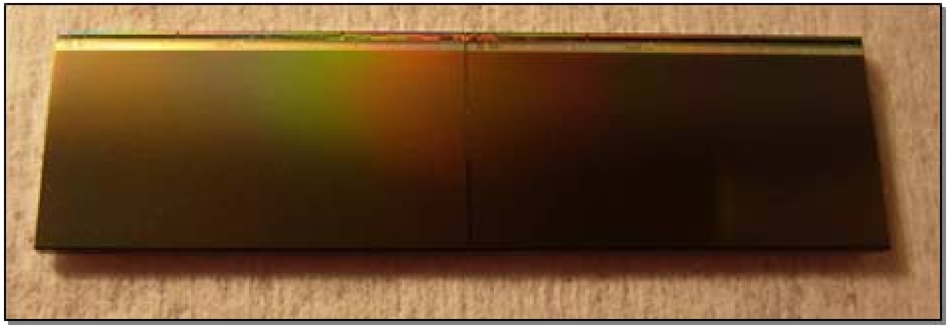
ILC / AIDA / superB

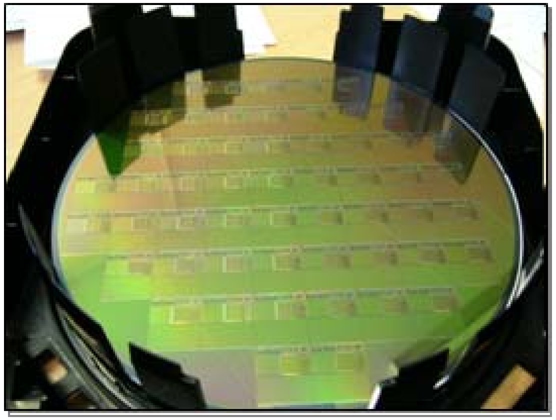
Integration, Plume project

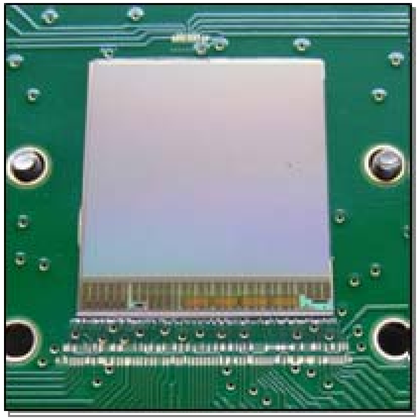
Summary and outlook

Auguste Besson on behalf of PICSEL team of IPHC-Strasbourg

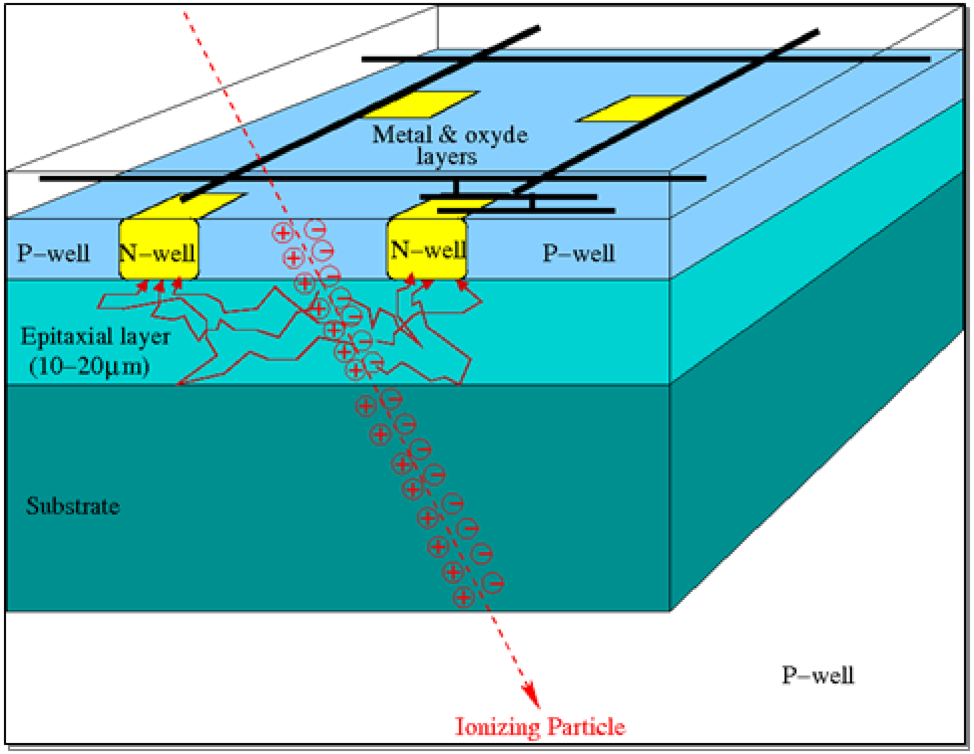
and collaborators



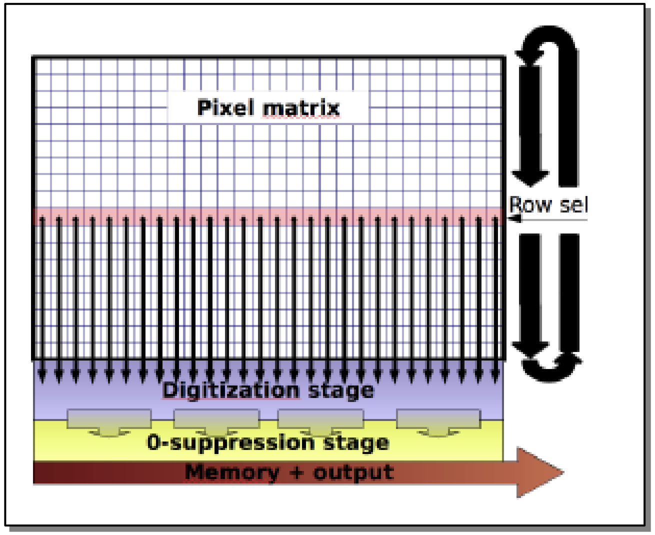




CMOS pixel sensor : State of the art

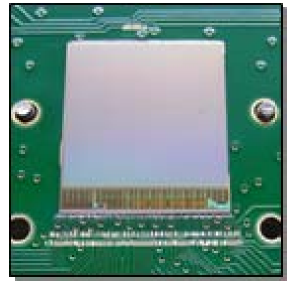


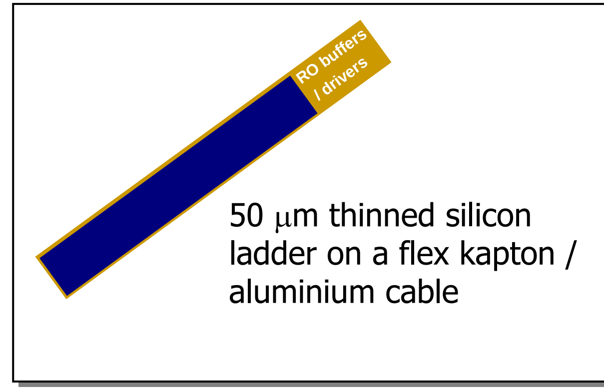
- Main application
  - Foreseen to equip vertex detectors
- Main features / Principle of operation
  - MIMOSA serie: manufactured in 0.35 µm OPTO process
  - Thermal diffusion of electrons in a thin epitaxial layer (10-20 µm)
    - ➢ Signal ~ 1000 e-
    - ➢ Low material budget (thinned down to 50 µm)
  - Charge collection shared between N-Well diodes
    - ➢ High granularity (10-40 µm pitch)
    - ➢ Excellent (micronic) spatial resolution
  - Signal sensing and analog processing in pixel (preamp, CDS, etc.)
  - Signal processing µ-circuits integrated on sensor substrate
    - ➢ ADC/digital output, Zero suppression circuitry integrated in chip periphery
    - ➢ Read-out in rolling shutter mode (columns read out in //)
      ⇨read out time = typically 200 ns per row
    - ➢ Impact on downstream electronics (cost)



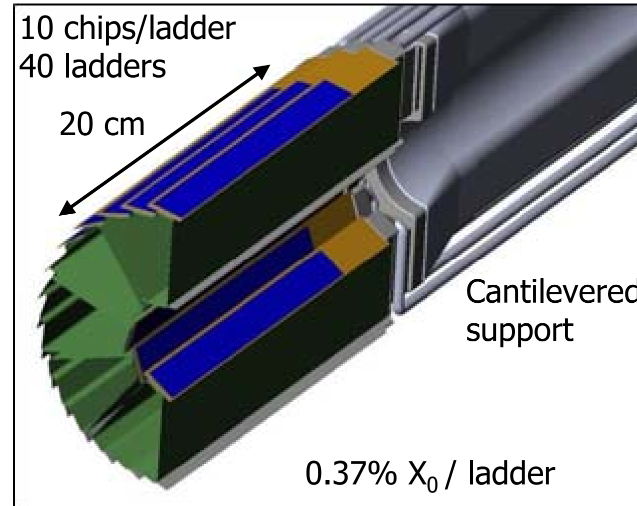
Priority given to high granularity, low material budget, low power consumption, with sufficient read-out speed and radiation tolerance.

Ultimate Sensor for STAR Vertex detector (1)

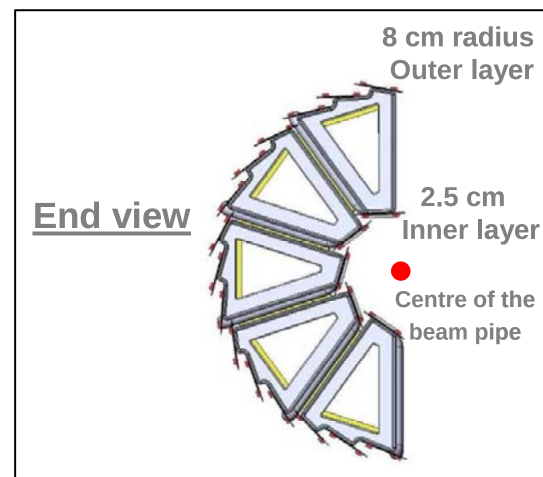




- STAR PIXL upgrade (physics run in 2014)
  - Requirements
    - ~ 150 kRad and few 10^{12} n_{eq} /cm²/year
    - Temperature 30-35 °C (air flow cooling only)
    - Power consumption ~130 mW/cm²
    - Spatial resolution < 10 µm
    - Integration time ~< 200 µs to cope with occupancy (~200 hits / 4 cm² sensor / read-out cycle)
  - Design
    - 2 layers (2.5/8 cm radius)
    - 40 ladders: 50 μm silicon, Flex kapton / aluminium cable
    - 10 Mimosa chips/ladder ⇨ 370 x 10^6 pixels
    - 0.37% X_0 per layer



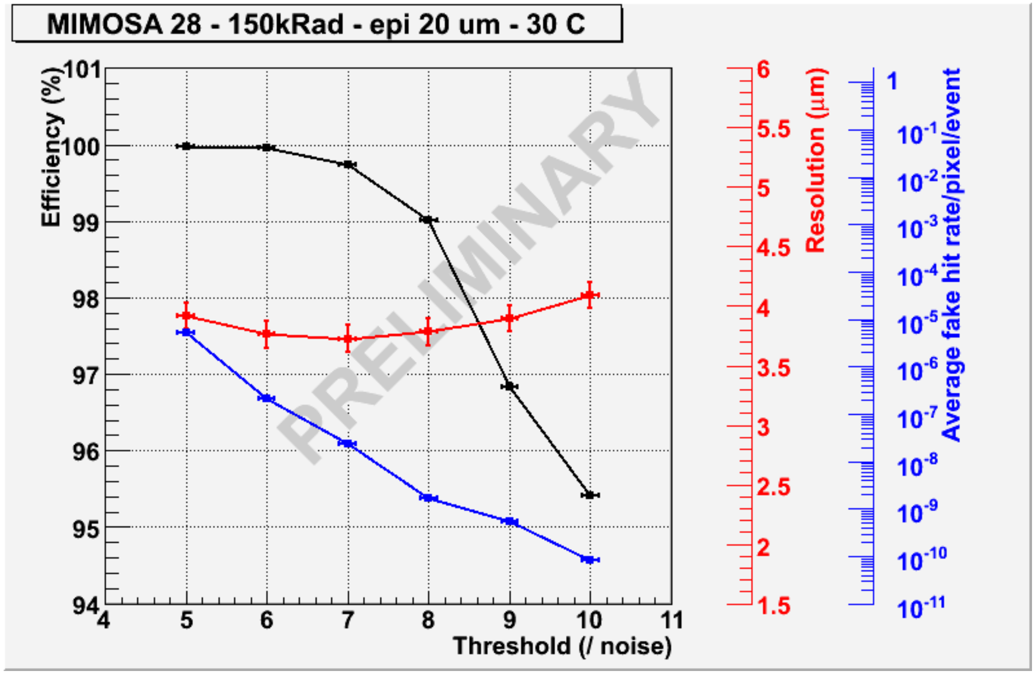
- Ultimate (alias Mimosa 28)
  - Final sensor for the upgrade of STAR pixel layers of the vertex detector
    - Design process Austria Micro System AMS-0.35 μm - OPTO, 4 metal- and 2 poly- layers
    - 15 µm thick epi. layer, High-Resistivity substrate (400 Ohm.cm)
    - Radiation tolerant structures
    - 928 (rows) x 960 (columns) pixels, 20.7 µm pitch ⇨ ~20 x 23 mm²
    - Fast binary readout, zero suppression
    - 200 µs read-out time: Suited for 10^6 part/cm²/s



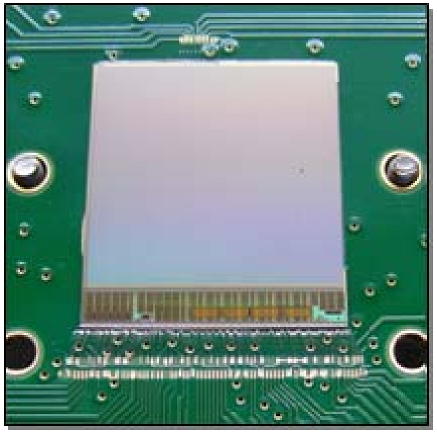
Chip delivered in spring 2011
First data taking in 2013
First vertex detector equipped with CMOS pixel sensors !

STAR – Ultimate (2) : Performances

- Test Beam @ CERN-SPS (July 2011), 120 GeV pion beam
  - Goal: approach STAR running conditions
    - T = 30 °C
    - Chip irradiated @ 150 kRad
    - Read-out time = 198 μs
- Results
  - Efficiency ≥~99.9% with a ~<10^{-6} fake rate
  - Spatial resolution ~ 3.7 μm
  - Uniformity checked
- Under study / to be done
  - Fluence of > 3×10^{12} n_{eq}/cm^2 (already tested with previous prototype M26)
  - Large incident angle



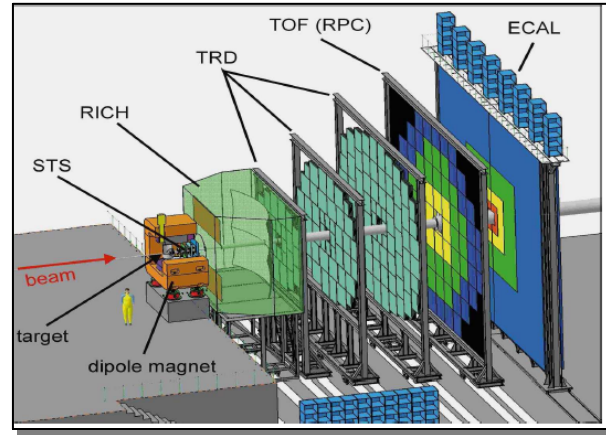
Ultimate sensor fulfilling STAR requirements demonstrated

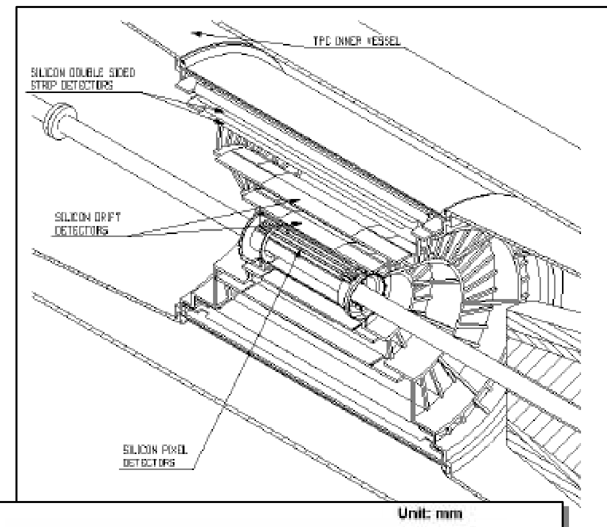


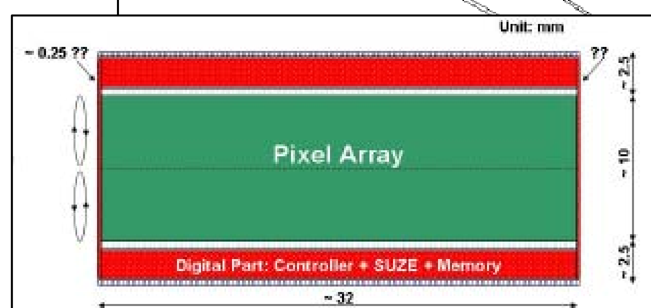
CBM / ALICE : towards 0.18 μm fabrication process

- CBM: Cold Baryonic Matter experiment @ FAIR
  - Micro-Vertex Detector made of 2 stations
  - Double sided stations
    - ➢ ~≤ 0.5% X_0 per station
  - Intermediate prototype in ~2016
  - Running conditions (ultimately in ~2020)
    - ➢ Operation in vacuum @ negative temp.
    - ➢ r.o. time ~≤ 10 μs; > 10^{14} n_{eq}/cm^2; ≥~ 30 MRad
- ALICE: ITS upgrade (~ 2016 LHC shutdown)
  - Different options:
    - ➢ hybrid pixels / CMOS sensors
    - ➢ Introducing a layer L0 ~ 25 mm radius
    - ➢ Potentially replace part of the ITS
  - Requirements
    - ➢ 2 x 10^{13} n_{eq}/cm^2; > 2 MRad ; @ 30 °C
- Upgraded sensors
  - 0.18 μm triple-well High Res. fabrication process
  - Presumably double sided read-out
  - Possibly double sided ladders (see PLUME)
  - Possibly large area sensors

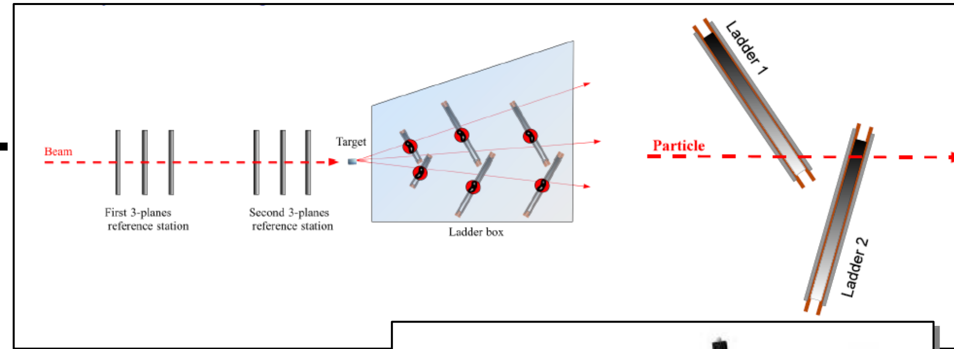
Hi. Res./0.18 μm ⇨ Extend application domains

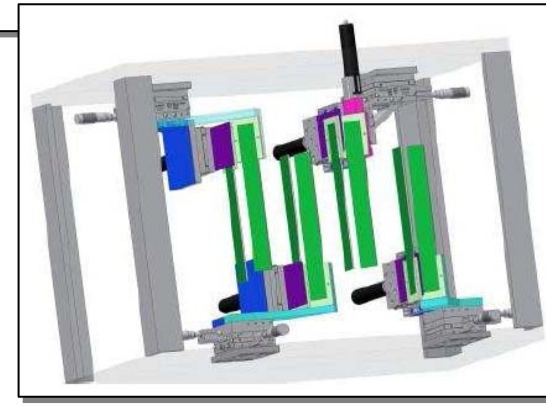




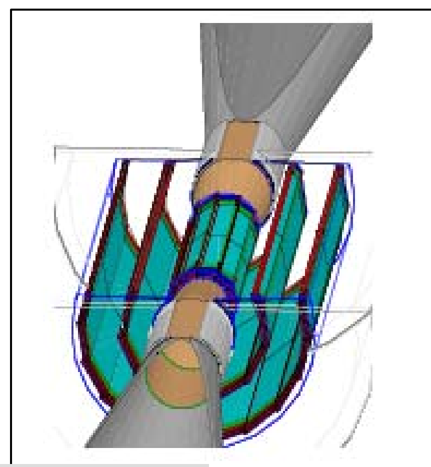


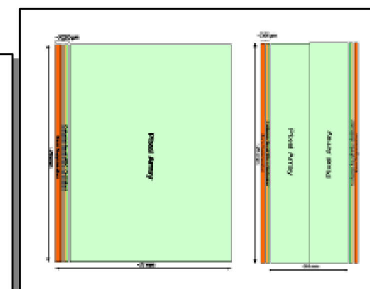
ILD - AIDA - SuperB

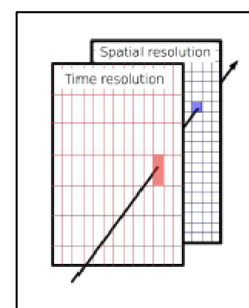




- AIDA (EU-FP7 WP9.3) test beam infrastructure (2014)
  - Large area beam tel. (~6x4 cm^2)
  - Alignment Investigation Device (AID)
    - ➢ Reproduce a VTX detector sector
    - ➢ Double sided ladders mounted on precise adjustable stages
  - Thermo-mechanical studies
- SuperB (≥~2016)
  - ~ 100 Mpart/cm^2/s @ 1.5 cm radius (safety factor of 5)
  - Baseline: Babar VTX + boost/2. ⇨ Δt/2 ~ needs to improve σ_{IP}
  - 1st option add a layer zero with striplets (1.8cm)
  - Upgrade: CMOS sensors or Hybrid pixel
    - ➢ Charge collection optimisation (chip by V.Re et al., INFN Pavia/ Bergamo)
- ILD for International Linear Collider
  - Detector Baseline Document (2012)
  - Inner layers
    - ➢ Optimize r.o. speed and spatial resolution
    - ➢ 16x16/80 μm^2 pitch, 10/40 μs r.o. time
    - ➢ 3/5 μm sp. resolution
  - Outer layers
    - ➢ Optimize Power dissipation
    - ➢ 4bits ADC, 35 μm pitch, 100 μs r.o. time
  - 2 demonstrator prototypes being designed (2011)



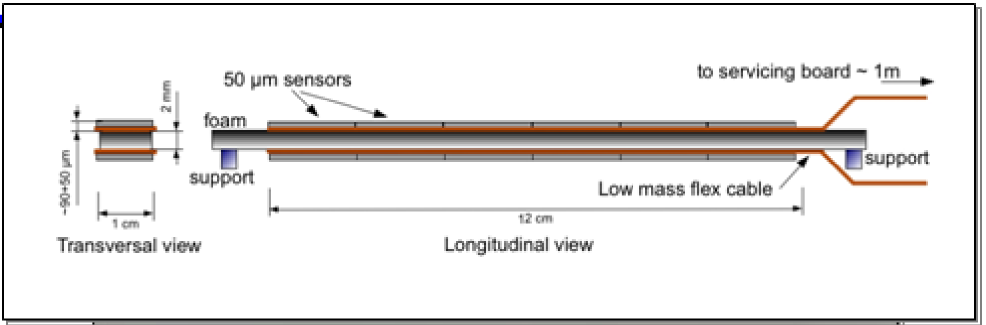


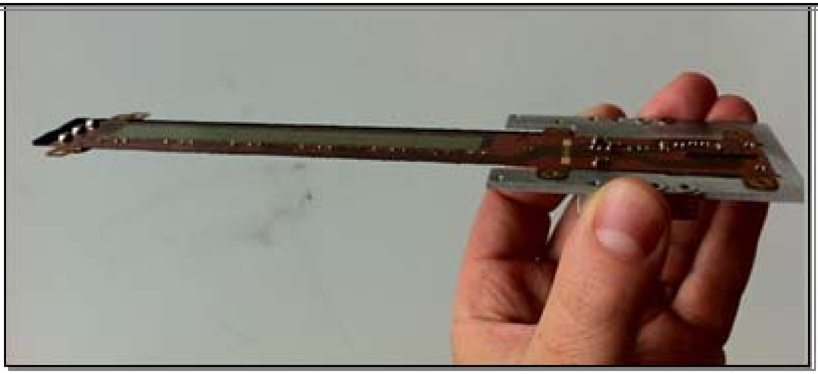


Study/demonstrate full potential of double sided ladders

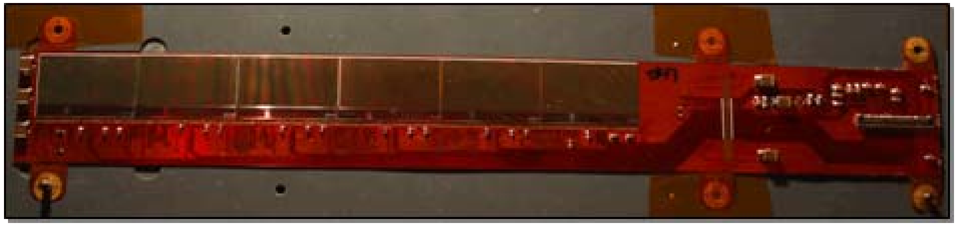
Integration – Plume - Serwiete (1)

- Plume
  - Proof of principle for ILD-VXD concept (DBD 2012)
  - Pixelated Ladder with Ultra low Material Embedding
  - Double sided ladder
    - Sensors thinned down to 50 um
    - Silicon carbide foam/support (2mm)
    - Low mass flex cable :
    electrical services: power, control, data





- 1st prototype (2010)
  - Goal: focus on functionnalities
  - 1 double sided ladder = 8.4M pixels (12 chips)
  - Mat. Budget:
    - 0.8% X0 (average)
    - 0.6% X0 (active area)
  - On a module: 12 channels in //.
  - 1 ladder produced
    - chips+flex are fully functionnal tested
    at 80 MHz = 80Mbits/sec
  - Air cooling assumed
  - Extendable concept in length.

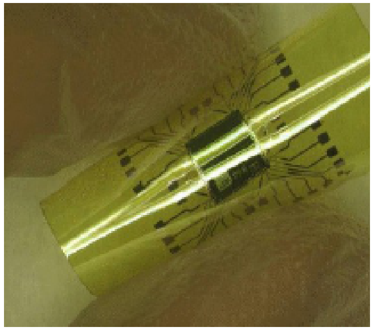


- 2nd prototype (end 2011)
  - Focus on material budget
    - ~ 0.5% X0 (average)
    - ~ 0.3% X0 (active area)
  - Narrower flex (mirrored on both side)
    - Copper replaced by aluminium
  - New support (lower mass spacer)

[1]IPHC/IN2P3 Strasbourg, France
[5]University of Bristol, UK
[6]DESY, Hamburg, Germany
[7]University of Oxford, UK
[2]IMEC, Leuven, Belgium
[3]CMST, University of Gent, Belgium
[4]IFK, Goethe University, Frankfurt/M, Germany
[8]CERN, Geneva

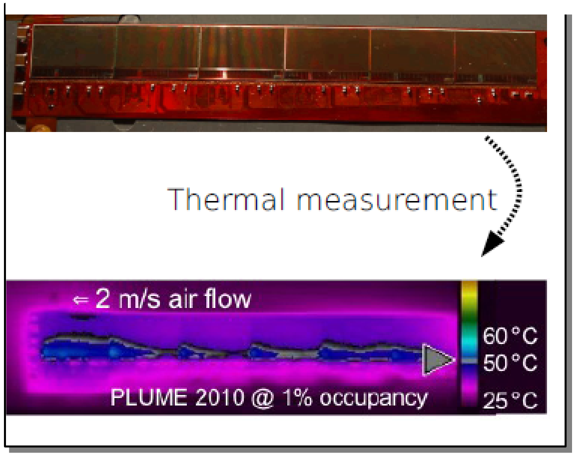
Integration – Plume - Serwiete (2)

- SERWIETE
  - SEnsor Row Wrapped In an Extra Thin Envelop
  - Idea (with IMEC comp., CERN)
    - Sensor mounted on flex and wrapped in polymerised film
    - Reduce bounding material
    - Proto in summer 2011



Fully functional microprocessor chip in flexib
plastic envelope. Courtesy of Piet De Moo
IMEC company, Belgiu

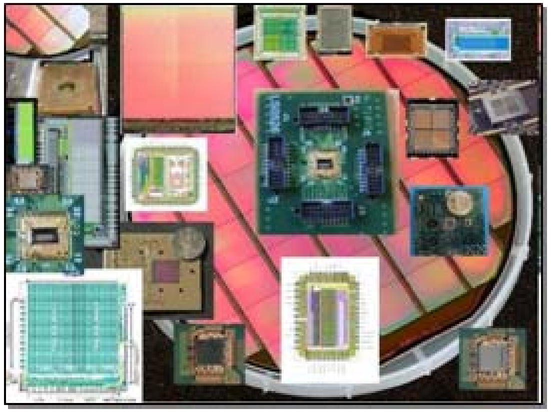
- Mid term objectives:
  - 2011: mechanical tests
    - measure vibration sagitta under air flow and operation)
  - Thermal studies
  - Data output path studies
    - Digital output at ~200 MHz with optic fibers ?
  - Produce 10 ladders for AID box (~2013)
  - Space for improvement:
    - Reduce mat. Budget (SERWIETE)
    - Narrower flex, less bounding material
    - Increase active area w.r.t. to digital part. (Mimosa26 ⇨ ultimate)
    - Reduce thickness of the support ?
  - AID: 50 M pixels ! (zero supp. + PXI DAQ)



Global material budget under control
CMOS sensors will benefit from steady industry progress for integration

Summary

- CMOS sensor technology, initally developped for ILC is mature and extends its domains of applications
  - Great potential when granularity, material budget and power comsumption are the leading constraints.
  - Now used successfully (e.g. EUDET beam telescope)
  - 1st vertex detector (STAR) equipped with CMOS in ~ 2013

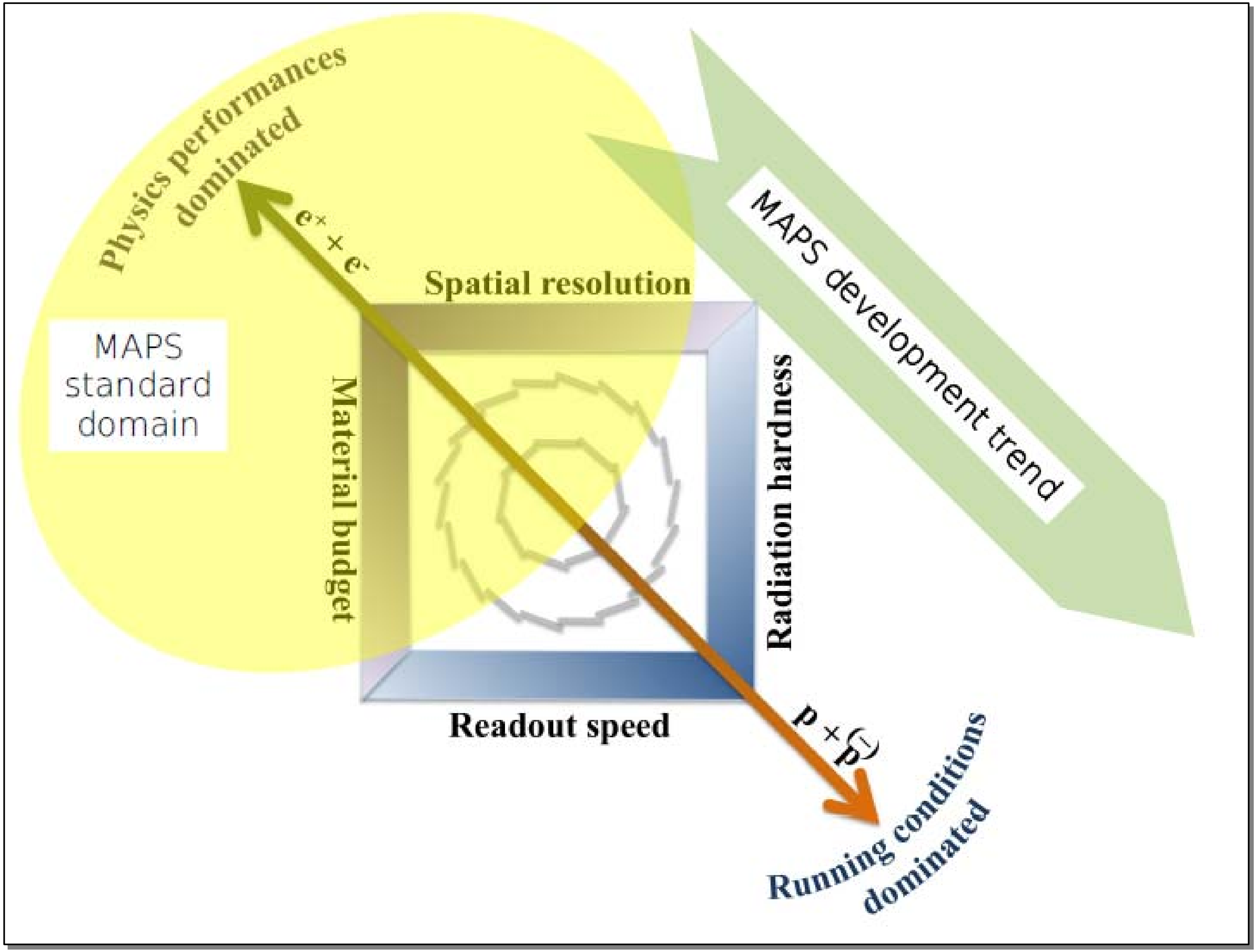


- Mid term plans
  - Many projects / options under study
    - CBM-MVD ≥~2015 (rad.tol.)
    - ALICE-ITS option: Technical proposal end 2011 ~ 2017
      also considered: ALICE-FOCAL, FW tracker
    - ILD-VTX (Linear Collider) option Det.Baseline.Doc.
      (double sided ladders, ADC, elongated pixels, etc.)
    - AIDA (Large sensors, stitching): 2014
    - R & D for Electron-Ion Collider (eRHIC) (Large sensors for forward disks) ~ 2017
    - R & D for superB (in pixel FEE, speed) ~ 2017
    - NA63 (e^+ source for CLIC)
  - Other domains of application
    - Hadrontherapy, dosimetry, etc.

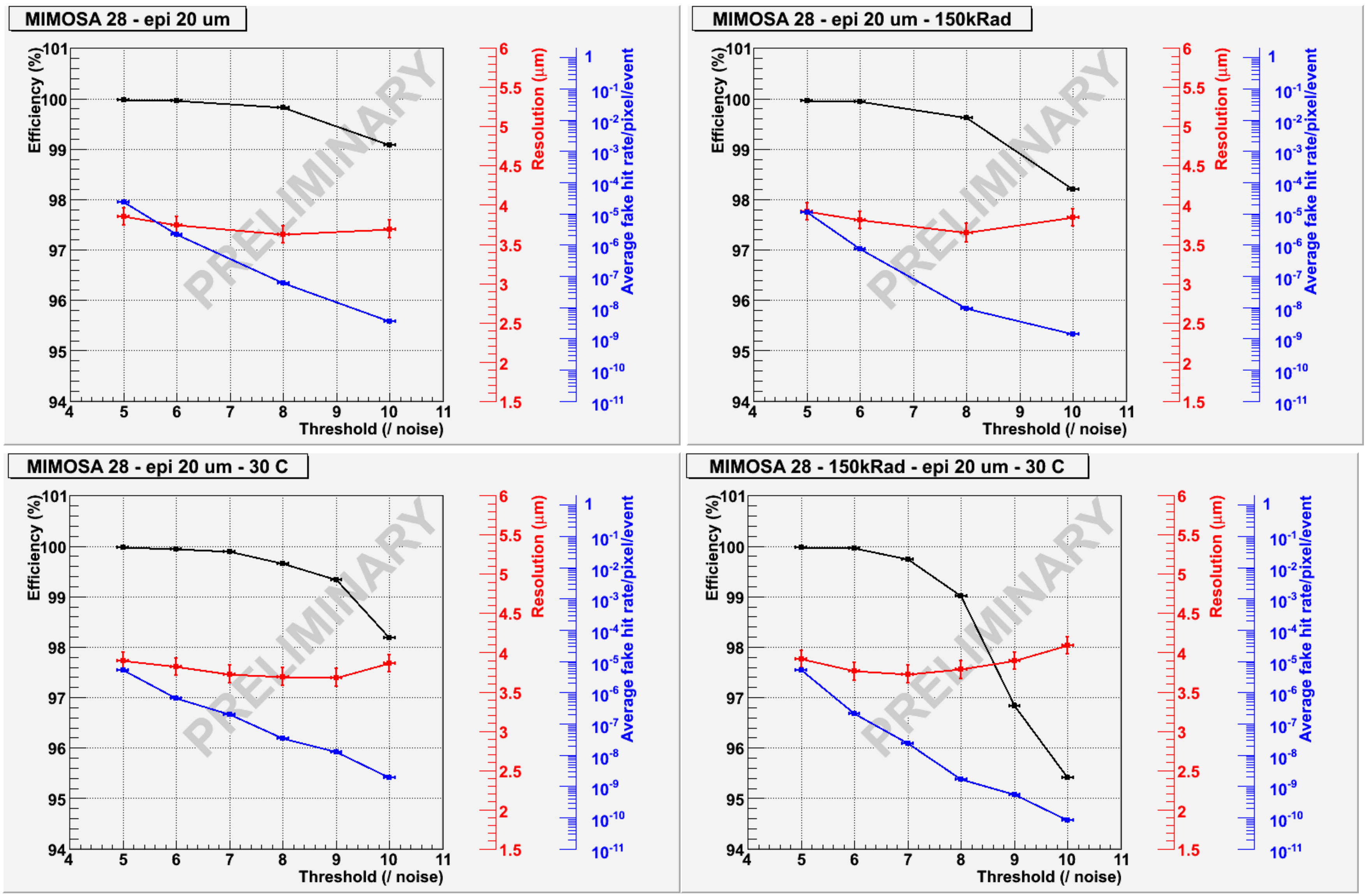
- The CMOS technology has not reached its limits yet
  - Higher resistivity ⇨ enhance S/N
  - 0.18 μm feature size (first proto in 2011) ⇨ rad.tol., read-out speed, mat. budget
  - Deep P-well ⇨ S/N
  - Long term: multi-tier (3D) sensor

Back up

MAPS development trend



STAR – Ultimate Preliminary results

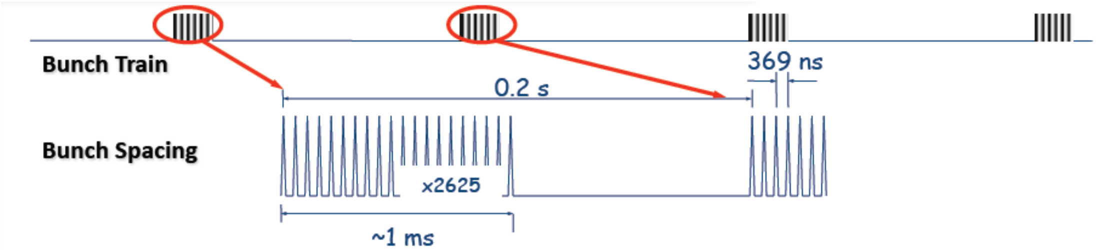


T°C

Ionising radiation

International Linear Collider (ILC) running conditions

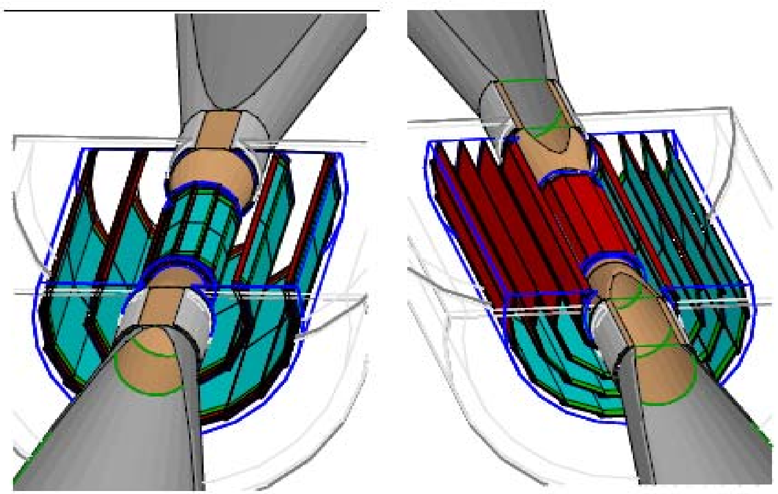
- e+e- : √s up to 1 TeV
- 5 trains/s
- 2680 bunches/train
- 337 ns between bunches
- Occupancy governed by beam background (beamstrahlung)



Physics goals & running conditions

- single point resolution ~ 3µm
- material budget ~0.2% X_0/layer
- integration time 25 – 100µs
- radiation tolerance > 300Rad, few $10^{11} n_{eq}/cm^2$
- P < 0.1 – 2 W/cm²

$$\sigma_{IP} = a \oplus b/p\sin^{3/2}\theta$$
a = 5µm, b = 10µm GeV



Radius:
16 – 60 mm for double-sided ladders,
15 – 60 mm for single-sided ladders

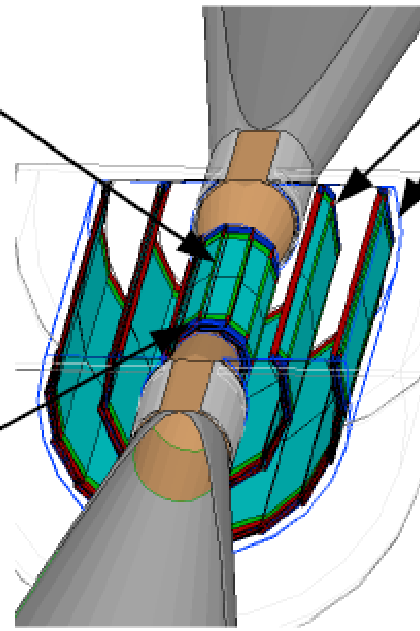
CMOS sensor-based Vertex detector for ILD

Inner layer – internal side

- Optimized for resolution
- 16 x 16 µm²
- Q encoding: binary
- $t_{Integration}$ ~40 µs
- Sensitive area ~ 2 cm²

Inner layer – external side

- Optimized for r.o. speed
- 16 x 64 µm²
- Q encoding: binary
- $t_{Integration}$ ~10 µs
- Sensitive area ~ 2 cm²



Outer layer

- Optimized for low power
- 35 x 35 µm²
- Q encoding: 4-bits
- $t_{Integration}$ ~100 µs
- Sensitive area ~ 4 cm²

- **Sensor prototyping :** design under way
  - MIMOSA-30: inner layer prototype with 2-sided read-out
    - ↪ one side : 256 pixels ($16 \times 16\ \mu m^2$)
    - other side : 64 pixels ($16 \times 64\ \mu m^2$)
  - MIMOSA-31: outer layer prototype
    - ↪ 48 col. of 64 pixels ($35 \times 35\ \mu m^2$) with 4-bit ADC

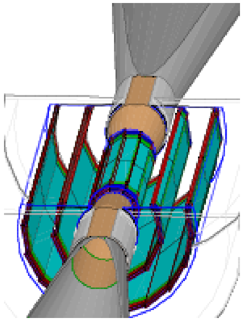
12

layer	radius (mm)	length (mm)	# ladders	# sensors*	#.10⁶ pixels	t_{int} (µs)	$\sigma_{s.p.}$ (µm)
1	16/18	125	14	168	66 + 16	40 / 10	< 3 / ~5
2	37/39	250	26	312	2x112	100	< 4
3	58/60	250	40	480	2x173	100	< 4
total			80	960	652		

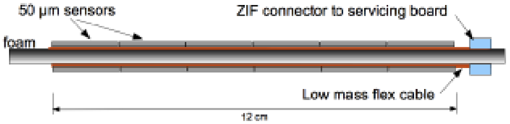
* Numbers corresponding to current CMOS technology (0.35 µm) prototypes

ILD

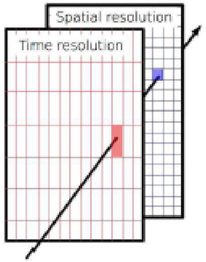
CMOS sensors for the ILD-VTX



- **Two types of sensors :**
  - ⁎ Inner layers ($\lesssim$ 300 cm^2) : priority to read-out speed & spatial resolution
    - ↪ small pixels (16×16 / 80 μm^2) with binary charge encoding
      - ↪ $t_{r.o.} \sim$ 50 / 10 μs; $\sigma_{sp} \lesssim$ 3 / 5 μm
  - ⁎ Outer layers ($\sim$ 3000 cm^2) : priority to power consumption and good resolution
    - ↪ large pixels (35×35 μm^2) with 3-4 bits charge encoding
      - ↪ $t_{r.o.} \sim$ 100 μs; $\sigma_{sp} \lesssim$ 4 μm



- **2-sided ladder concept for inner layer** (see W.Dulinski's talk) **:**
  - ⁎ square pixels (16×16 μm^2) on internal ladder face ($\sigma_{sp} < 3\ \mu m$)
    & elongated pixels (16×80 μm^2) on external ladder face ($t_{r.o.} \sim 10\ \mu s$)



- **Sensor prototyping :** design under way
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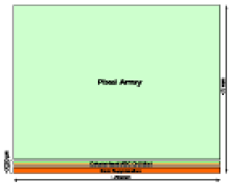
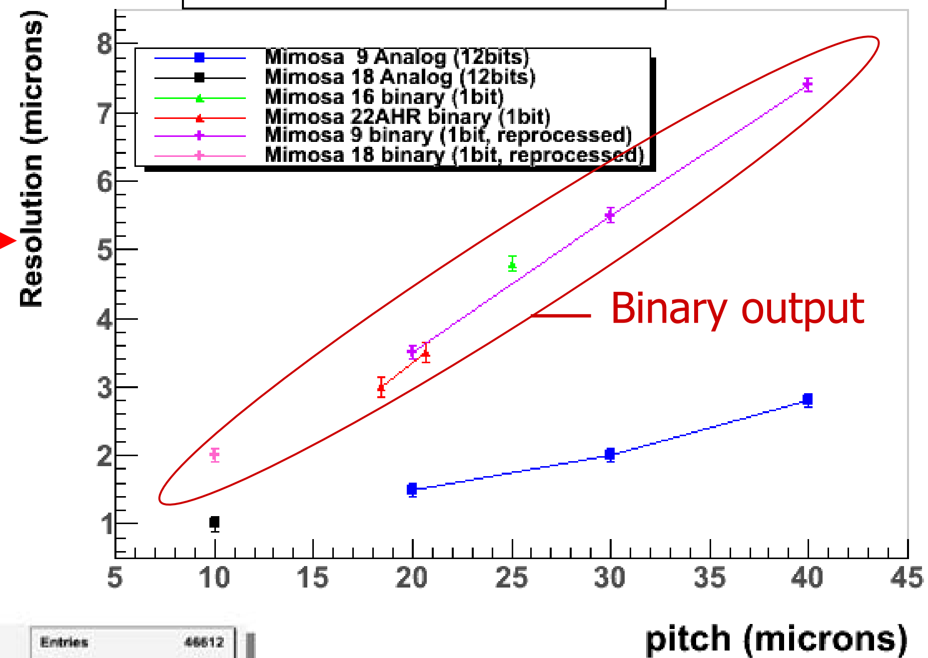


12

Spatial resolution examples

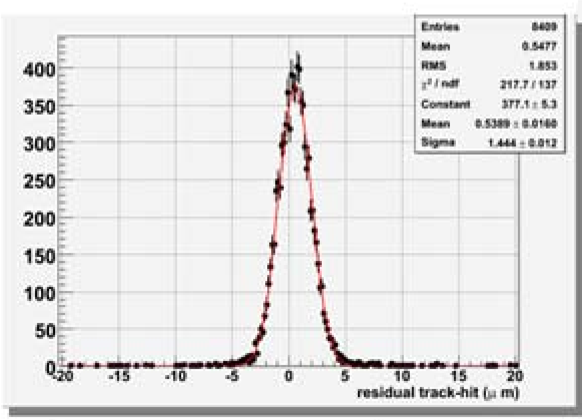
$$\sigma^2_{residual} = \sigma^2_{multiple\ sc.} + \sigma^2_{track\ resolution} + \sigma^2_{spatial\ resolution}$$

Resolution vs pitch

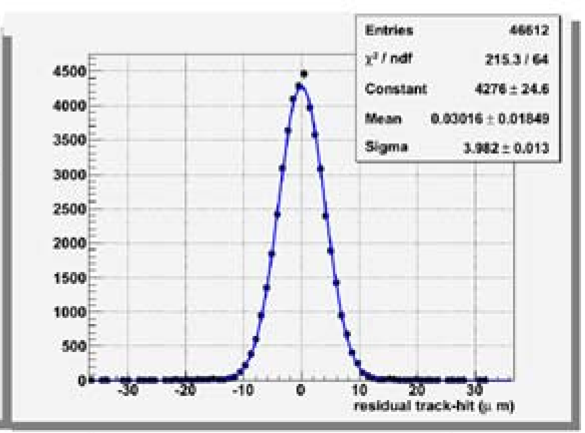


Typical residual

(includes track and m.s. uncertanties)



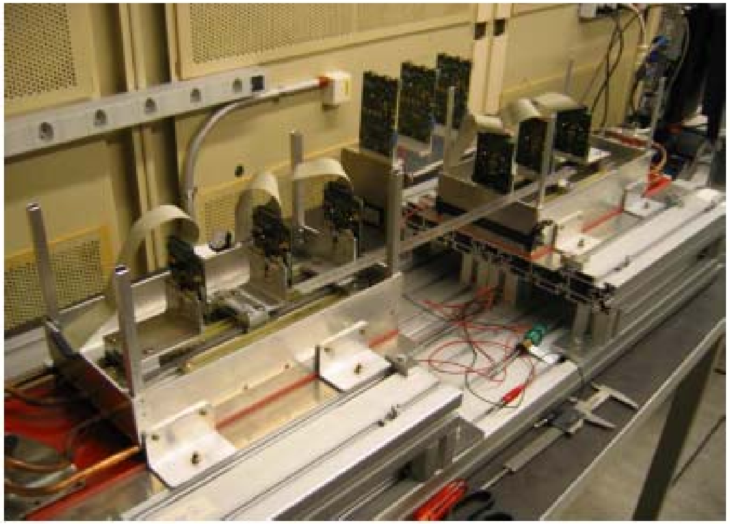
Analog sensor case:
MIMOSA 18, pitch 10 µm



Binary sensor case:
MIMOSA 26, pitch 18.4 µm

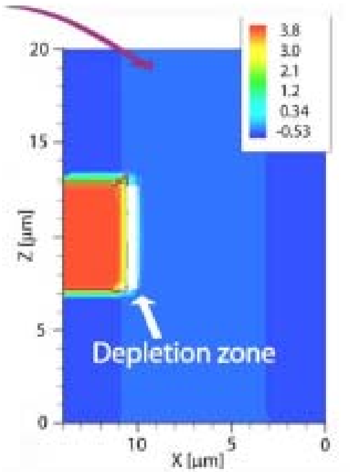
EUDET telescope

- Beam telescope of the FP6 project EUDET
  - ⁎ 2 arms of 3 planes (plus 1-2 high resolution planes)
  - ⁎ MIMOSA-26 thinned to 50 μm
  - ⁎ $\sigma_{extrapol.} \sim$ 1-2 μm EVEN with e^- (3 GeV, DESY)
  - ⁎ frame read-out frequency O(10^4) Hz
  - ⁎ running since '07 (demonstrator: analog outputs)
    at CERN-SPS & DESY (numerous users)



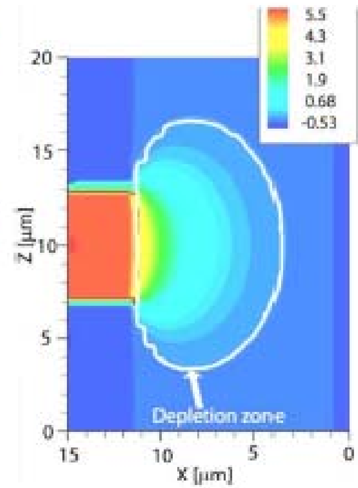
From low to High resistivity

- High resistivity ⇨ larger depleted region ⇨enhance S/N



past ⟶ present

Industrial availability of high resistivity substrate (epi) in a standard CMOS process



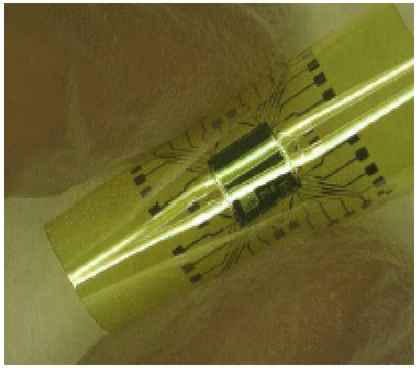
Fast and more efficient charge collection
→ should be radiation tolerant

SERWIETE *SEnsor Raw Wrapped In an Extra-Thin Enveloppe* (HP2, EU-FP7)

Goals :

- to achieve a sensor assembly mounted on flex and wrapped in polymerised film with <0.15 % X_0 for 1 **unsupported layer** (sensors – flex cable – film)

- to evaluate the possibility of mounting supportless ladder on cylindrical surface like beam pipe (used as mechanical support). Proof of principle expected in 2012

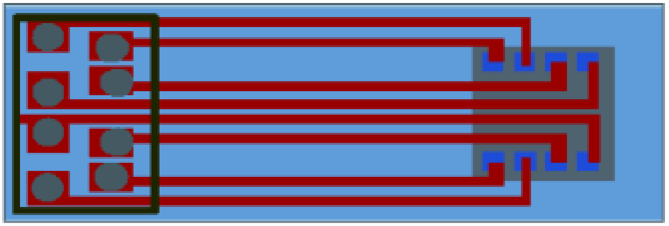


Fully functional microprocessor chip in flexib plastic envelope. Courtesy of Piet De Moo **IMEC company**, Belgiu

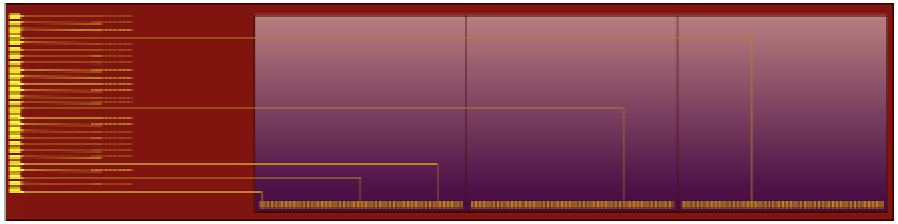
Working program :

- prototype Nr. 1 (2010) made of 1 **analog** sensor : **MIMOSA-18** (analog output, ~4 ms @16MHz)

- prototype Nr. 2 (2011) made of 3 **digital** sensors : **MIMOSA-26** (binary output, ~100 μs @80MHz)



prototype Nr. 1 : April 2010



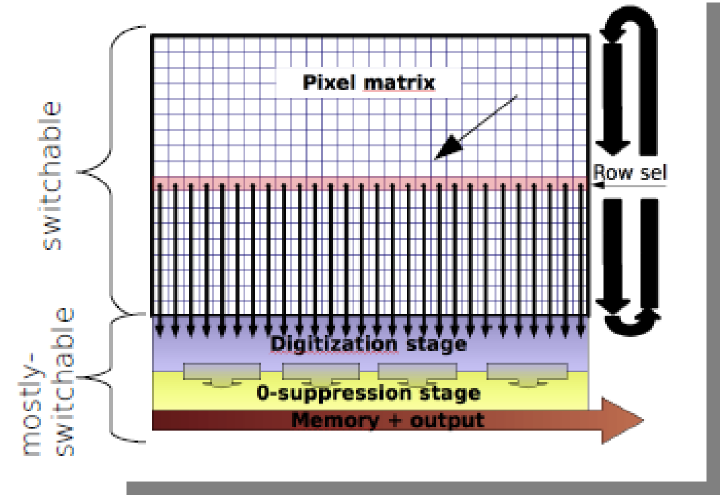
prototype Nr. 2 : summer 2011

Context of development :

- Collaboration with IK-Frankfurt and GSI/Darmstadt (CBM coll.) within **HP2 project** (WP26)
- Synergy with Vertex Detector R&D for CBM, ALICE (?) etc.

Power dissipation and power pulsing (ILC example)

- **Pulsing strategy**
  - Activity period ~ 2 to 4 ms over the 200 ms train
    - ➔ Estimated duty cycle range: 1/50 to 1/100
  - For stability reasons, not all element switchable
    - ➔ Test started for the analog part
    - ➔ To be done for the digital circuitry



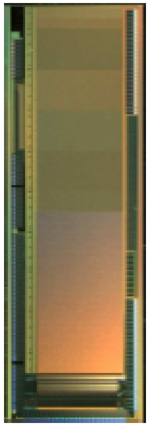
Assuming: 0.18µm techno. & 1.8 V voltage & continuous operation		sensor switch.	sensor not-swi.	sensor total	2-sided ladder switch.	2-sided ladder not-swi.	2-sided ladder total	whole detector switch.	whole detector not-swi.	whole detector total
inner layer	power (W)	1,575	0,025	1,6	18,9	0,3	19,2	688 W	12 W	700 W
	current (A)	0,875	0,014	0,89	10,5	0,17	10,67			
outer Layers	power (W)	0,490	0,010	0,5	5,88	0,12	6	382 A	7 A	390 A
	current (A)	0,272	0,006	0,28	3,27	0,07	3,33			

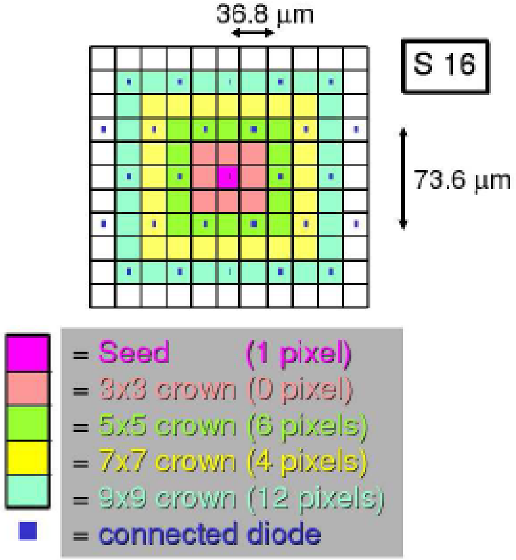
Average power (integrating pulsing) 20 to 30 W

→ Air cooling probably good enough

Elongated pixels and large pitch

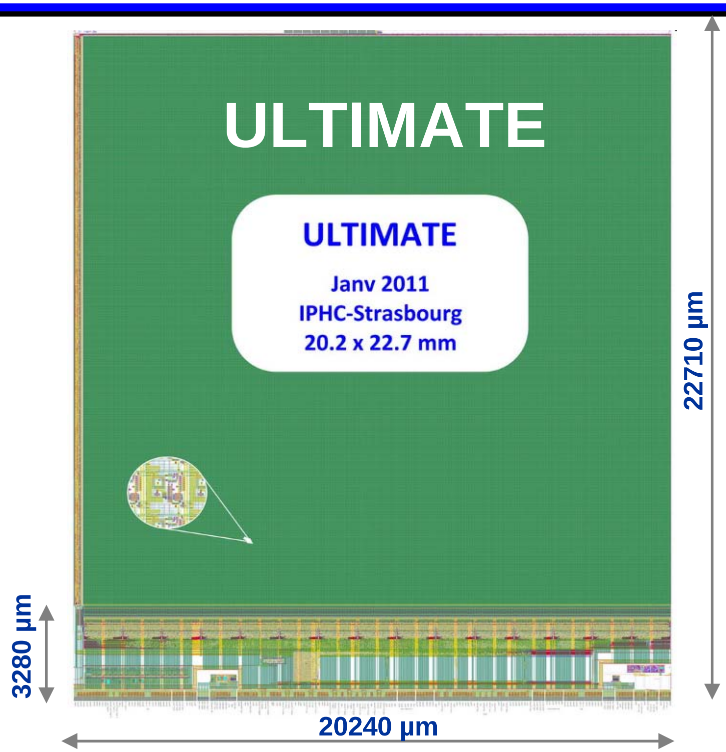
- **Large pitch : Motivations**
  - ⋇ trackers require $\sigma_{sp} \gtrsim 10\ \mu m$ ⋇ calorimeters require O(100×100) μm^2 cells
    - ⇛ minimise number of pixels for the sake of power dissipation, integration time and data flow
- **Large pitch : Limitations**
  - ⋇ DANGER: increasing distance inbetween neighbouring diodes
    - ⇛ particles traversing sensor "far" from sensing diodes may not be detected because of e^- recombination
  - ⋇ "fragile" detection efficiency, exposed to losses due to irradiation, high temperature operation & slow read-out
- **Elongated pixels : Test results**
  - ⋇ elongated pixels allow minimising the drawbacks of large pitch
  - ⋇ concept evaluated with MIMOSA-22AHR prototype, composed of a sub-array with 18.4×73.6 μm^2 pixels ▷▷▷
  - ⋇ m.i.p. detection performances assessed at CERN-SPS (T ∼ 15°C)
    - ⊸ $\epsilon_{det} \sim 99.8$ %
    - ⊸ $\sigma_{sp} \sim$ 5-6 μm (binary charge encoding)
- **Square pixels : prototype under fabrication**
  - ⋇ MIMOSA-29 being fabricated on high-res epitaxy
  - ⋇ pixels of $\leq 80 \times 80\ \mu m^2$





Ultimate

- Process Austria Micro System AMS-C35B4/OPTO uses 4 metal- and 2 poly-layers.
- The thickness of the epitaxial layer stretches out up to 15 µm in Hi-Resistivity substrate (400 Ohm.cm)
- Full reticle 960 x 928 pixel matrix
  - Longer integration time ~200 µs
- size of the chip of 20.22 mm x 22.71 mm
- Temperature 30-35 °C
- Power consumption ~100 mW/cm²
- Space resolution < 10 µm
- 150 kRad / yr & few 10^{12} Neq /cm² /yr

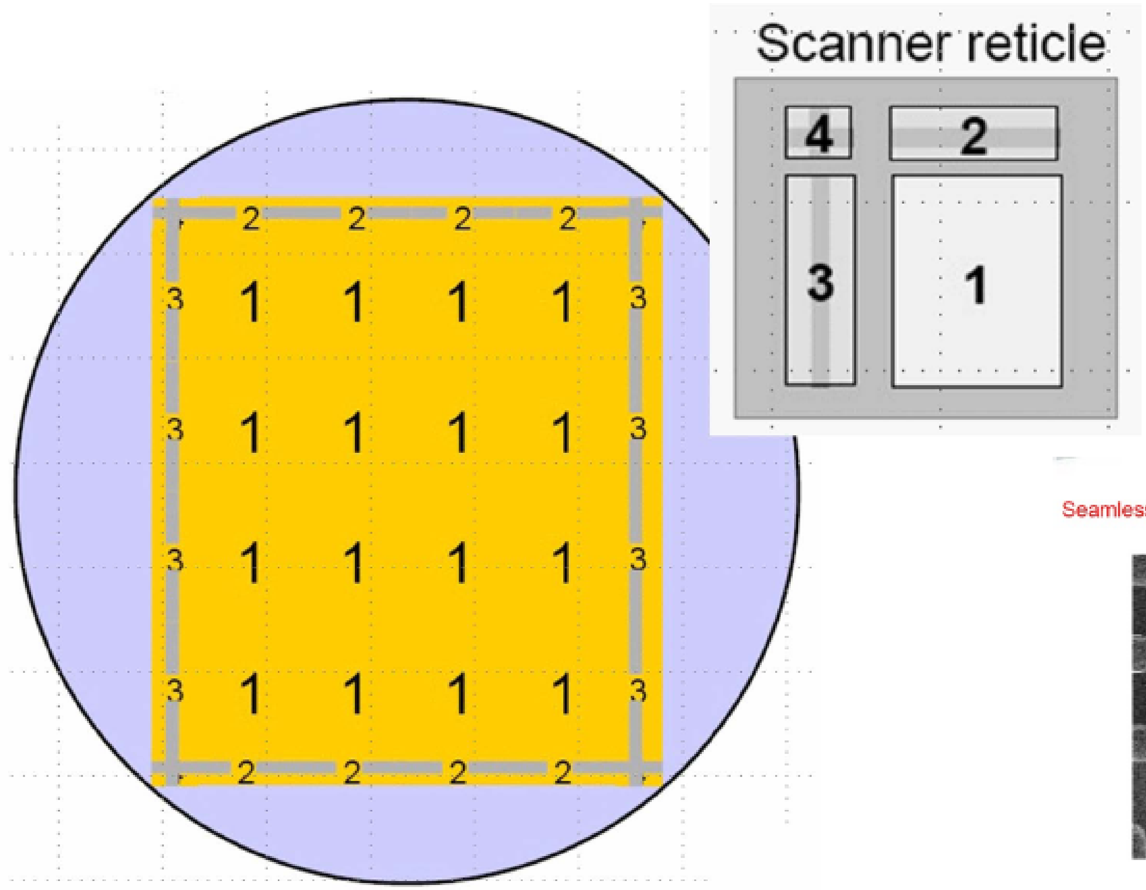


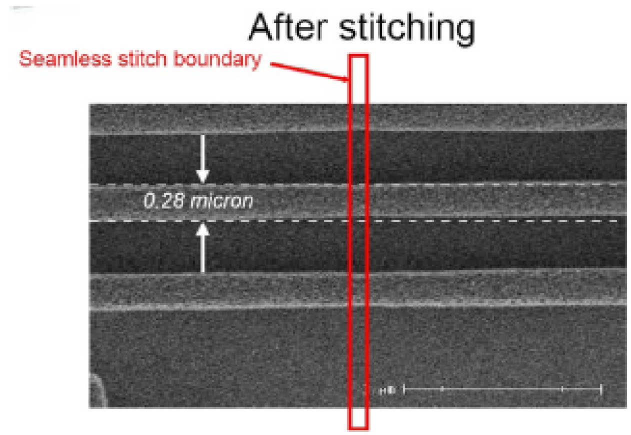
Luminosity = 8 x 1027 / cm² / s at RHIC_II

~200-300 (600) hits / sensor (~4 cm2) in the integration time window

Shot integration time ~< 200 µs

Future techniques: stitching ("one die per wafer")





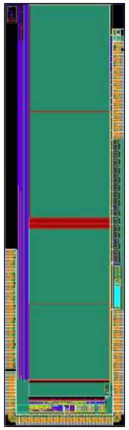
Maximum length of monolithic ladder (8' wafer): 10 –15 cm

ULTIMATE Design & Optimisation (1)

- ***Reduction of power dissipation:***
  - *Power supply voltage reduced from 3.3 to 3 V*
  - *Optimisation of pixel pitch v.s. non ionising radiation tolerance*
    - *Larger pitch: 18.4 µm ➔ 20.7 µm*
      - *Shorter integration time: 185.6 µs*
    - ➔ *Validated by a small prototype*
  - *Optimisation of power consumption of some blocks*

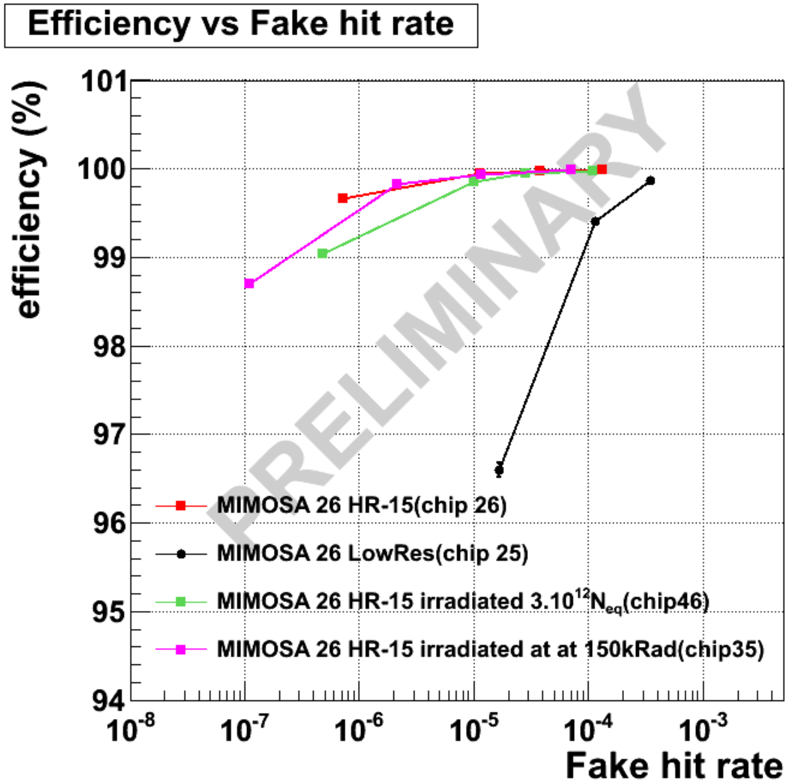
➔ *Estimated power consumption ~130 mW/cm²*

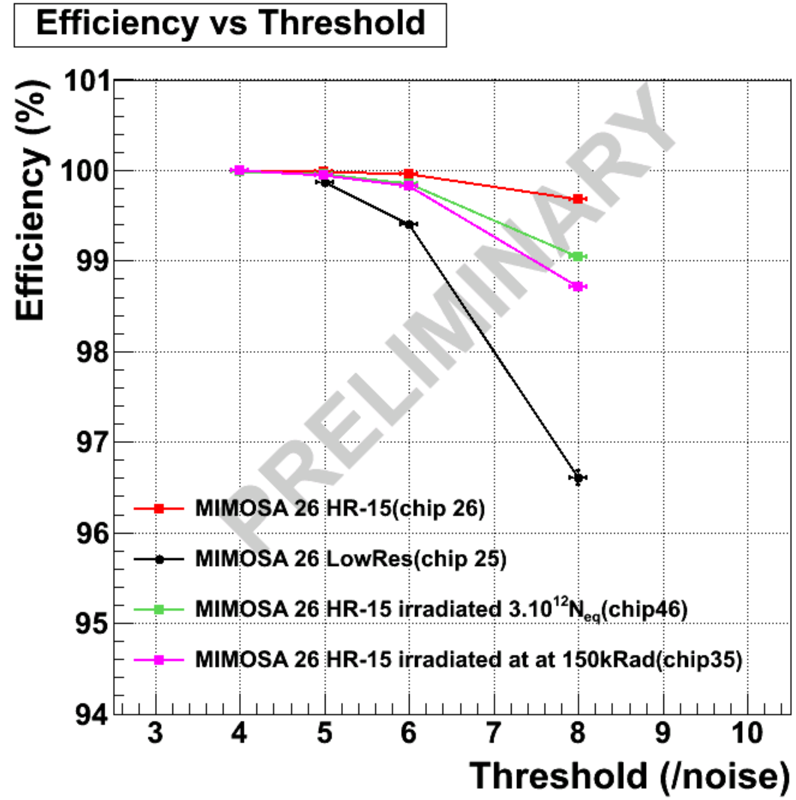
- ***Pixel improvement: charge collection, radiation tolerance***
  - *High resistivity EPI substrate & radiation tolerance design*
    - *Lab test with ^{55}Fe at 35 °C and integration time imposed by the STAR requirements shows:*
      - *Conversion gain is improved by a factor of two*
      - *ENC >~ 10 e^- before irradiation*
      - *ENC >~ 13 e^- after irradiation with 150 kRad*
      - *ENC >~ 16 e^- after irradiation with 3 x 10^{12} Neq/cm²*
      - *SNR up to 30 after irradiation*
SNR ~30 for standard resistivity EPI before irradiation
    - *Beam test measurements are in progress*
      - *Preliminary results show further performance improvements*



MIMOSA26 with high resistivity EPI layer (2)

- ***Beam test at CERN SPS (120 GeV pions)***
  - *Test conditions:*
    - *50 MHz to emulate the longer integration time in ULTIMATE*
    - *35 °C temperature!*





resolution < 5um