

ATLAS-IBL: a challenging first step for ATLAS Upgrade at the sLHC

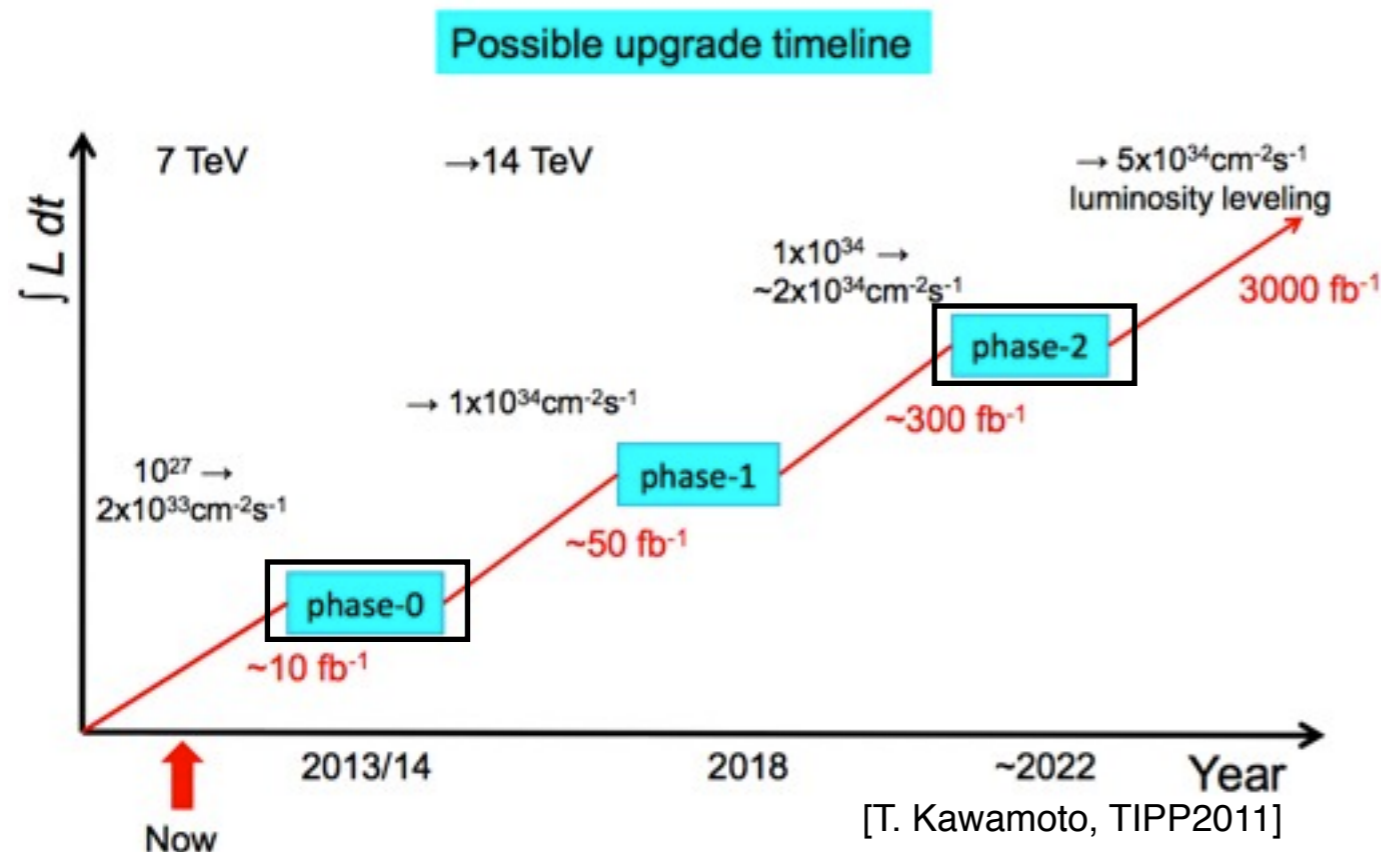
A. La Rosa / U. Wisconsin and CERN
on behalf of the ATLAS Collaboration

International Europhysics Conference on High Energy Physics.
Grenoble, France July 21-27 2011.



Why Upgrades ?

- LHC/ATLAS physics goals
 - Improve standard model (SM) measurements (W, Z, top)
 - Higgs: understand the electroweak symmetry breaking
 - Beyond the SM: SUSY, extra dimension, even something totally new
- **Whatever will be discovery in the next years at LHC, need much data to understand what has been discovered**
- Higher luminosity allows extending discovery/ studies to higher masses and processes of lower cross-section
- LHC has plans of upgrade by increasing luminosity to collect ultimately $\sim 3000 \text{ fb}^{-1}$



- **Consequence:**
 - higher data rate
 - higher occupancy
 - more radiation damage
- **Detector upgrade are necessary due to:**
 - improve TDAQ
 - finer granularity to limit occupancy
 - more rad-hard sensors and electronics

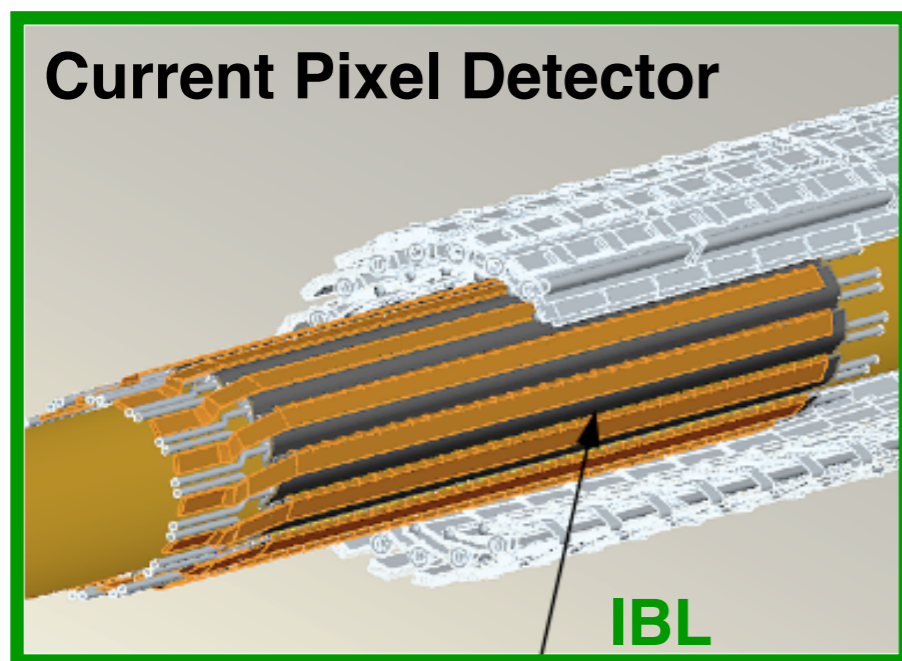
In this talk:

- Phase-0: new Pixel layer (IBL);
- Phase-2: Overview of new Silicon Inner Tracker.

Calorimeter and Muon Systems will be also upgraded (their projects are not treated in this talk).

ATLAS Insettable B-Layer (IBL)

- **Installation of new pixel layer (the major project for ATLAS/ Phase-0)**
 - Excellent vertex detector performance is crucial:
 - improve heavy flavor tagging, primary and secondary vertex reconstruction/ separation
 - Additional innermost layer will boost tracking performance
 - adds additional redundancy of the detector in case of radiation damage
 - Idea: Insertion of new pixel layer inside current Pixel detector: Insettable B-Layer (IBL)
 - Phase-1 was initially in 2016 and now is postponed to 2017 or 2018
 - Advance the project schedule and **install it in 2013/14**.



**Two competing sensor technologies:
Planar and 3D pixel sensors.**
*Diamond tech was dropped: sensors
production not compatible with IBL in 2013*

IBL mounted on new beam-pipe

Length: ~64cm

Envelope: $R_{IN}=31\text{mm}$, $R_{OUT}=40\text{mm}$

14 staves, each stave: 32 FE-I4 chips

- for 3D sensors: 1 sensor + 1 chip = 1 module

- for Planar sensors: 1 sensor + 2 chips = 1 module

Total: 448 3D modules or 224 planar modules

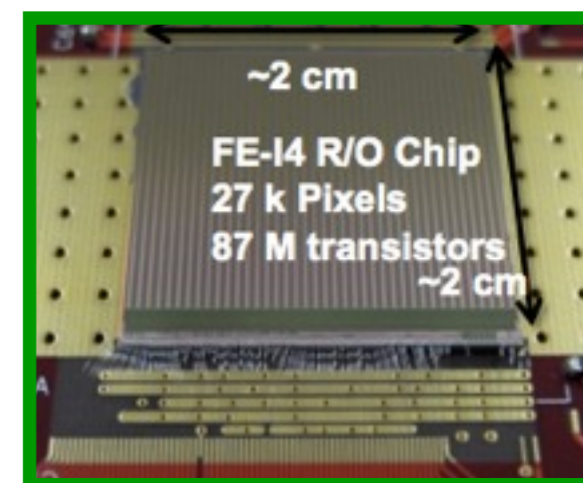
FE-I4 R/O chip

- IBM 130nm CMOS tech.

- cel size: 50um x 250um

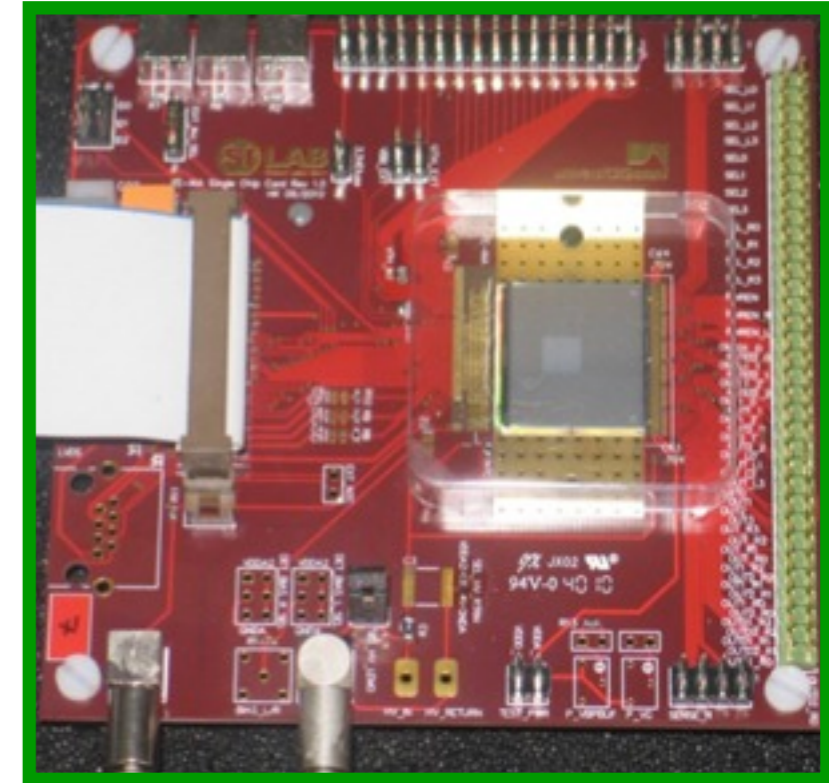
- 80 (col) x 336 (row) = 26880 cels

- 2cm x 2cm



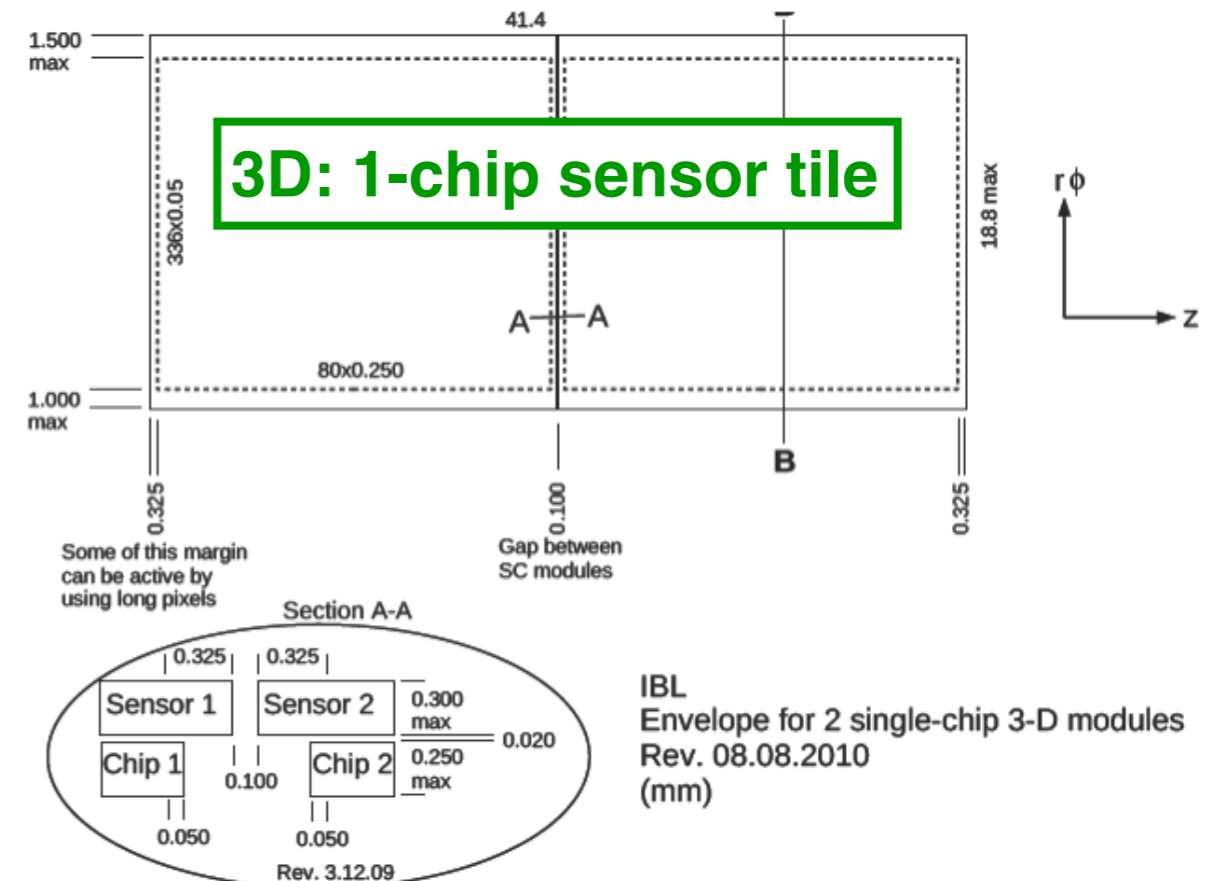
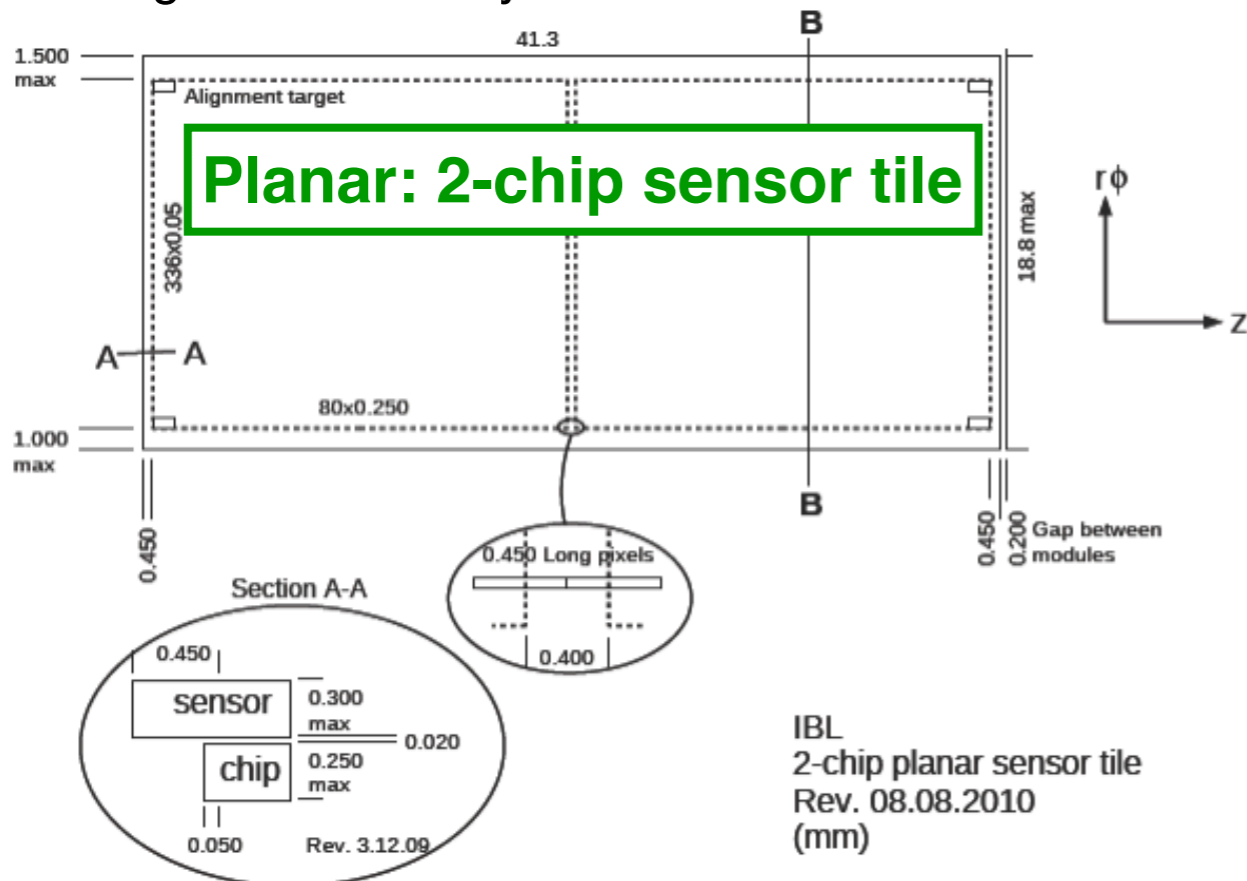
IBL sensor specs and module prototyping

	PLANAR	3D
Active size W x L [mm ²]	16.8 x 40.9	16.8 x 20.0
Total size W x L [mm ²]	18.54 x 41.27	18.8 x 20.5
Thickness [mm]	0.20	0.23
Typical depletion voltage [V]	< 35	<15
Typical initial operation voltage [V]	60 (V _{dep} +30V)	25
At of at end of lifetime [V]	1000	180



Sensor specifications for IBL:

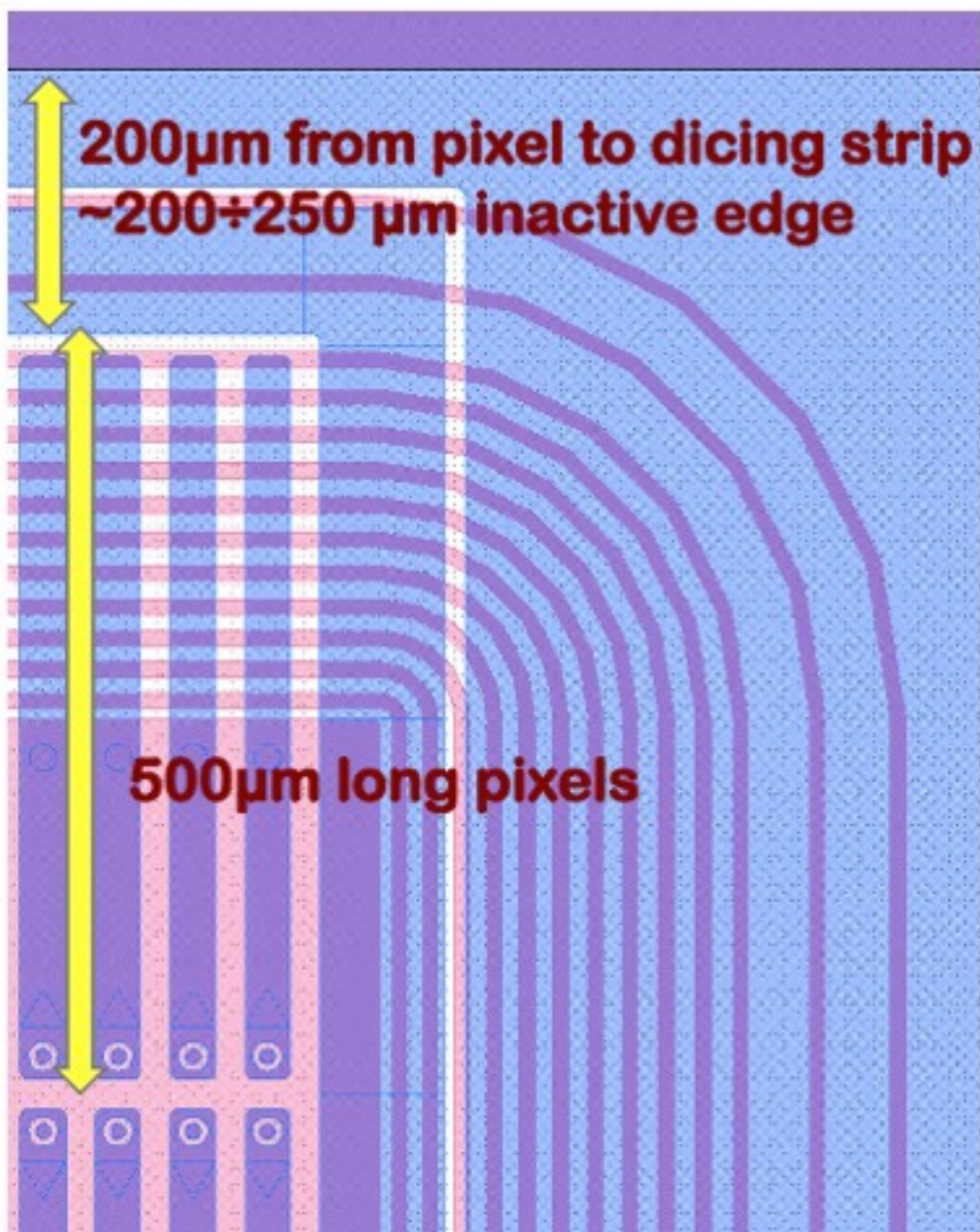
- qualify to $5 \times 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$
- sensor max. power dissipation: 200 mW/cm² at -15 °C
- single-hit efficiency > 97%



IBL sensor types

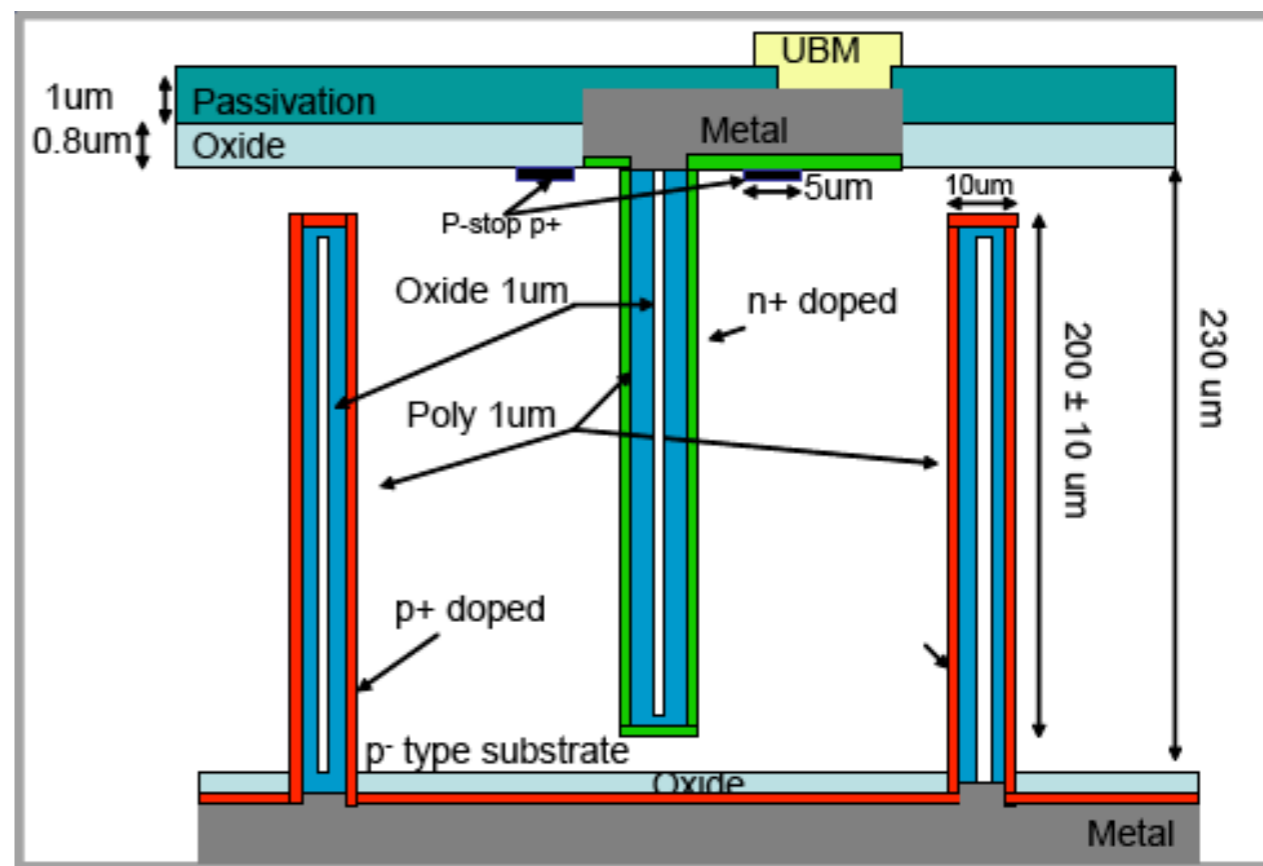
Planar n-in-n Slim Edge Design (CiS)

- minimize inactive edge by shifting the guard-rings underneath active pixel region
 → 200 - 250 μm inactive edge achievable
- manufactured by CiS like present Pixel



3D Slim Edge Design (FBK and CNM)

- column through ~full bulk with 2 electrodes per pixel (so-called 2E-type)
- depletion horizontally (short depletion width leads to low bias voltage)
- manufacturing yield now being tested with pre-production runs by FBK and CNM



Irradiation

- A total of 77 modules (bump-bonded & assemblies) have been produced
 - 40x Silicon 3D
 - 37x Silicon Planar n-in-n
- Several irradiation campaigns have been performed
 - 11x IBL 1-chip modules (3D+Planar) have been irradiated at IBL target fluence ($5 \times 10^{15} \text{neq/cm}^2$)
 - Proton irradiation at KIT (nominal beam energy: 23 MeV)
 - *Due to the low energies used the ionizing radiation damage to the FE went well beyond the requirements (250 Mrad). Estimated TID: ~750 Mrad (with 23 MeV) and ~1Grad (with ~18 MeV)*
 - Neutron irradiation with n-TRIGA reactor in Ljubljana

FE-I4 Assemblies for Sensor Review

Foundry	Technology	Batch ID	Thickness (μm)	Sensor EdgeType	Number of Assemblies			Target Fluence (neq/cm ²)
					Done	p-irradiated	n-irradiated	
CiS	Planar n-in-n	<n-in-n 150>	150	slim	2	1		2 x 10e15
				conservative	2			
		<n-in-n 200>	200	slim	12	3	2	5 x 10e15
				conservative	2		1	5 x 10e15
		<n-in-n 250>	250	slim	9	1	2	5 x 10e15
				conservative	10		1	5 x 10e15
CNM	3D, double side	5306	230	slim	16	1		2 x 10e15
						3	2	5 x 10e15
FBK	3D, double side	ATLAS 07	230	slim	8			
	3D, double side	ATLAS 09	230	slim	16	1		2 x 10e15
						1		5 x 10e15
<i>Total Planar</i>					37		11	
<i>Total 3D</i>					40		8	
Grand Total					77		19	

Green: IBL Design

Test-beams

- Three test-beam periods:
 - February and April in DESY
 - June at CERN
- Most of devices ready/ prepared for CERN test-beam
 - original 24 days, then reduced due to TAX problem and rescheduled. Very short beam time finally delivered ~100 hours (2.5 days) !

Test Beam	Beam type	Sensor Techn	Measured devices		Angle (degree)		B-field
					0	15	
Desy Feb	4 GeV electrons	Planar	█	█	█	█	
		3D-CNM					
		3D-FBK					
Desy Apr	4 GeV electrons	Planar	█	█	█	█	█
		3D-CNM					
		3D-FBK	█	█	█	█	
CERN June	180 GeV pions	Planar-CiS	█	█	█	█	█
		3D-CNM	█	█	█	█	
		3D-FBK	█	█	█	█	

Legend

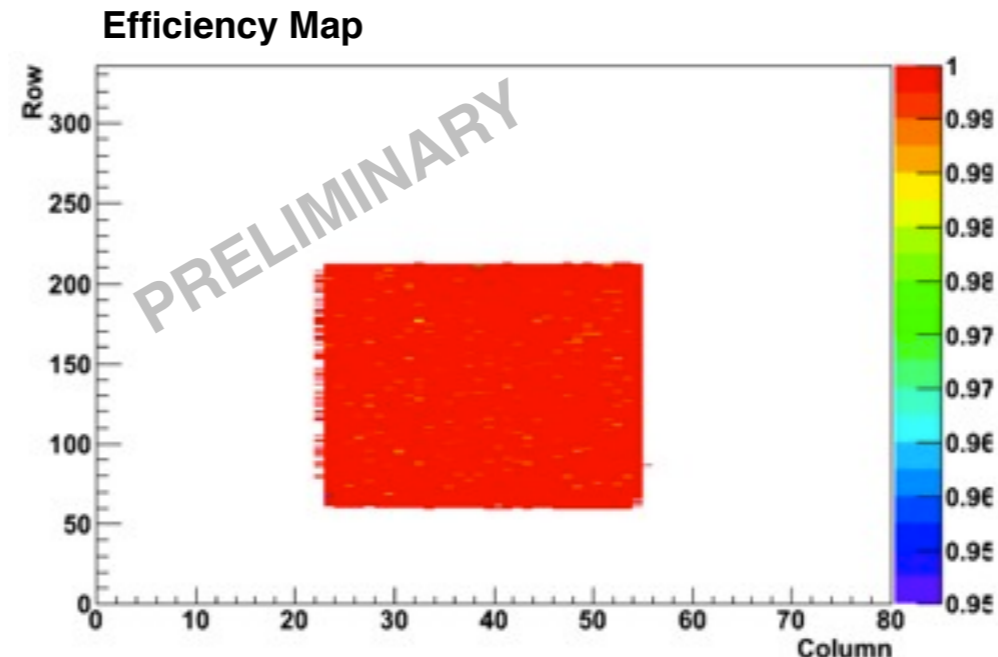
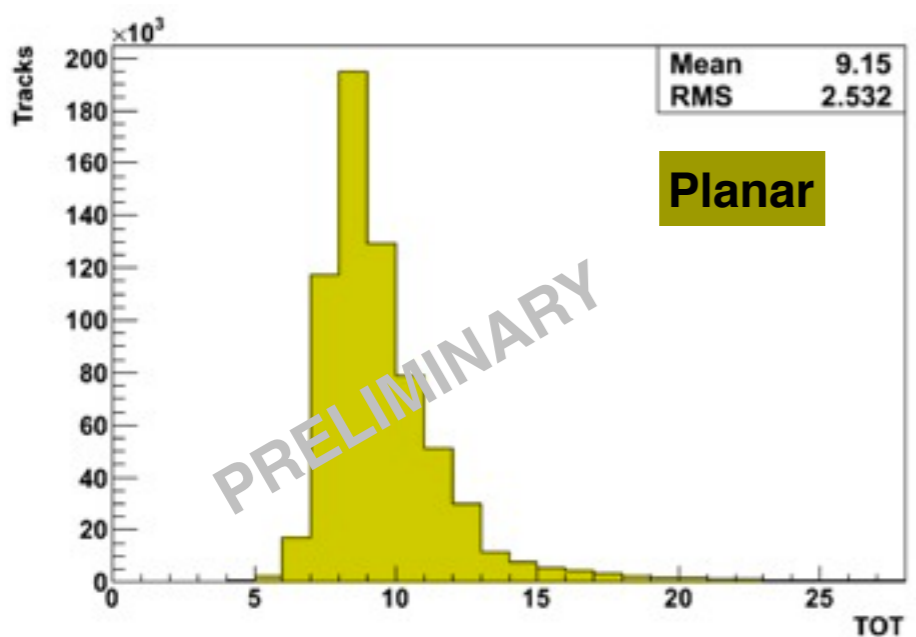
- Non-irradiated █
- p-irradiated 2e15 █
- p-irradiated 5e15 █
- n-irradiated 5e15 █



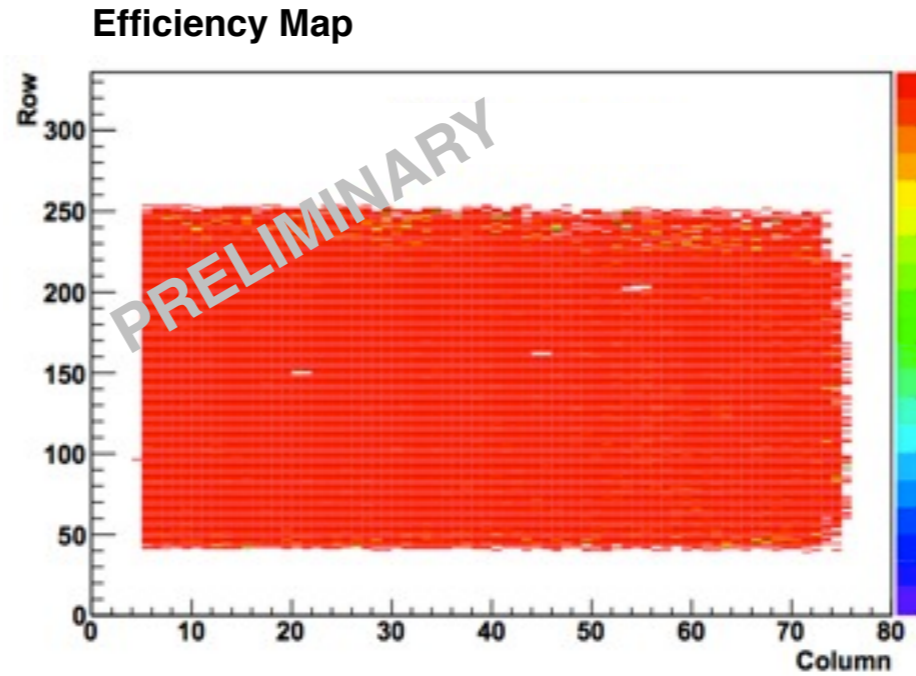
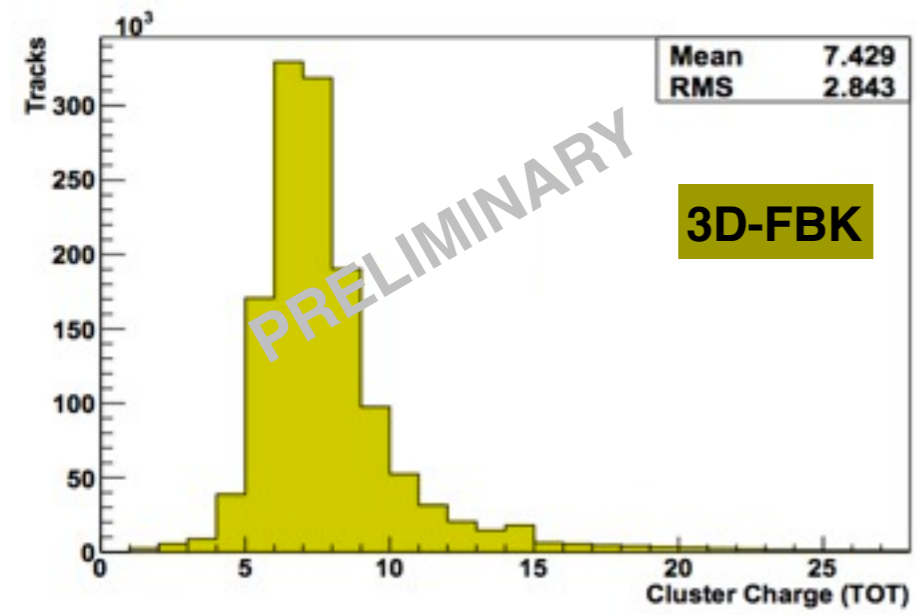
Preliminary: Unirrad sensors + FE-I4 at DESY TB



Charge collected measured in units on 25ns of Time over Threshold (TOT)



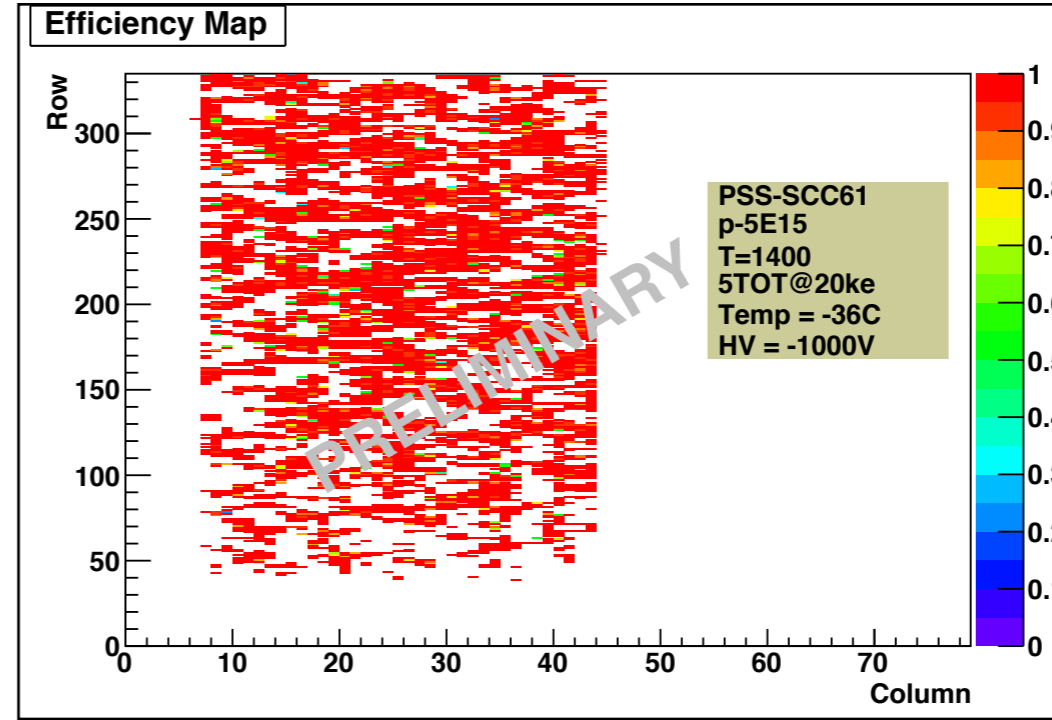
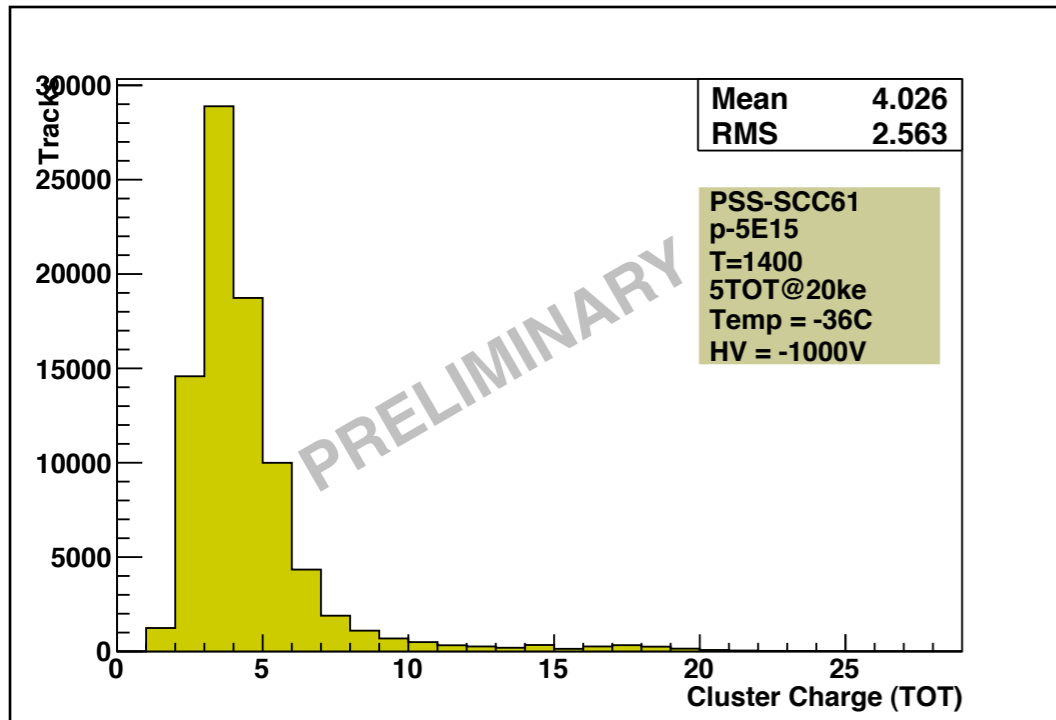
Planar 250um thick
Calibration 10TOT at 30ke
larger than expected (under investigation !)
A few noisy/dead pixel
Hit efficiency: 99.95%



3D-FBK 230um thick
TOT distribution as expected !
A few noisy/dead pixel
Hit efficiency: 98%,
efficiency loss for tracks going through electrodes (electrodes not filled).

Preliminary: Irrad Planar + FE-I4 at CERN TB

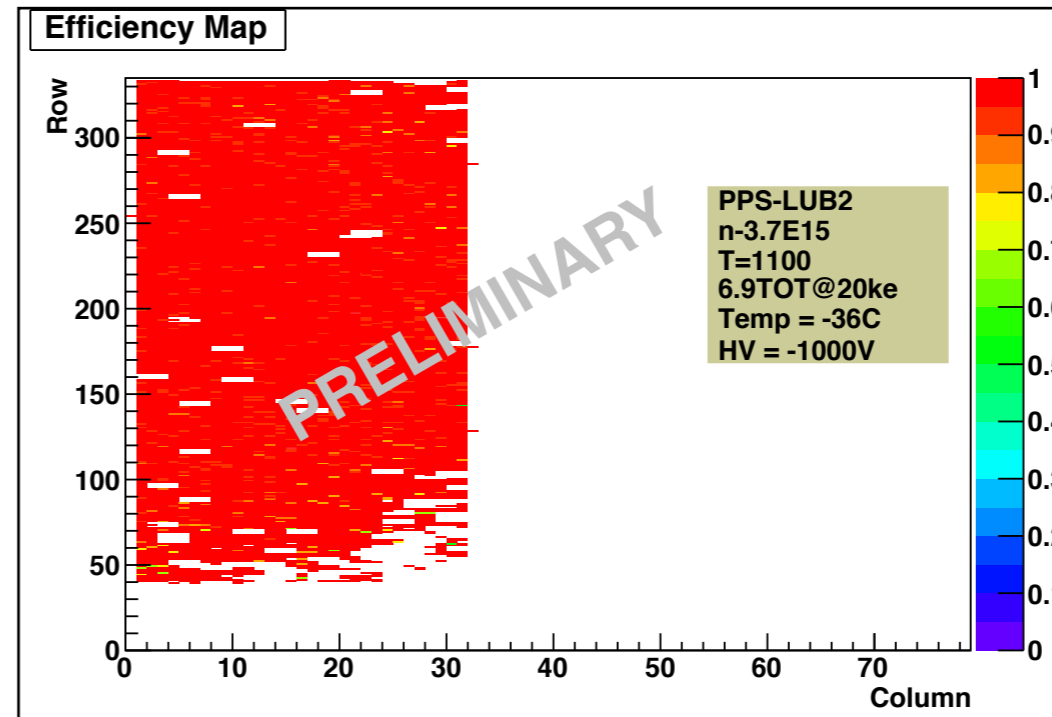
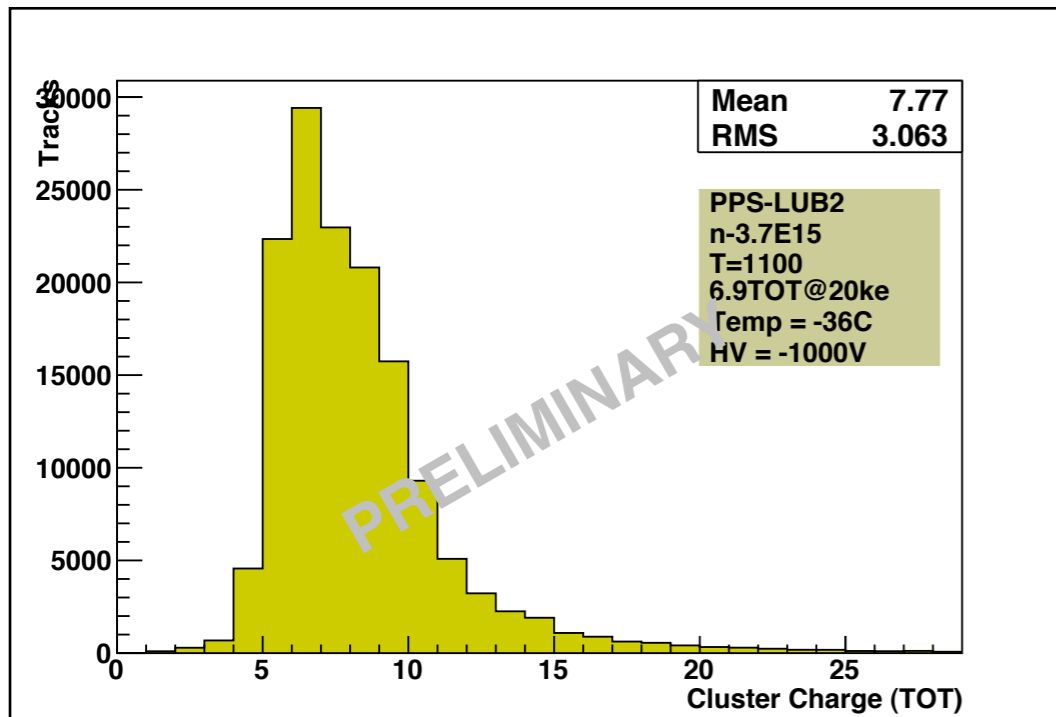
SCC61: Planar 200um thick, p-irrad $6 \times 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$, HV=-1000V, phi=15°



Efficiency Map:
Noise & dead pixel
masked out;
Some (most?) are due
to FE itself (**Large TID**)

*Num. of noisy pixels
(FE/Sensors): 560
Hit efficiency: 96.9%
Overall charge sharing
probability: 43.0%*

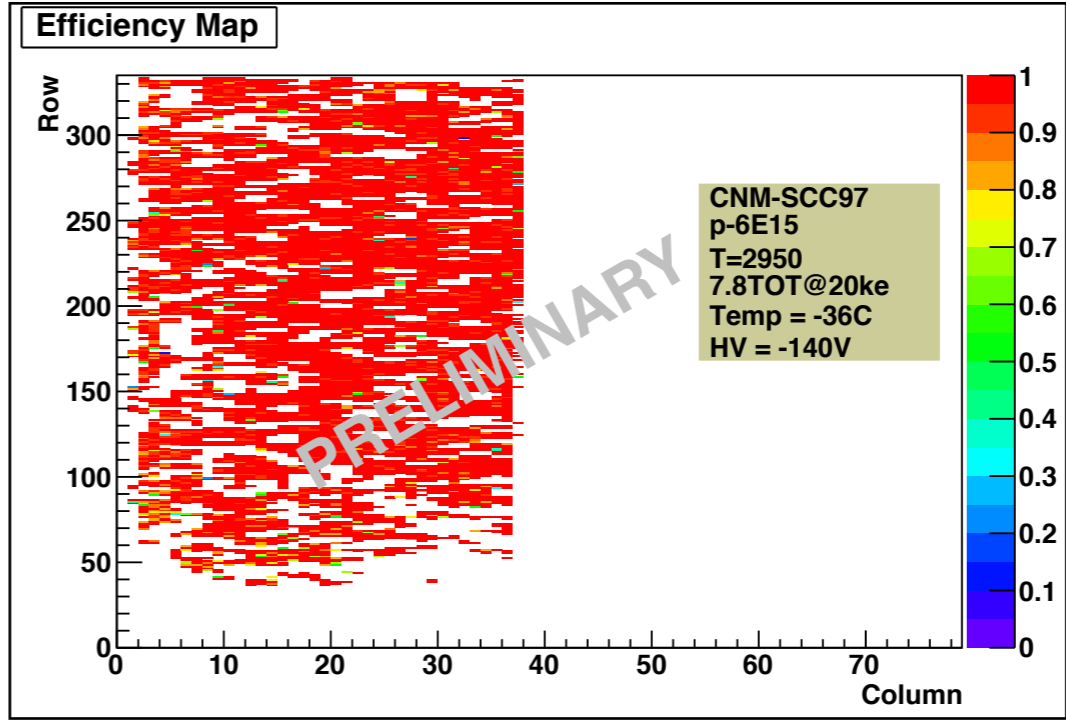
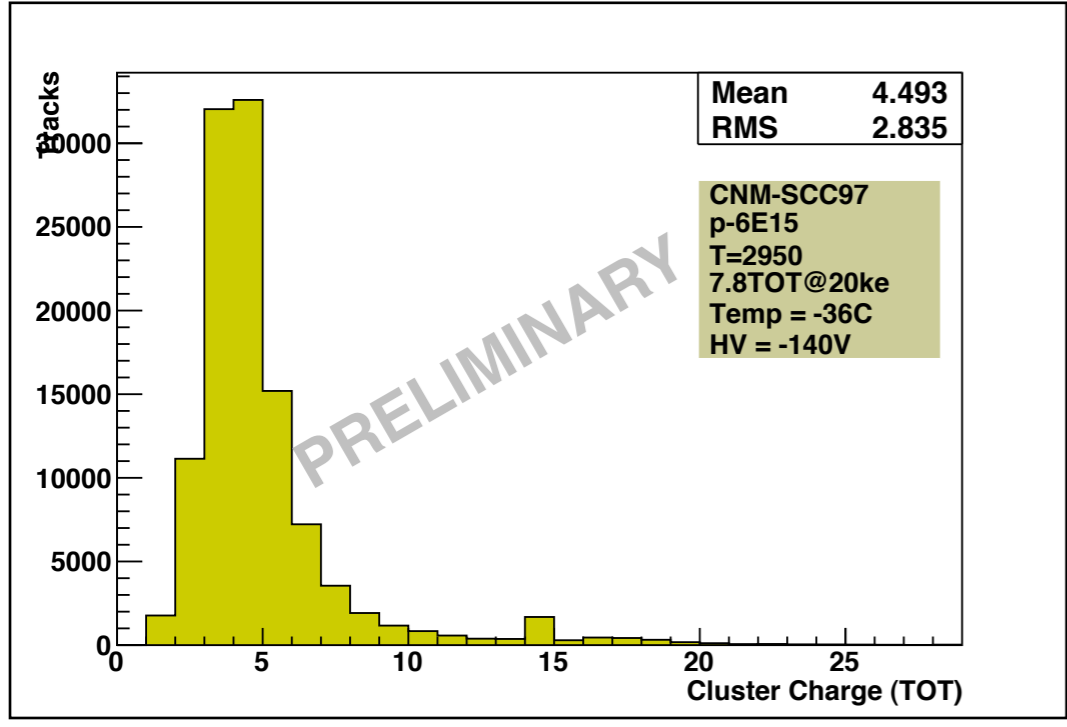
LUB2: Planar 250um thick, n-irrad $4 \times 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$, HV=-1000V, phi=15°



*Num. of noisy pixels
(FE/Sensor): 80
Hit efficiency: 99%
Overall charge sharing
probability: 43.5%*

Preliminary: Irrad 3D + FE-I4 at CERN TB

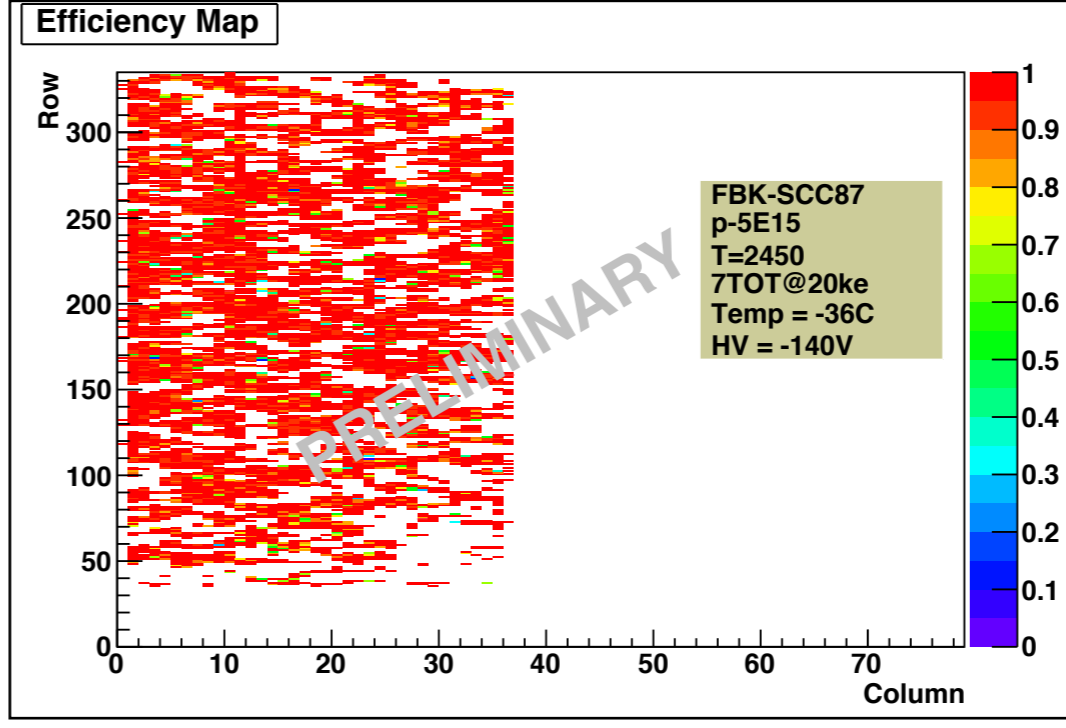
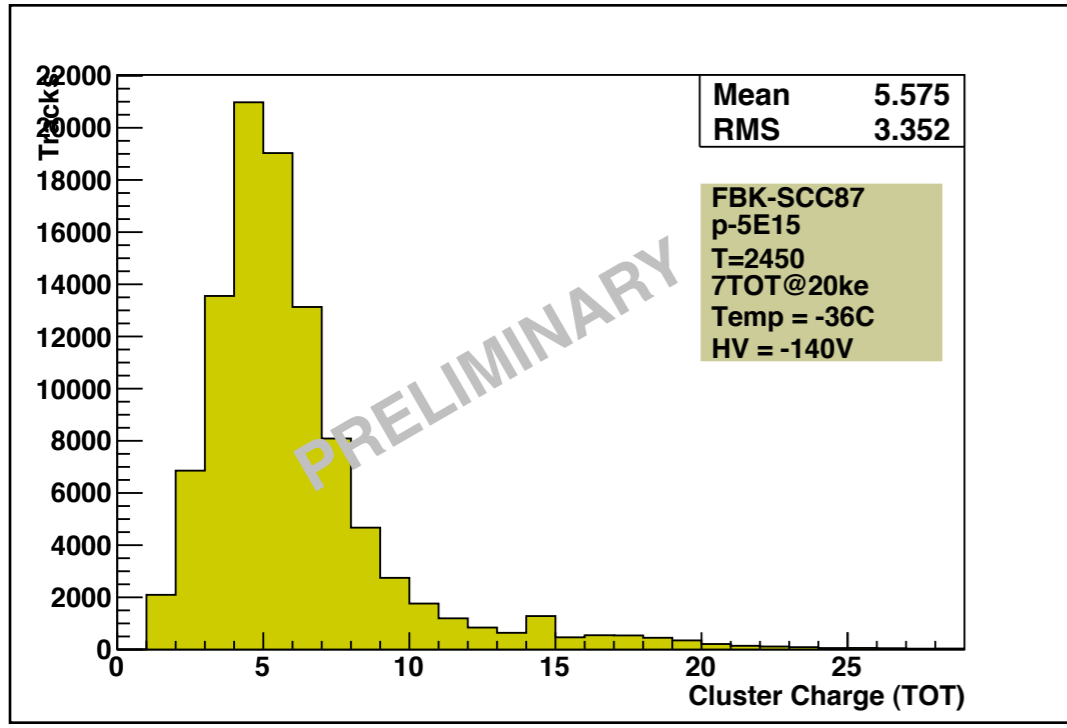
SCC97: 3D-CNM 230um thick, p-irrad 6×10^{15} n_{eq} cm⁻², HV=-140V, phi=15°



Efficiency Map:
 Noise & dead pixel masked out;
 Some (most?) are due to FE itself (**Large TID**)

Num. of noisy pixels (FE/Sensors): 244
Hit efficiency: 97.4%
Overall charge sharing probability: 22.1%

SCC87: 3D-FBK 230um thick, p-irrad 5×10^{15} n_{eq} cm⁻², HV=-140V, phi=15°

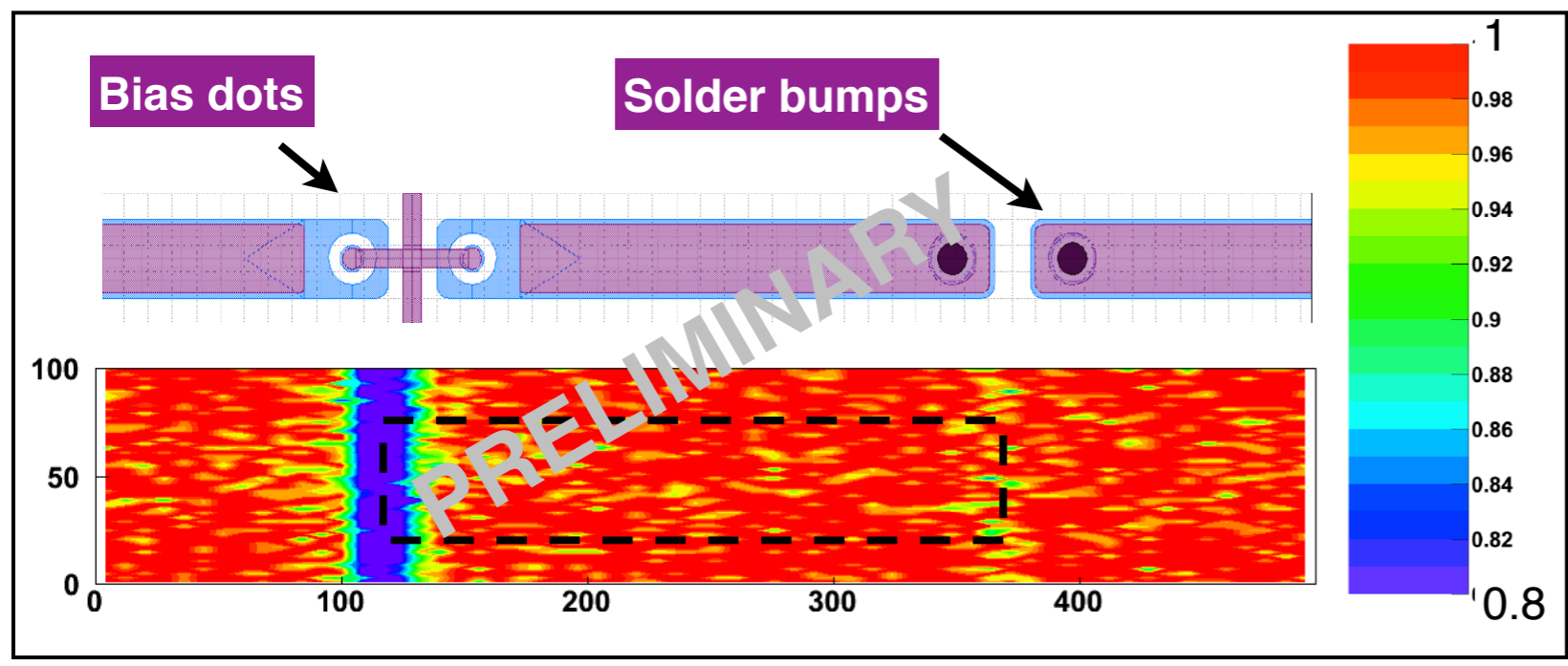


Efficiency Map:
 Noise & dead pixel masked out;
 Some (most?) are due to FE itself (**Large TID**)

Num. of noisy pixels (FE/Sensor): 290
Hit efficiency: 95.3%
Overall charge sharing probability: 39.5%

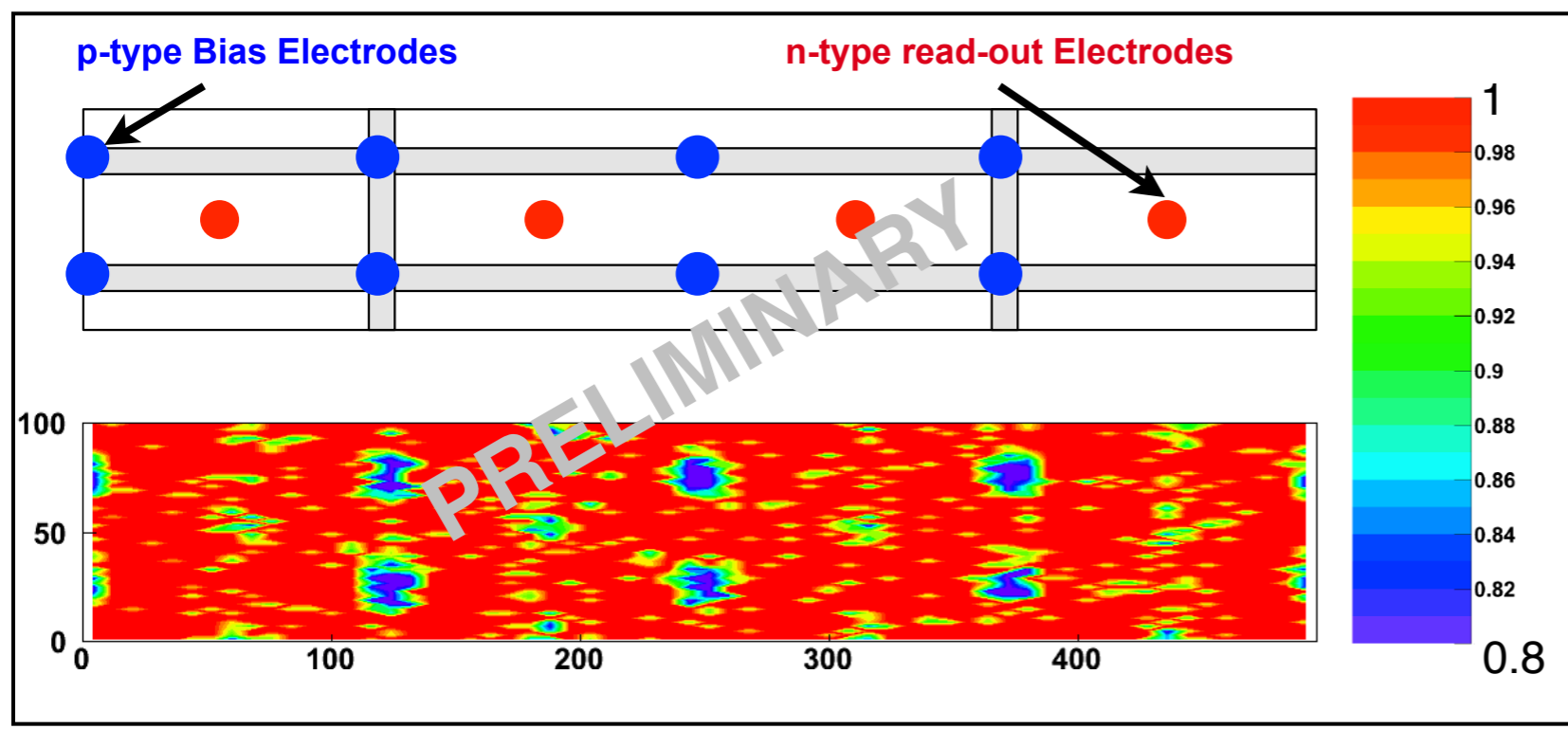
Preliminary: Cell efficiency map

SCC61: Planar 200um thick, p-irrad $6 \times 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$ (Large TID), HV=-1000V, phi=15°



Efficiency distribution within pixel cells.
 Efficiency loss at cell borders mainly due to the charge sharing.
 More charge loss on bias side: trapping in bias dots and grid

SCC97: 3D-CNM 230um thick, p-irrad $6 \times 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$ (Large TID), HV=-140V, phi=0°



Efficiency loss for tracks going through (not filled) electrodes: no charge produced
 Large effect on bias electrodes as lower field.

IBL schedule key dates

Activities	Starting	Ending
FE-I4_B	July 11: Submission	Oct to Dec 11 for wafer test
Bump bonding	Aug 11: pre-production	July 12: Completion
Module assembly	Feb 12: 1 st modules ready for loading	Oct to Dec 12 depending of sensor
Module loading	Feb12: --> 4 staves to be ready by Apr 12	Jan 13: completion
Stave loading	Sept 12: starting with the 1 st available staves	Feb-Mar 13: Completion
Final tests and commissioning	Sept 12	July 13: IBL Installation

[H. Pernegger, VERTEX2011]

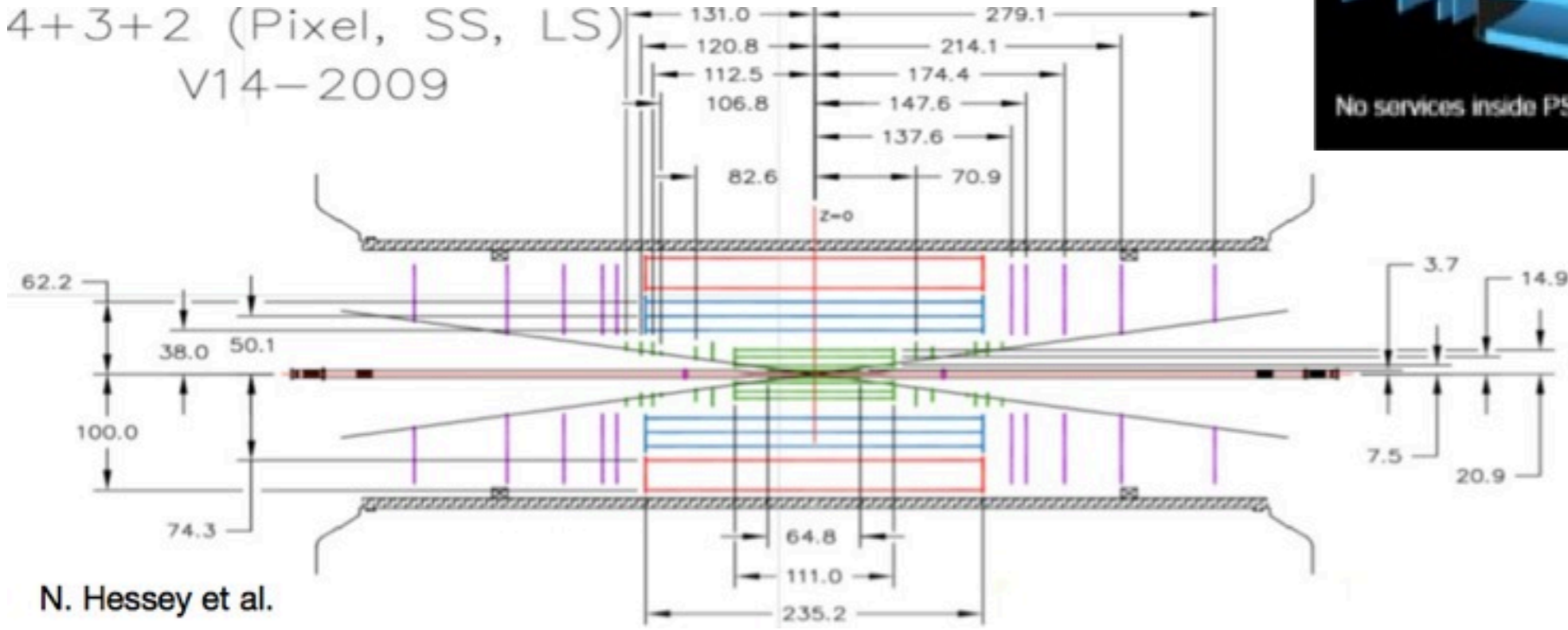
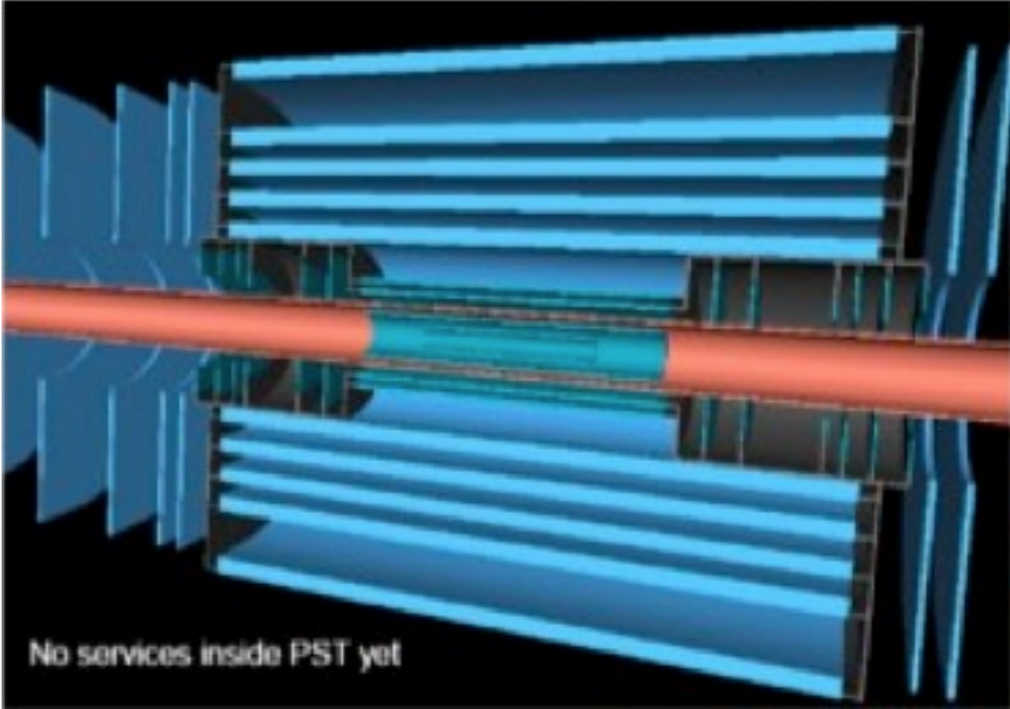
- Tight schedule for installation in 2013, very challenging but possible !

Upgrade for phase-2

- **~2022**: to prepare for the following period of ~10 years after having collected some 100 fb⁻¹ at sqrt(s)=14 TeV. To run at 5x nominal luminosity: 5x10³⁴ with luminosity leveling, collecting a total of 3000 fb⁻¹ and 200 events per beam crossing

[T. Kawamoto, TIPP2011]

- **All new Inner Tracker**
 - higher granularity to keep occupancy low
 - improved material budget
 - baseline: all silicon strip and pixel



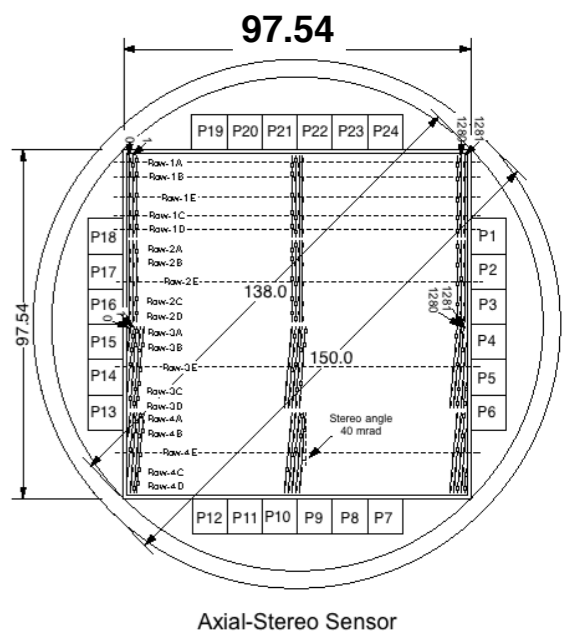
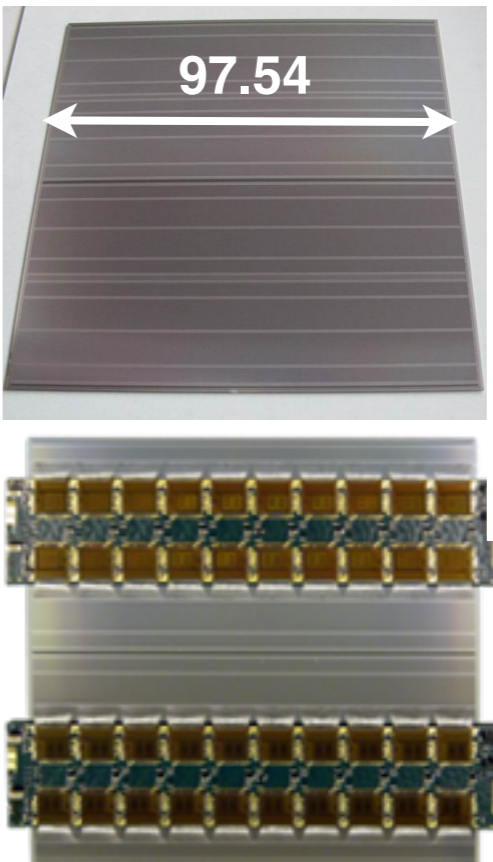
Tracker Layout (under discussion):

- 2 long strip layers
- 2-3 short-strip layers
- 4-5 pixel layers

Strip and Pixel prototyping

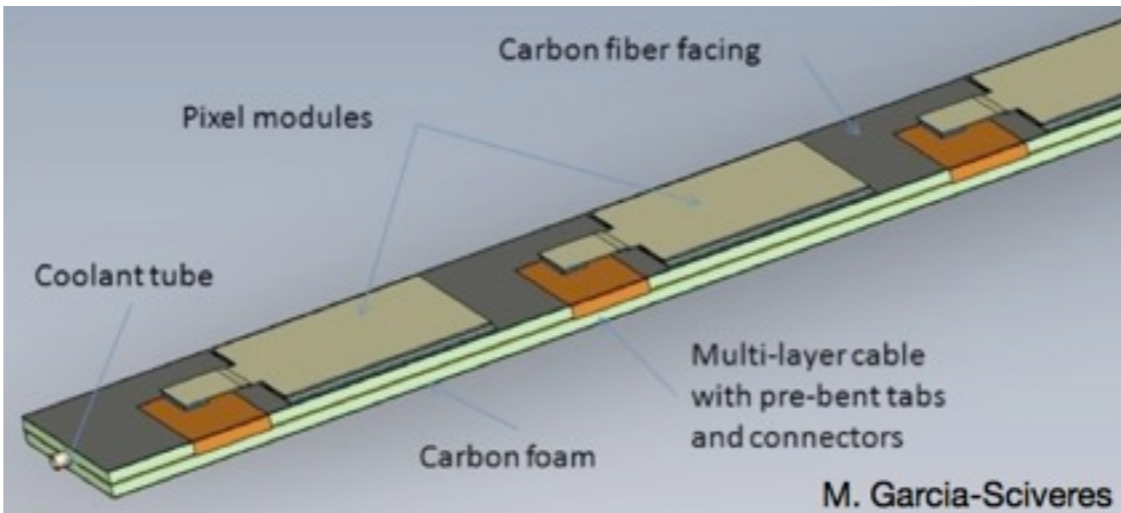
STRIP prototyping

- n-in-p sensors baseline (rad hard verified up to $2 \times 10^{16} \text{ n}_{\text{eq}} \text{ cm}^{-2}$ and with irradi modules up to $2 \times 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$)
- Successful production (ATLAS07 sensors) at Hamamatsu
- Extensive stave prototyping program exists (focused on short-strip)
- New front-end VLSI chip: ABCNext (prototyped in 250um CMOS tech and underway in 130um CMOS tech.)
- Hybrid with FE chips glued directly to sensor
- Sensor glued to cold mechanical support (Stave)



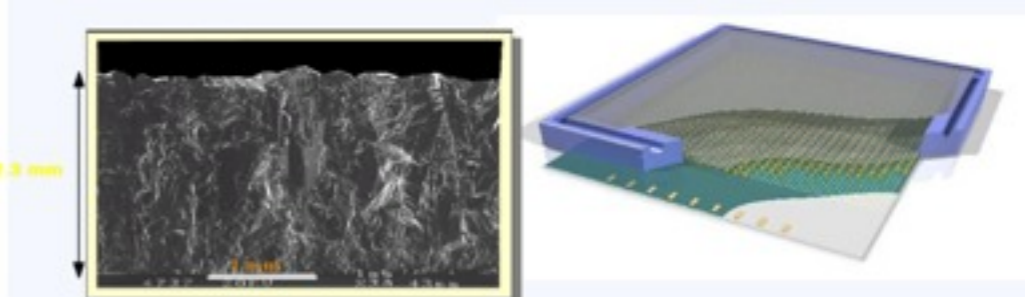
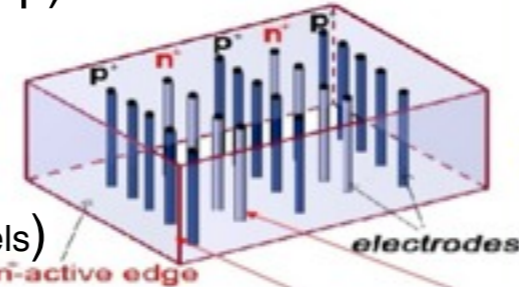
PIXEL prototyping

- Basic concept:
 - double side staves
 - carbon foam
 - flex inside of stave
 - 2x2 MultiChip-Modules



- Several sensors under investigation for radiation hardness
 - outer layers: planar (n-in-n and n-in-p)
 - innermost layer:

Thin Planar, 3D, Diamond and GOSSIP (Gas on Slimmed Si-Pixels)

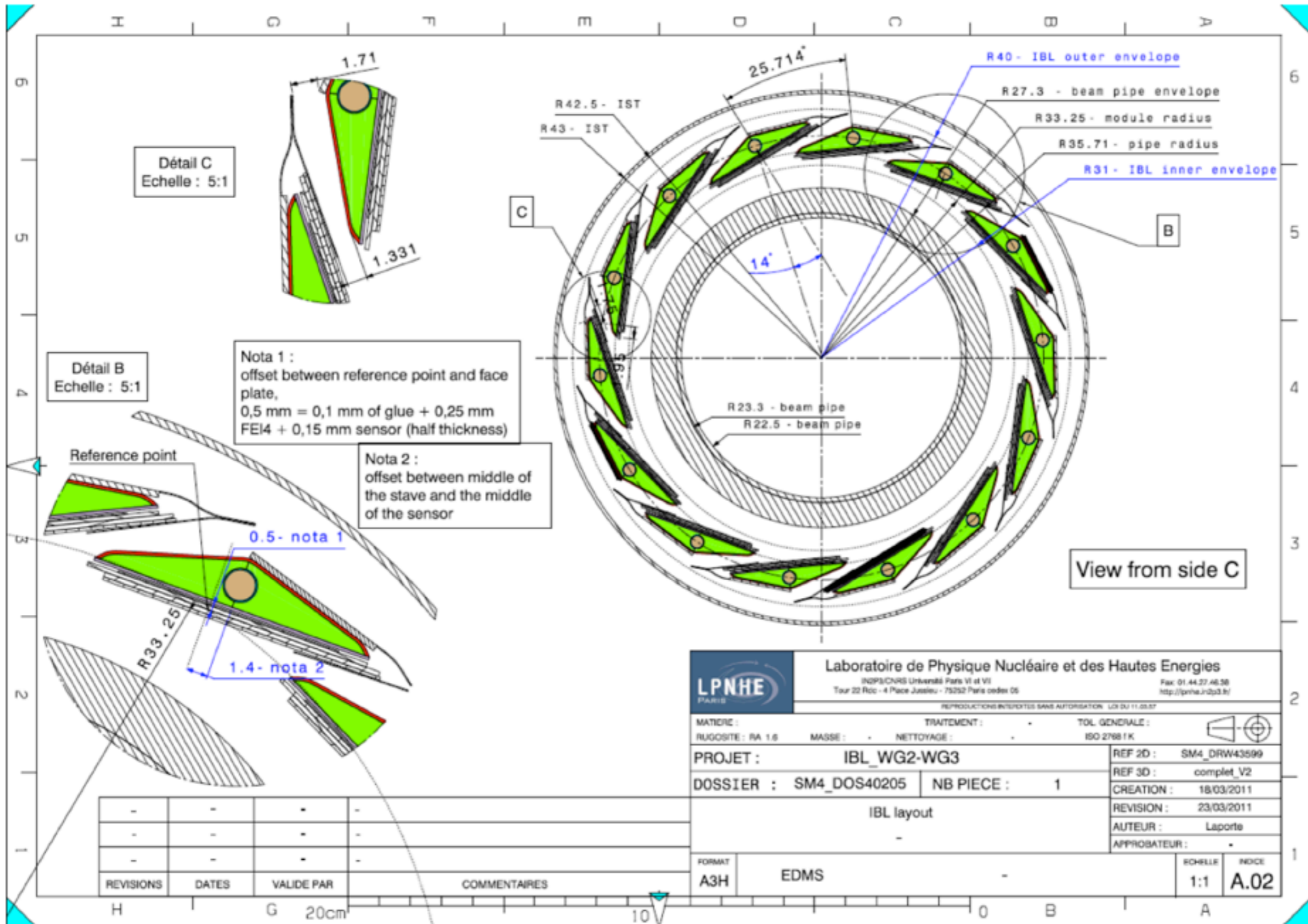


Summary

- ATLAS Tracker plans to upgrade in two (three) phases:
 - Phase-0: Insertion of new pixel inside current Pixel detector - Insertable B-Layer (IBL)
 - First technology step to sLHC (sensors, FE, readout system, cooling, etc...)
 - Installation in 2013: start production of IBL now
 - *Phase-1: Under consideration new Pixel detector based on IBL experience*
 - Phase-2: Full all-Silicon tracker replacement with pixels, short-strips and long-strips
 - Radiation-hardness for
 - innermost pixel layer being investigated
 - outer pixel and strip layer established with planar Silicon
 - Prototype program for outer pixel layers has started
 - Short-strip prototypes already under construction
 - Upgrade also planned for many other subsystems:
 - new front-end electronics and trigger architecture, upgrades to far forward calorimetry, possible implementation of level-1 track trigger, possible further improvements to forward muon stations, ...

Additional Slides

IBL Layout: 14 staves around beam-pipe



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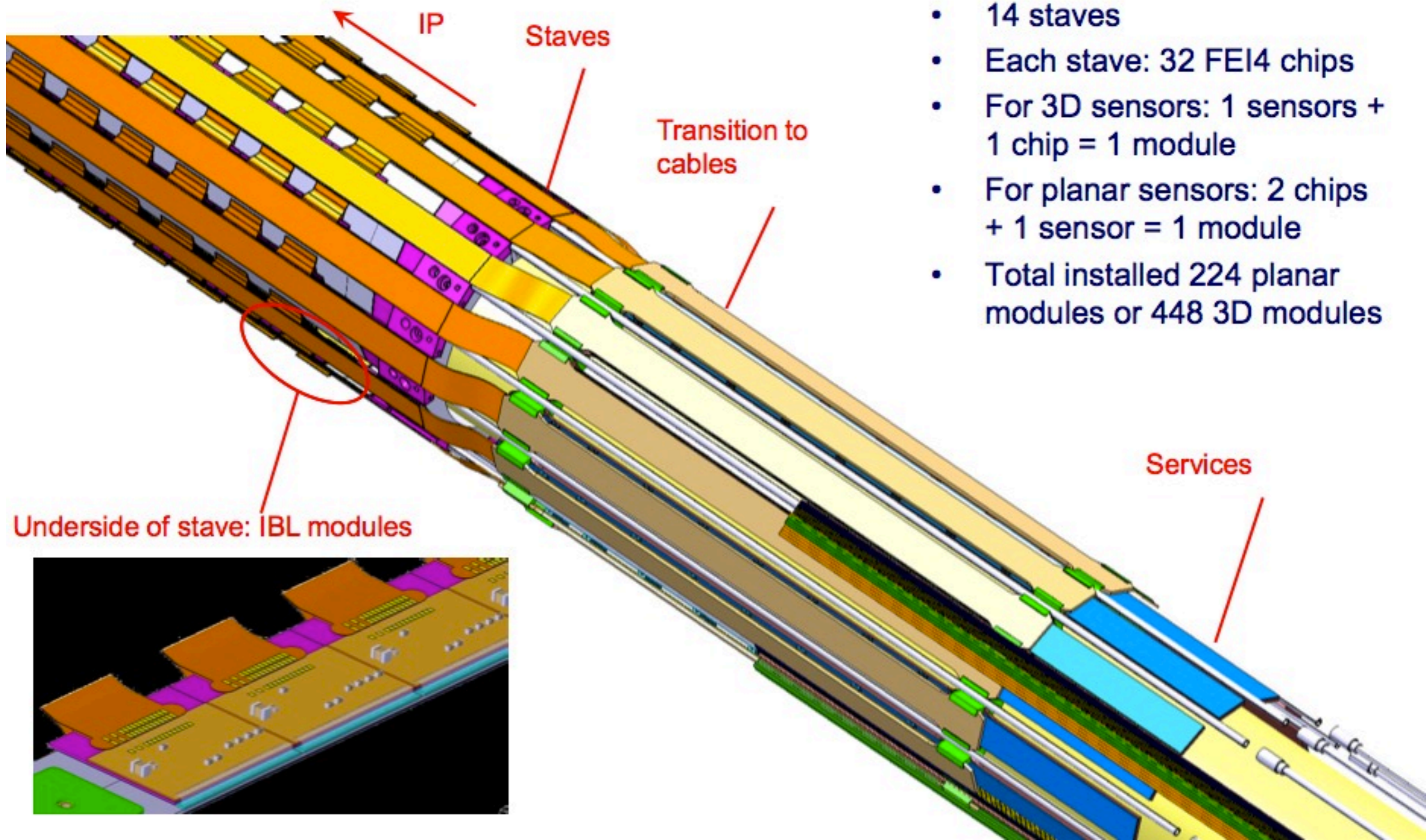
REPRODUCTIONS INTERDITES SANS AUTORISATION. LOI DU 11.03.57

MATIERE :	TRAITEMENT :	TOL. GENERALE :	
RUGOSITE : RA 1.6	MASSE :	NETTOYAGE :	ISO 2768 1 K
PROJET :	IBL_WG2-WG3		REF 2D : SM4_DRW43599
DOSSIER :	SM4_DOS40205	NB PIECE : 1	REF 3D : complet_V2
IBL layout			CREATION : 18/03/2011
			REVISION : 23/03/2011
			AUTEUR : Laporte
			APPROBATEUR :

FORMAT	EDMS	SCHELLE	INDICE
A3H		1:1	A.02

REVISIONS	DATES	VALIDE PAR	COMMENTAIRES
-	-	-	-
-	-	-	-
-	-	-	-

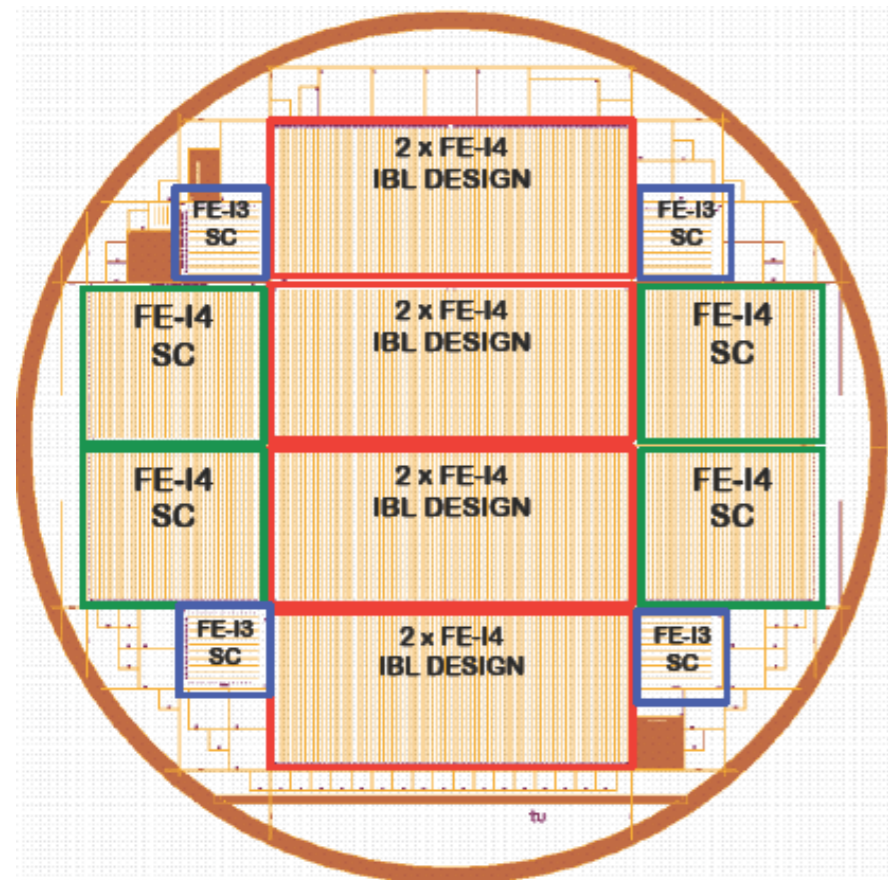
IBL Staves and module arrangement



- 14 staves
- Each stave: 32 FEI4 chips
- For 3D sensors: 1 sensors + 1 chip = 1 module
- For planar sensors: 2 chips + 1 sensor = 1 module
- Total installed 224 planar modules or 448 3D modules

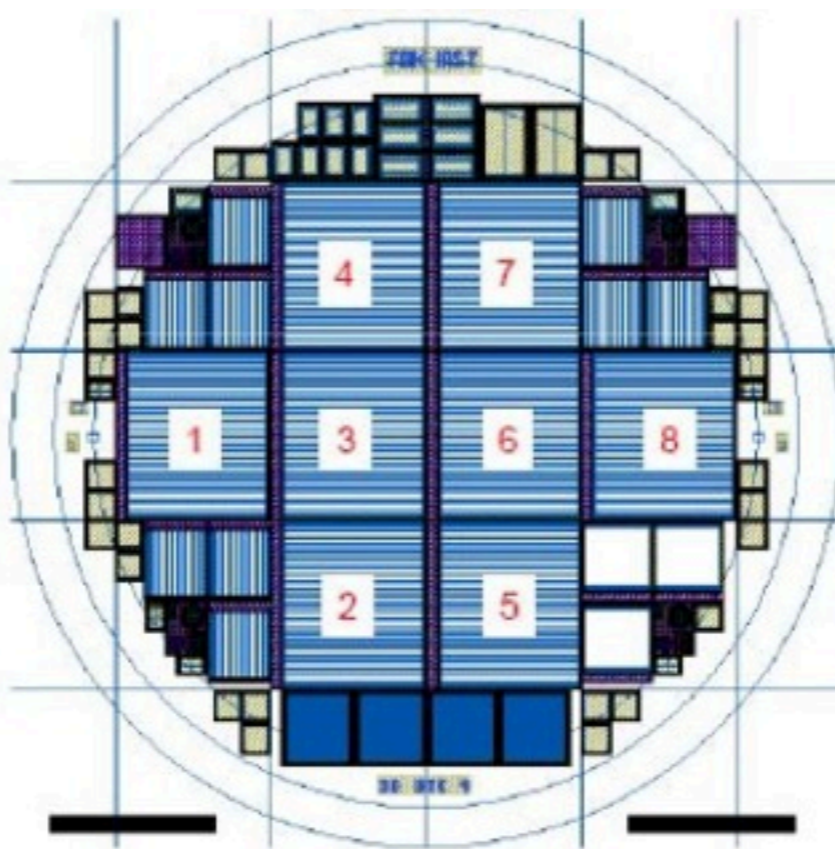
IBL sensor floor-plan

Planar at
CiS, Germany



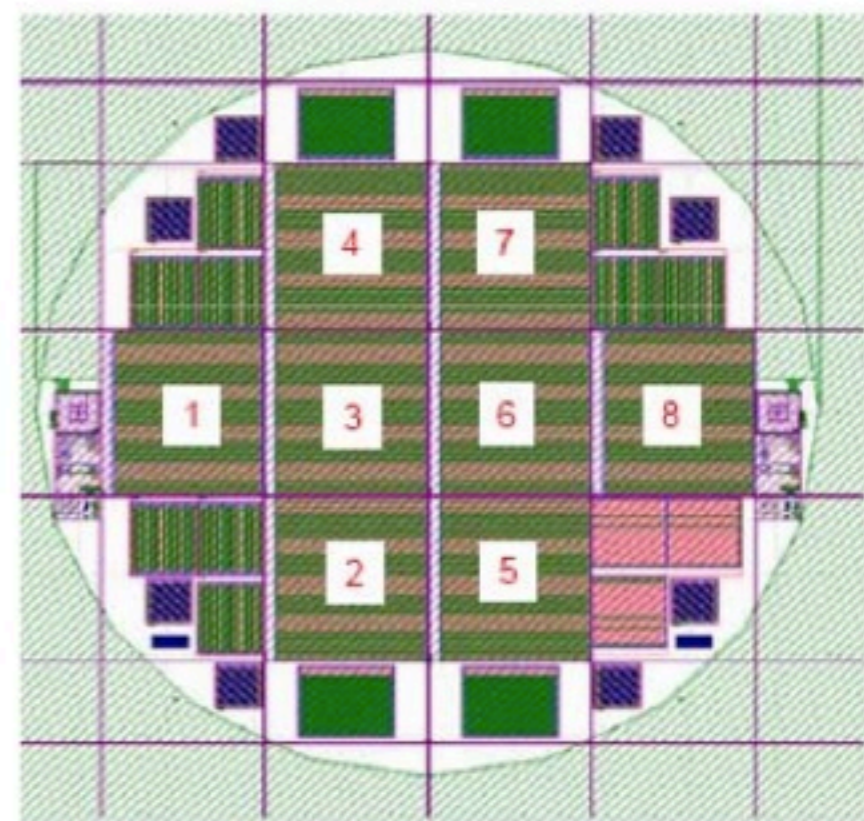
- Planar n-in-n sensor type
- 4x IBL (2-chip sensor) tiles
- 4x 1-chip sensor tiles
- test structures

3D at
FBK-irst, Italy



- 3D n-in-p sensor type
- 8x IBL (1-chip sensor) tiles / for both producers
- test structures

CNM, Spain



FE-I4: low threshold operation

- Studied on Planar and 3D assemblies (irradiated with proton to $5 \times 10^{15} n_{eq}/cm^2$)
 - Noise occupancy increase when threshold below $1500e^-$
 - At $1100e^-$, occupancy is $\sim 10^{-7}$ bits/BC/pixel
- Low threshold operation with irradiated assemblies demonstrated

