Prototype of Integrated Preprocessing and Readout System for GALILEO/AGATA

Bortolato Damiano

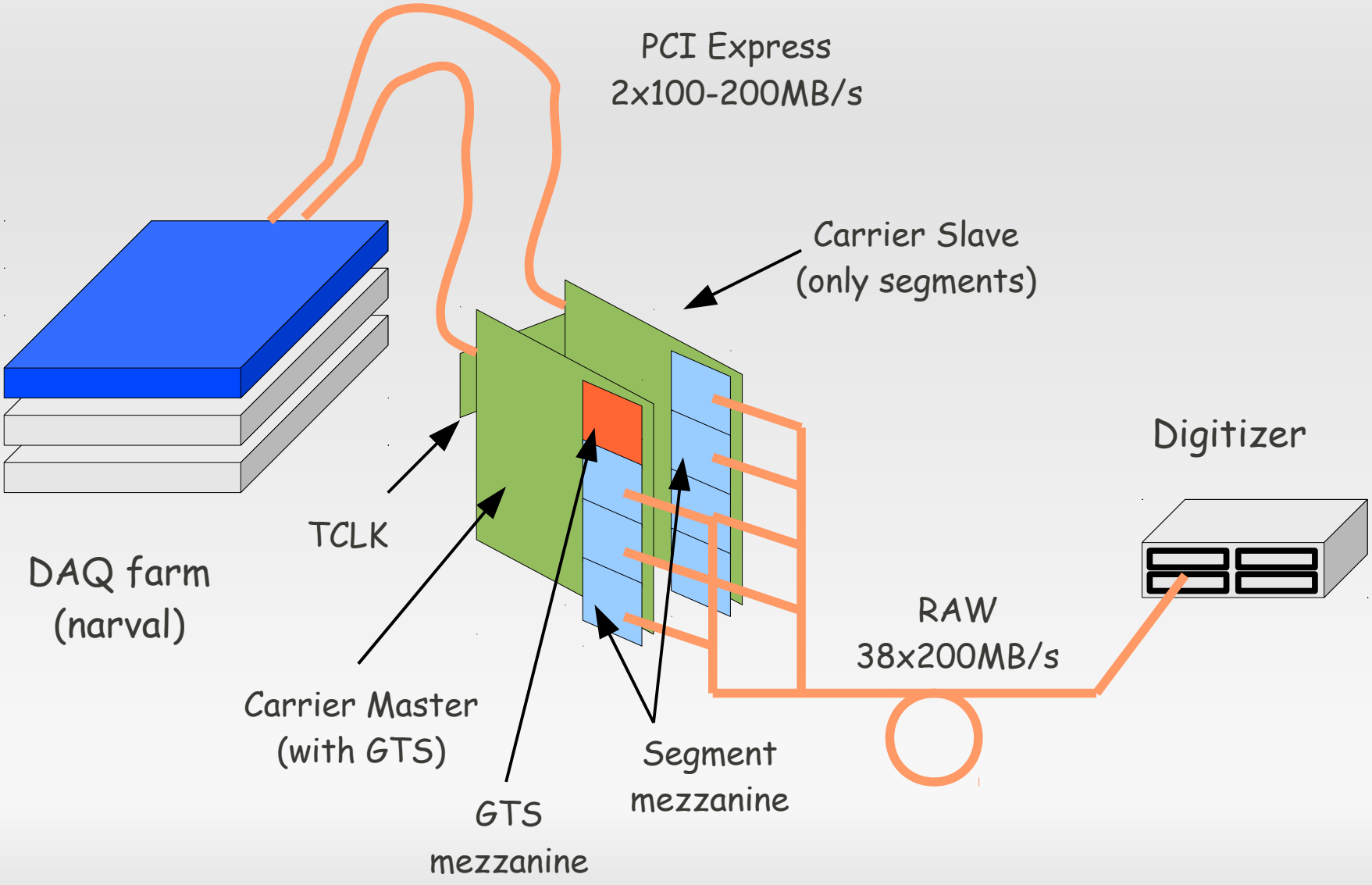
LNL INFN ITALY

10th AGATA week - Lyon November 22nd-26th - 2010

Outline

- Description of current AGATA architecture
- Motivation for new project
- Architecture comparison
- Prototype development
- Prototype tests
- Project development

Current AGATA Architecture



Current AGATA Architecture

- Original requirements has been slightly overestimated in order to be safe.
- Now the demonstrator phase is going well, but the HW is still quite expensive and the management of the system is rather complex.
- Current HW is built with 5 year old technology, even if it probably will be available for some more years, its cost will tend to increase.
- Scalability to a full AGATA detector would be problematic also from the point of view of logistics & total power consumption.

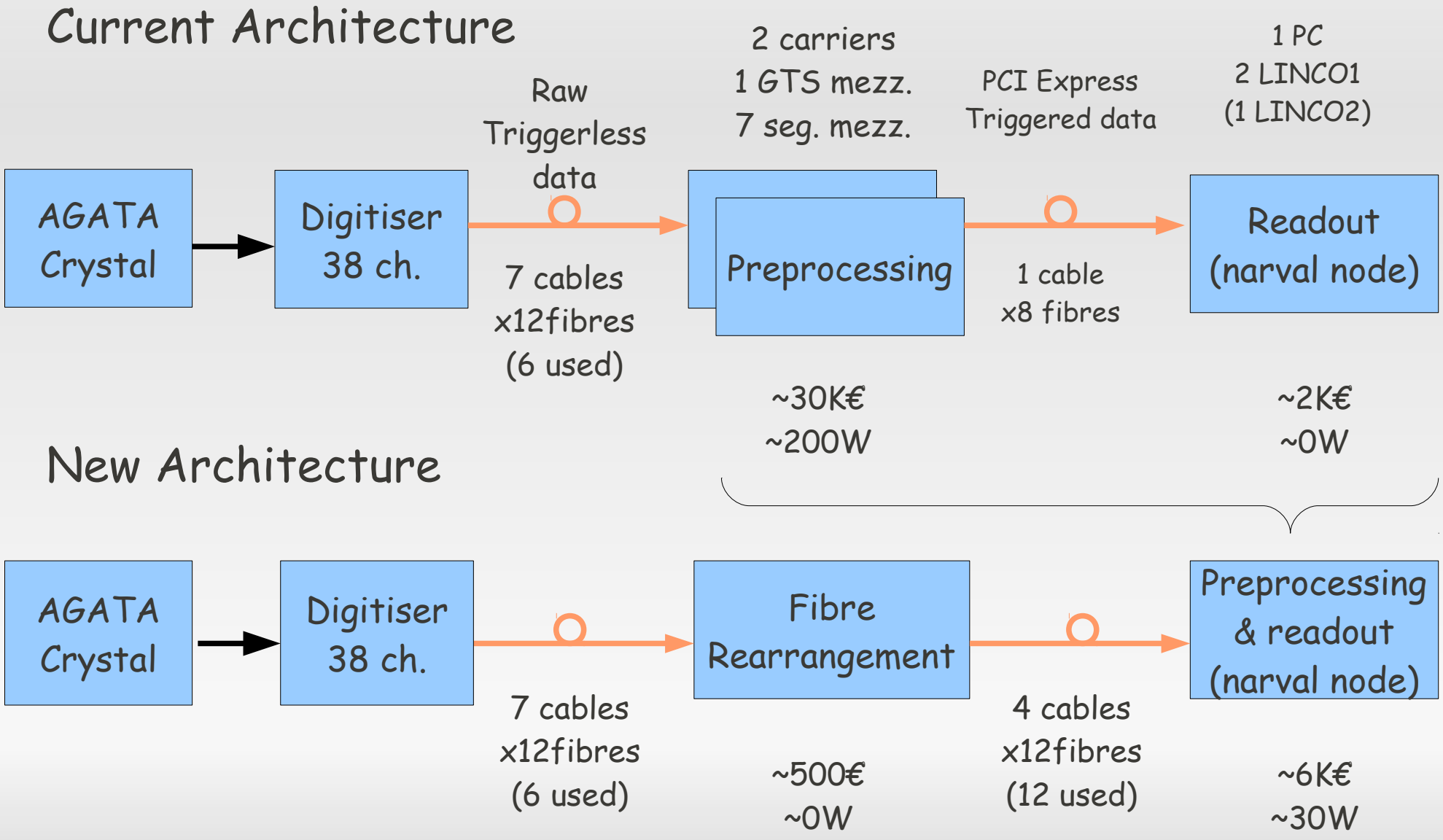
New proposal: motivations

- Cost reduction
- Power consumption reduction
- Integrated compact solution: physically different objects integrated in one object (easier to scale and less cumbersome)

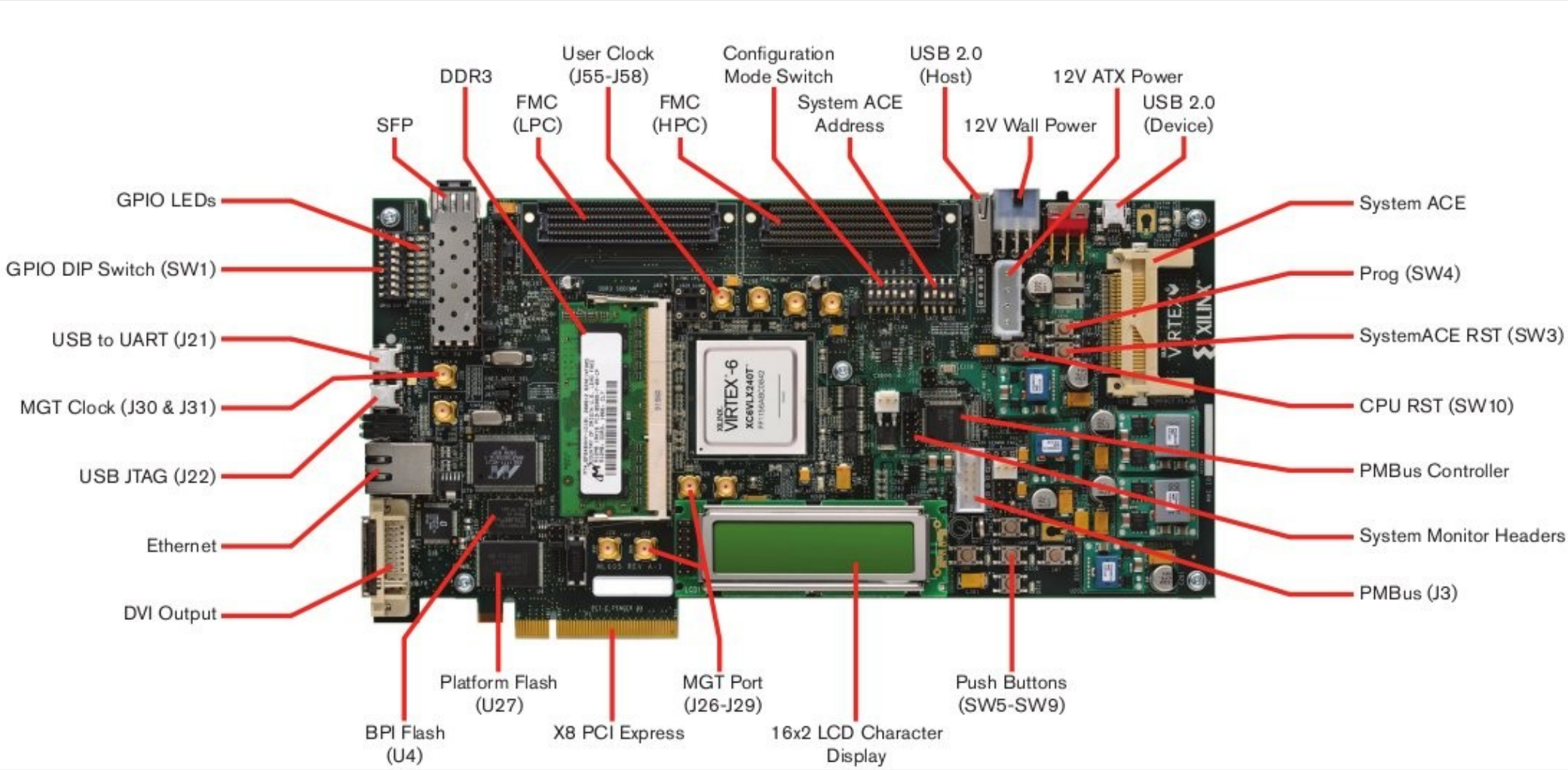
Requirements:

- Backward compatibility: new solutions must be back compatible with other existing AGATA subsystems (GTS, digitizers).
- Synergy and reuse of HW/FW/SW: the new acquisition system can be used for other projects (i.e. GALILEO and maybe others).

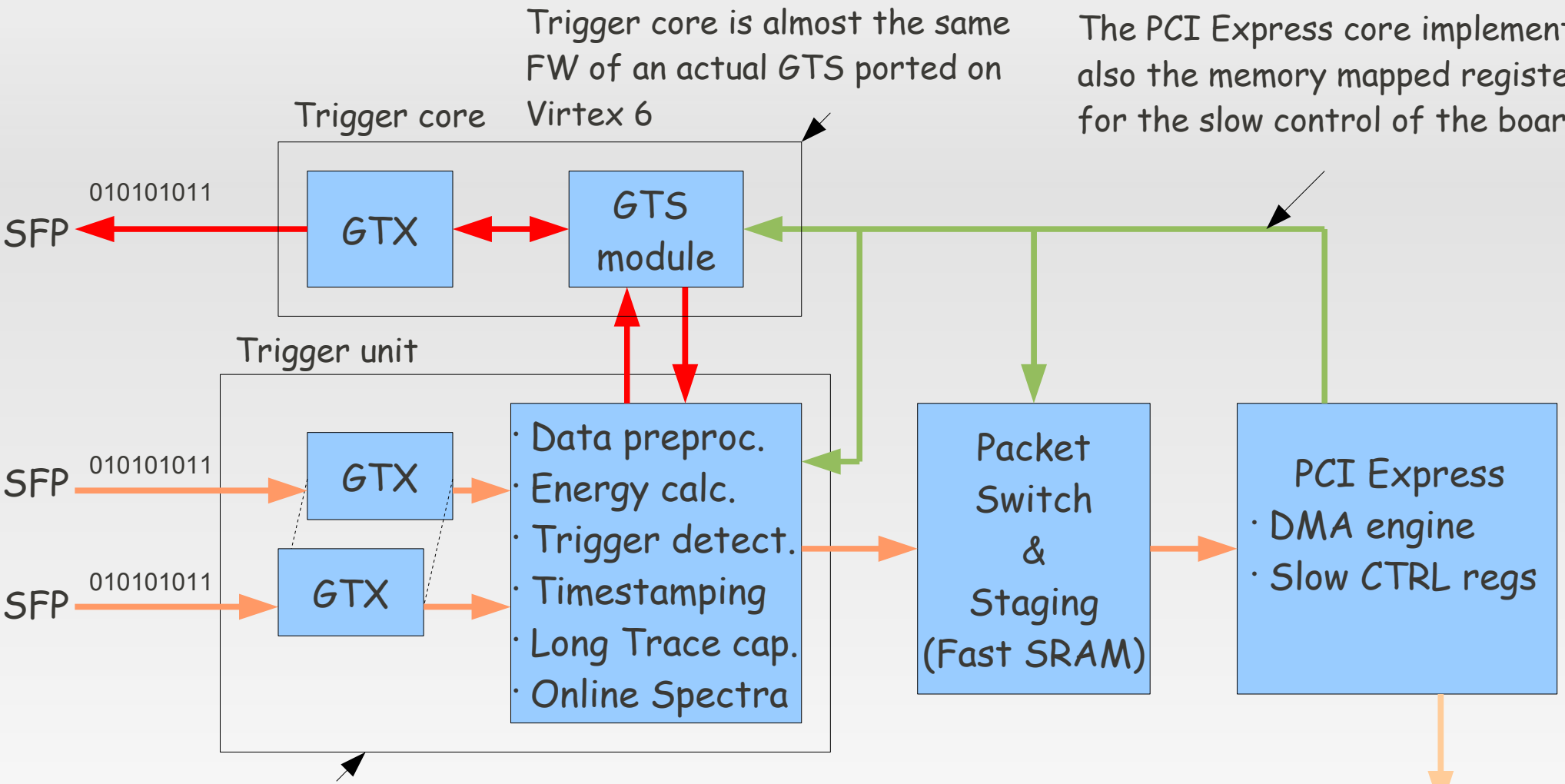
Architecture comparison (AGATA case)



Prototype: Xilinx ML605



Firmware


Trigger core is almost the same FW of an actual GTS ported on Virtex 6
The PCI Express core implements also the memory mapped register for the slow control of the board
Trigger core
010101011
SFP
GTX
GTS module
Trigger unit
SFP
010101011
GTX
SFP
010101011
GTX
· Data preproc.
· Energy calc.
· Trigger detect.
· Timestamping
· Long Trace cap.
· Online Spectra
Packet Switch & Staging (Fast SRAM)
PCI Express
· DMA engine
· Slow CTRL regs
The number of channels per Trigger unit and the number of trigger units are parameters in the VHDL code
Data staging (SRAM) and DMA engine allow to fully exploit the wide bandwidth of the PCI Express technology.
8x 4x PCI Express connector

Software

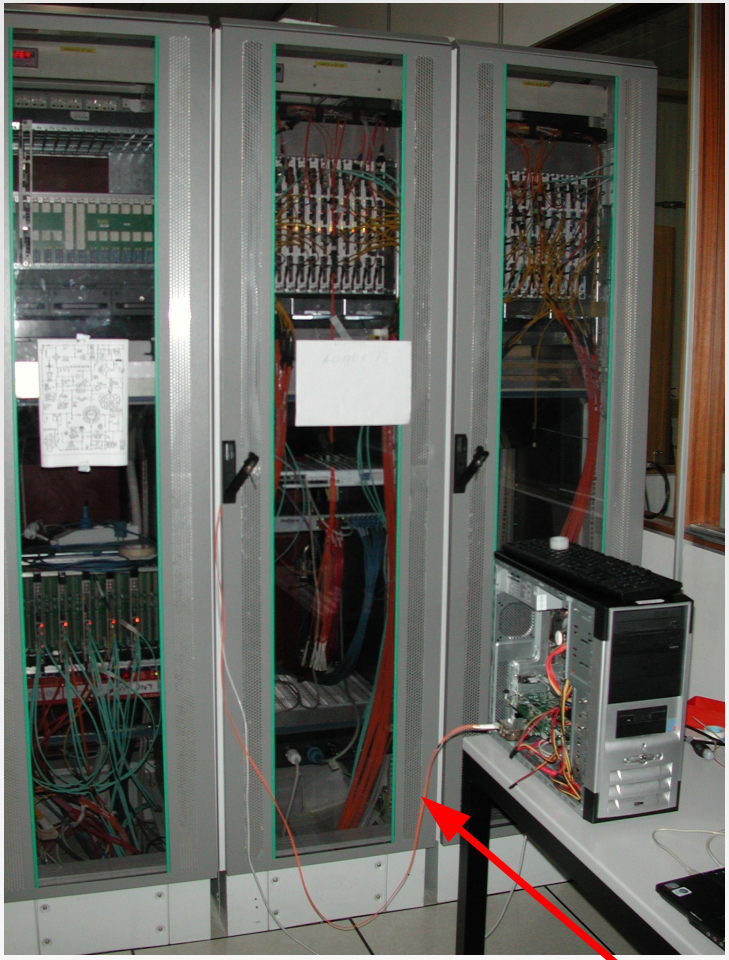
- Linux kernel 2.6x supported
- HW supported DMA Scatter-list simplify data transfers on large memory buffers.
- Driver will provide three devices /dev/xdev[n] (data), /dev/gts[n], (trigger slow control) /dev/carr[n] (data-path slow control).
- Beside the usual kernel copy DT, the driver can also perform zero-copy DMA data transfers to user buffer (direct IO).

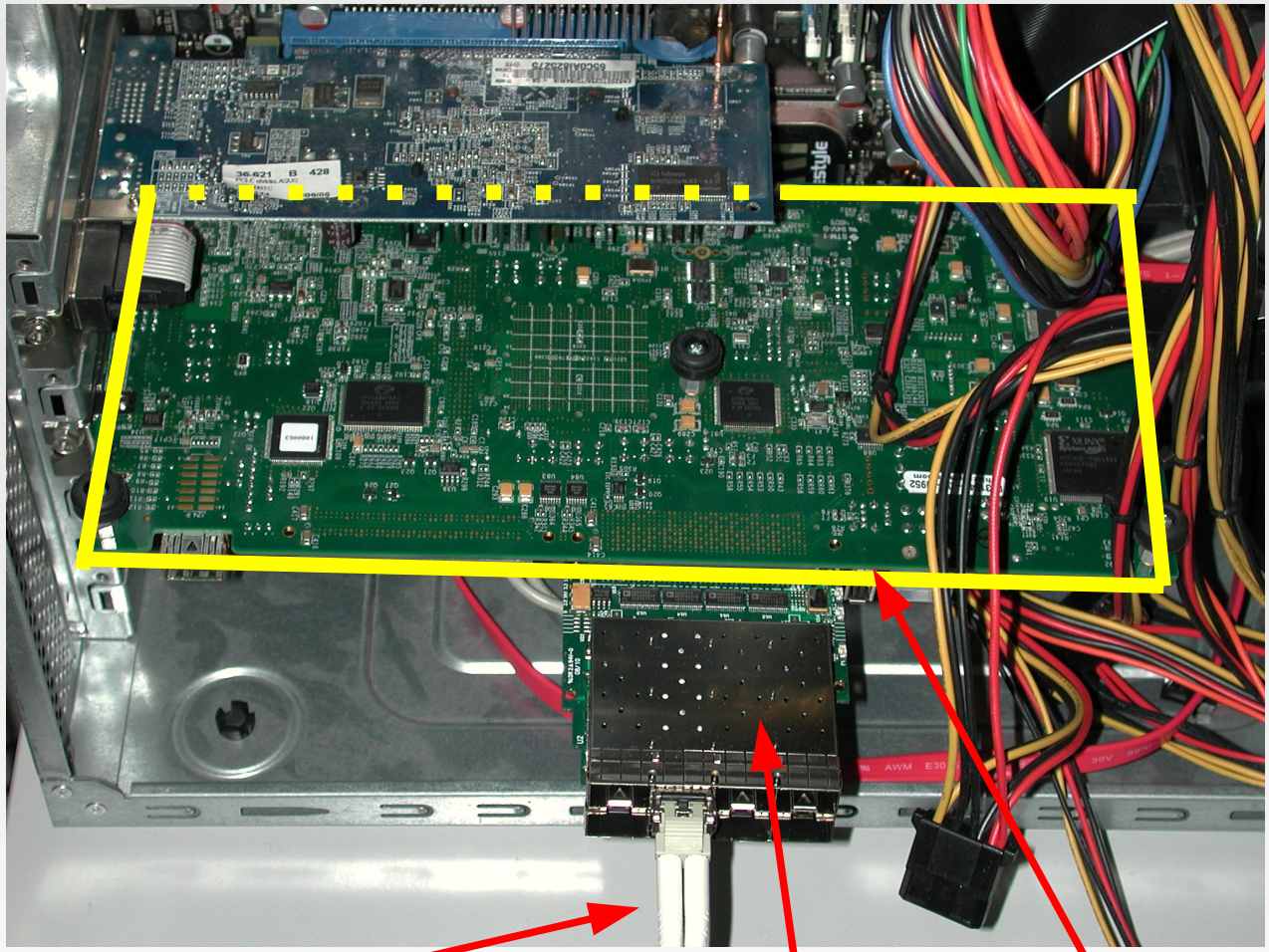
Prototype tests

Tests done:

- PCI Express readout on Linux machine with zero-copy scatter gather DMA (950MB/s).
- Full preprocessing & readout tested with internally generated test waveform (pulser).
- Full preprocessing & readout tested with AGATA digitiser (1 core signal).

Tests: setup



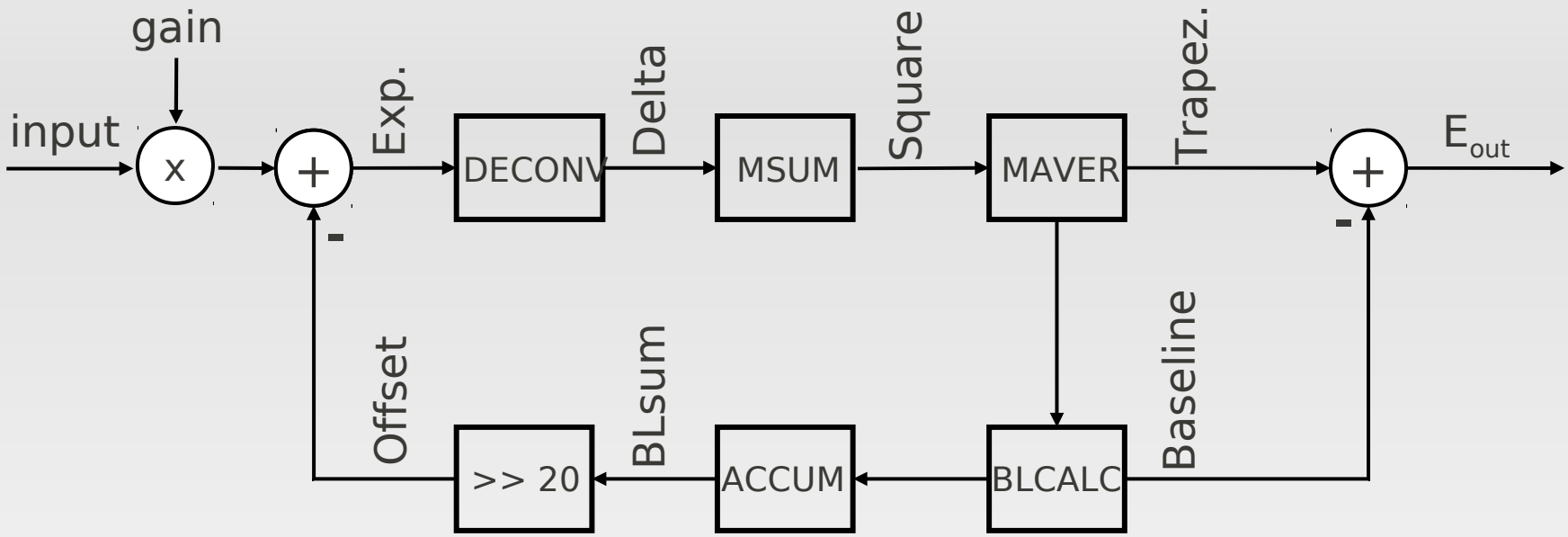


Core signal fibre

IO board

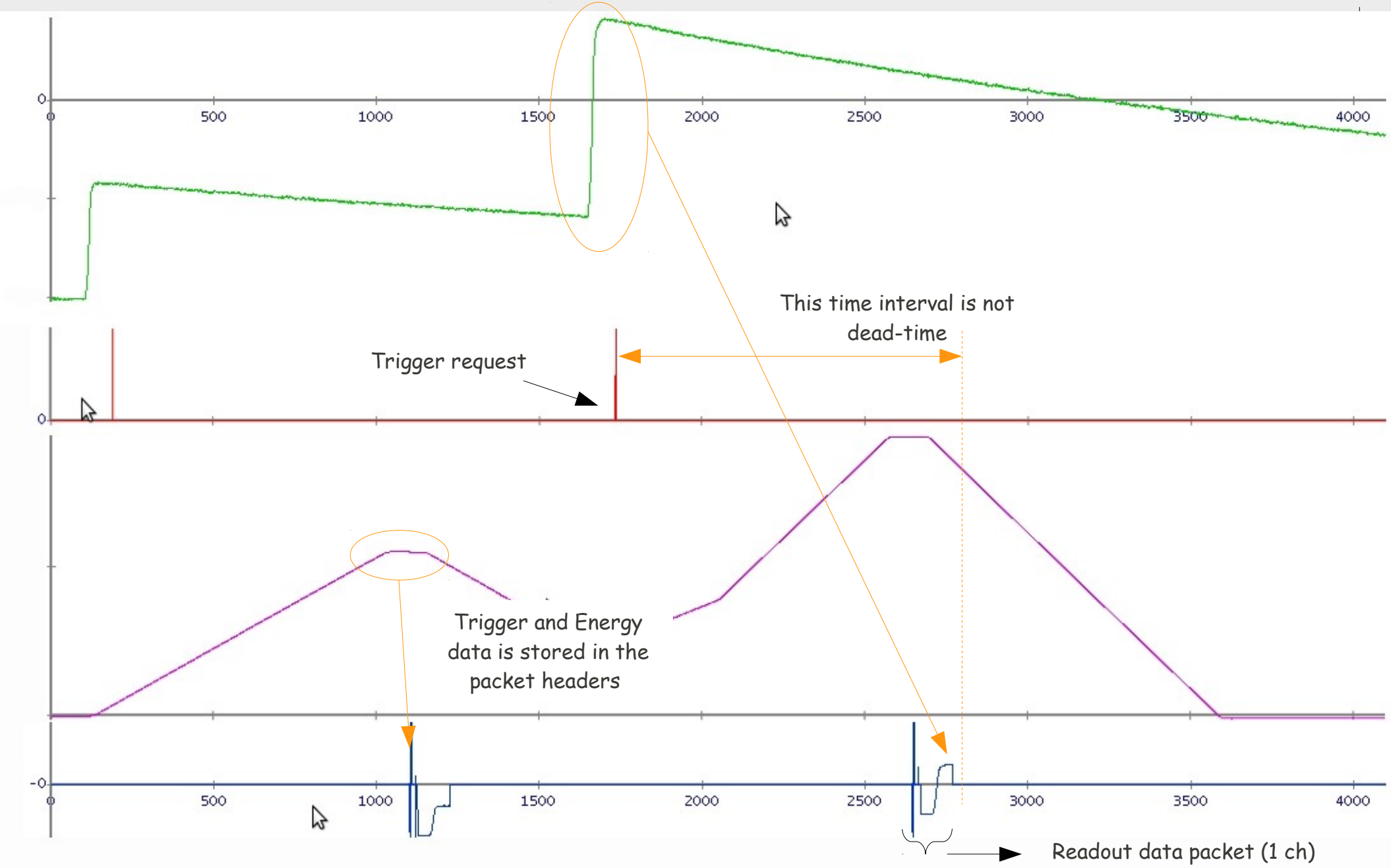
Virtex-6 evaluation board

Preprocessing: channel diagram

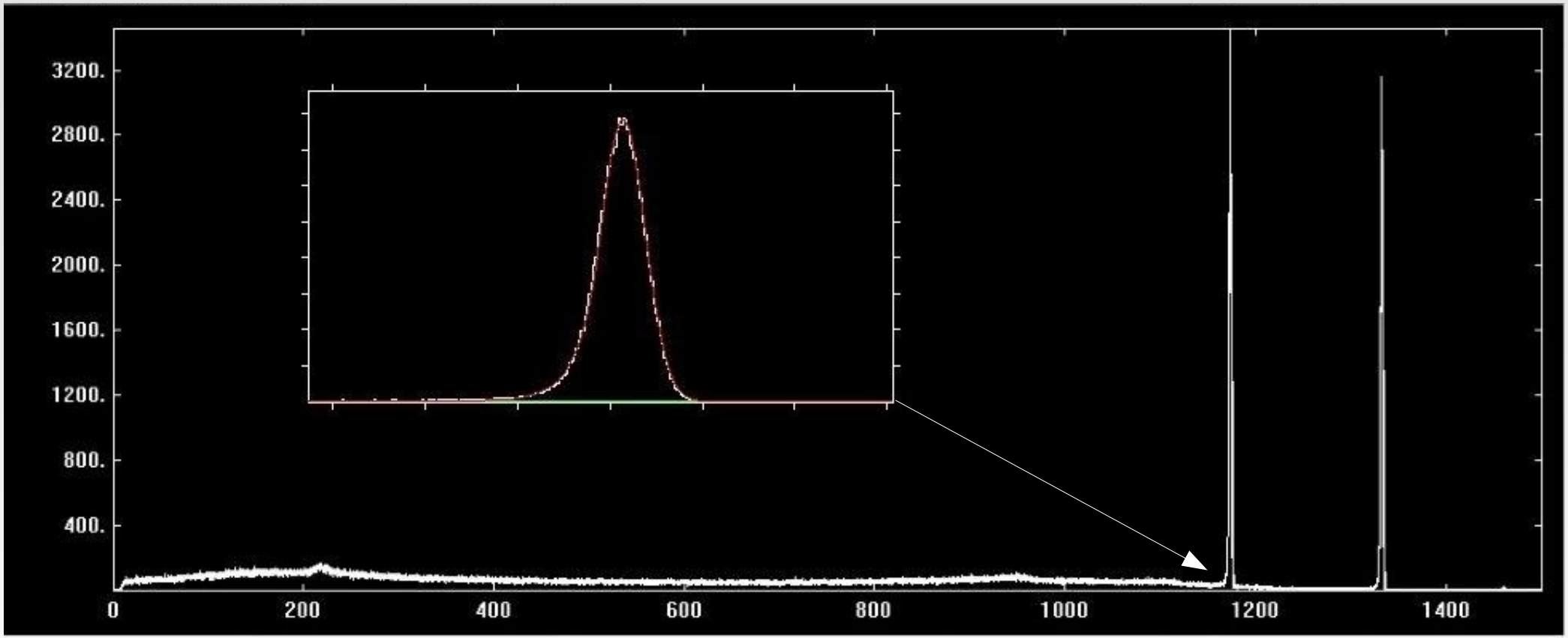


- Fixed-point arithmetic with 36 bits: 20 (integer) + 16 (fraction)
- Input is re-scaled so that the integer part is in keV output is calibrated
- Exponential-average Baseline Restorer with automatic threshold
- Negative feedback of the Baseline to the Input, to remove preamp. offset
- Traces are baseline-subtracted (and deconvolved, if taken after DECONV)
- Deconvolution of 2nd pole

Test: preprocessing example



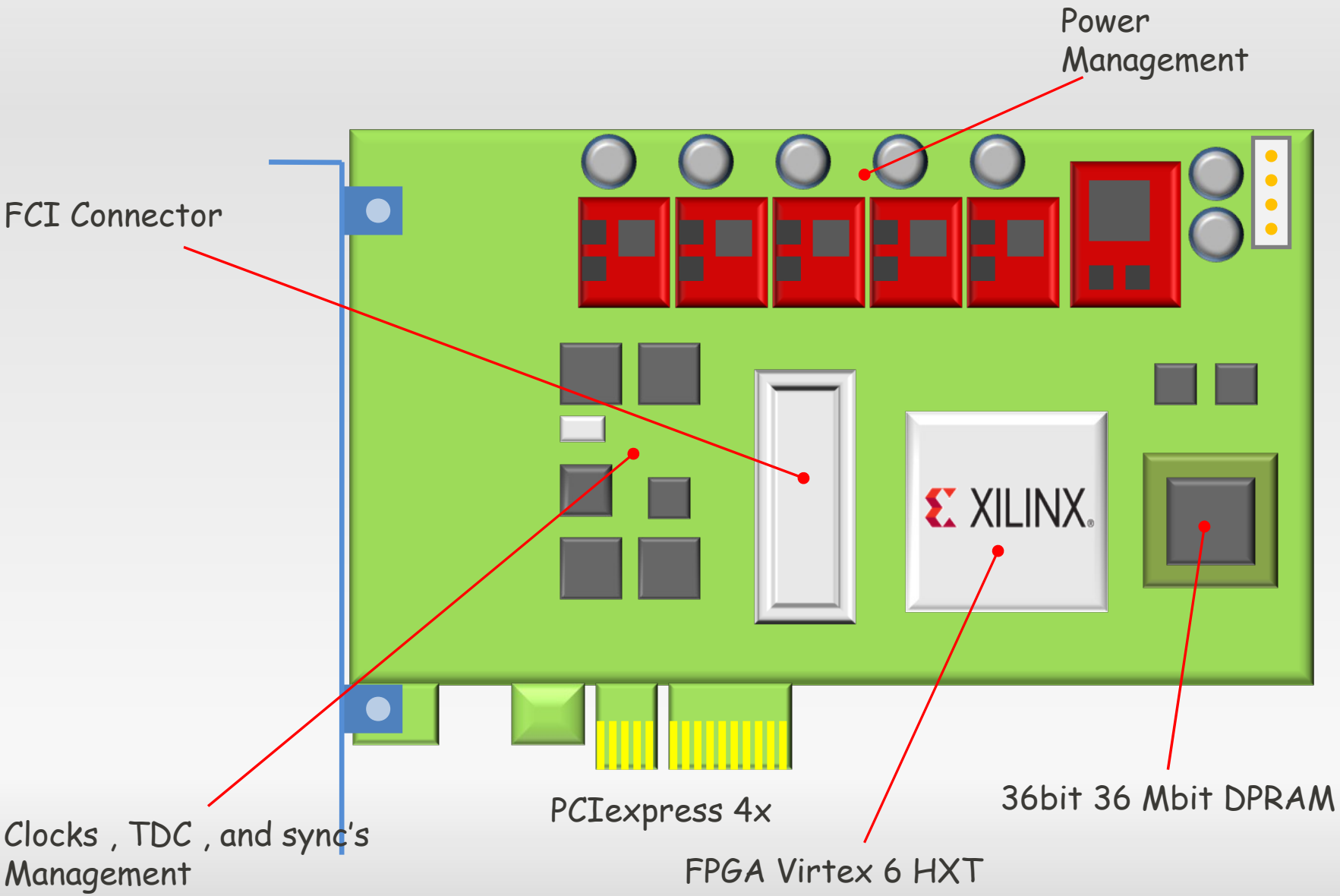
Test: first spectra (^{60}Co source)



25	spec__1-32768-UI__ener.spec	0	UI	1	(D:\zData\testACQ\101117\spec__1-32768-UI__ener.spec)						
26	GFit	2.215	0.00000	0.00169	2.260	1.823 &	1.73	24.358	24.397	49.720	
	0	86471.737	14352.762	24.397	1332.532	2.265	516.37	0.0516	0.0958	0.0048	0.0089

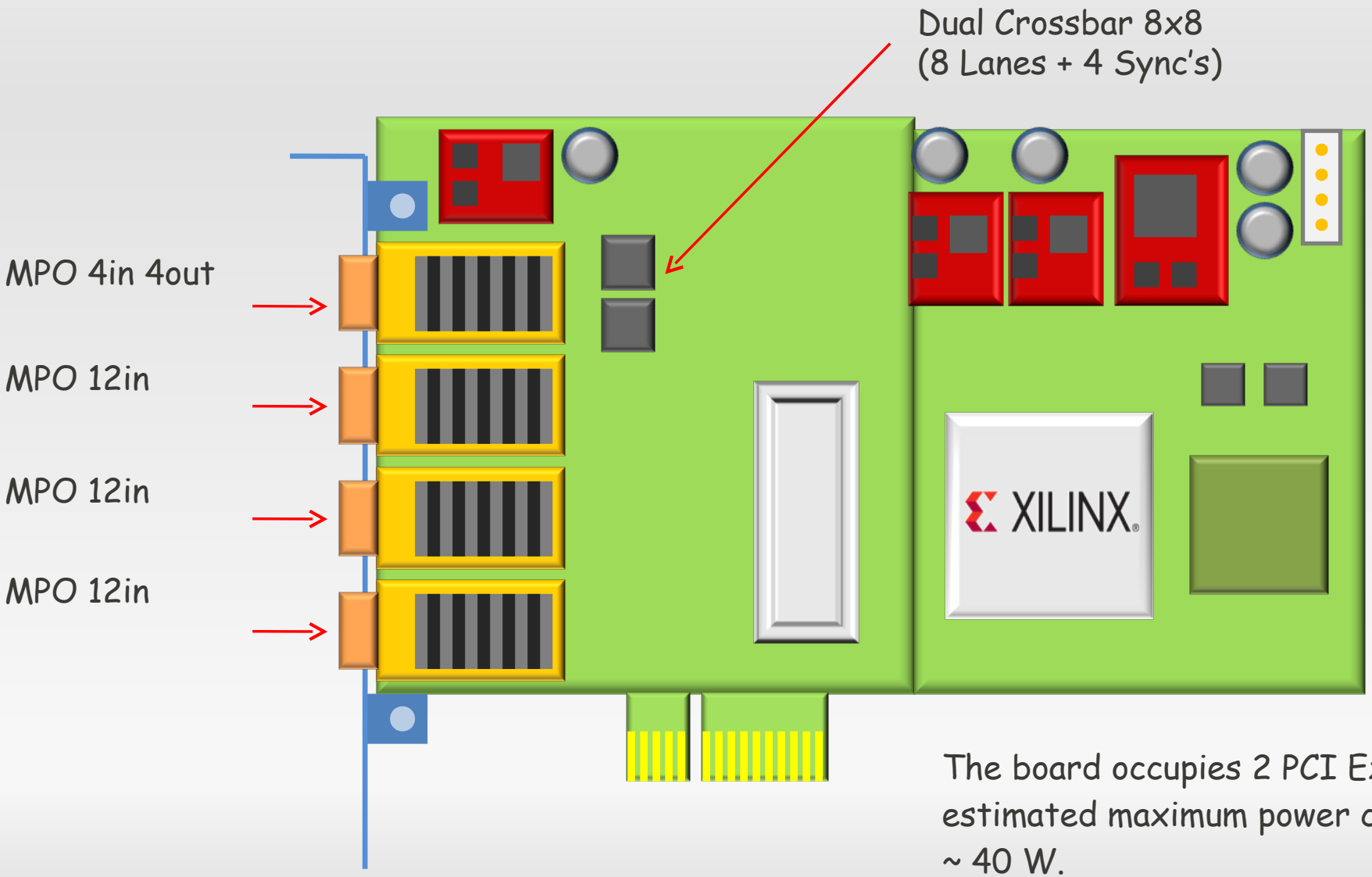
Project: main board

Main board layout



Project: IO module

Mezzanine Option #1 ("Agata" Crystal Pre Processor)



The board occupies 2 PCI Express slot, estimated maximum power consumption ~ 40 W.

Project: XCV6HX250T

Chosen to allow the placement of a 38 AGATA channels preproc. + GTS + PCI Express readout.

- Time enclosure allows 250 MHz sync. logic
- 1154 pin device (320 available IO)
- 48 GTX transceivers (up to 6.6 Gb/s each) (44 used)
- 576 DSP48 cores (used for energy calculation)
- Up to 18 MB of integrated static RAM (staging, pipe-lining)
- Cost should be lower than 2.8K€
- PCI Express Gen1 (2.5 Mb/s) and Gen2 (5 Mb/s) integrated cores (no IP license needed)

Project: FPGA resource needed

Slice Logic Utilization for 38 channel implementation on XC6VHX250T

(GTS & readout code excluded < 10%)

Number of Slice LUTs:	109290 out of 157440	69%
Number used as Logic:	106484 out of 157440	67%
Number of Block RAM/FIFO:	348 out of 504	69%
Number of DSP48E1s:	345 out of 576	59%