Pre-processing status November 2010

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for AGATA pre-processing team

Pre-processing team

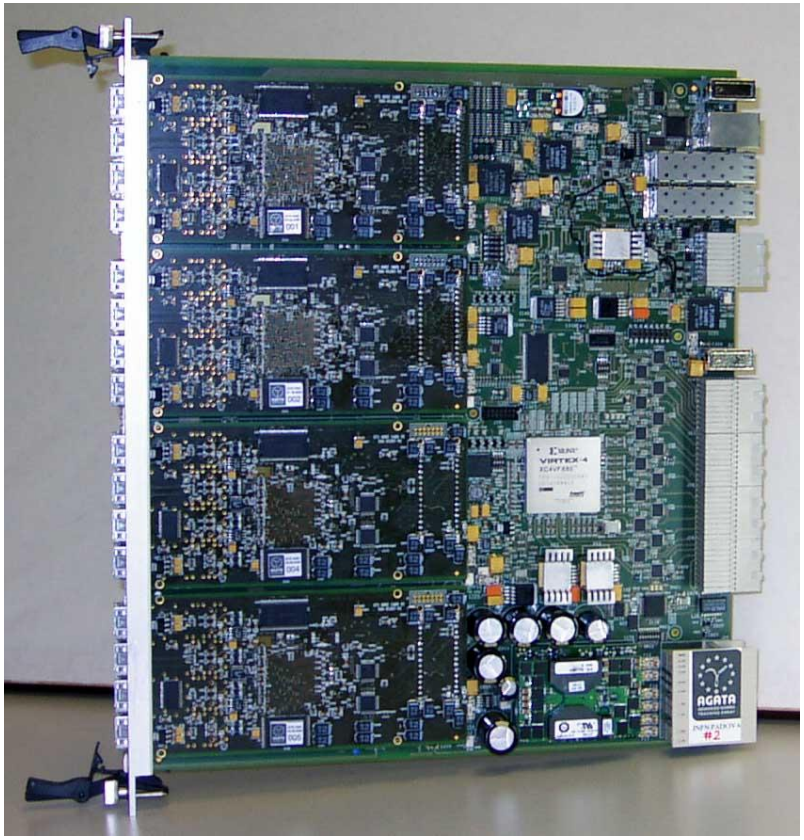
People involved:

- CSNSM Orsay
- INFN Padua
- STFC Daresbury/RAL
- (IPN Orsay)

Work since last AGATA week:

- 8 videoconference meetings
- 2 face to face meetings about future electronics
- Operating and enhancing LNL system
- Producing final batches of hardware for demonstrator
- VHDL improvements

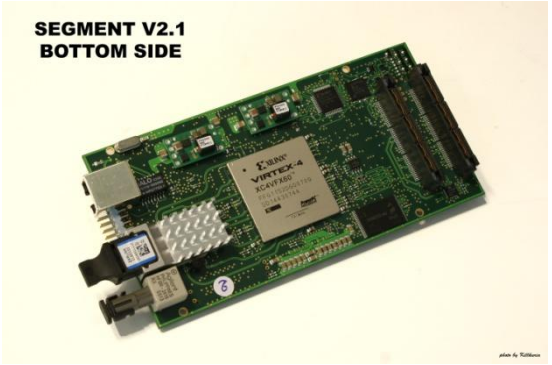
AGATA Pre-processing system



Carrier (ATCA format)

Pre-processing for 1 crystal comprises:

- Carrier (2)
- Mezzanine for detector signals (7)
- GTS Mezzanine (1)
- Linco (2 or 1 dual)
- VHDL for Carrier, mezzanines, GTS.



Mezzanines (PMC format)

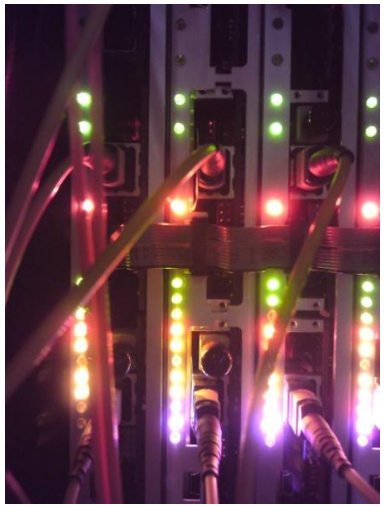
Photos- INFN Padova and CSNSM Orsay

What pre-processing does

- Deserialises data from the digitiser
- Extracts all useful parameters which can be calculated on a per-channel basis in real time.
  - *Energy*
  - *Digitiser input offset control,*
  - *Time Over Threshold (preamp saturation = Pion energy)*
  - *Trigger (core only)*
  - *Timestamps the data when a local core trigger is found*
- Passes on these parameters, with leading edge of the digitised trace, to PSA.

Pre-Processing status at LNL

- Pre-processing hardware exists for 5 ATC's



Item	5 ATC	Available
Carrier	30 carriers	24+4+4 = 32 *
Processing mezzanine	105	107
GTS	15	30+
Linco	30 (or 15 dual)	22+ 1 dual prototype + 3 new dual
TClk	15	20

** Carriers- 28 working cards from IPN; 24 in use @ LNL, 4 in use @CSNSM, 6 pre-production from Padua (4 repairable) to be swapped with cards at CSNSM*

What to do with 4 non-working and partially working IPN carrier boards?

Firmware at LNL

- Firmware v0 for carrier is fairly stable and used for experiments
- Firmware v0 for processing mezzanines is fairly stable and used for experiments

- Firmware v1 for processing mezzanines (cf talk from Nabil Karkour) has enhancements- e.g. better slow control. Tested and waiting for slot to install and test long term stability in system.

TOT firmware

- Protocol designed by Ian Brawn to transmit non-ADC data from digitiser to pre-processing during recovery time after overload.

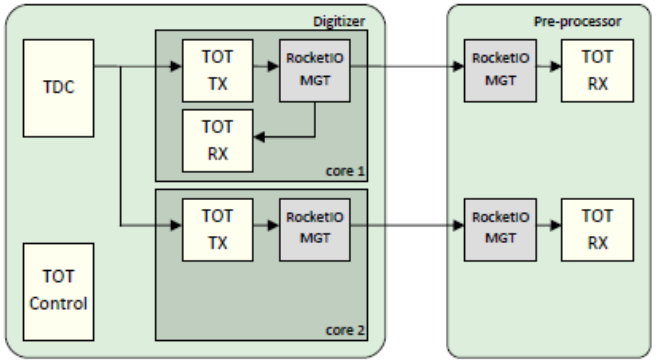


Figure 1. The organisation and modularity of the four blocks of TOT logic: the TDC, the TOT Transmitter (TX), the TOT Receiver (RX) and the slow-control interface (TOT Control).

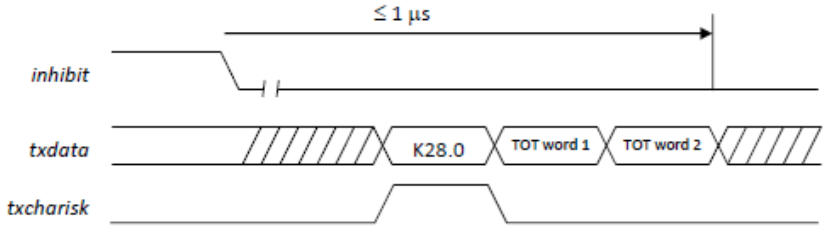


Figure 2. The format of the TOT packet as seen at the input to the RocketIO transceiver on the Digitizer. Here, *inhibit* is the signal from the pre-amplifier, *txdata* is the 16-bit data input to the transceiver, and *txcharisk* is the control signal to the transceiver that flags K characters.

TOT firmware

- RX Code module for pre-processing integrated and tested at CSNSM. Ready for use.

- RX/TX, Control and TDC code in digitiser tested with pulses and ready for test with preamps. (cf Patrick Coleman-Smith talk). *(TDC code based on principles from unfinished Strasbourg code but completely re-written)*

Pre-Processing for GSI

- Pre-processing hardware for 5xATC 5xADC

Item	Now	Production	Total	5 ATC + 5 ADC
Carrier	32	24 *	56	50
Processing mezzanine	107	80 segment 30 Core	187 30	175
GTS	5	30+	35+	25
Linco	22 single 1+3 dual	12 dual	22 single 16 dual	20 single + 15 dual
TClk	20	10/15	30/35	25

* Updated carrier PCB design fixing known problems in 1st batch.

Pre-processing

... More details on production for GSI and also the new v1 mezzanine VHDL in next talk...