

Status report on the 1 m² Micromegas prototype for Digital Hadronic Calorimetry

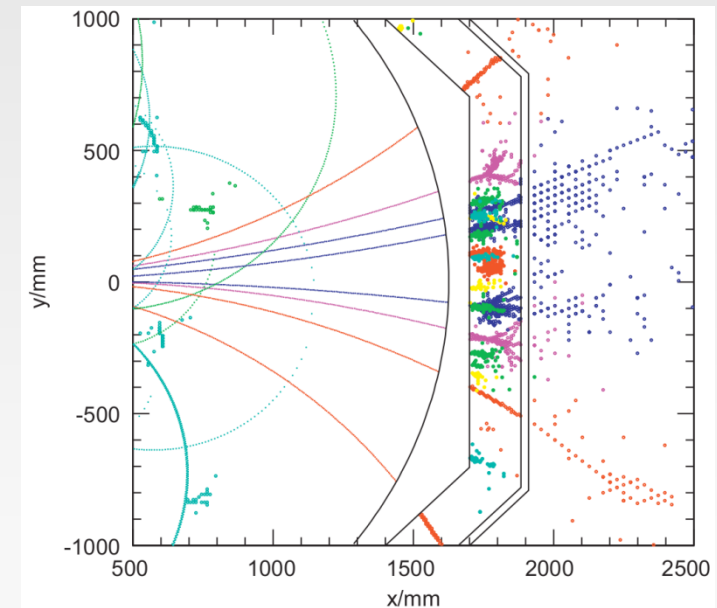
*M. Chefdeville, LAPP, Annecy
RD51 collaboration meeting, Bari, October 2010*

Outline

- Calorimetry at ILC
performance of small sized prototypes
- Board test and prototype assembly
- Test in a beam
- New front-end electronics
- Conclusion

Introduction

- Calorimetry at the International Linear Collider is based on the Particle Flow
→ granularity more important than resolution
- The ILD concept calorimeter would have 30 millions of channels
→ digital readout of 1 cm² cells
- Loss of linearity at high energy (≥ 100 GeV/c)
→ semi-digital readout
- Large area with gaseous detectors
→ RPC, GEM, Micromegas



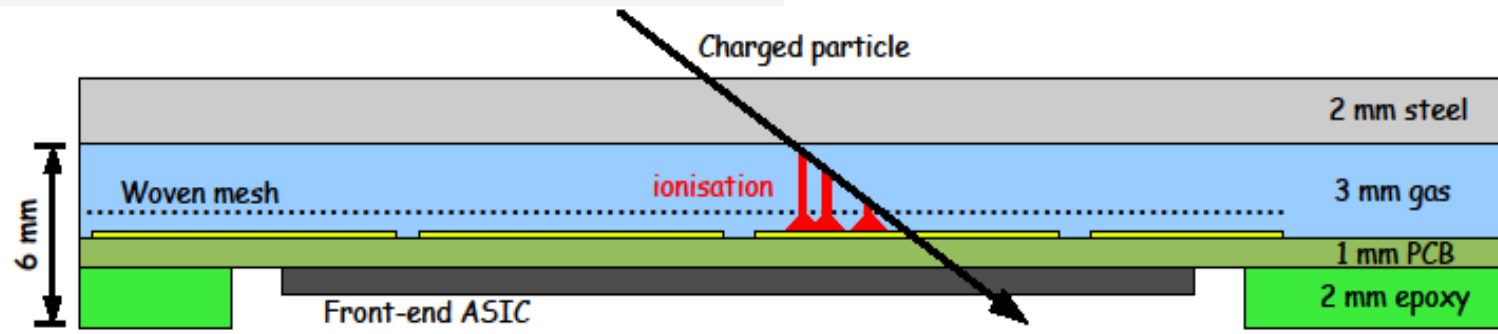
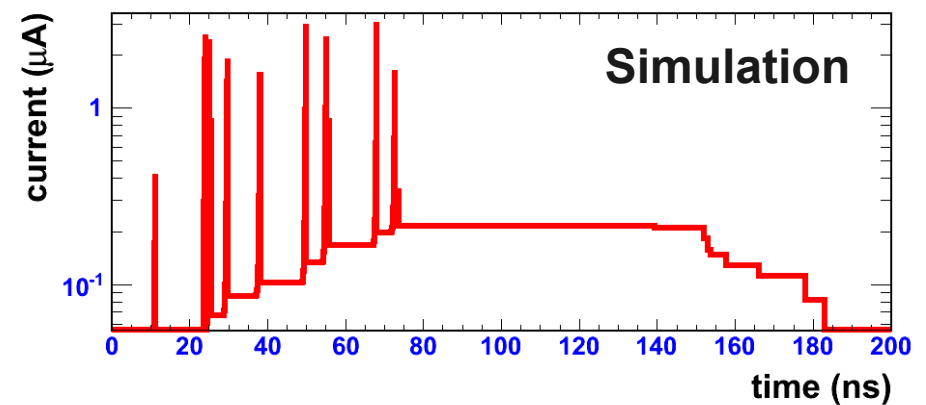
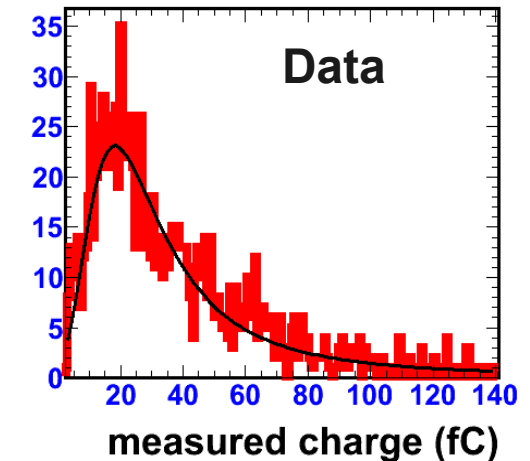
Detector layout and signal

Layout

- 3 mm drift gap (Ar-based)
→ 30 primary electrons (10 MPV)
- 128 μm amplification gap
→ gas gain up to 15.000 with MIPs
- 1 cm^2 pads
- Embedded frontend electronics
→ Total thickness < 8 mm

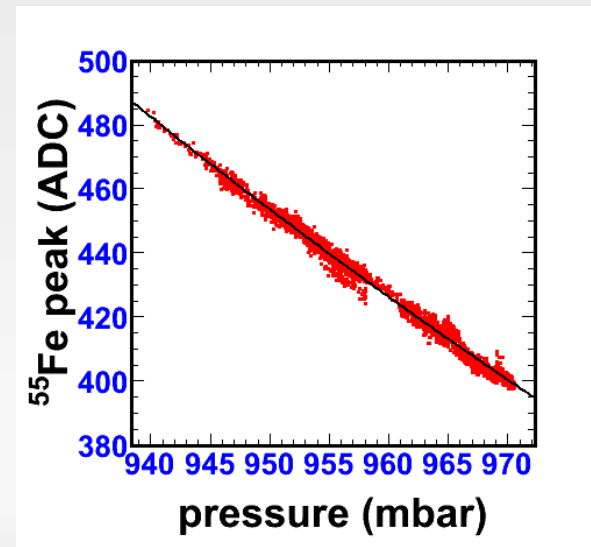
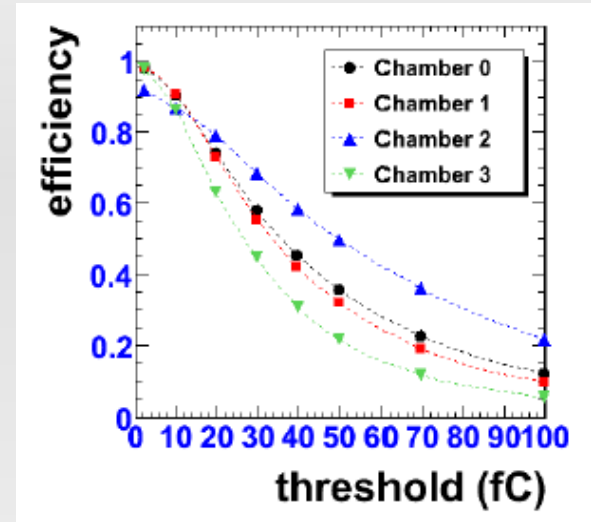
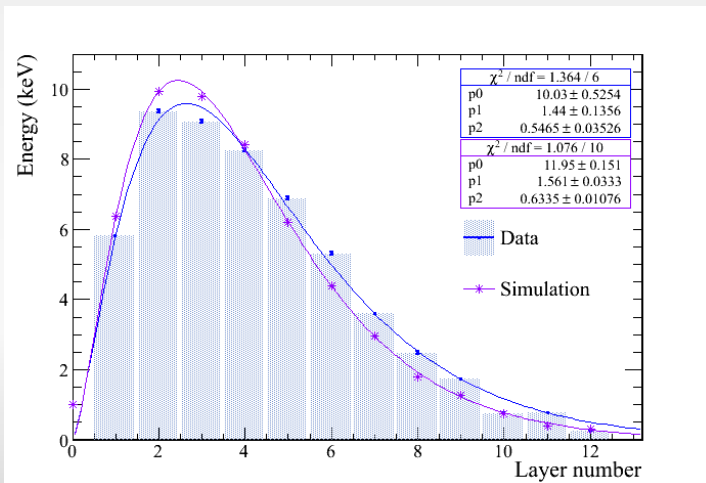
Signals

- Collection in 60-80 ns
- Amplification in 100-200 ns
- Most probable charge of 20-25 fC



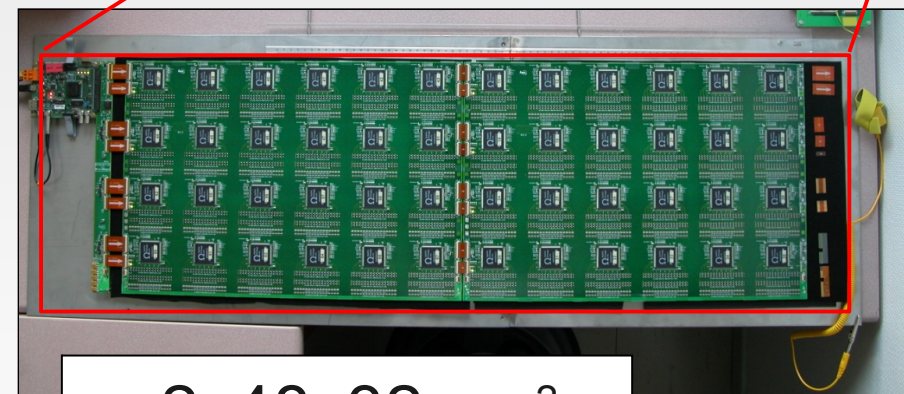
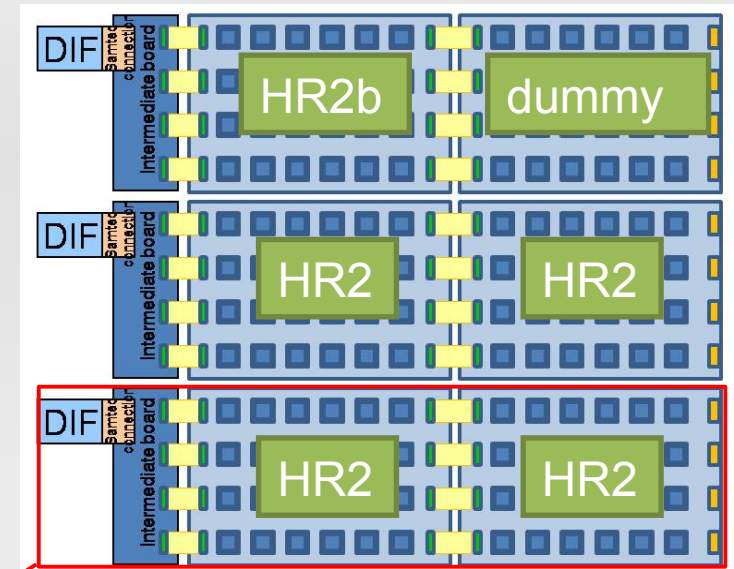
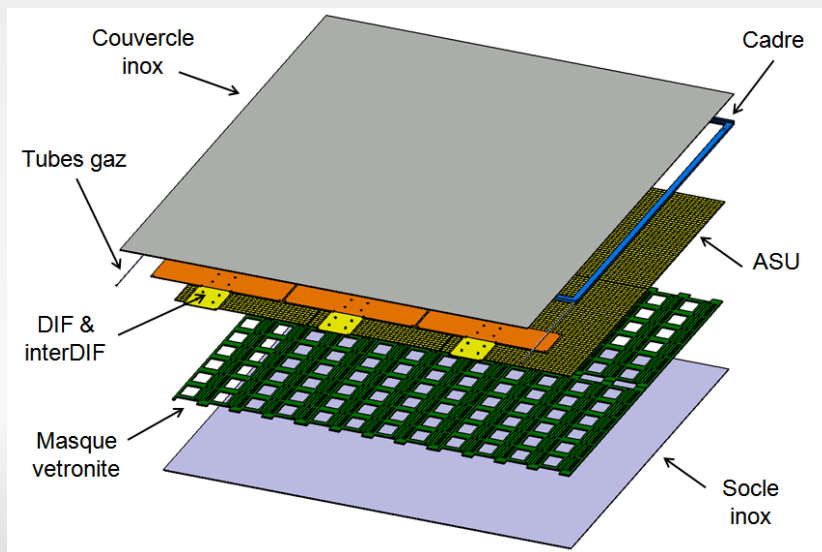
Performance of small prototypes

- Threshold of 1.5 fC – area of 6x16 cm²
 - Signal uniformity dominated by gap variations
20 fC with 10 % variations
 - Very good efficiency
97 % with 1% relative variation
 - Pad multiplicity close to geometric limit
between 1.05-1.10 (decreases with threshold)
- Gain sensitivity to ambient parameters
 - 0.6 %/mbar & 1.4 %/K
- Successfully tested in showers (CERN/PS)



1 m² prototype design

- Choice : 6 meshes of 32x48 m² (1536 channels)
→ Active Sensor Unit (ASU)
- 1 mm gap between ASU + cathode spacers
→ 2 % dead area inside gas volume
- 24 ASIC / ASU
data from 2 ASU (= slab) read out in line (flex cables)
1 Detector interface board (DIF) per slab
→ 3 boards for m² prototype
- Total thickness = 2*2 mm steal covers + 8 mm = 1.2 cm
- Assembly procedure validated with mechanical prototype in 2009



2x48x32 cm²

Front-end chips

- HARDROC2 chip
 - 64 channels with preamplifier, fast shaper (20 ns shaping time)
3 discriminators and a 127 event depth memory
 - Individually adjustable preamplifier gain
 - Global discriminator threshold
 - Power pulsing capability
- 2 bit information (0/1/2/3)
but 1 threshold used so far
- Channel response to input charge is an S-curve, at 0 charge
 - inflexion point is the pedestal
 - width is the noise

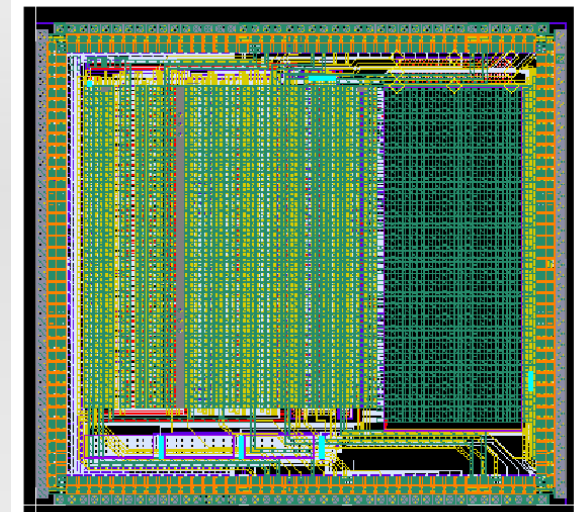
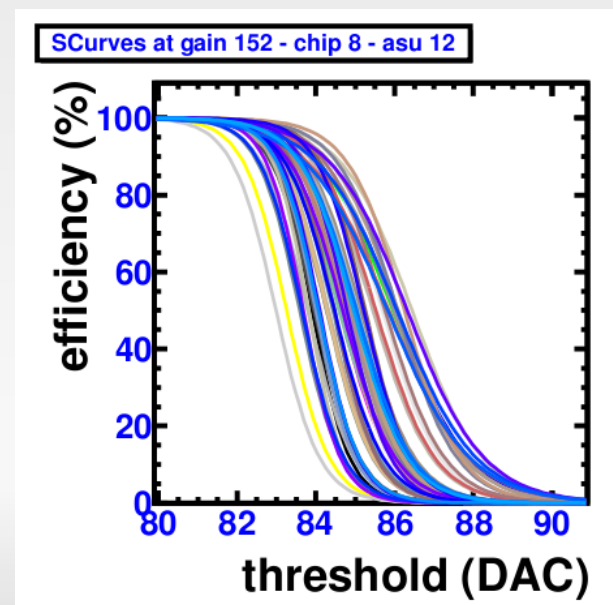
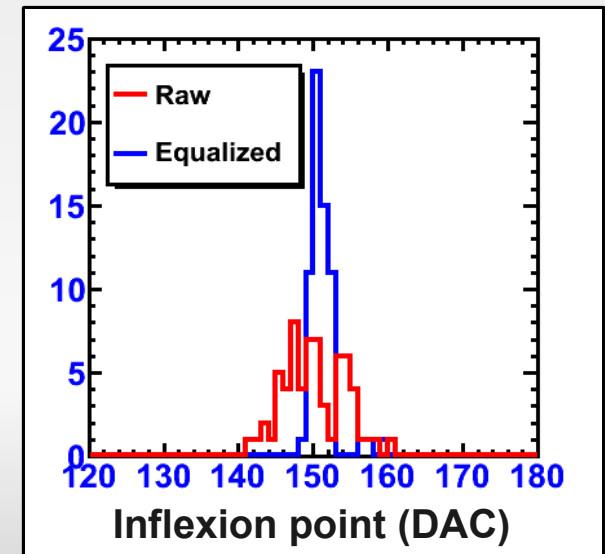
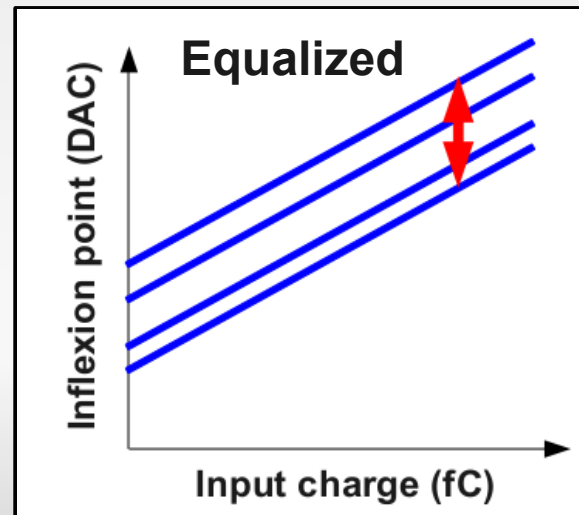
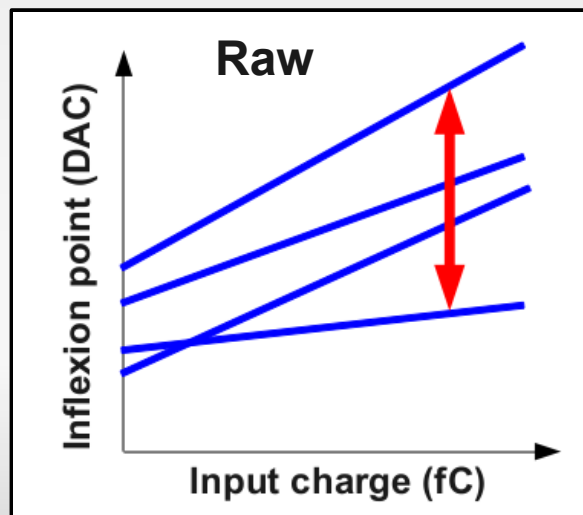


Figure 1 - Hardroc2 layout



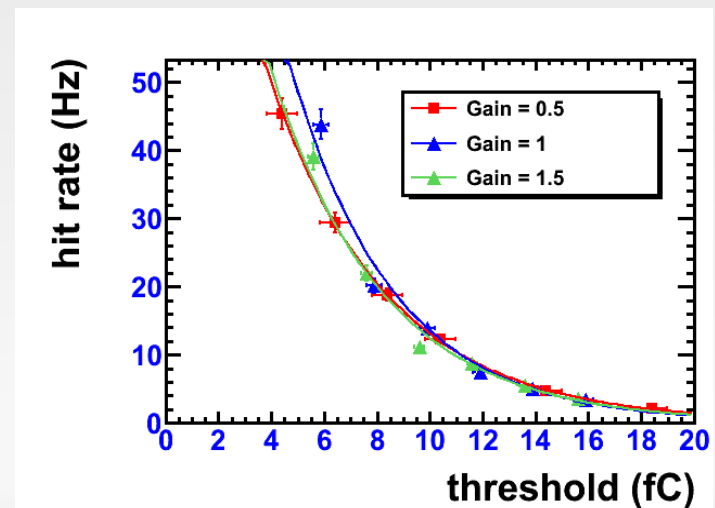
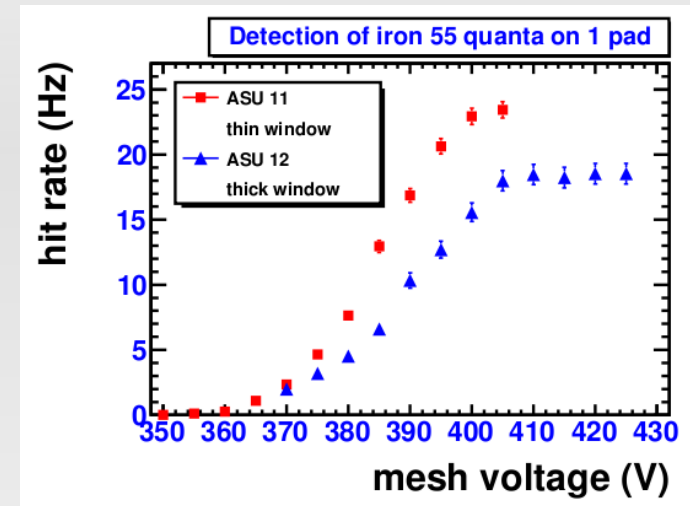
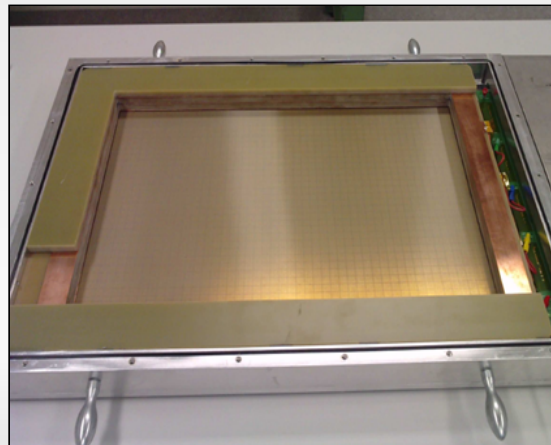
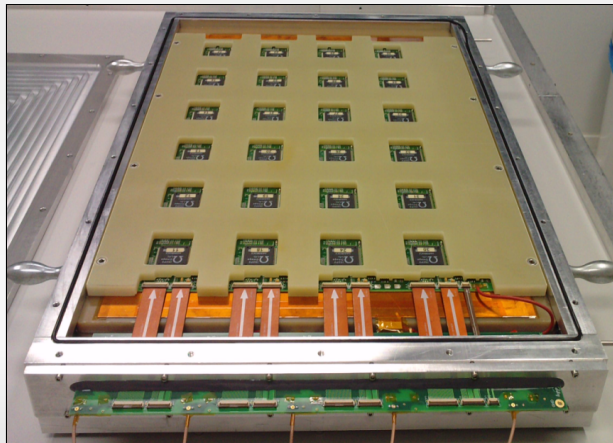
Board test (I)

- Prior to assembling
 - HV training
 - Measure detector signal uniformity (10 % RMS var.)
 - Correct non-uniformity with individual preamplifier gains
- What was done
 - Preamplifier response measured with test charges
→ Corrections reduce Scurve spread by a factor of 8
 - Detector response inside a gas test box
Ideally with particle beam, ^{55}Fe quanta used
Adjust chip parameters to detect the maximum of quanta



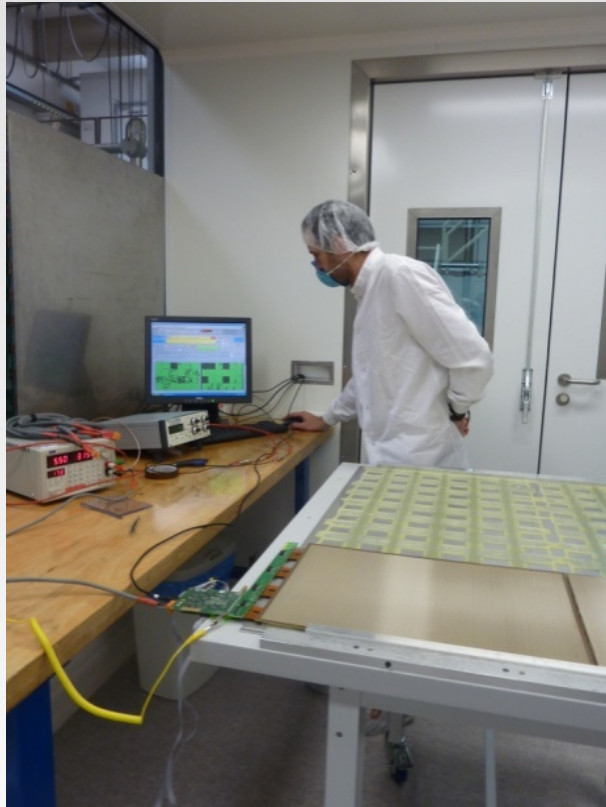
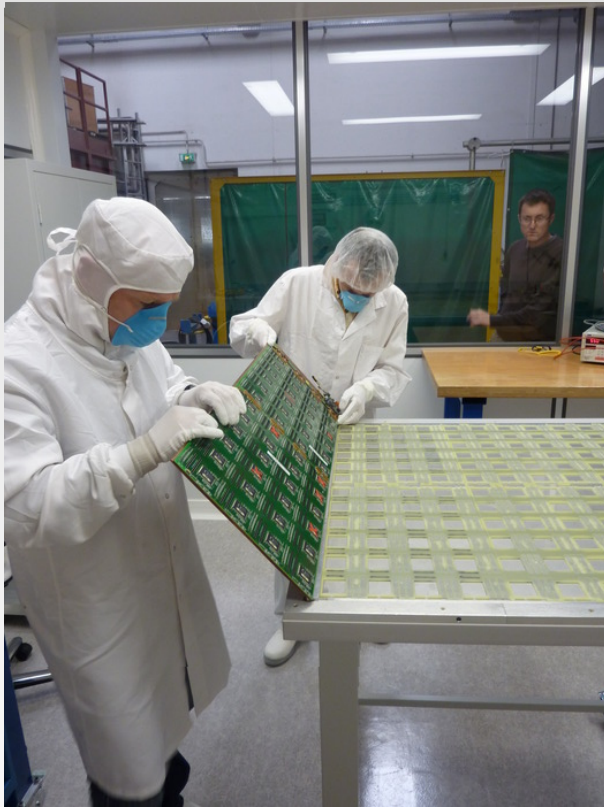
Board test (II)

- Prior to assembling
 - HV training
 - Measure detector signal uniformity (10 % RMS var.)
 - Correct non-uniformity with individual preamplifier gains
- What was done
 - Preamplifier response measured with test charges
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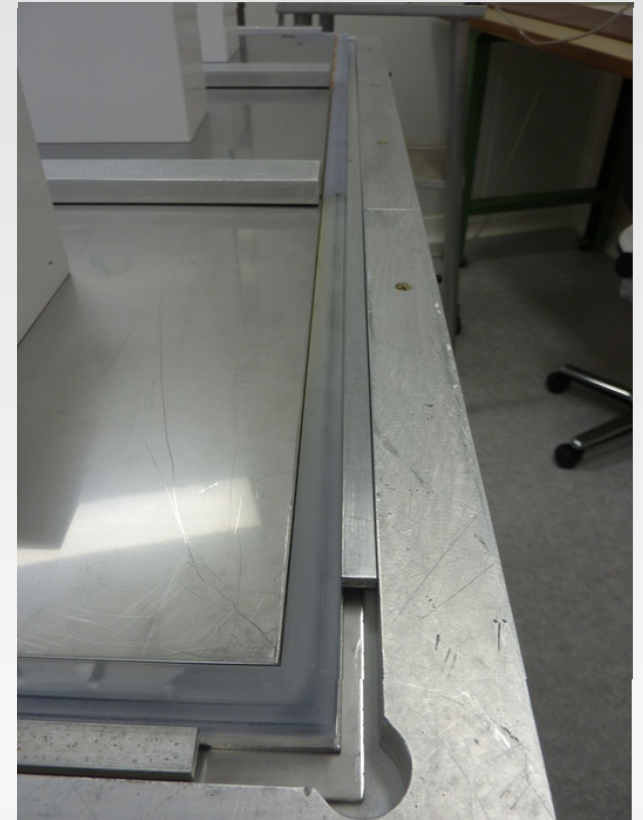
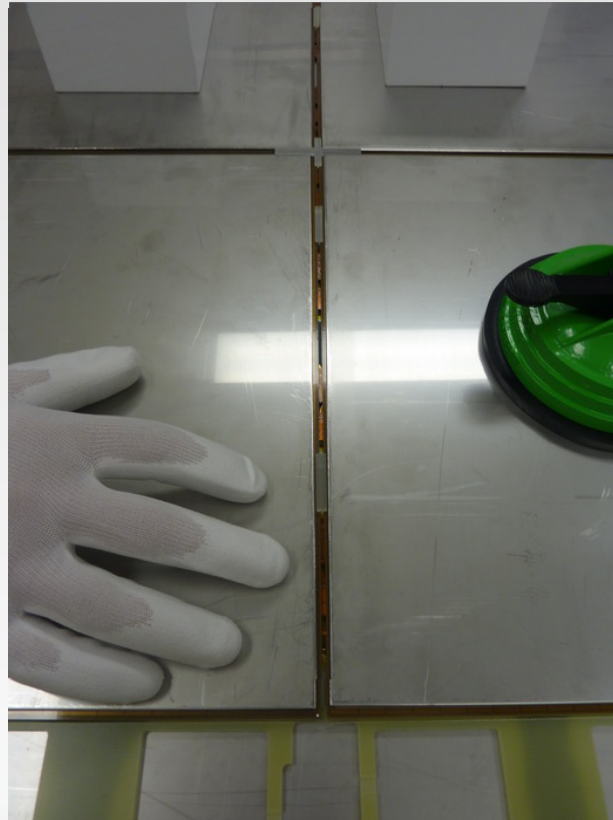
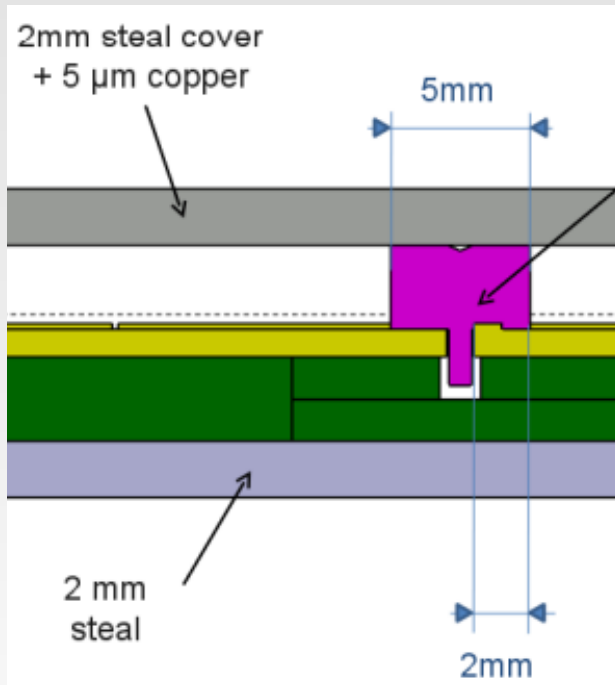
Assembly of the 1 m² prototype

1. Gluing of ASU slabs on vetronite mask



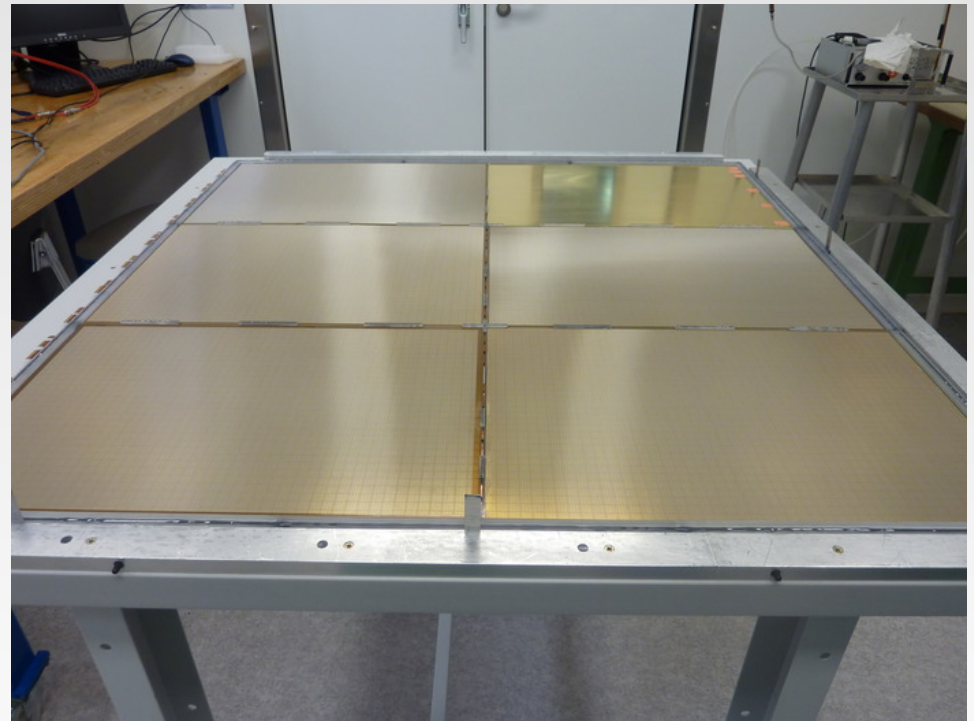
Assembly of the 1 m² prototype

1. Gluing of ASU slabs on vetronite mask
2. Gluing of spacers and frame



Assembly of the 1 m² prototype

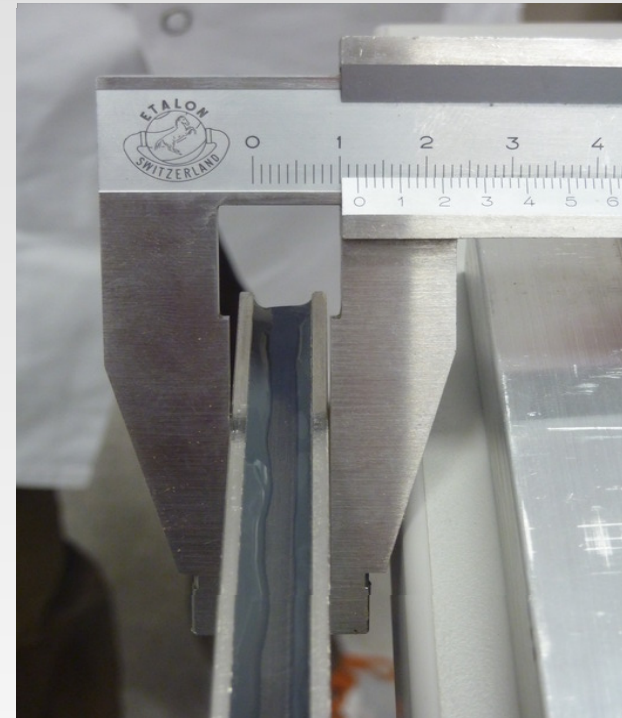
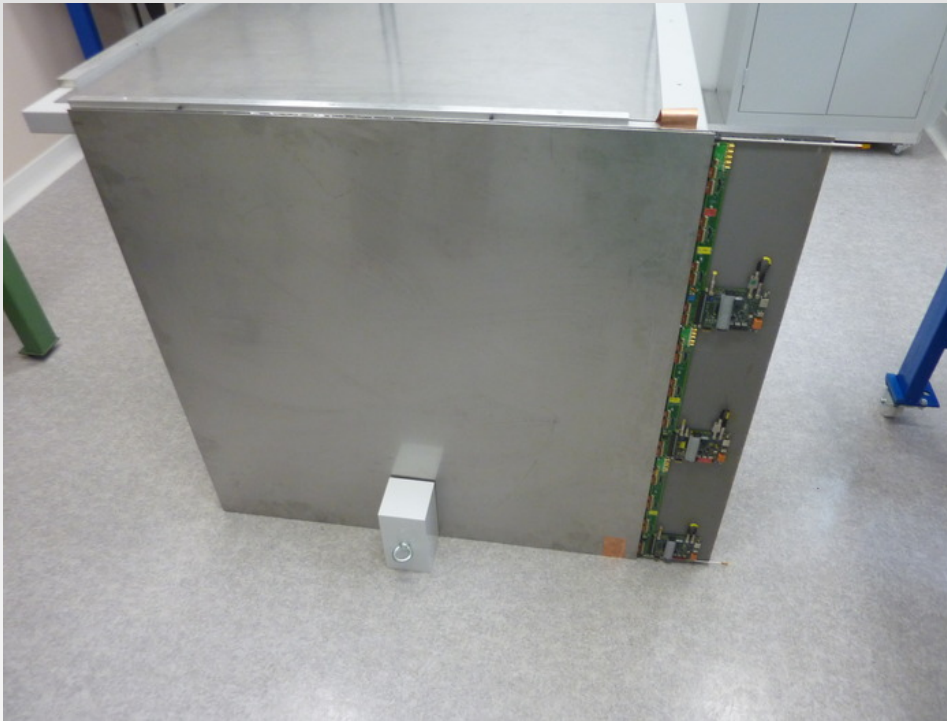
1. Gluing of ASU slabs on vetronite mask
2. Gluing of spacers and frame
3. Gluing of cathode cover



7680 pads!

Assembly of the 1 m² prototype

- After 1 week, the assembly is completed



Total thickness is 12 mm which includes 2+2 mm of steel
→ 8 mm effective thickness complies with ILC goal
(can be reduced to 7 mm by shrinking the meask from 3 to 2 mm)

Test beam - goals

- 4 weeks on SPS/H4
 - 10th / 24th June, CALICE period
 - Until 8th of July, RD51 period, shared beam
- TB program with 150 GeV/c low intensity muon beam
 - Test overall functionality
 - Reach high gas gain and lowest detection threshold on chips
 - Validate/rule out assembly and technical choices
 - Measure efficiency, multiplicity, uniformity
 - Compare performance with/without power-pulsing of chips

NB : The 1m² prototype efficiency will be low (Shaping time short w.r.t. Micromegas signals), nevertheless, several technological choices can be validated and unforeseen problems can be found before the next prototype with an optimised electronics (MICROROC)

Test beam set-up

SPS/H4 beam

- 4 weeks in June/July 2010
- 150 GeV/c muons and pions

Detectors

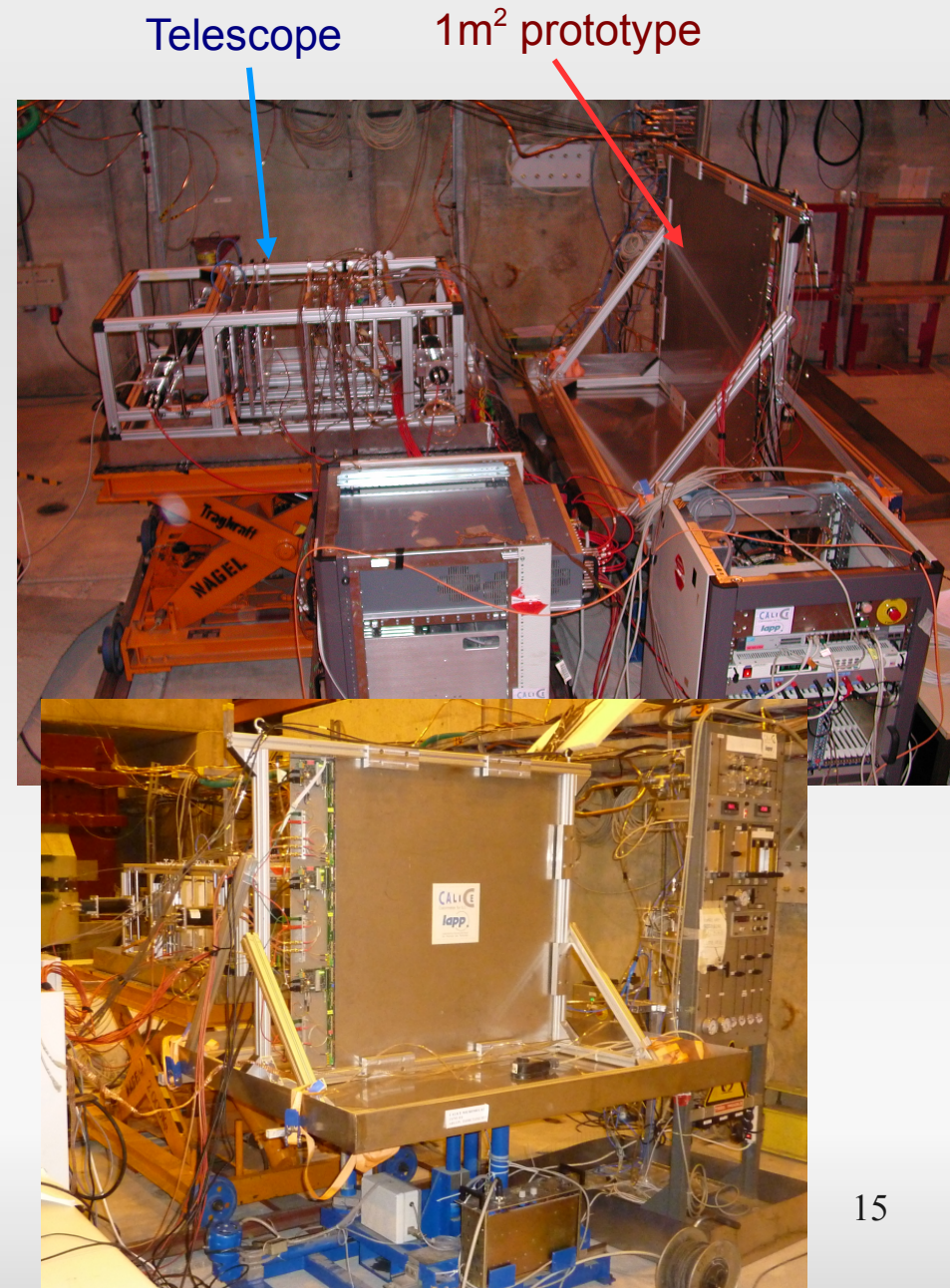
- 3 scintillators for triggering
- Telescope with 4 Gassiplex chambers
- 1m² chamber downstream of the telescope

DAQ

- CAEN ADC/sequencer VME module and LabView Centaure module
- DIF (synchronized with CCC) and LabView program
- Trigger obeys BUSY and READY signal logic → common event numbering for off-line reconstruction

Rates

- Beam rate and scintillators trigger rate < 1kHz,
- Acquisition rate ~ 300Hz



Trigger set-up

Chip settings

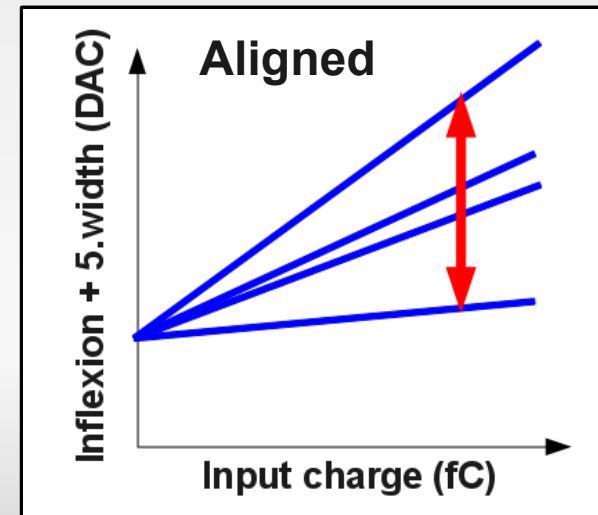
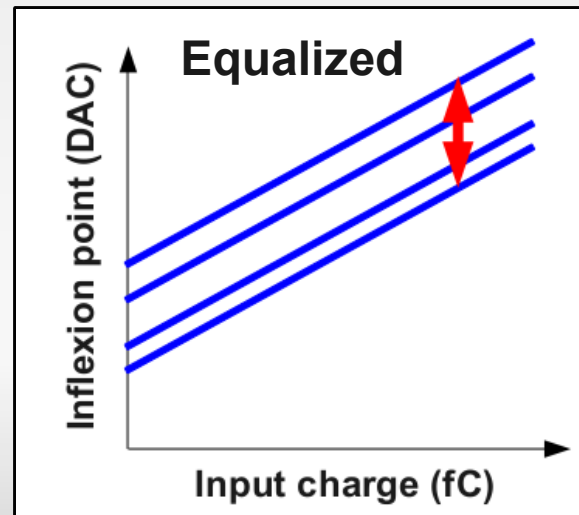
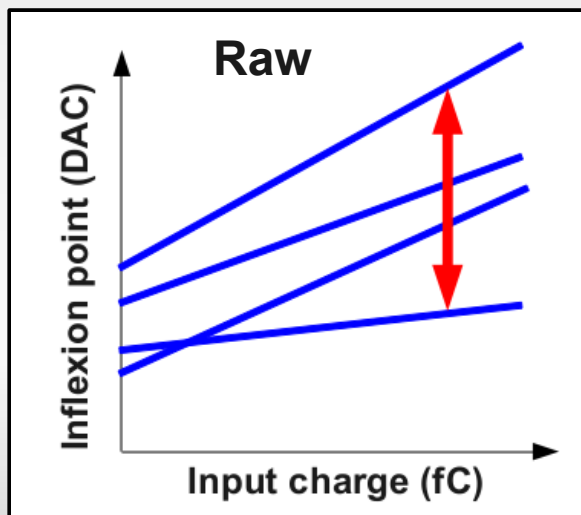
Chip parameters : Shaping time (per chip) set to max ~ 20 ns,
threshold (per chip), preamplifier gain (per channel)

1. Uniform response settings

- Correct detector non-uniformity with preamp gains
- Proved to work in laboratory
- Threshold given by pedestal dispersion (~ 10 fC)

2. Low threshold settings (used during TB)

- Align Scurve end-points using preamp gains
- Increase gain dispersion but reduce thresholds



Chip settings

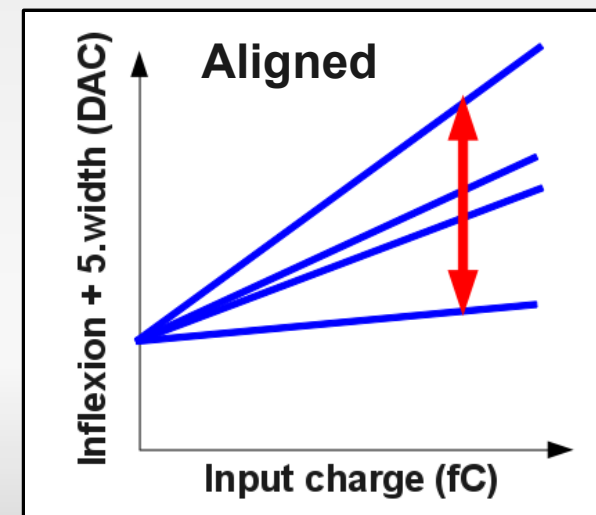
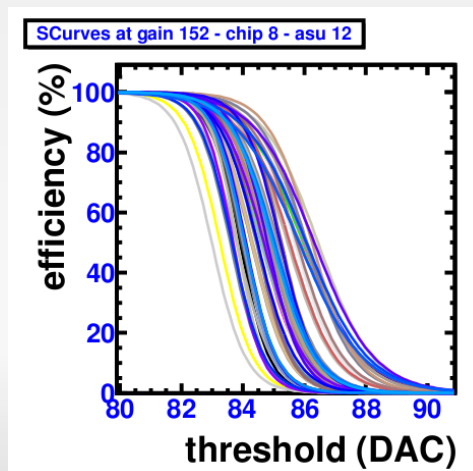
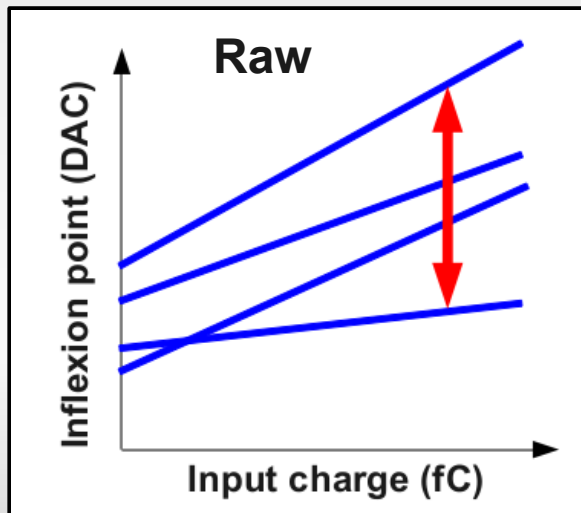
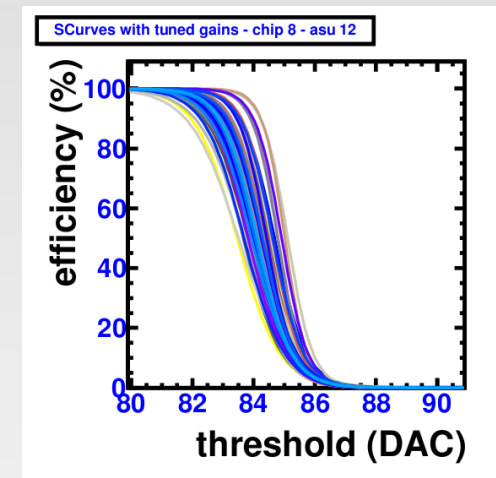
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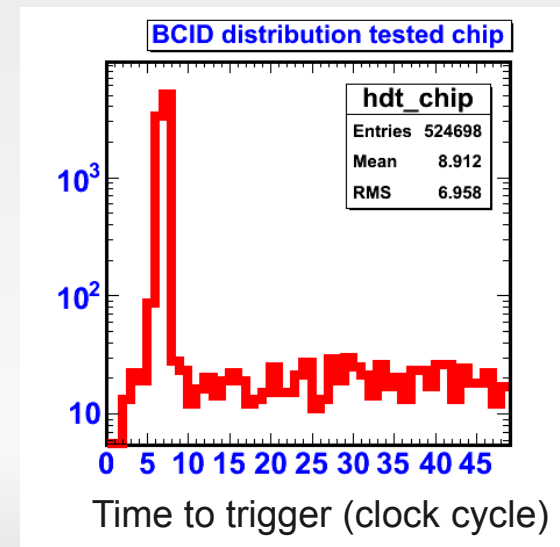
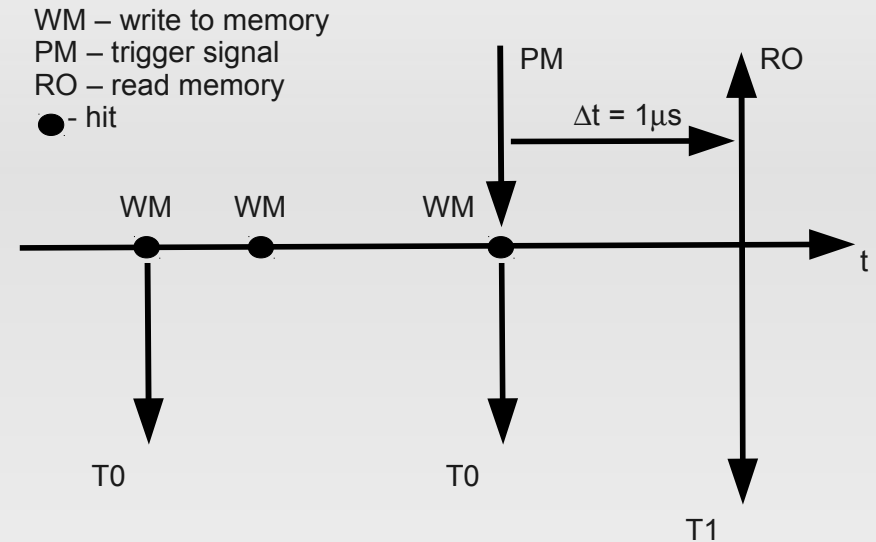
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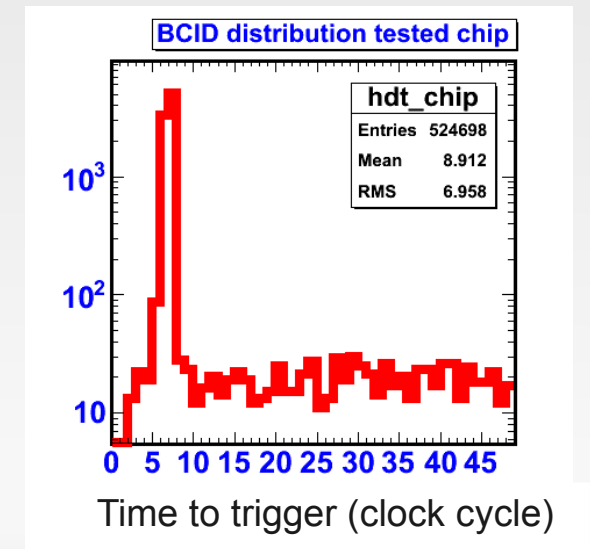
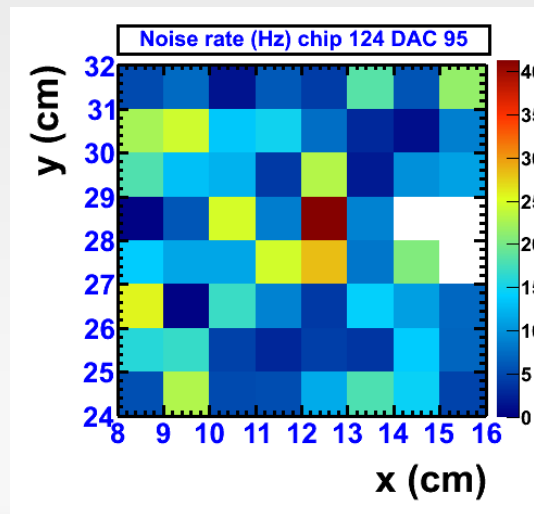
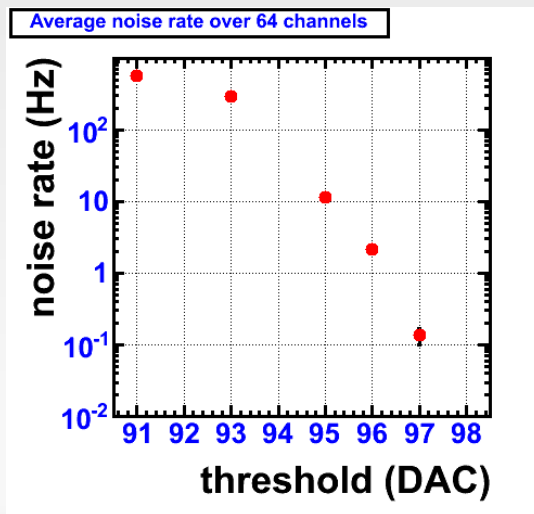
Time-stamping

- Timing features
 - Time-stamping with 200 ns precision
 - Clock distributed to DIF by Clock Control Card
 - 127 event depth memory (reset above)
- Time-stamping
 - Time of hits T_0
 - Time of readout T_1
~ time of trigger if READY state
- Signal selection
 - Insert module
→ 1 us delay between trigger and readout
 - Hits from triggering particles have
 $T_1 - T_0 = 1 \text{ us} = 5 \text{ clock cycles}$



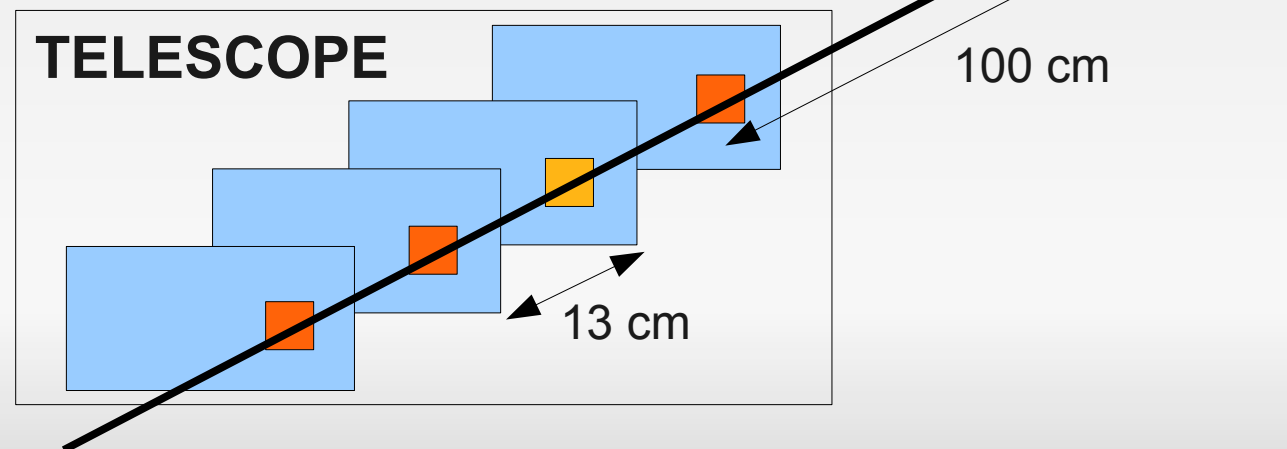
Noise rate

- Low threshold settings
 - Noise hits un-avoidable
- Typical rates per channel of tens of Hz
- After time cut, however, drops to negligible value
 - Chip S/N ratio > 100
 - Noise hit probability/chip < 1 %



First results

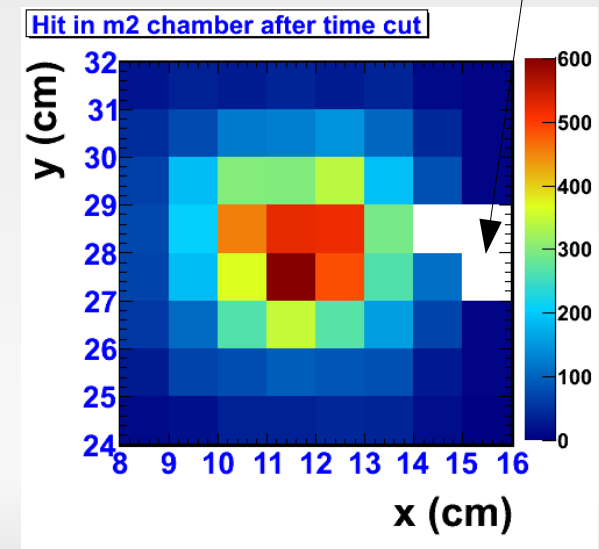
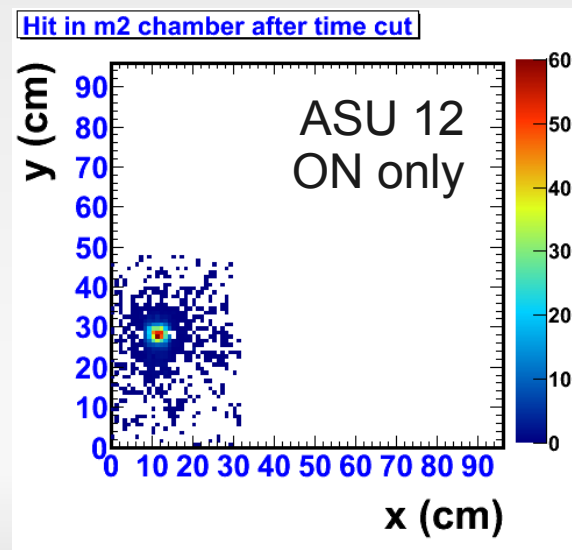
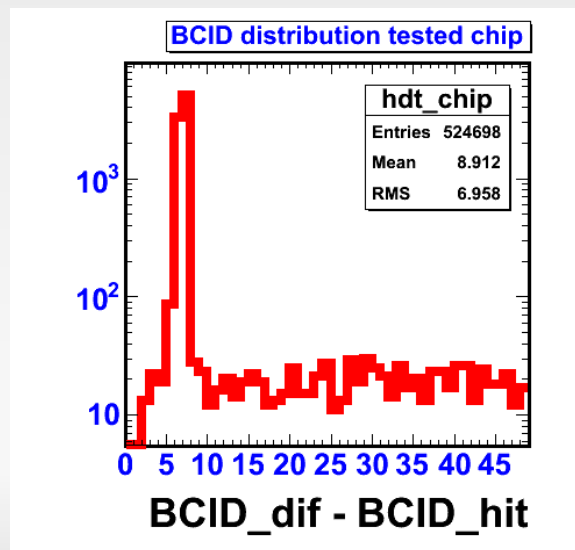
- Runs @ 420 V to determine the maximum efficiency (given the shaping time issue)
- Runs @ 410 V to determine the efficiency/multiplicity values and uniformity
- Use telescope to extrapolate tracks to m2 chb. Same pad size (1 cm²) in telescope and m2 chb.
 - select straight tracks in telescope: single aligned hits in at least 3 of the 4 chb.
 - look for hits in m2 chb. in 3x3 cm² area around extrapolated track impact



Runs @ 420 V

- Gas gain of 15000 → expected Landau MPV ~ 20 fC
Remember: only 10 % of the signal is seen → effective signal MPV is 2 fC !
- Approx. 40000 triggers recorded
 - 200 Hz muon beam centered on 1 chip of ASU 12
- S/N ratio in time peak of 208 (3 noisy channels switched OFF)
 - Peak contamination after time cut < 0.5 % for the chip
 - Noise hit probability after time cut ~ 0.01 % per channel

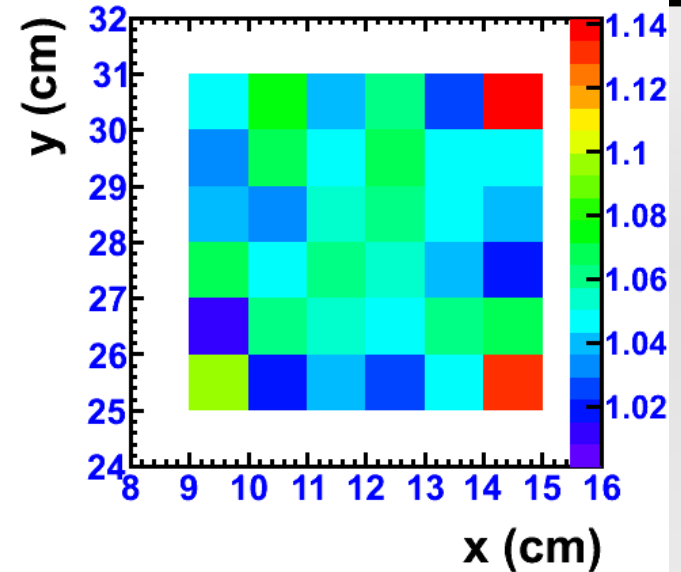
Noisy channels
switched off



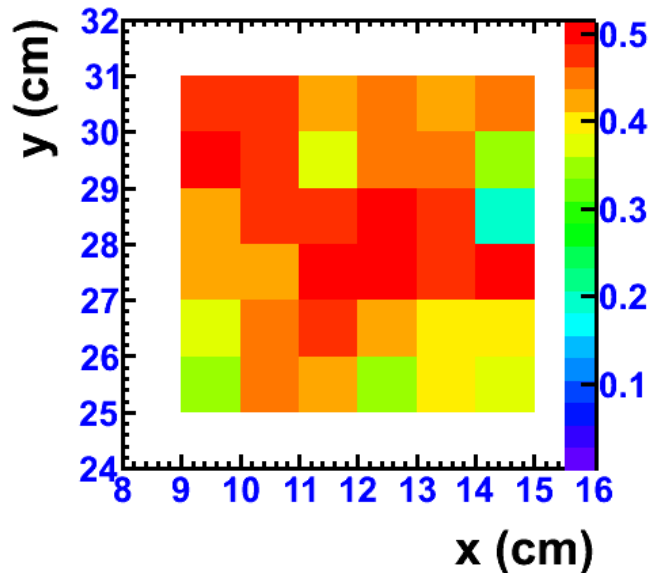
Runs @ 420 V

- Average efficiency of $45.2 \pm 4.1 \%$
Remember: only 10 % of the signal is seen!
- Average multiplicity of 1.05 ± 0.02
Compatible with previous measurements with Gassiplex

Multiplicity in 3x3 cm² area

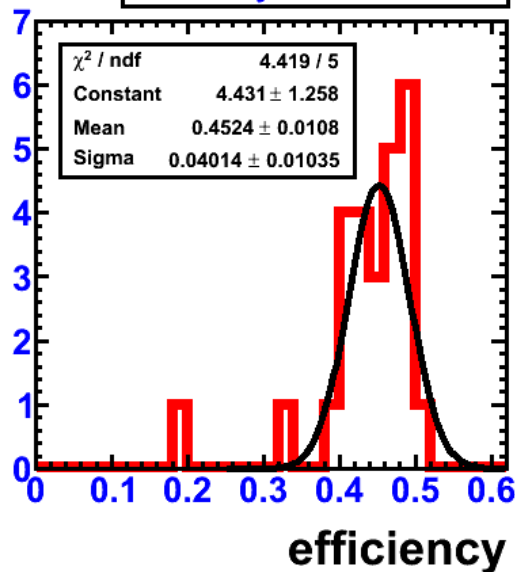


Efficiency in 3x3 cm² area



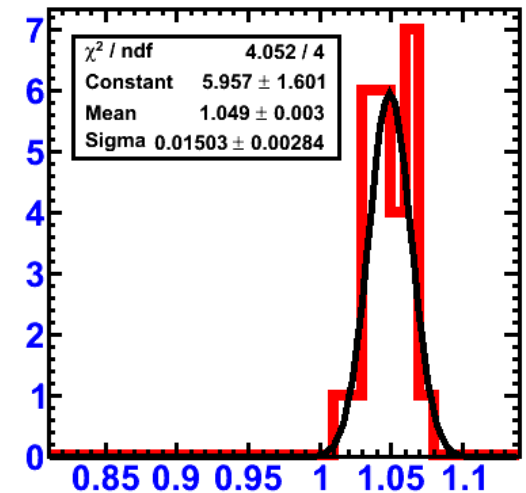
Efficiency error < 5 %

Efficiency in 3x3 cm² area



Efficiency error < 2.5 %

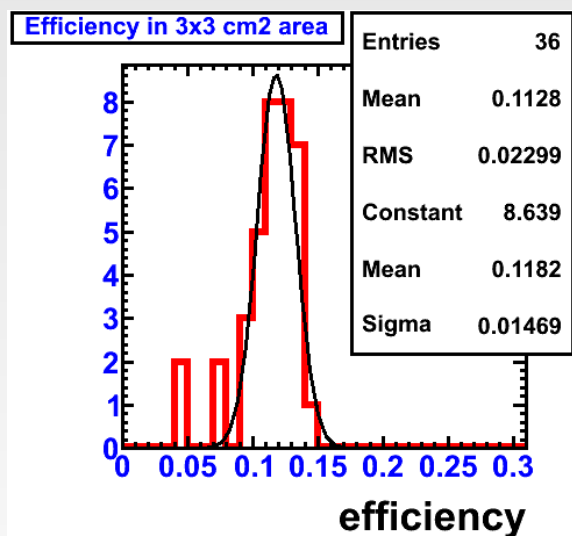
Multiplicity in 3x3 cm² area



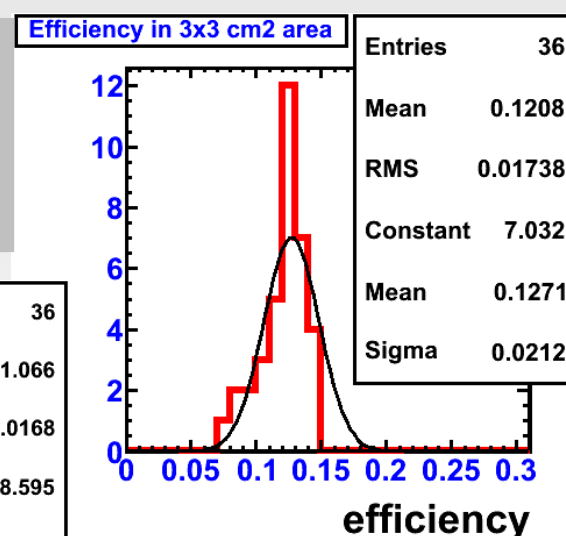
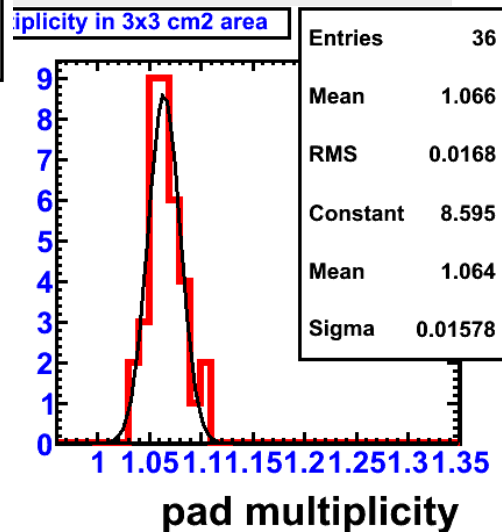
pad multiplicity

Runs @ 410 V

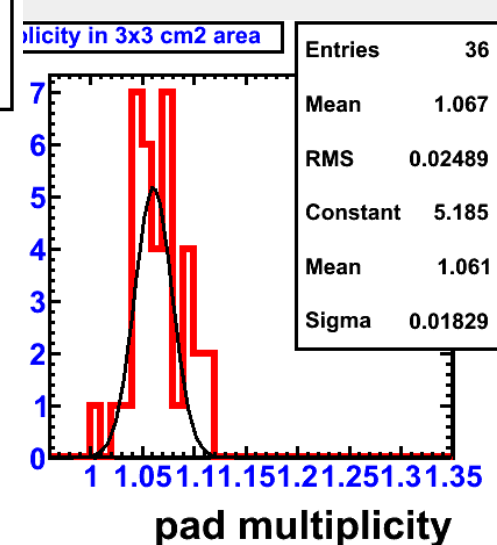
- Lower gas gain and higher threshold configurations → much lower efficiency
- Determine the uniformity of efficiency and multiplicity over the m2 chamber area → beam directed at a few chips with 400000 triggers per chip
- First results on 2 chips indicate that the mean values and RMS remain the same
 - To be completed with more results on more chips



CHIP 124
Close to center
11.2 % +/- 1.5 %
1.07 +/- 0.02

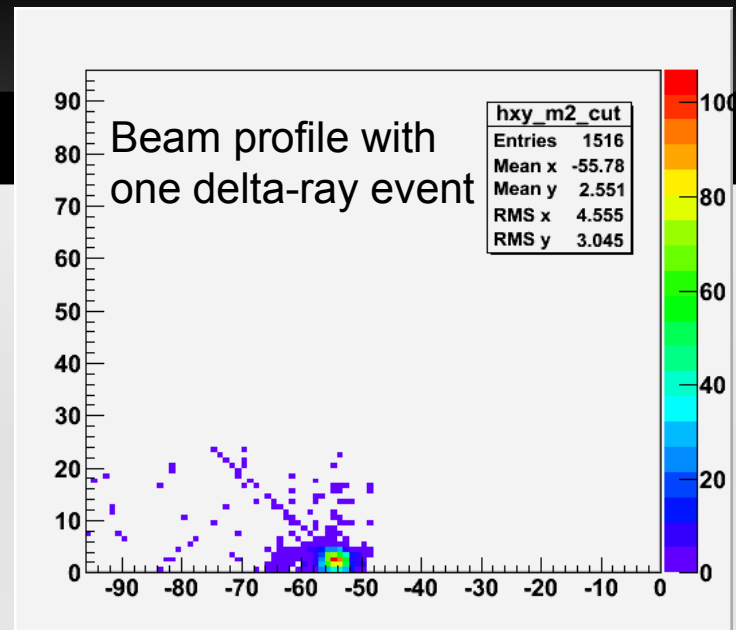


CHIP 114
Close to spacers
12.7 % +/- 1.6 %
1.07 +/- 0.02



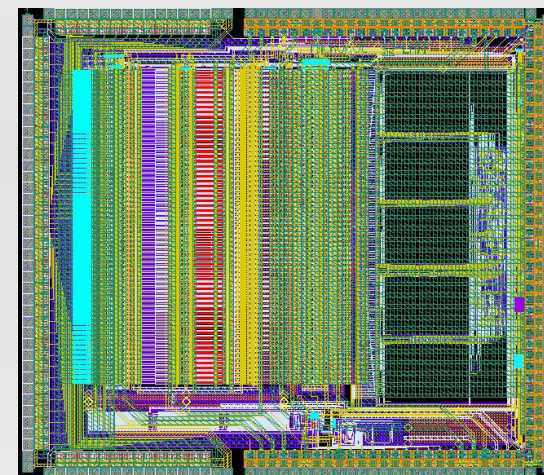
TB summary

- Mechanics
 - The 1 m2 is gas tight and robust
- Electronics
 - Successful synchronization between telescope and 1 m2 prototype DAQ
 - Preamp gain adjustment to lower thresholds works
 - Stable and reliable DAQ
- Detector
 - Very few mesh HV trips (limit @ 1 uA)
 - Gas gain up to 15000 reached, (@ low beam intensity of 200 Hz)
- Software
 - Reconstruction of simultaneous events from both DAQs realized
 - Data file book keeping under development for next test beam

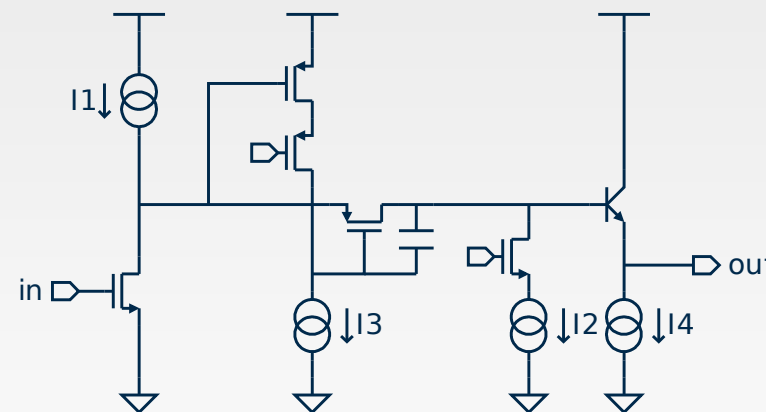


New front-end electronics

- Shaping time need to match the detector signals
→ modify analog part of the chip & keep same digital
- MICROROC
 - Collaboration between LAL/Omega and LAPP/LC
 - Pin to pin compatible with HR
→ very few developments on firmware, software, boards



- Features
 - Charge preamplifier
 - Shaping time of 30, 100, 150 or 200 ns
 - 3 thresholds with 10 bits resolution
 - 400 fC dynamic range
 - Noise RMS (C_{det} of 80 pF) of 0.24 fC with 200 ns shaping time
 - Consumption of 6.9 mA



Spark protections

- Some experience gained on spark protection with diode networks
 - Network test setup @ LAPP
 - See presentation of R. Gaglione in WG2 session at previous collaboration meeting (Freiburg)
- MICROROC protections on board and on chip
 - A serial decoupling capacitor ($C_s = 470 \text{ pF}$) and a diode network (BSV99 or NUP4114)
 - Two clamping diodes (D1 and D2), the parasitic serial resistor (R_s) and another diode network (D3 and D4)

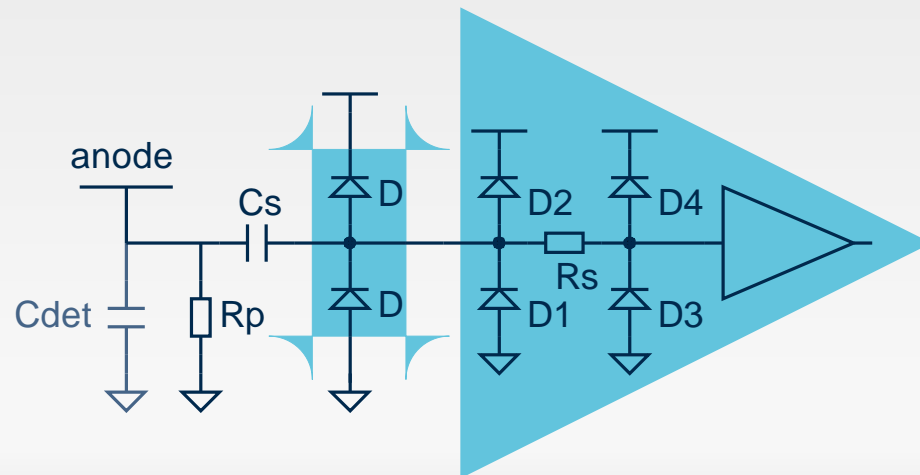
Protection network :

$C_{det} = 80 \text{ pF}$

$R_p = 1 \text{ M}\Omega$

$C_s = 470 \text{ pF}$

$D = \text{BAV99/NUP4114}$



Next steps

- Actual 1 m² prototype with HR2 chips
 - Finish TB data analysis
 - Mainly thresholds and P/T dependence of detector performance
 - Test behaviour in hadron showers
 - Join TB of AHCAL in 1 m³ W-structure as last active layer
 - Start on October the 18th on T7 (muon run)
 - Move to T9 on November the 3rd (low energy hadron)
- Next prototype with MICROROC
 - First chip received (5 over 300 produced) and test started
 - If working, fabricate and equip 6 ASU with MICROROC
 - First 1 m² plane ready before mid-2011
 - A few planes available before end-2011
- 2011 TB plans
 - Repeat 2010 TB campaign → efficiency/multiplicity, behaviour in showers + spark rate
 - Within CALICE and RD51 → use RD51 telescope

Conclusion

- Small size Micromegas chambers show very good performance and are well suited for an HCAL
Maintaining these results when scaling up the detector size is challenging
 - Mechanics, electronics, gas distribution, HV stability, DAQ

- First attempt is satisfactory
 - Front-end chip input stage brings the efficiency down BUT
 - No true road blocks, detector operated up to high gas gain
 - Several technical choices validated
 - Potential improvements for next prototypes revealed

- Second attempt with new ASIC (MICROROC)
 - Longer shaping time, first chip in hands
 - Aim at producing and testing as many prototypes as possible in 2011