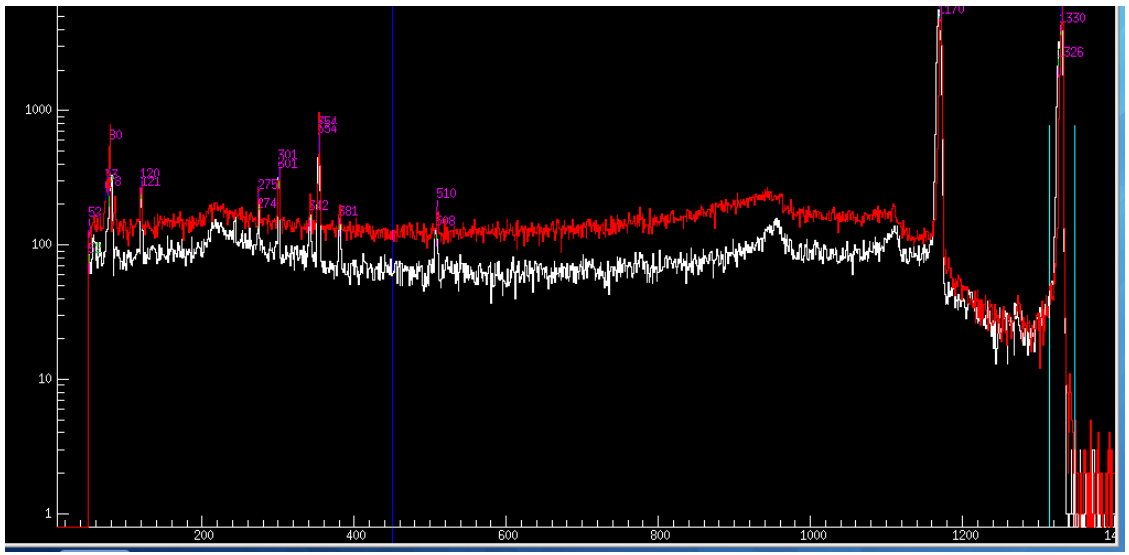
Possible avenues of Pulse processing

Vandana Nanal, TIFR

- R&D in digital signal processing in our lab
- ASIC development in India
- Possible contribution to PARIS readout

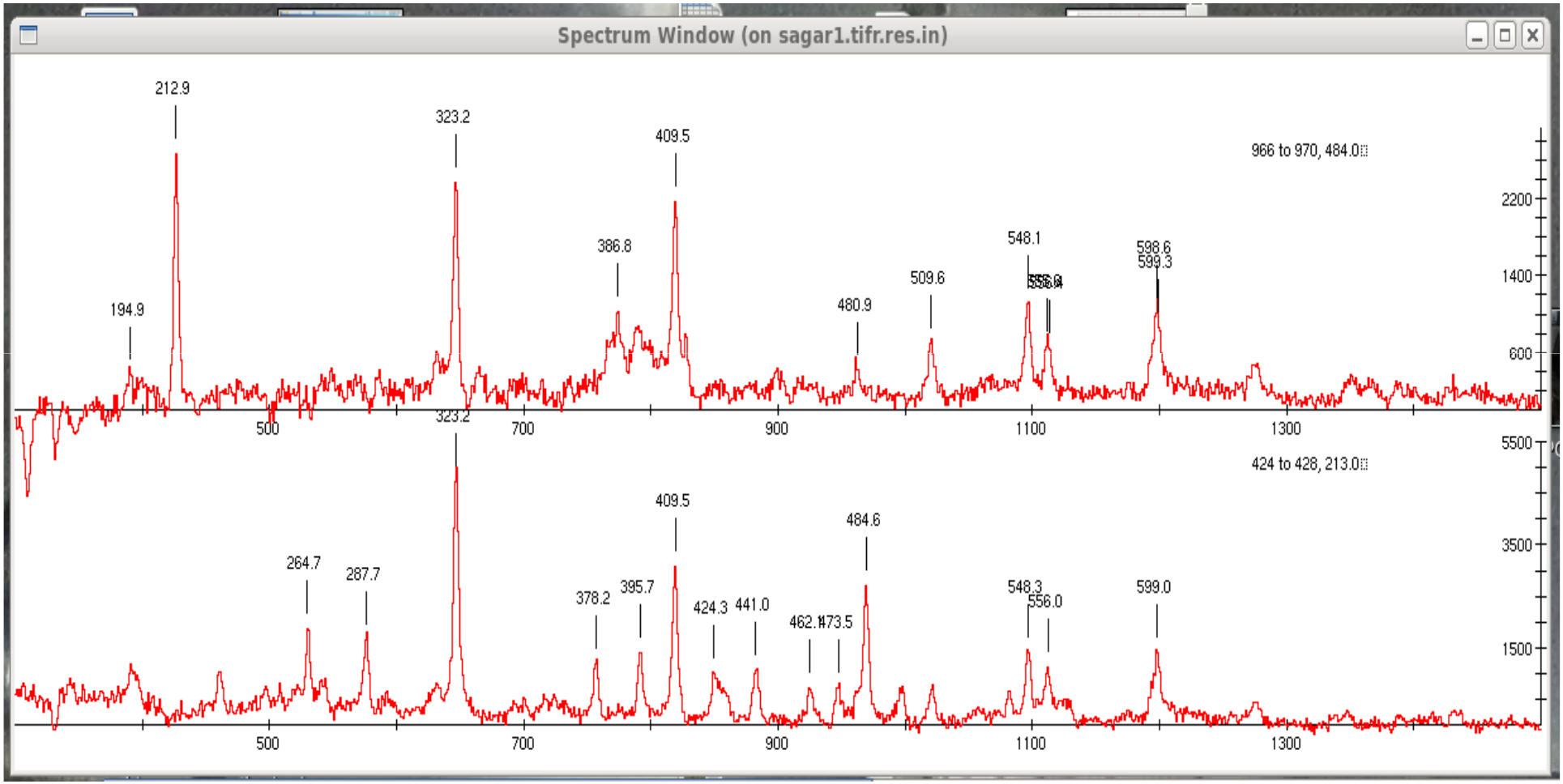
DSP based DAQ for 24 CS-Clovers and Ancillary detectors INGA at TIFR (R. Palit, TIFR)

- 100 MHz & 12-bit ADC's
- Data rate: 80 MB/sec
- E resolution better than analog
- Handle high count rate with good E,T.
- Particle ID in CsI detectors using digital pulse shaping
- Trigger less system
- For in-beam Clover + CsI expts and off-line expts with planar detectors.



Commercial PXI system

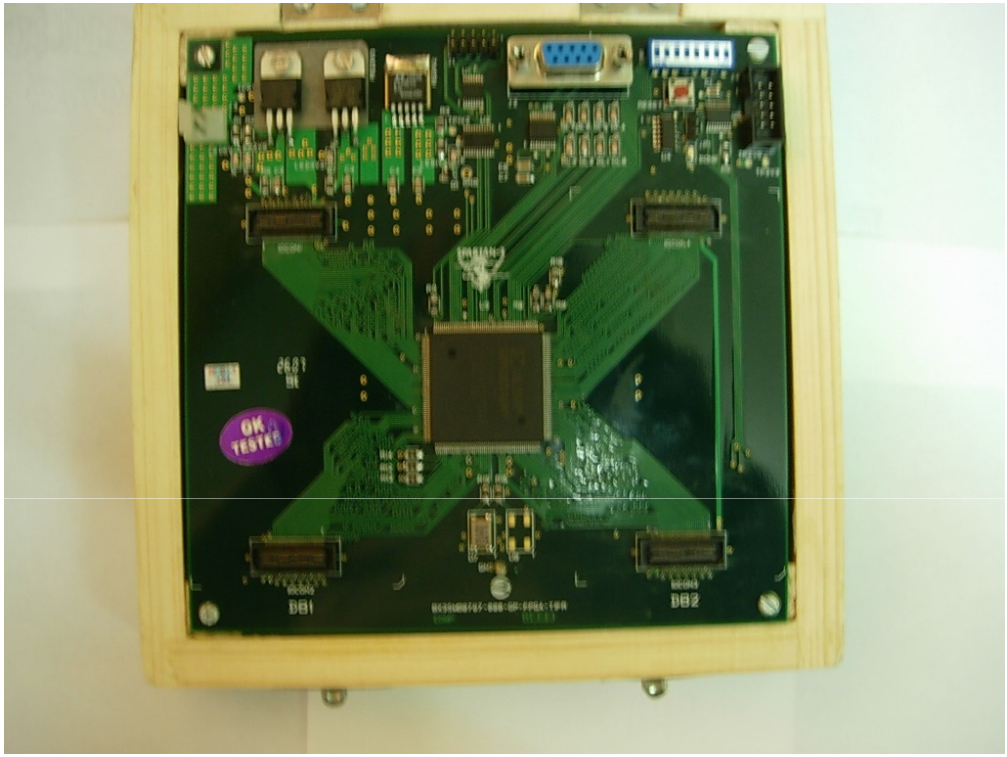
Coincident spectra for level scheme of ^{185}Au with New DDAQ



R&D on digital electronics
(J.A. Gore & S.G. Kulkarni, NPD-BARC)

- High speed analog I/O board
- High speed digital I/O board
- BPM digitizer
- CAMAC modules
    - Controller
    - ADC, DAC
    - Output register
- Stand alone analog I/O board

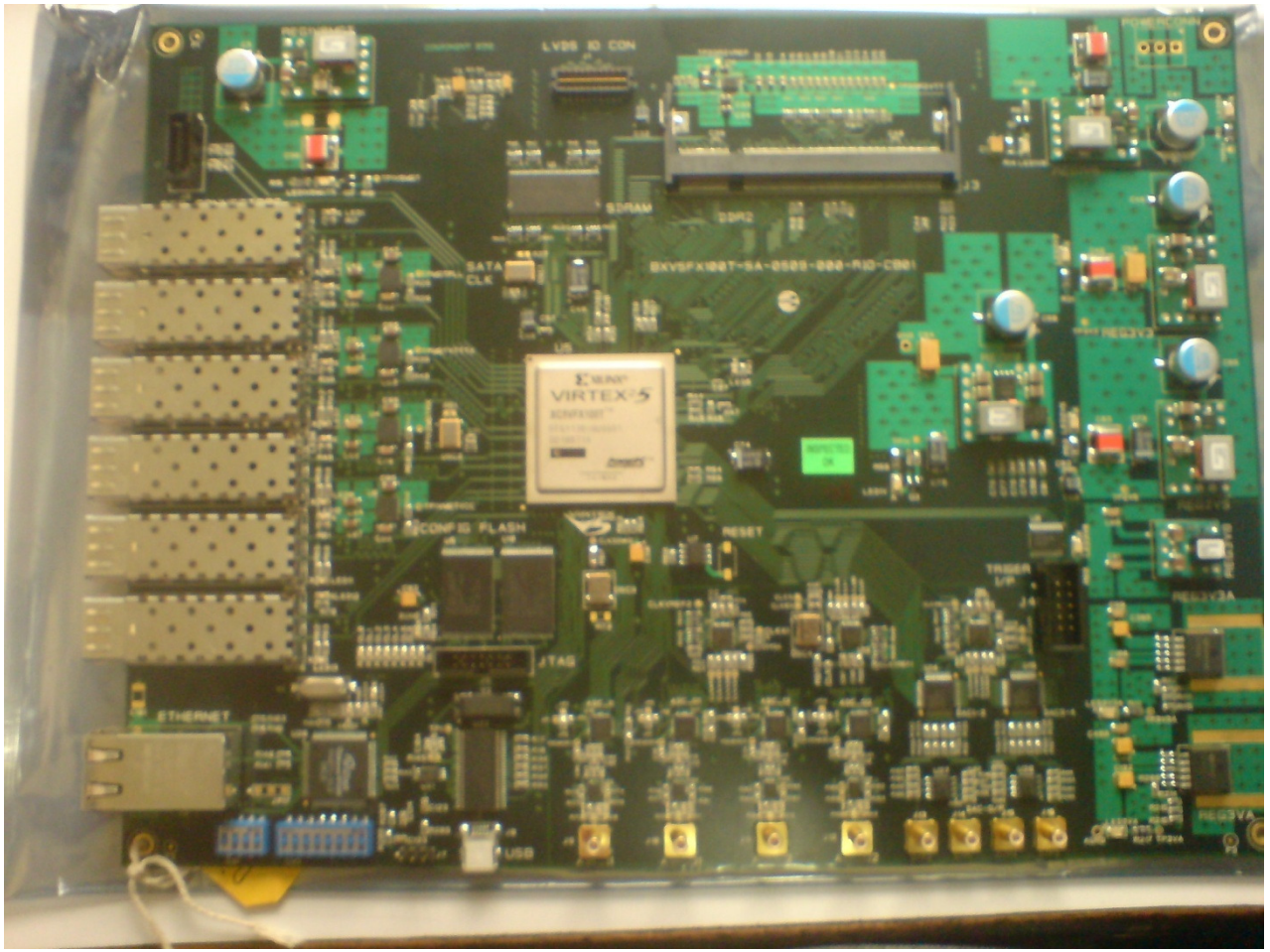
High speed digital I/O board



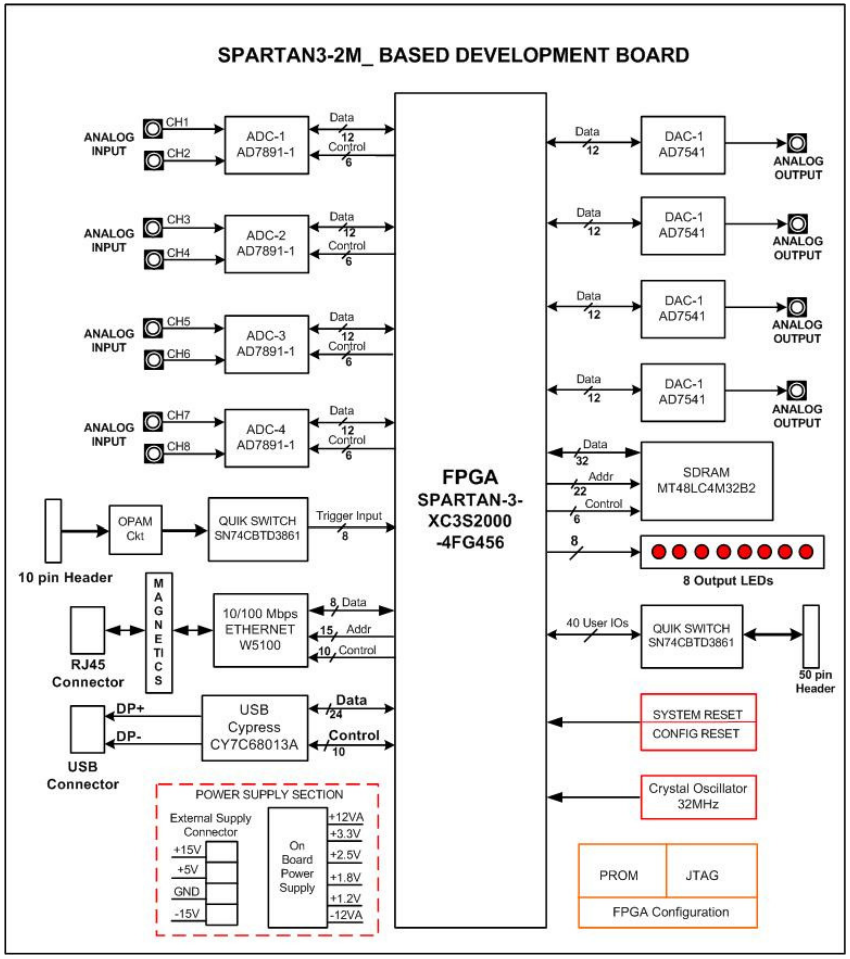
Features:

- Spartan -3 (XC3s400)
- 140 impedance matched I/Os
- RS-422 interface

Virtex-5 Stand-alone board



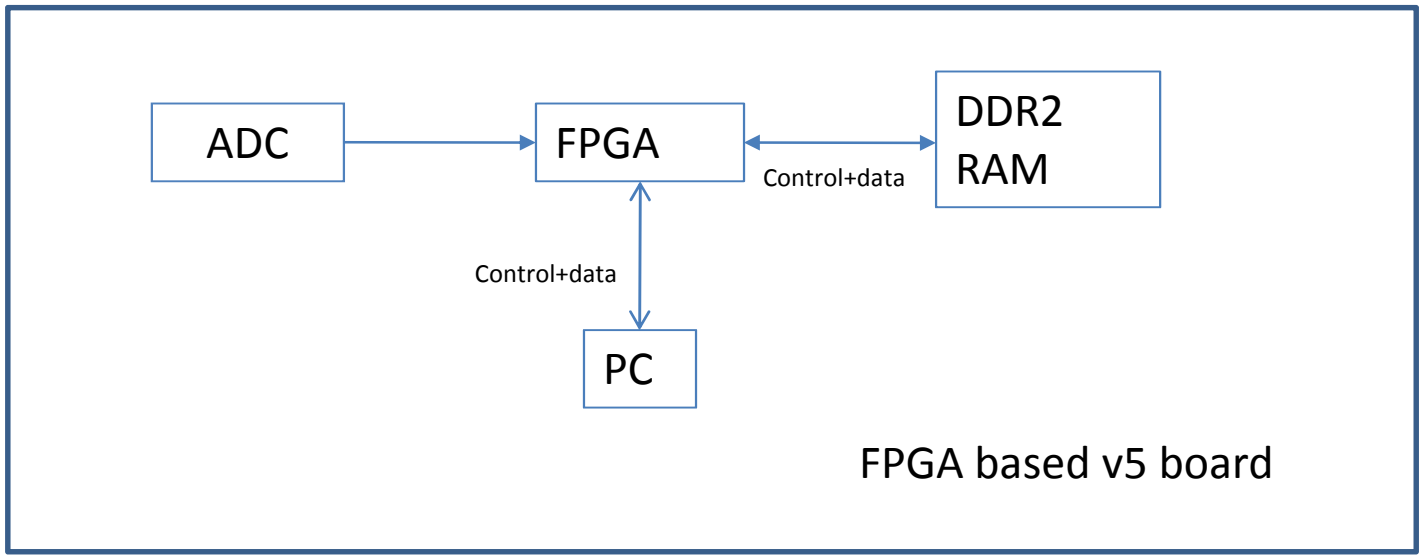
Standalone analog I/O board



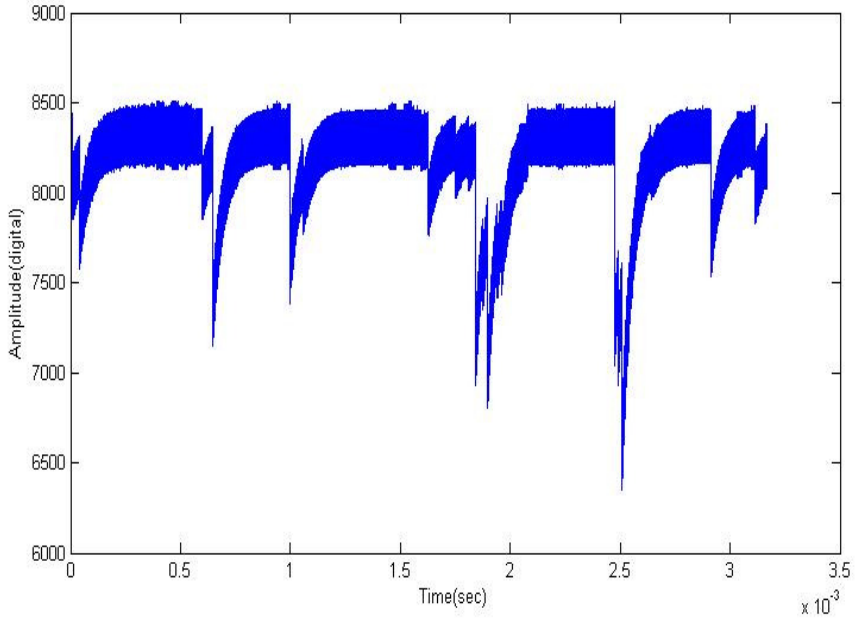
- Plan to use for Low level RF control
- Board with 1 GHz sampling rate has been designed, fabrication in process

Board Details:

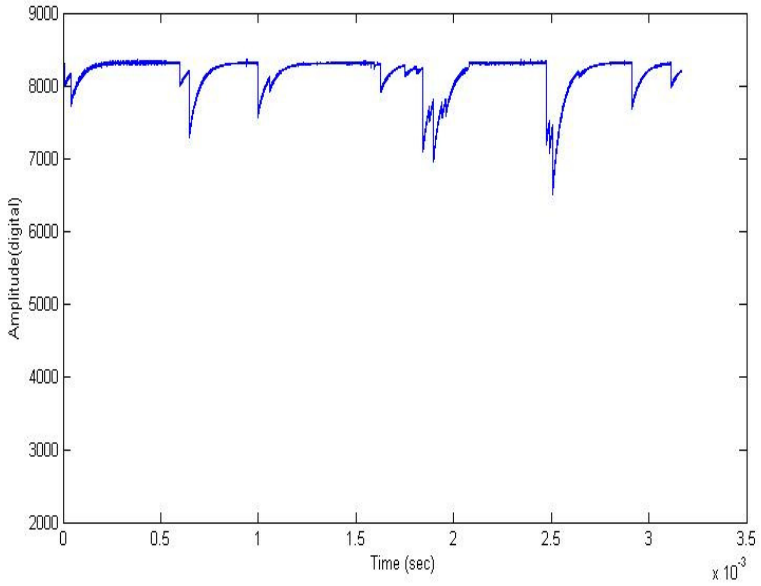
- 4, 14 bits, 125 MHz Analog inputs.
- 4, 14 bits, 125 MHz Analog outputs.
- On-board, 2 GB DDR2 RAM.
- 6 SFP connectors (Connected to Rocket IO), Tested @1.5Gbps
- On-board USB and ethernet interfaces.



Pulse_data



Noisy Data



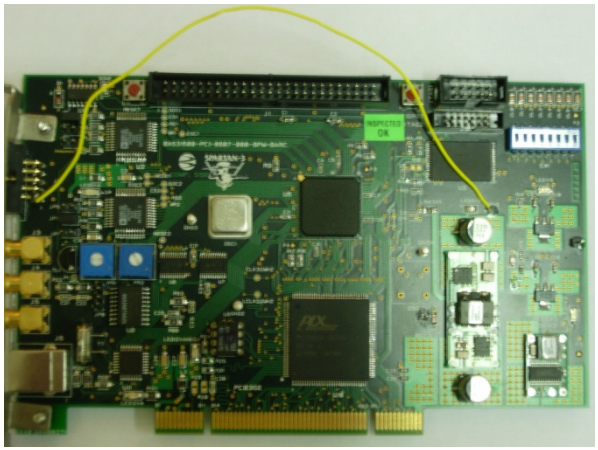
Moving Average Data (4 datapoints)

- Data Acquired for ~3 msec.
- Filtered with a simple moving average filter implemented in VHDI
- Data transfer through a USB interface.

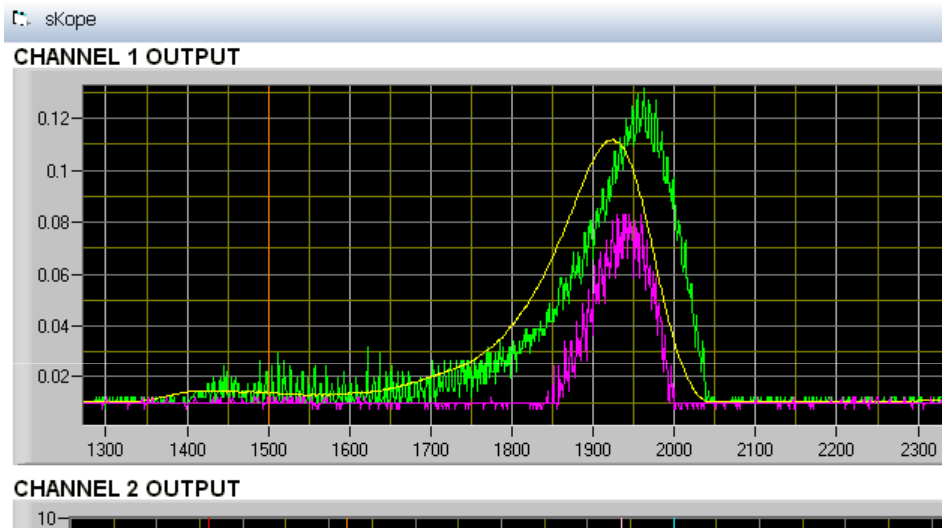
FPGA based boards designed and developed

Beam Profile monitor digitizer

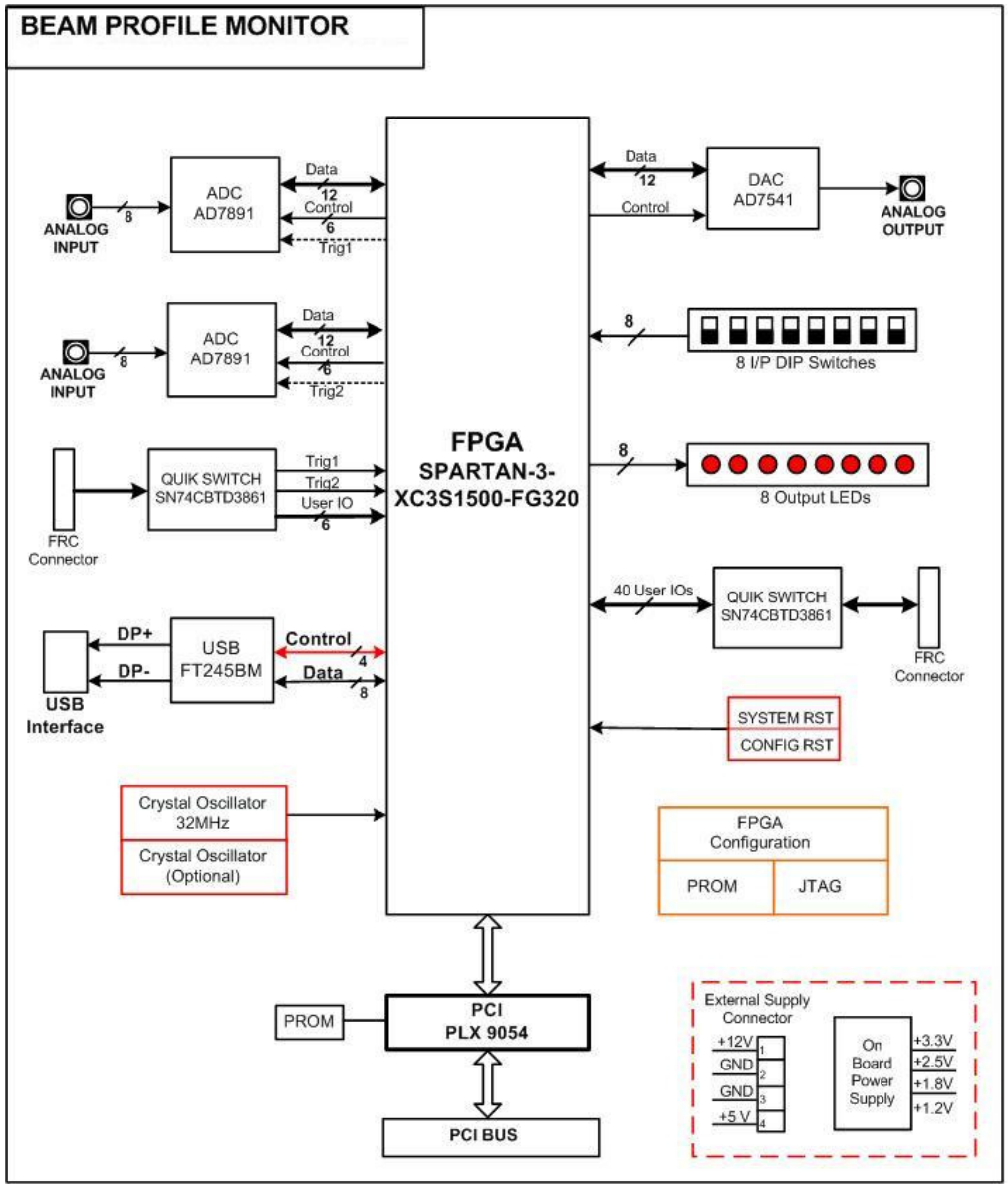
- 12 bit, upto 500KHz, 2 channels
- 32 bit, 33 MHz PCI interface



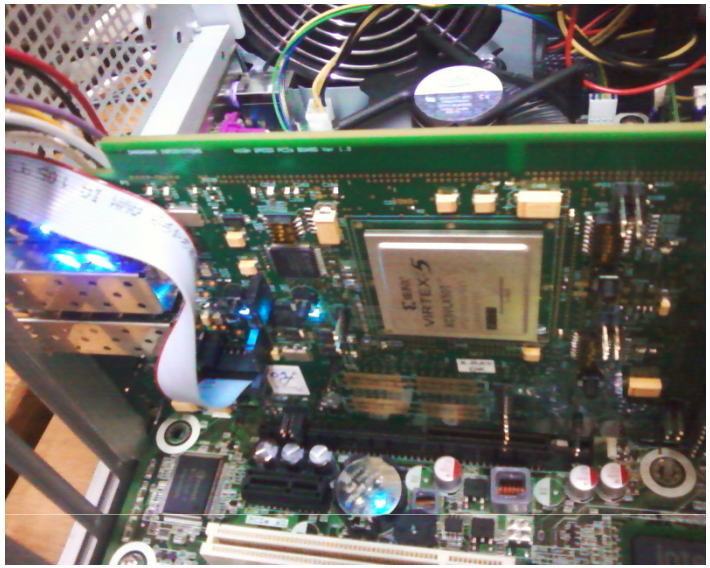
GUI in visual basic for BPM



40 uncommitted I/Os can be used to acquire/control additional accelerator parameters.


BEAM PROFILE MONITOR
ANALOG INPUT
8
ADC AD7891
Data
12
Control
6
Trig1
ANALOG INPUT
8
ADC AD7891
Data
12
Control
6
Trig2
FRC Connector
QUIK SWITCH SN74CBTD3861
Trig1
Trig2
User IO
6
USB Interface
DP+
DP-
USB FT245BM
Control
4
Data
8
Crystal Oscillator 32MHz
Crystal Oscillator (Optional)
FPGA SPARTAN-3- XC3S1500-FG320
PROM
PCI PLX 9054
PCI BUS
Data
12
Control
DAC AD7541
ANALOG OUTPUT
8
8 I/P DIP Switches
8
8 Output LEDs
40 User IOs
QUIK SWITCH SN74CBTD3861
FRC Connector
SYSTEM RST
CONFIG RST
FPGA Configuration
PROM
JTAG
External Supply Connector
+12V
GND
GND
+5 V
1
2
3
4
On Board Power Supply
+3.3V
+2.5V
+1.8V
+1.2V

PCI-Express card



•8 lane interface with PCI Express and uses Xilinx Virtex-5 FPGA for protocol implementation.

•48 differential pairs for interfacing with external components .

• Two SFP fibre channel interfaces which can facilitate high speed data transfer from PC to other devices.

ASIC developments in India

V.B. Chandratre et al. , BARC Newsletter Oct. 2007

- **Detectors, devices, modeling new process**:
  Silicon strip detectors micro/macro & pixel, Avalanche photodiode (APD), Silicon drift detectors (SDD),
  Extended gate devices
  Novel semiconductor process development with Spice modeling & PDK development

- **Application Specific Integrated Circuit design** :
  ASICS for detector signal processing PDK kit integration

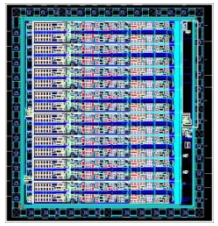
- **System Circuit design & prototyping** :
  HMC, FPGA, IP core , device driver development

Nuclear Instrumentation: Detectors, ASIC's and Hybrid Microcircuits (HMC's)

ASIC's : 0.7u Mixed CMOS Process

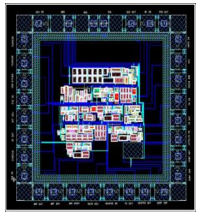
Detector Front-End Signal Processing ASIC's

INDIPLEX



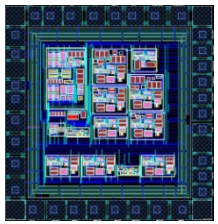
16-Channel Pulse Processing ASIC

SINGLEPLEX



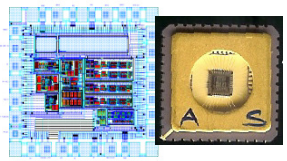
Single Channel Pulse Processing ASIC

Low Noise Pulse Processing Channel for Silicon Drift Detector



Data Conversion ASIC's

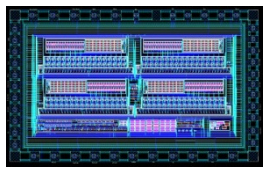
ANU-SHIKHAR ASIC



Low Power Peak Detect & Hold Circuit

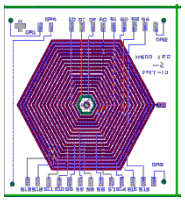
Wilkinson ADC

ANUSMRITI ASIC

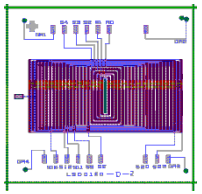


128-Cell, 500MHz Analog Memory

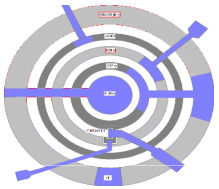
Sensors : Silicon Drift Detectors



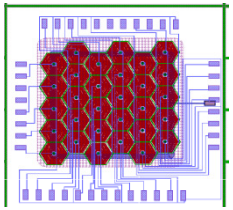
Hexagonal SDD



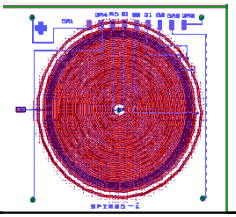
Linear SDD



SDD with Jfet



Imaging Array

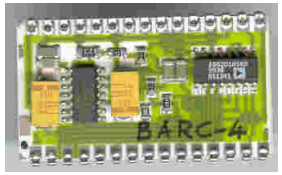


Spiral SDD

Hybrid Micro Circuits (HMC's)

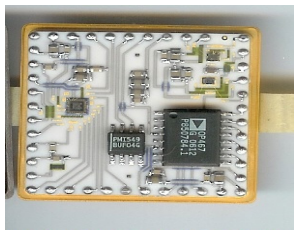
FS 500ns-10us
Resolution
75ps@500ns FS

Time To Amplitude Converter



Peak stretcher for 8K Nuclear ADC

"Singleplex" ASIC in Hybrid For Neutron Monitors

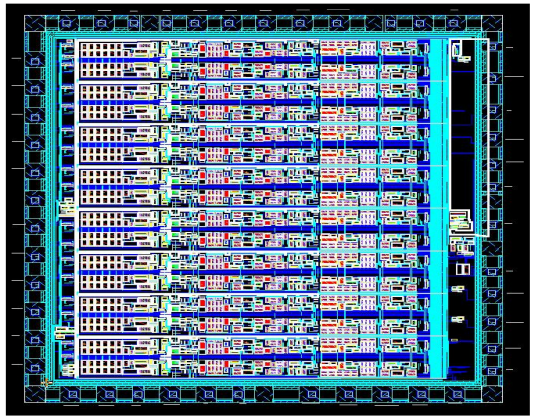


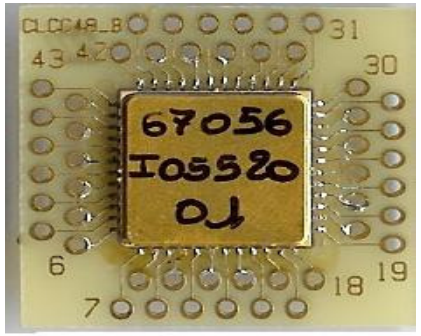
Fast Preamp family for Indian neutrino Observatory Gas RPC tr 1.5 ns 27,000 Qty requirement

Indiplex and Singleplex ASICS
Sub-micron 0.7u CMOS process

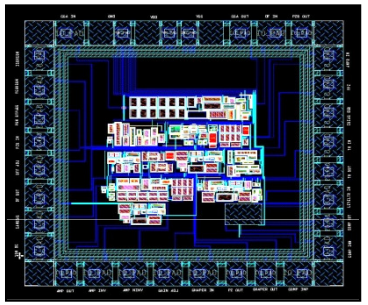
INDIPLEX: 16 channel pulse processing ASIC comprising CSA, PZ-block & Semi Gaussian shaper.

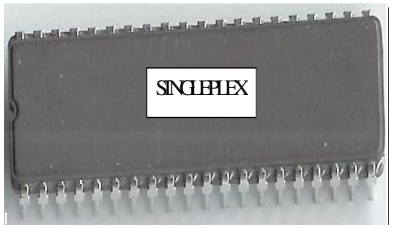
SINGLEPLEX:
Single pulse processing channel ASIC similar to INDIPLEX





INDIPLEX





High Dynamic Range (+/- 600fC)
Low Noise with Low Noise Slope (600e @0pf , 7e/pf Noise slope)
Output Signal Swing +/-2V
Active DC pedestal cancellation
Optimized for Proportional pad detectors made BY VECC for ALICE experiment

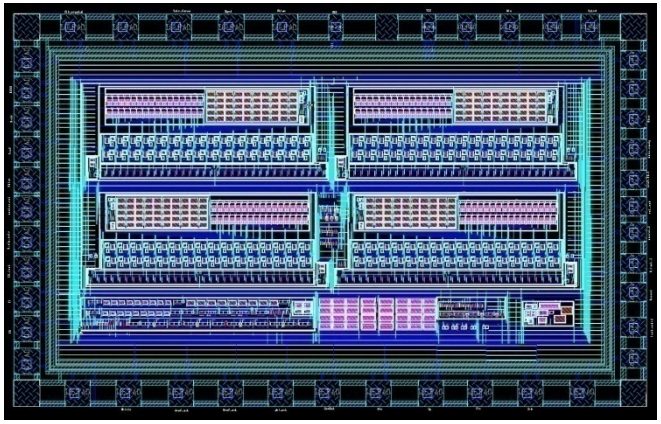
ANUSMRITI ASIC

Analog Memory

Digital delay line based analog memory

Specifications :

Read-out Frequency	*1 MHz*
Dynamic range	*2V*
Power Supply	*0-5V*
Power Consumption	*400mW*
Die Area	*4.5 mm by 2.5 mm*
Package	*CLCC-44*



High Speed transient Digitization 500MHz, 128 bin

ANU-KSHAN ASIC

DLL based Time to Digital Converter

Anu-Kshan is a DLL based Time to Digital Conveter implementing real time stamping of events with a resolution of 65 psec.

Key Features:

- ***10 MHz Reference Clock***
- ***32-bit coarse counter for real time stamping***
- ***Delay Locked Loop based Vernier Counter providing 1:100***

Various ongoing projects involving R&D on digital signal processing

- Nustar/R3B FAIR
- Exogam2
- SPIRAL2 BPM readout
- RPC based large scale detector at Indian Neutrino Observatory
- Cryogenic bolometer array for neutrinoless double beta decay

What we plan to do for PARIS

- Tests with 2x2 cluster with 4 $LaBr_3$ +NaI Phoswich
- Start with PXI based system/ Commercial CAEN system for $LaBr_3$ and phoswich readout
- Sampling rate 100 MHz- 1GHz
- Contribute to R&D as well as production of Readout electronics
- Contribute 4 detectors to prototype
- R&D on 1”/2” $CeBr_3$

Thank you