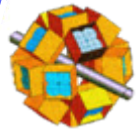


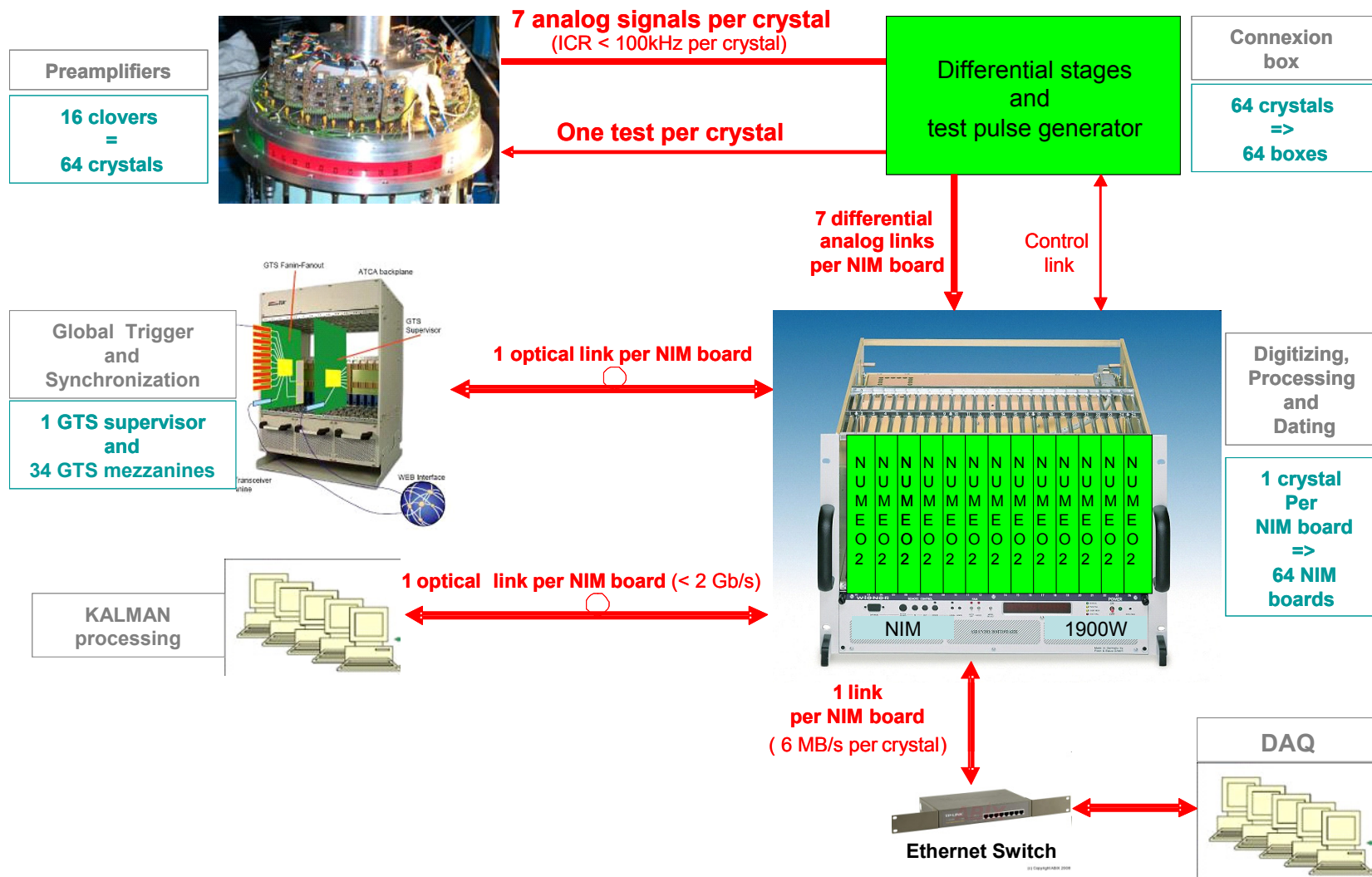
EXOAM2 project

Digital instrumentation of the EXOGAM detector

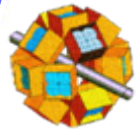
- Overview of the technical project
- Status of the digitizer prototype
- Synergy EXOGAM2 NEDA and PARIS



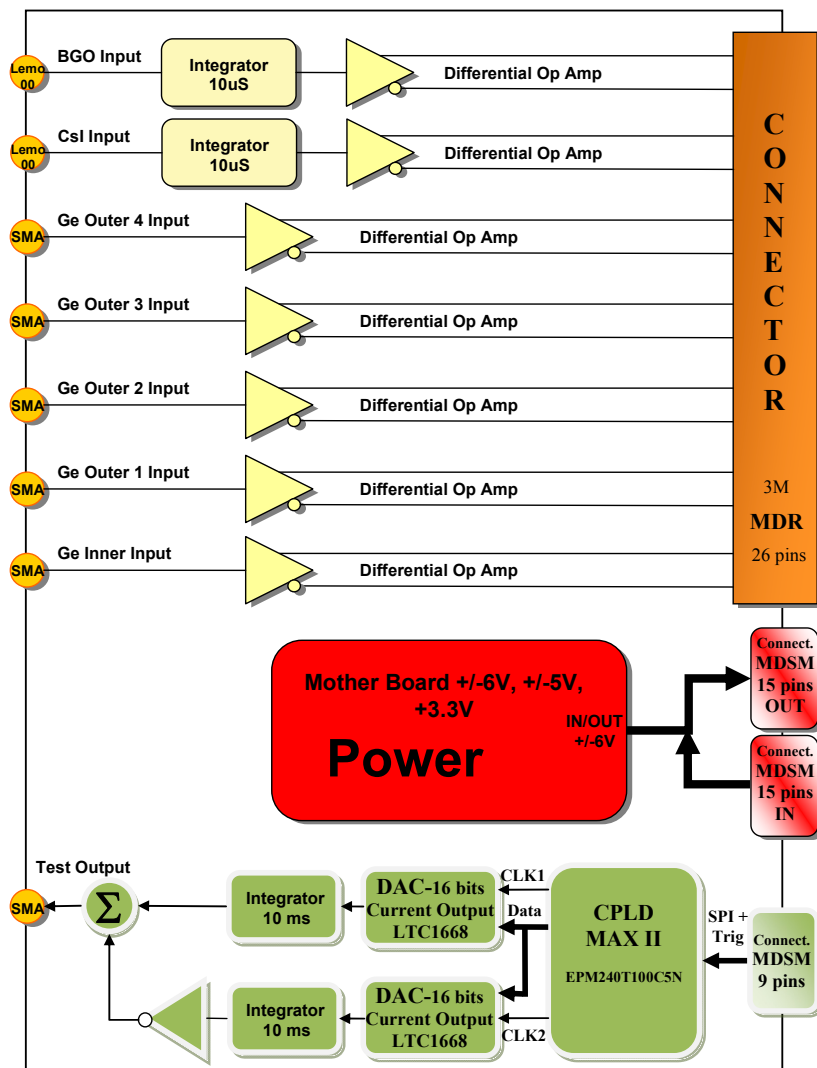
General architecture



FROM DETECTOR

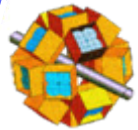
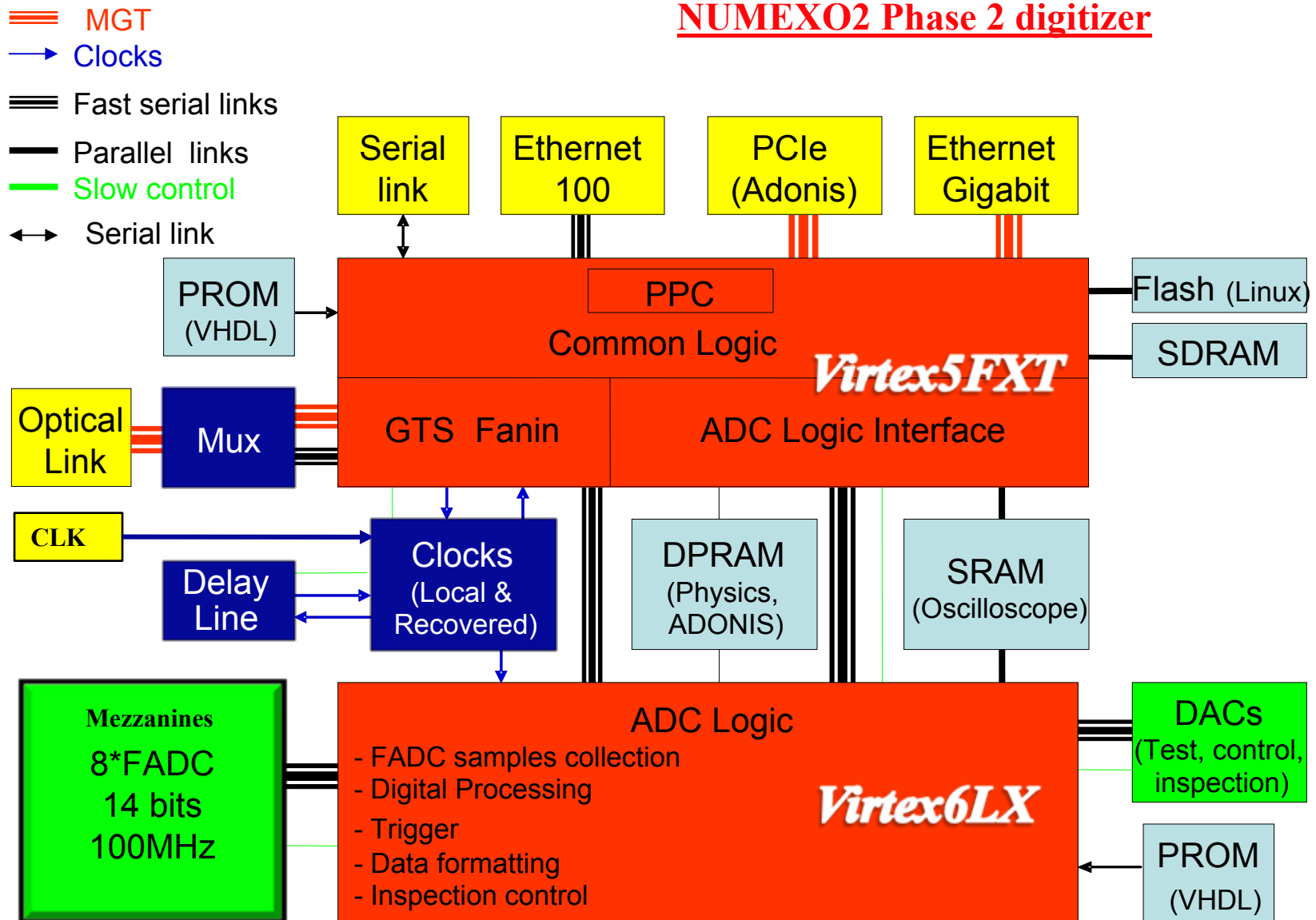


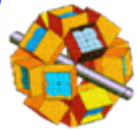
Connection box B3



FROM / TO NUMEX02



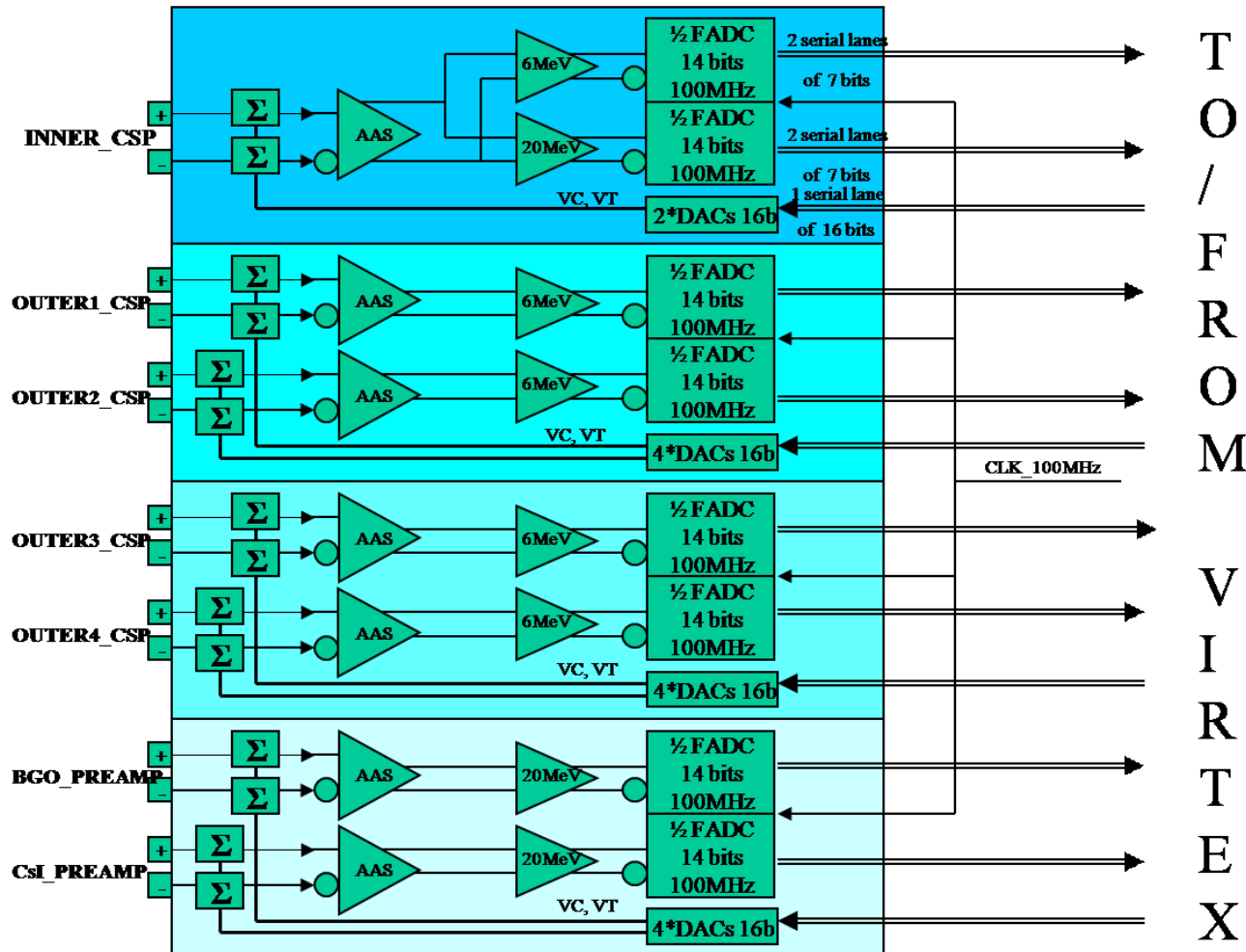
NUMEXO2 Phase 2 digitizer

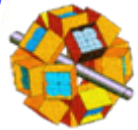


NUMEX02

Block diagram of 8 FADC channels

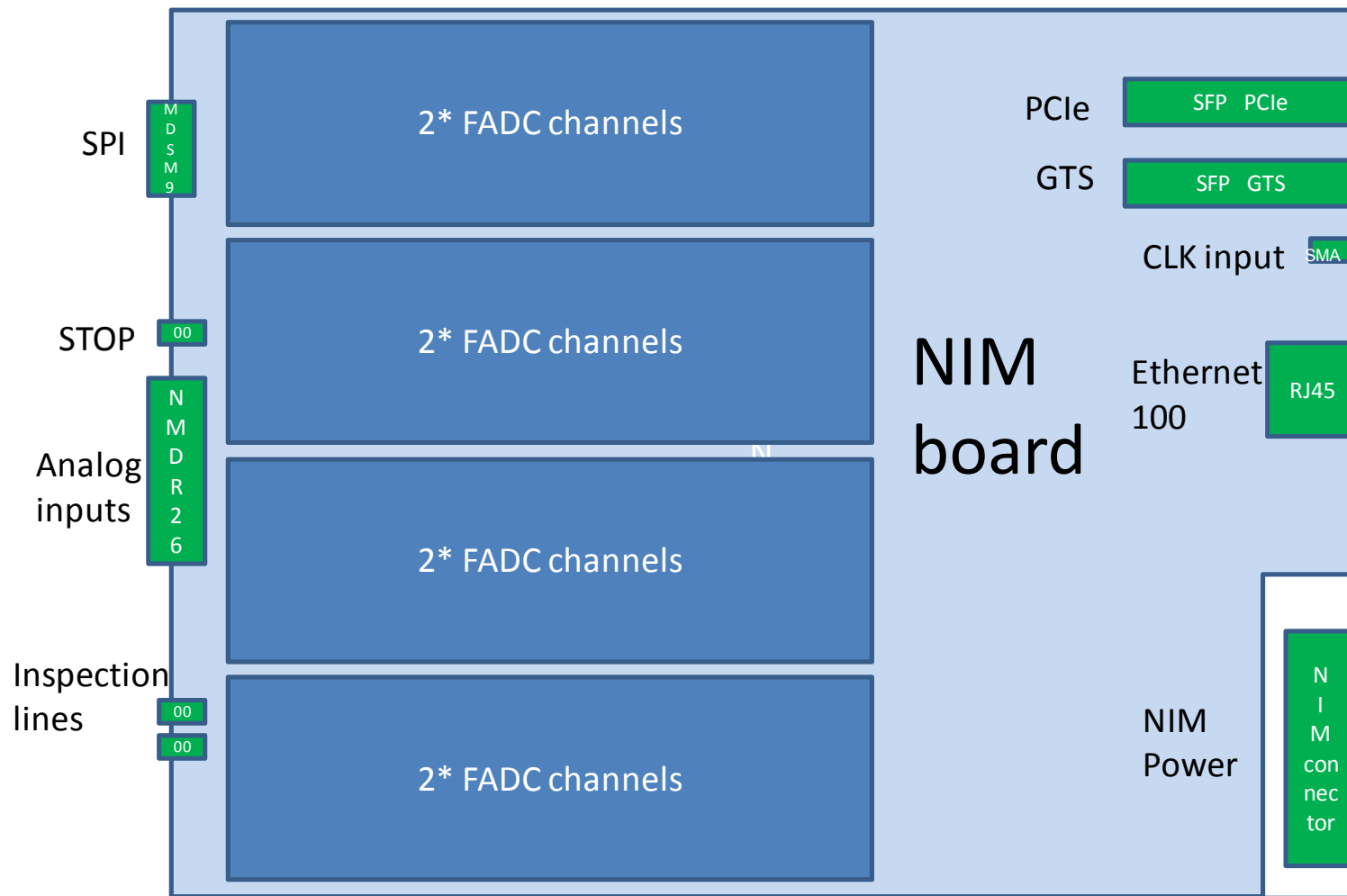
One crystal = 7 detector channels

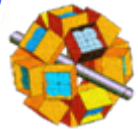




Option A : 8 FADC channels

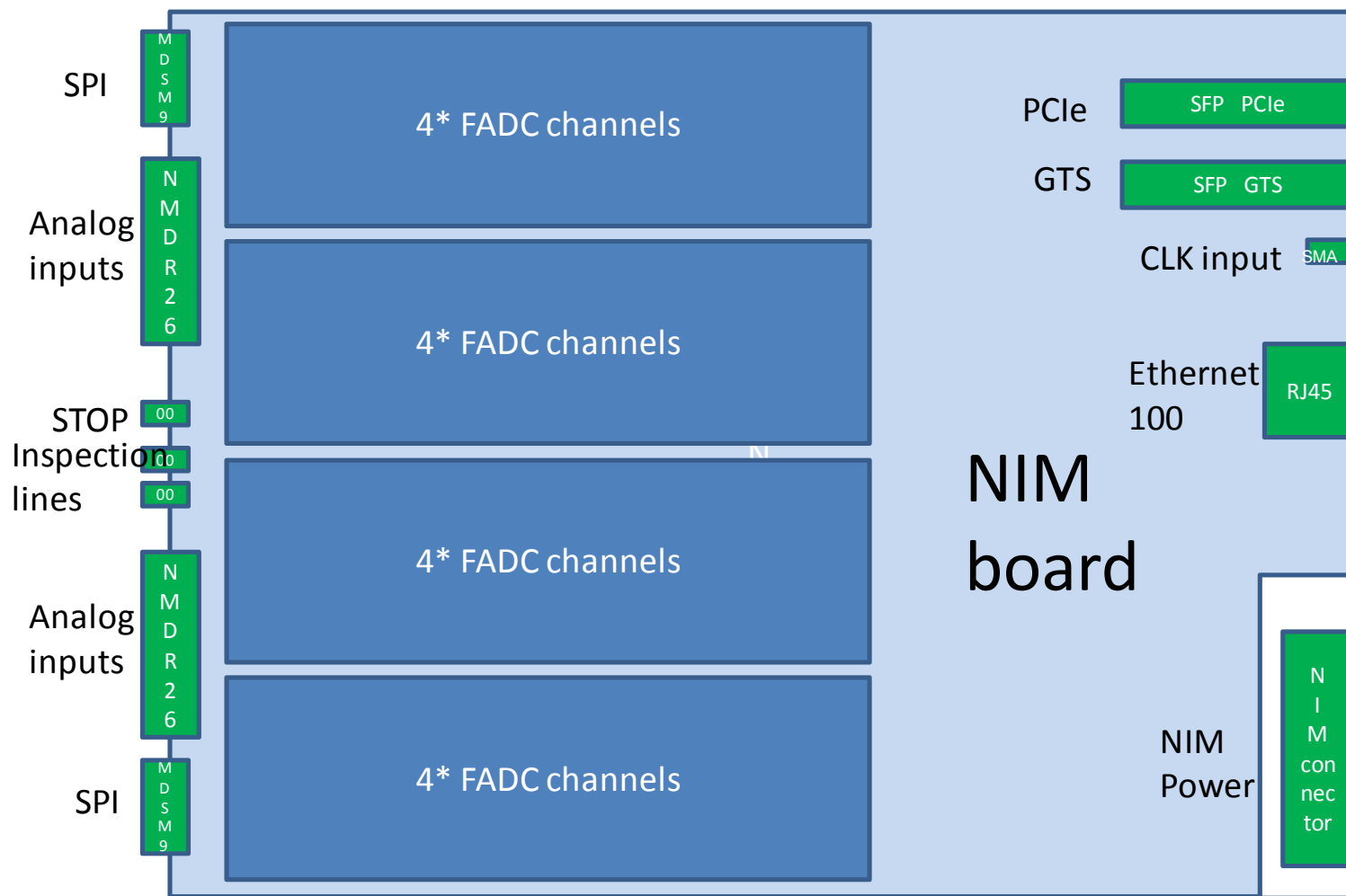
NUMEXO2 phase 2: NIM module layout

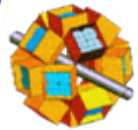




Option B: 16 FADC channels

NUMEXO2 phase 2: 16 channels NIM module layout



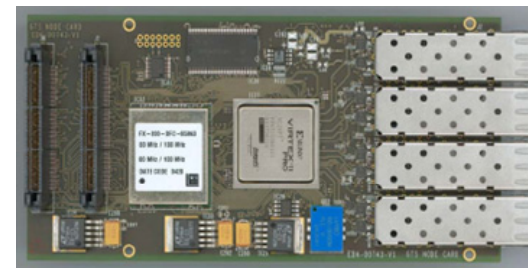
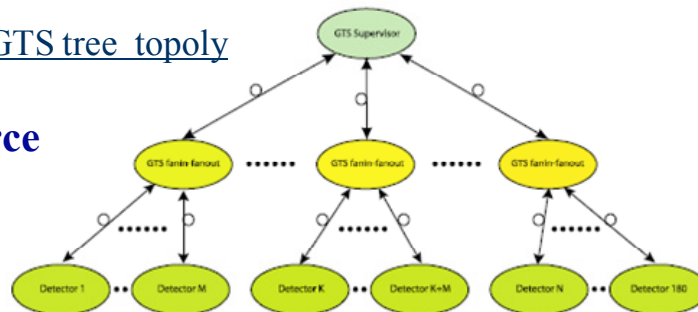


GTS implementation

3 main functions

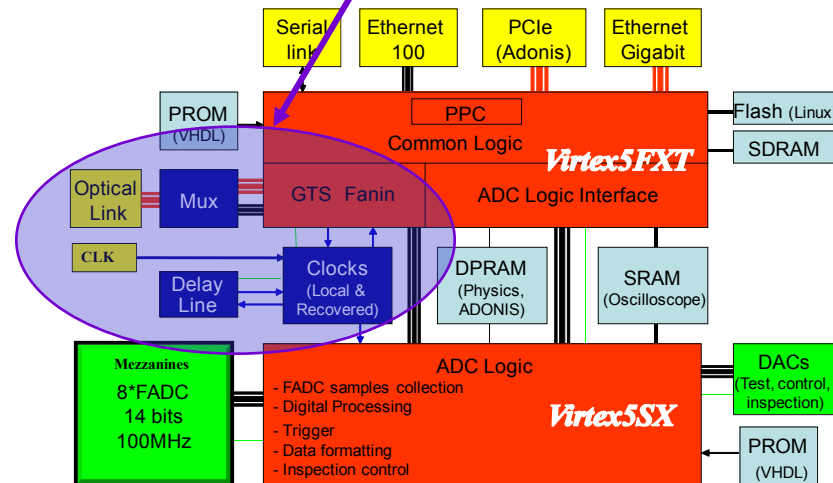
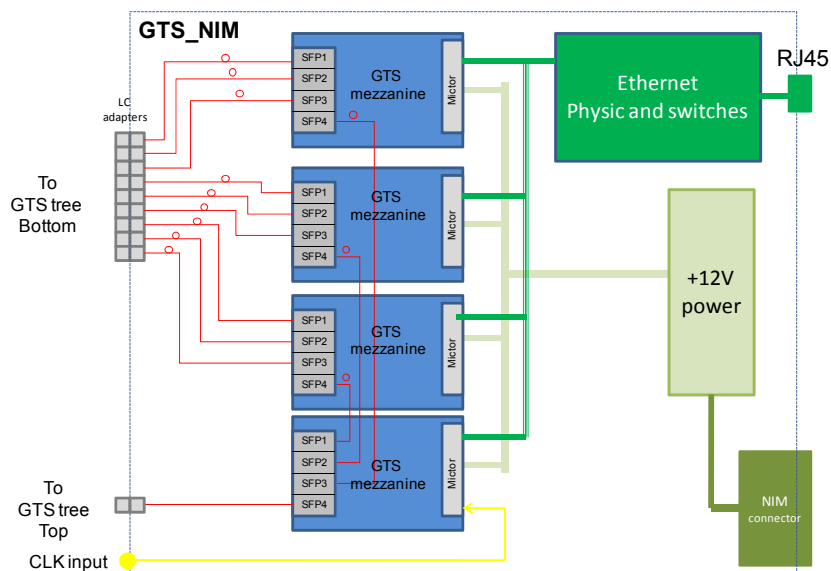
- 200 MHz clock source
- Time stamping
- Trigger

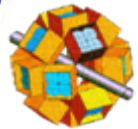
GTS tree topology



GTS V3 mezzanine

EXOGRAM2 GTS tree : 4 GTS mezzanines in one NIM module





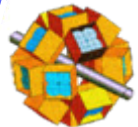
Schedule

	2009		2010				2011				2012				2013			
	Q 3	Q 4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Prototype (phase 1):																		
- Studies	■	■	■															
- Manufacturing		■	■	■	■	■	■											
- Tests			■	■	■	■	■	■										
Prototype (phase 2):																		
- Studies							■	■	■	■								
- Manufacturing								■	■	■	■	■						
- Tests											■	■	■	■				
Mass production:																		
- Test bench														■				
- Manufacturing															■	■	■	
- Tests																■	■	■

Prototype phase 1 : digitizer (NIM) + connection box

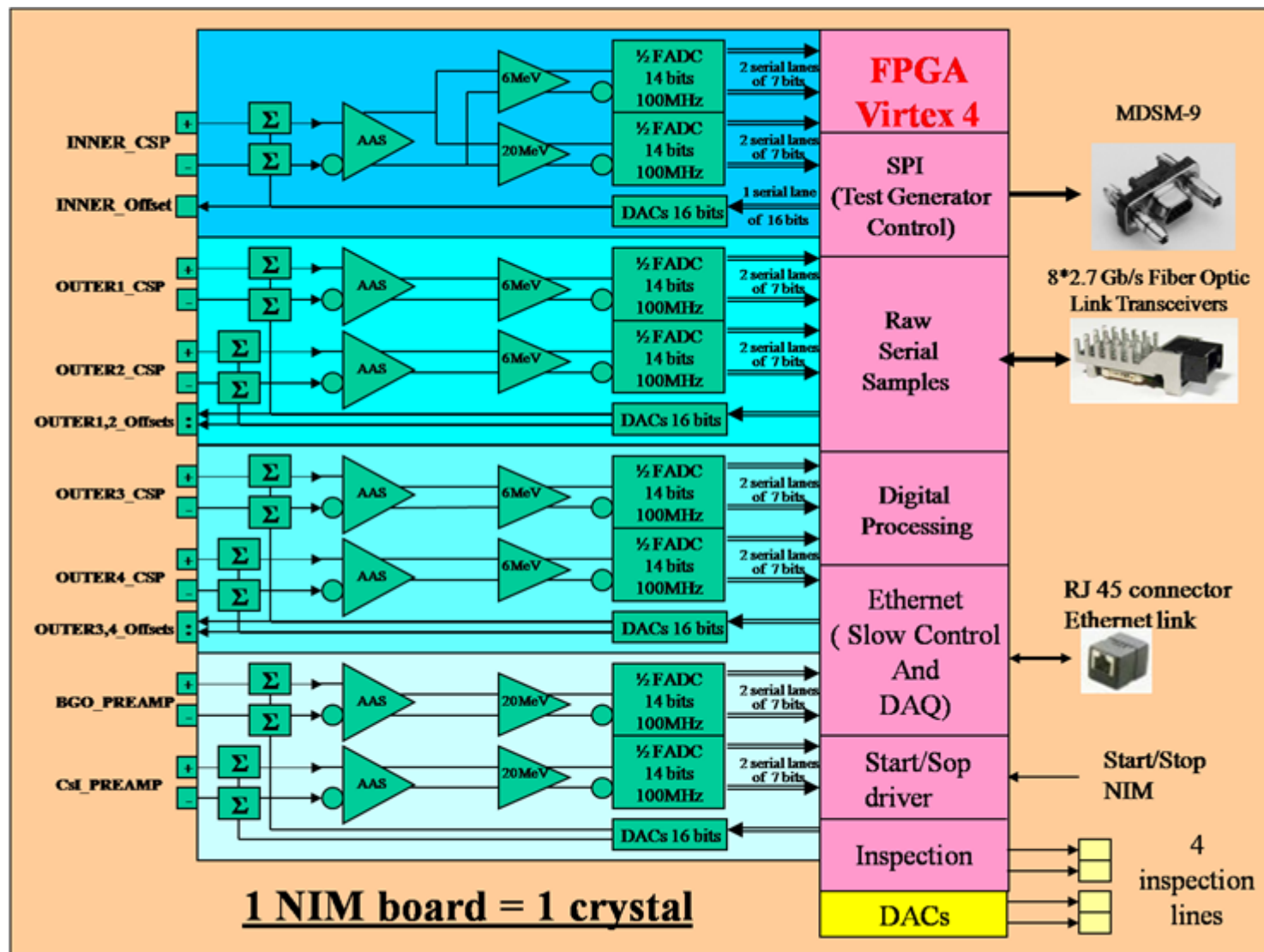
Prototype phase 2 : digitizer + GTS + ADONIS + connection box

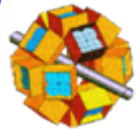
Studies : hardware design, VHDL and C files.



NUMEXO2, the NIM digitizer prototype (phase1)

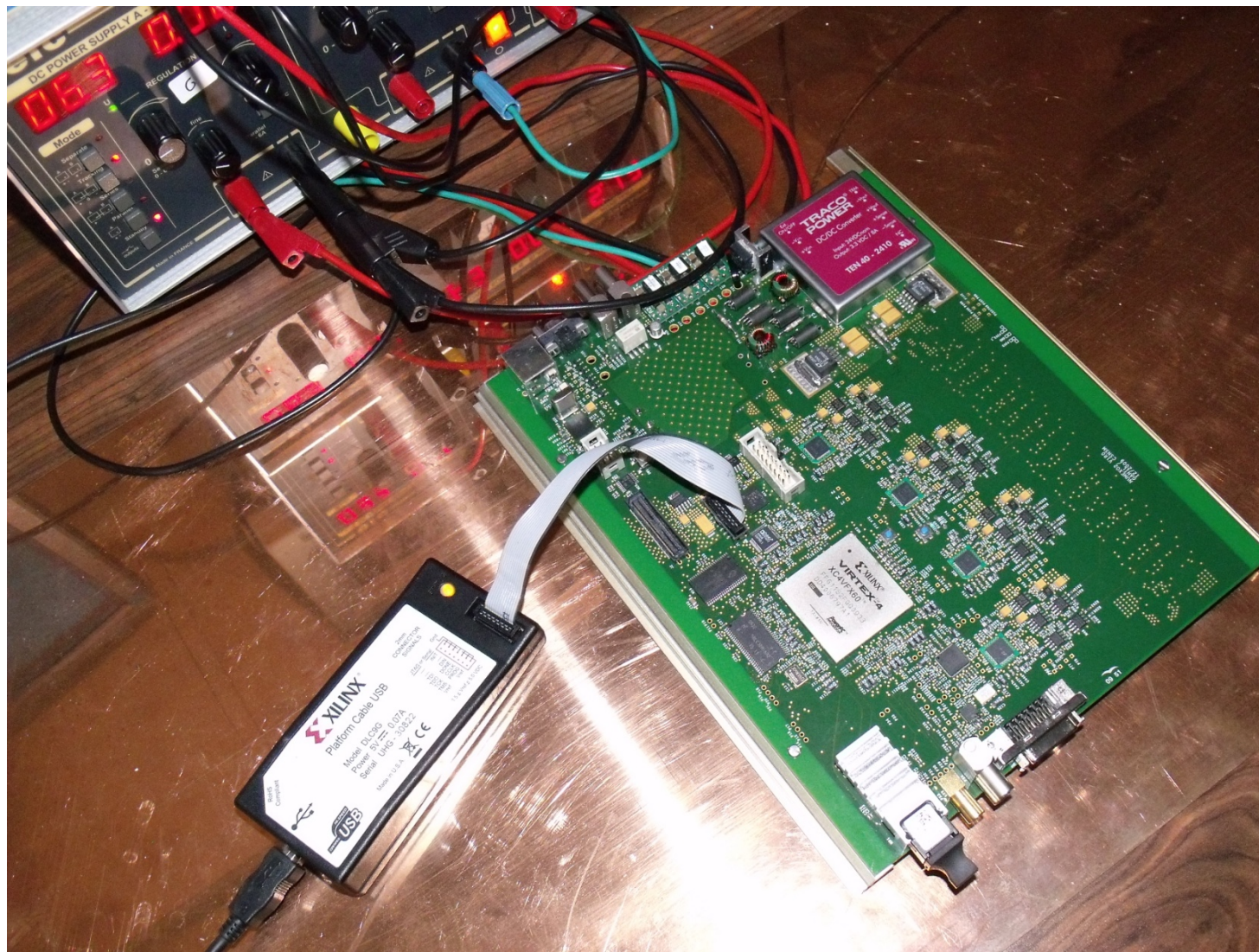
Block diagram

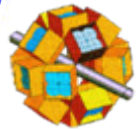




NUMEXO2, the NIM digitizer prototype (phase1)

Picture of the NIM prototype





Current status (NUMEXO2 digitizer, phase 1)

-Firmware

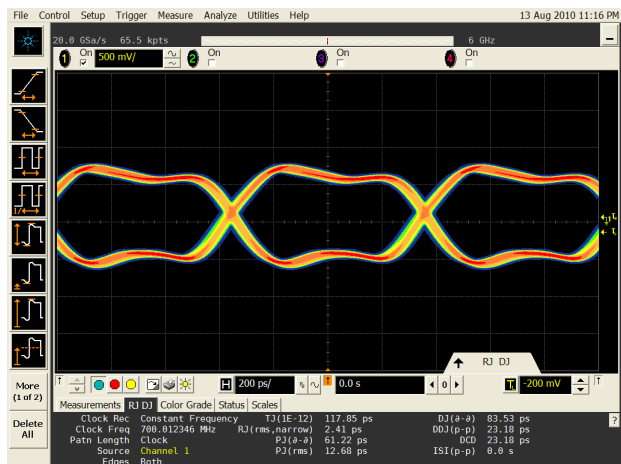
- Deserializer: 8 * (2 serial channels @ 700MB/s)
- Moving Window Deconvolution
- Discrimination
- FIFO interface

-Embedded software

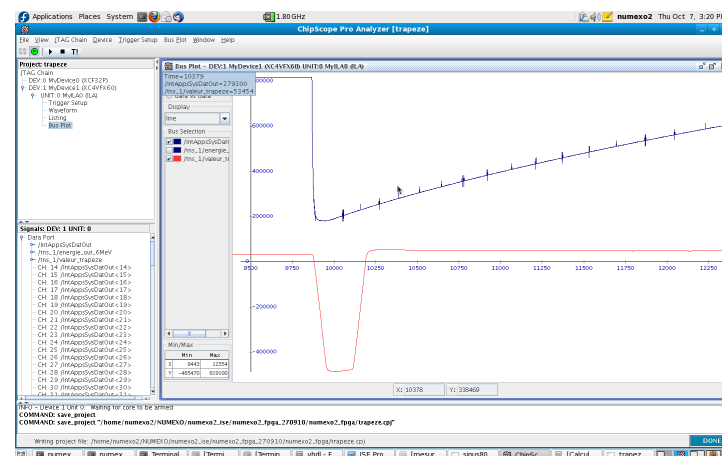
- Linux 2.6.60
- TCP/IP protocol (Ethernet) @ 400Mb/s
- SPI driver and register server

-Software

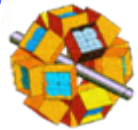
- Characterization tools: traces, FFT, histograms, INL, DNL
- Generic user interface for slow control
- DAQ readout : FIFO readout process



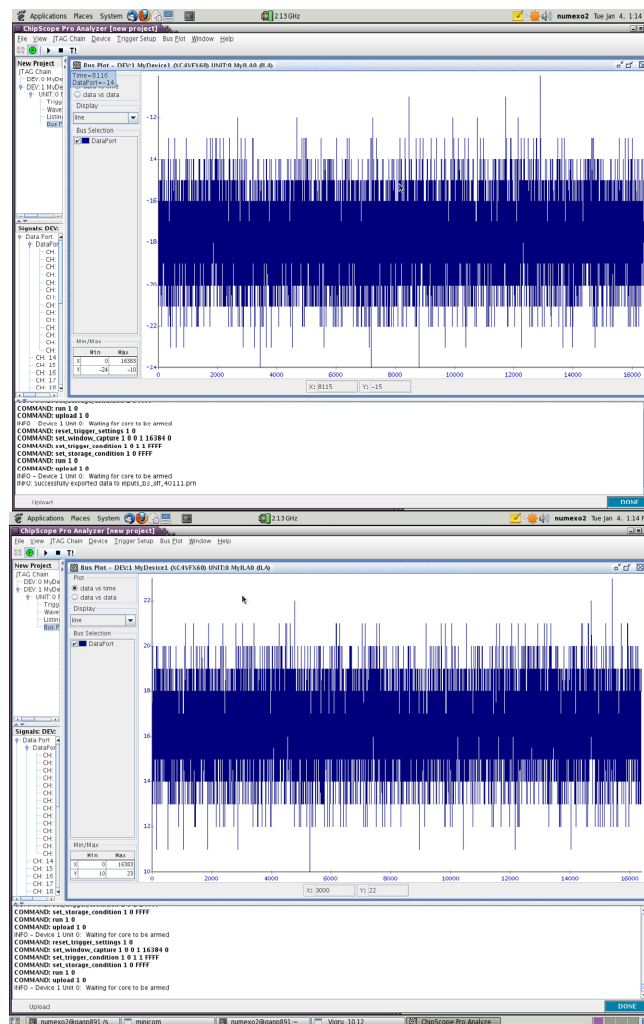
FADC serial output channel eye diagram



Moving Window Deconvolution processing



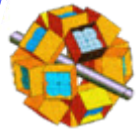
First results with NUMEXO2 phase1 : base line noise



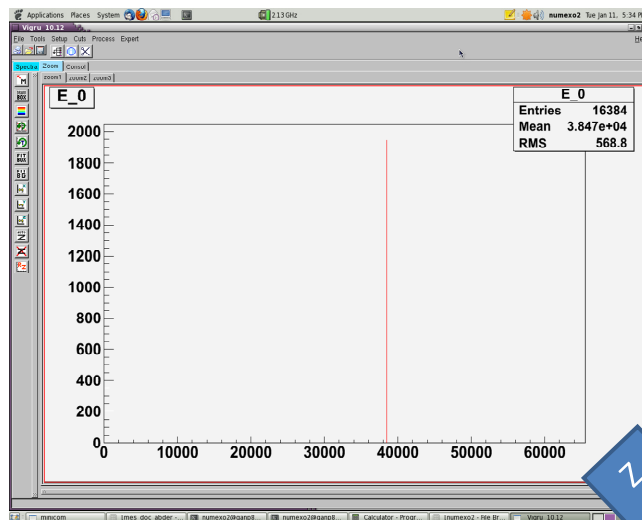
B3 and Numexo2 phase 1
(No inputs)
 $\sigma = 1.66$ (1.43 KeV)

Numexo2 phase 1 (alone)
(No inputs)
 $\sigma = 1.51$ (1.30 KeV)

A.Boujrad & C. Houarner

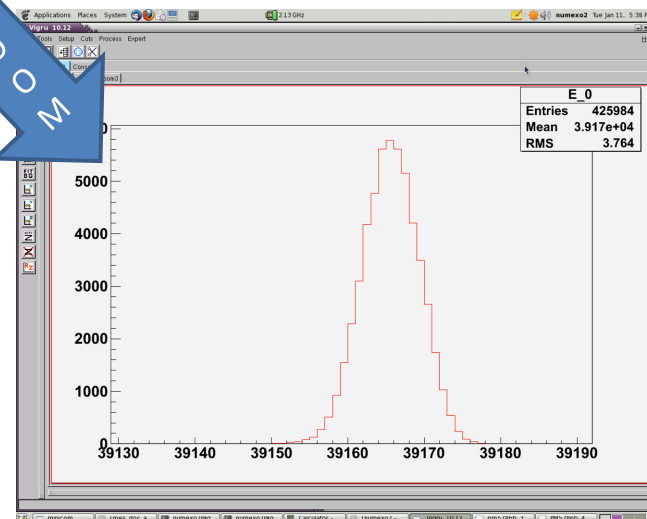


First results with NUMEXO2 phase 1: resolution from pulse generator

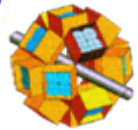


Energy spectrum (16 bits)
(from Pulse Generator)
 $\sigma = 3.76$

ZOOM



A. Boujrad & C. Houarner



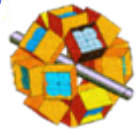
To do (NUMEXO2 digitizer, phase 1)

- Characterisation of the digitizer with a generator
- Characterisation of the digitizer with a Ge clover and a source

Collaboration to NUMEXO2 digitizer, phase 1):

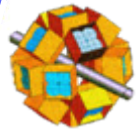
CSNSM Orsay

IPN Orsay



GTS deployment at GANIL

- Collaboration:
 - INFN Padova
 - IFJ PAN Krakow
 - IUAC New Delhi
- Tasks:
 - GTS tree deployment
 - GTS leaf implementation



Current status: GTS tree deployment at GANIL:



GTS ROOT

GTS LEAF

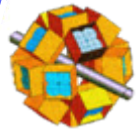
GTS LEAF

A) Training at Padova:

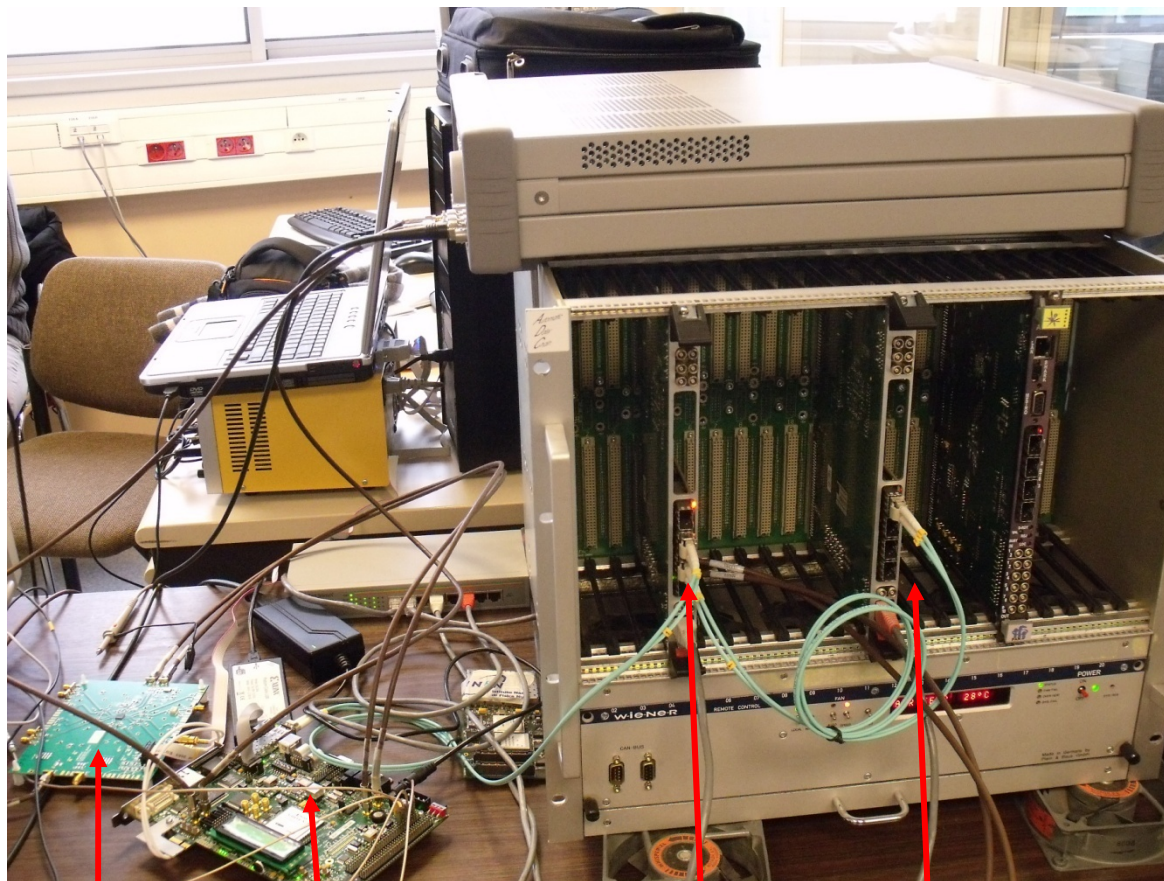
- GTS basics: functional blocks, tree setup, alignment
- Time stamp transmission: encoder/decoder, coarse delay implementation
- Trigger processing : packet transmission, trigger accept packets

B) GTS Control System development:

- GUI : tree population, alignment, test
- UDP server/client



Current status: GTS leaf implementation



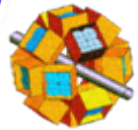
LMK 3001

ML507

GTS leaf like

GTS root

GTS leaf



Current status: GTS leaf implementation

EXO GAM2

Applications Places System

ISE Project Navigator (M.63c) /home/tripon/Padova/GTS_MLS07/gts_clk_rec/gts.cl

File Edit View Project Source Process Tools Window Layout Help

Design Overview

View: Implementation Simulation

Hierarchy

- gts_clk_rec
 - xc5vfx70t-1ff1136
 - Automatic 'includes'
 - defines.v
 - gts_leaf (gts_leaf.v)
 - gtx_wrapper - gtx_wrapper (gtx_wr

Design Properties

- Enable Message Filtering
- Optional Design Summary Contents
 - Show Clock Report
 - Show Failing Constraints
 - Show Warnings
 - Show Errors

Processes: gtx_wrapper - gtx_wrapper

Design Utilities

- Create Schematic Symbol
- View HDL Instantiation Template
- Check Syntax

Console

Command Line: -cwd "/home/tripon/Padova/GTS_MLS07/gts_clk_rec" analyzer -intstyle ise
Process "Analyze Design Using ChipScope" launched successfully

Started: "Launching ISE Text Editor to edit gtx_wrapper.v".

ChipScope Pro Analyzer [gts_leaf]

File View JTAG Chain Device VIO Window Help

JTAG Scan Rate: 250 ms

Project: gts_leaf

JTAG Chain

 - DEV:0 MyDevice0 (XC5VFX70T)
 - DEV:1 MyDevice1 (XC5VFX70T)
 - DEV:2 MyDevice2 (XC5VFX70T)
 - DEV:3 MyDevice3 (System_ACE_CF)
 - DEV:4 MyDevice4 (XC5VFX70T)
 - System Monitor Console
 - Static Timing
 - VIO Console

Signals: DEV: 4 UNIT: 0

 - Async Input Port
 - Sync Input Port
 - Async Output Port
 - DRP_ADDR
 - CH: 0 AsyncOut[0]
 - CH: 1 AsyncOut[1]
 - CH: 2 AsyncOut[2]
 - CH: 3 AsyncOut[3]
 - CH: 4 AsyncOut[4]
 - CH: 5 AsyncOut[5]
 - CH: 6 AsyncOut[6]
 - DRP_DIN
 - CH: 7 AsyncOut[7]
 - CH: 24 AsyncOut[24]
 - CH: 25 AsyncOut[25]
 - CH: 26 DRP_EN
 - CH: 27 AsyncOut[27]
 - CH: 28 AsyncOut[28]
 - CH: 29 DRP_WE
 - CH: 30 AsyncOut[30]
 - CH: 31 AsyncOut[31]
 - Sync Output Port
 - CoarseDelay
 - userTxData
 - CH: 24 ALIGN_MODE
 - CH: 25 GT_RESET
 - CH: 26 TX_CHAR_IS_K
 - CH: 27 TX_RESET
 - CH: 28 RX_RESET
 - CH: 29 PLL_RESET
 - CH: 30 CDR_RESET
 - CH: 31 BUF_RESET
 - CH: 32 SyncOut[32]

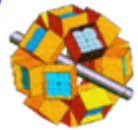
VIO Console - DEV:4 MyDevice4 (XC5VFX70T) UNIT:0 MyVIO0 (VIO)

Bus/Signal	Value
CoarseDelay	00
LOOP_TX_AS_RX	0
ALIGN_MODE	1
GT_RESET	0
TX_CHAR_IS_K	0
TX_RESET	0
RX_RESET	0
PLL_RESET	0
CDR_RESET	0
BUF_RESET	0
rxData	000A
txData	BC88
hammingError	0
gtsStreamError	0
GTX_STATUS	026
DRP_EN	0
DRP_DOUT	A0D9
DRP_ADDR	04
DRP_DIN	A0D9
DRP_WE	0
REC_CLK_SE	1
userTxData	000A

INFO: Successfully opened Xilinx Platform USB Cable
INFO: Cable: Platform Cable USB, Port: USB2.1, Speed: 3 MHz
INFO: DEV:4 MyDevice4 (XC5VFX70T) is not configured
COMMAND: configure 4 "/home/tripon/Padova/GTS_MLS07/gts_clk_rec/gts_leaf.bit" 0
INFO: Found 1 Core Unit in the JTAG device Chain.

Reading file: /home/tripon/Padova/GTS_MLS07/gts_clk_rec/gts_leaf.bit

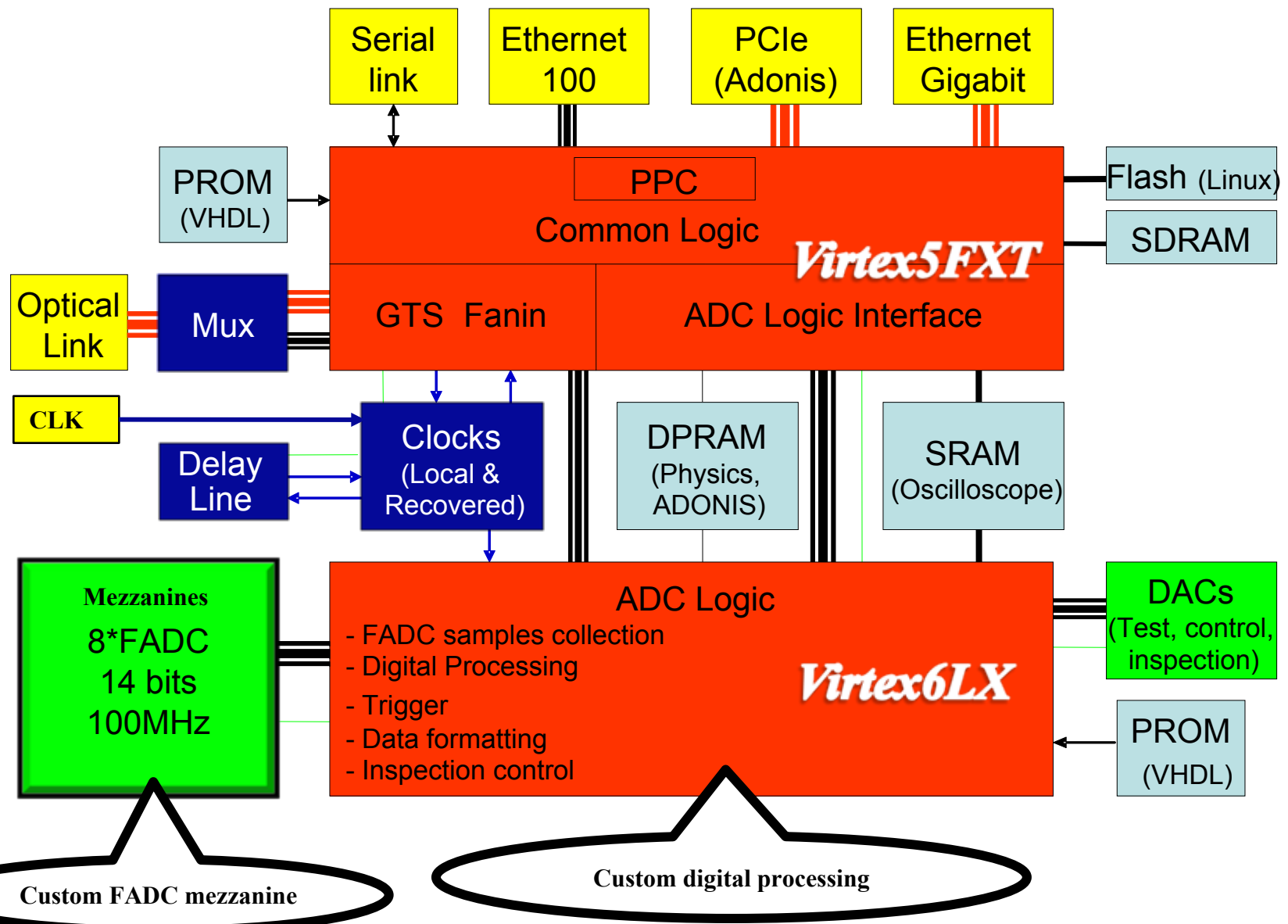
- GTS leaf ISE project on Viretx 5
- DRP registers are controlled by firmware



Current status: GTS leaf implementation



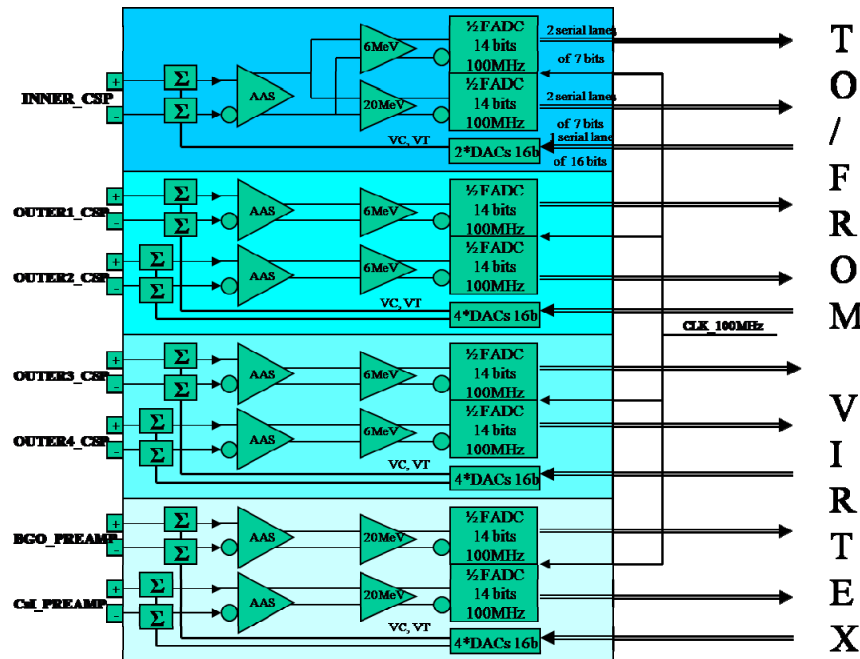
GTS recovered clock is locked :
100MHz clocks of the GTS root and leaves are synchronous

NUMEXO2 for NEDA and PARIS?

NUMEXO2 for NEDA and PARIS?

NUMEXO2: 2*4 channels FADC mezzanines block diagram

FADC: ADS6244, 14 bits, 100MHz, 2 binary samples serial lines @700Mb/s



Differential inputs

- Binary samples serial lines
- Clock line

⇒ NEDA, PARIS:

FADC mezzanines must be redesigned according to frequency bandwidth of inputs

- Sample frequency of FADC?
- Clock jitter?
- Number of binary samples serial lines?
- Power?
- MDR26 connector?
- SAMTEC connector?

3M™ Mini D Ribbon (MDR) Cable Assembly

.050" High Speed Digital Data Transmission System - 26 to 26 Pos.

14526-EZ8B-XXX-07C



- Solution for Digital Displays, Datacom and Telecom applications
- Supports LVDS FPD Link™, FlatLink™, ChannelLink™, PanelLink™/TMDS™ electrical interfaces
- Each differential twin-ax pair has a foil shield and drain
- Entire cable bundle is shielded with foil and braid for additional signal protection
- Rugged MDR ribbon type contact
- Quick release latches
- RoHS* compliant

Electrical

Voltage Rating: 30 V

Current Rating: 1 A

Insulation Resistance: $> 1 \times 10^8 \Omega$ at @100 Vdc

Withstanding Voltage: 350 Vrms for 1 minute

Individually Shielded Twisted Pairs

Characteristic Impedance: $100 \pm 10 \Omega$

Conductor Size: 28 AWG Stranded

Propagation Velocity: 1.25 ns/ft [4.1 ns/m]

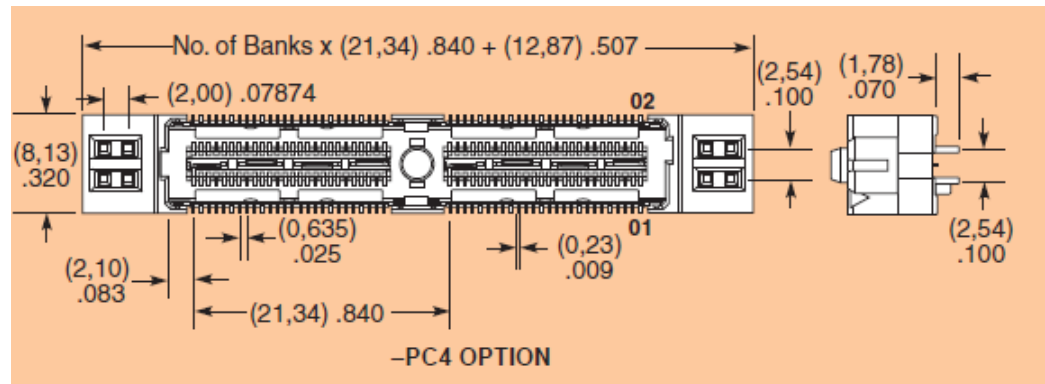
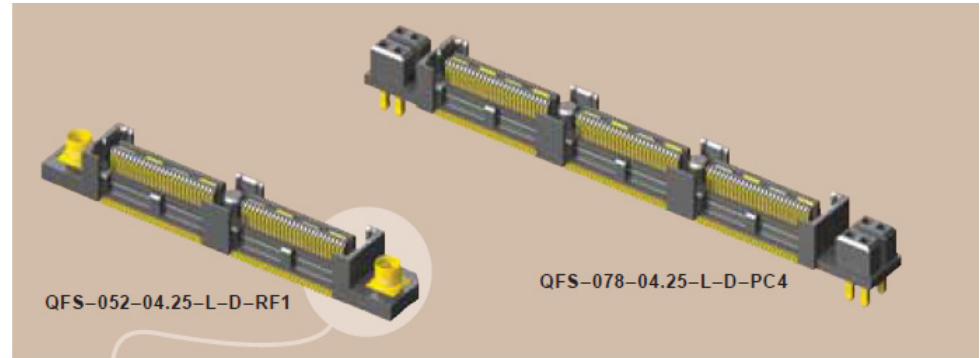
TS-0757-17
Sheet 1 of 4

NEDA, PARIS:
MDR26 Cable
and
connector
must be tested

NUMEXO2 for NEDA and PARIS?

Carrier-mezzanines connector: QFS-026-06-75-X-D-PC4

F-210-1

samtec**(0,635mm) .025"****QFS-PC, QFS-RF SERIES**

10mm Stack Height	Rated @ -3dB Insertion Loss
Single-Ended Signaling	9 GHz / 18 Gbps
Differential Pair Signaling	7.5 GHz / 15 Gbps

NEDA, PARIS: Does pins diagram fit?

FADC highlights

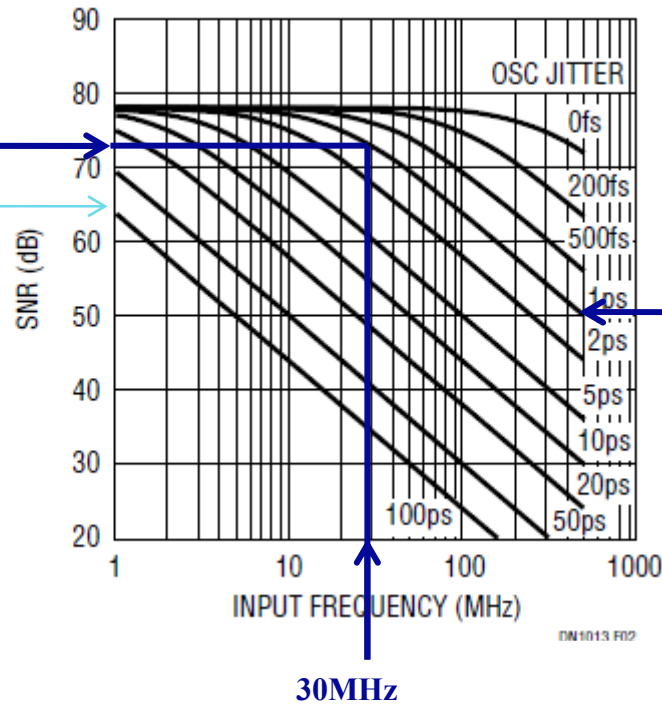
TI FADC	ADS6244	ADS62P49	ADS5463
Résolution (bits)	14	14	12
Sample rate (MSPS)	105	250	500
Input channels	2	2	1
Interface	LVDS serial // (2 LVDS lines)	LVDS serial // (7 LVDS lines)	LVDS // (12 LVDS lines)
Analog BW (MHz)	500	700	2300
SNR (dB)	73	73	65
ENOB (bits)	11.7	11.3	10.4
Power (W)	0.9	1.2	2.3

Clock jitter specifications

- FADC clock

14 bits

12 bits



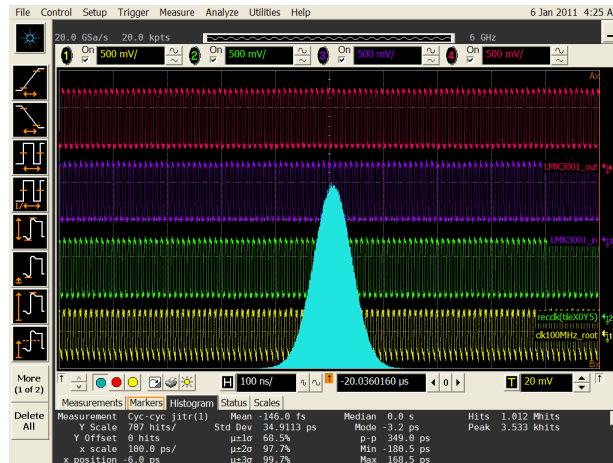
1 ps jitter

Jitter clock: degradation of SNR

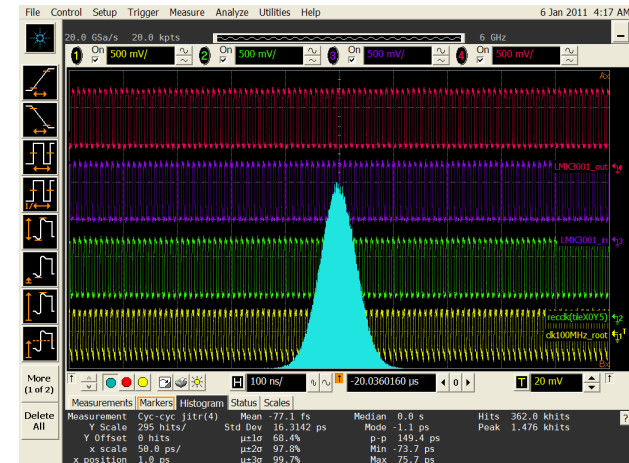
- High resolution timing

NUMEXO2 for NEDA and PARIS?

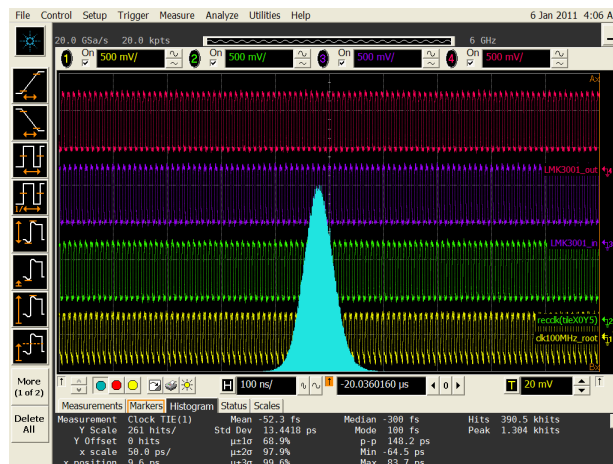
100MHz GTS clock jitter



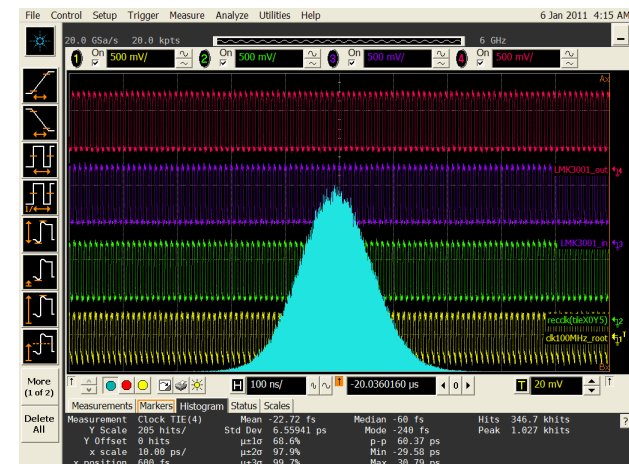
GTS ROOT: Std Dev (cycle to cycle) = 35ps



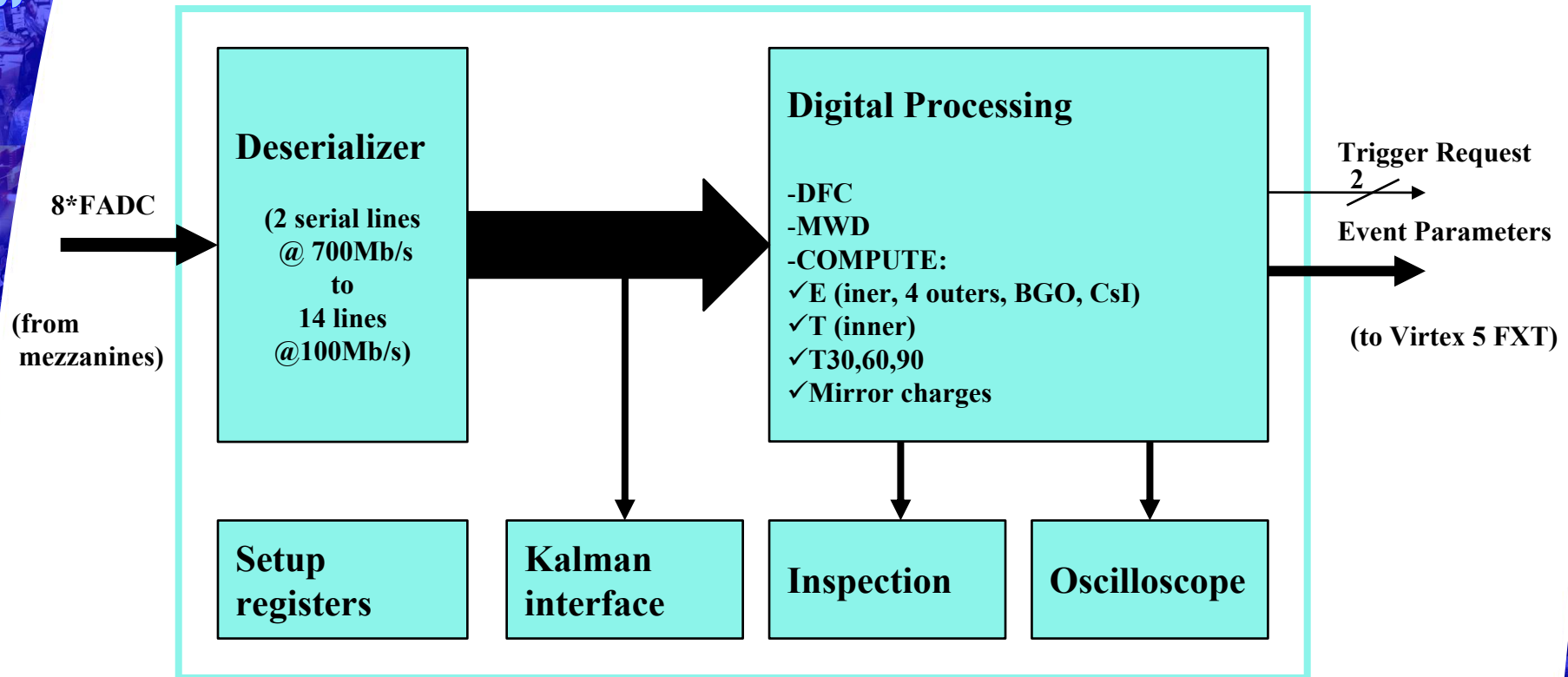
GTS leaf_like : Std Dev (leaf to leaf) = 16 ps



GTS ROOT: Std Dev (TIE) = 13ps



GTS leaf_like : Std Dev (TIE) = 6 ps

Block diagram of EXOGAM2 signal processing

⇒ NEDA, PARIS:

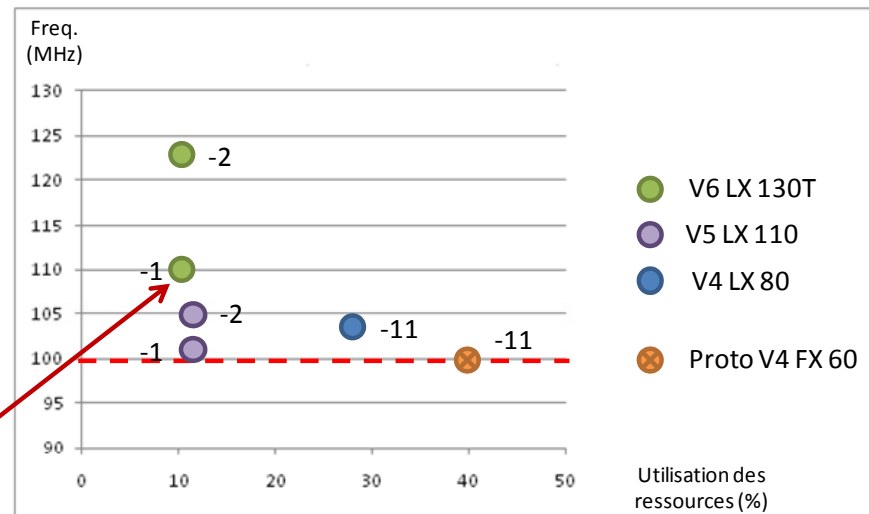
- Deserializer and Digital Processing IPs must be written
- Kalman interface suppressed
- Number of Trigger Request signals > 2
- Setup registers, Inspection and Oscilloscope IPs must be modified

NUMEXO2 for NEDA and PARIS?

FPGA target choice: Virtex 6 LX130T -1

PROJET EXOGAM2/NUMEXO2/FPGA TNS VIRTEX6

Quel composant VIRTEX4, 5, 6...

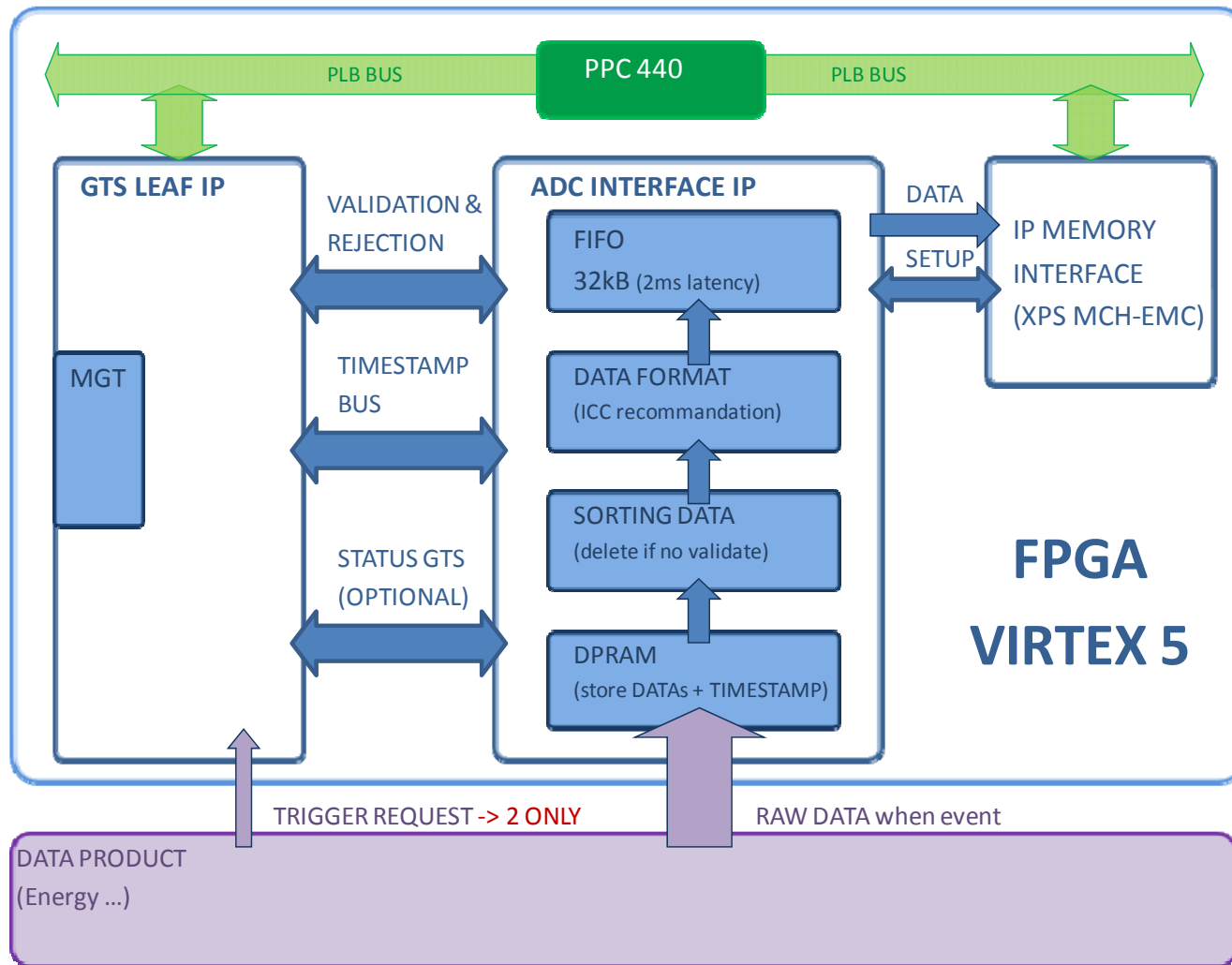


8 voies MWD

Cible choisie : Virtex 6 LX130T -1 1094 \$ - distributeur Avnet

Marge de fréquence de 10% -> 40% désormais avec une optimisation plus poussée
Faible taux de remplissage

Is the Virtex 6 LX130T -1 powerfull enough for NEDA, PARIS signal processing?

Block diagram of EXOGAM2 GTS and ADC interfaces

- ⇒ NEDA, PARIS :
- DPRAM and FIFO depths?
 - Data format?