EXOGAM2 project

Digital instrumentation of the EXOGAM detector

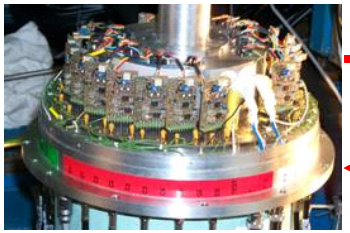
- Overview of the technical project
- Status of the digitizer prototype
- Synergy EXOGAM2 NEDA and PARIS

M. Tripon

General architecture

Preamplifiers

16 clovers
=
64 crystals



7 analog signals per crystal
(ICR < 100kHz per crystal)

One test per crystal

Differential stages
and
test pulse generator

Connexion box

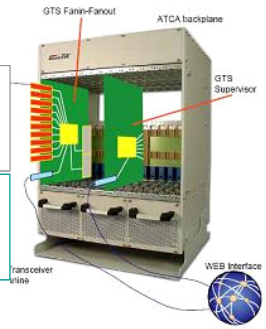
64 crystals
=>
64 boxes

7 differential analog links per NIM board

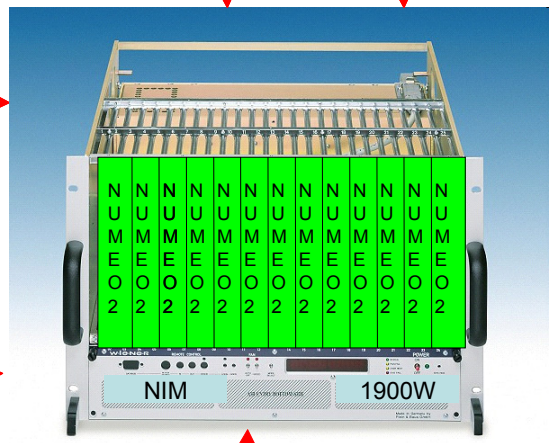
Control link

Global Trigger and Synchronization

1 GTS supervisor
and
34 GTS mezzanines



1 optical link per NIM board



Digitizing, Processing and Dating

1 crystal
Per
NIM board
=>
64 NIM boards

KALMAN processing

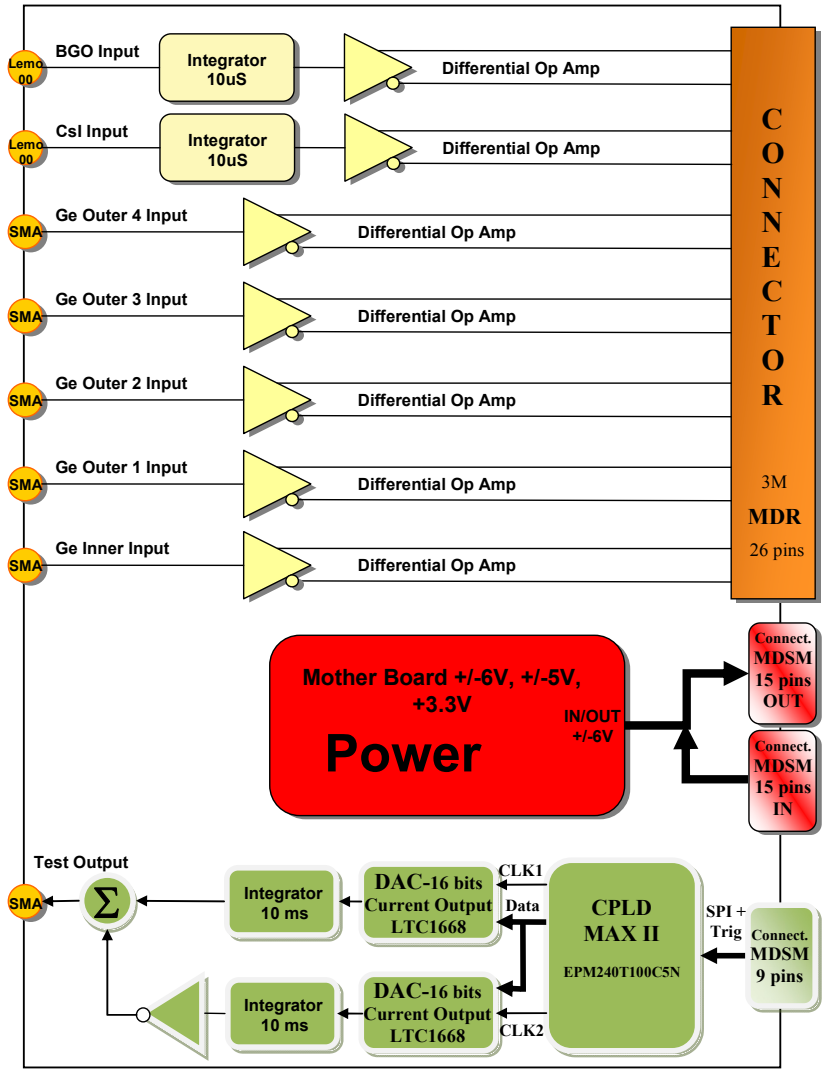
1 optical link per NIM board (< 2 Gb/s)

1 link per NIM board
(6 MB/s per crystal)

Ethernet Switch

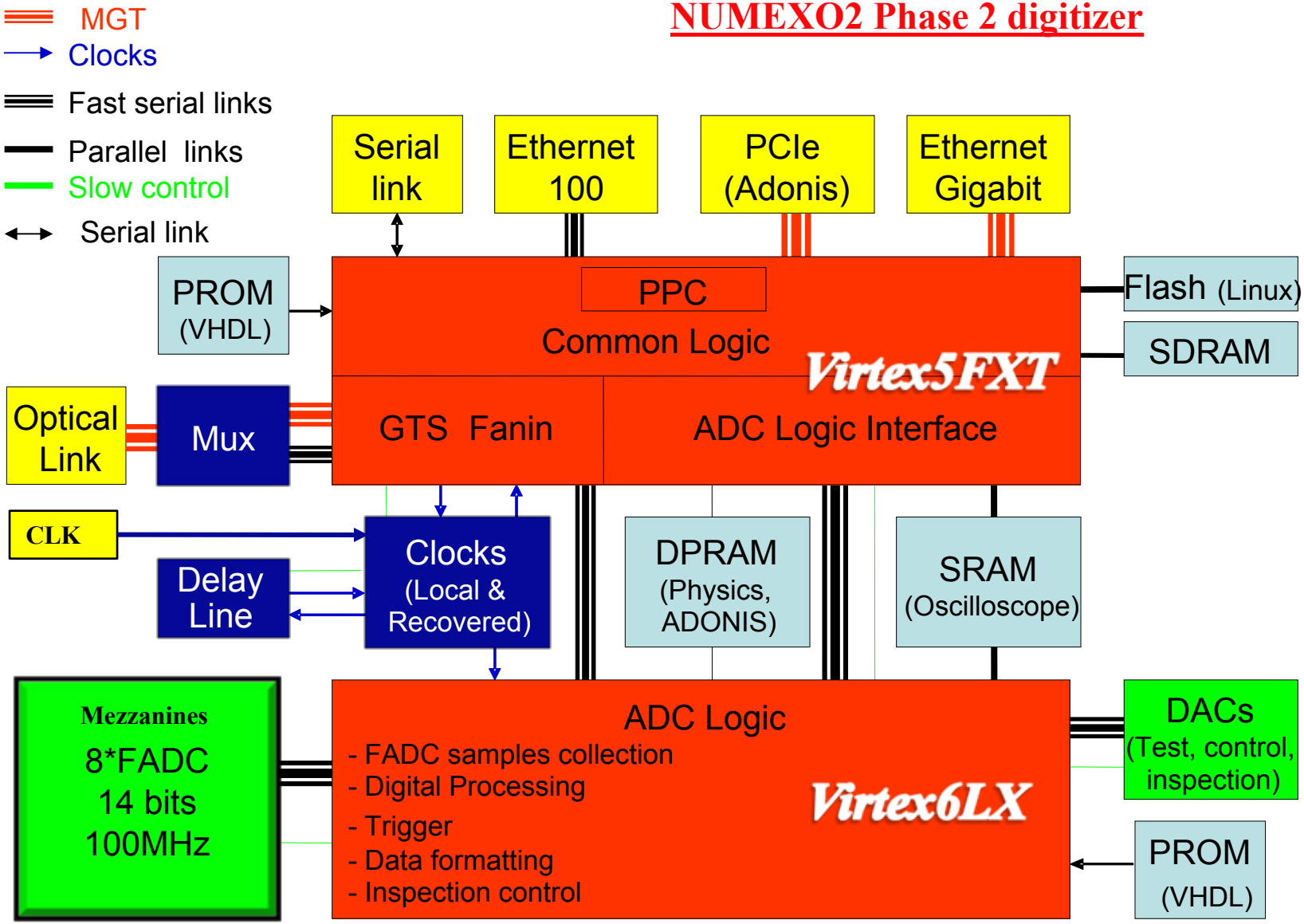
DAQ

Connection box B3



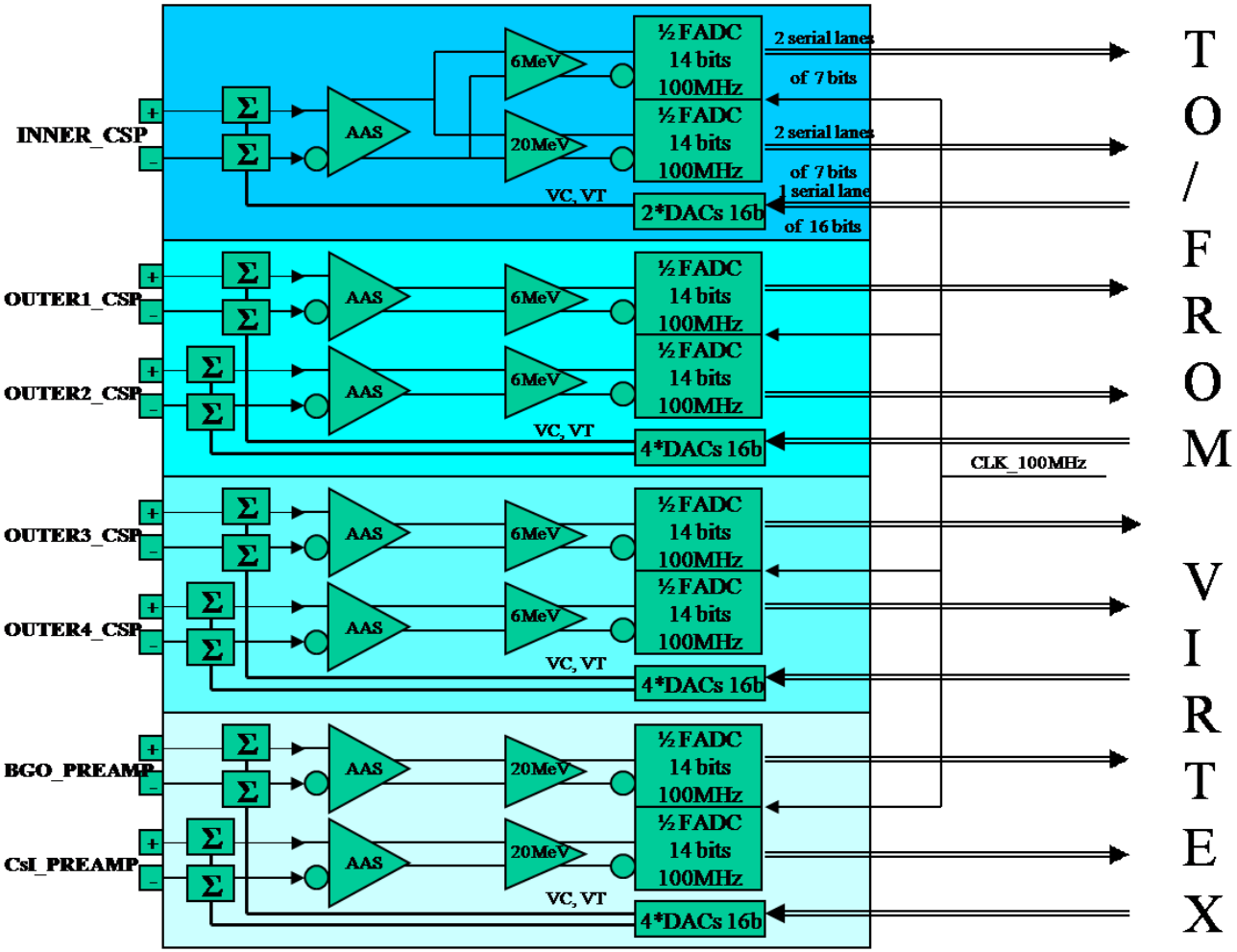
EXOGAM2

NUMEXO2 Phase 2 digitizer



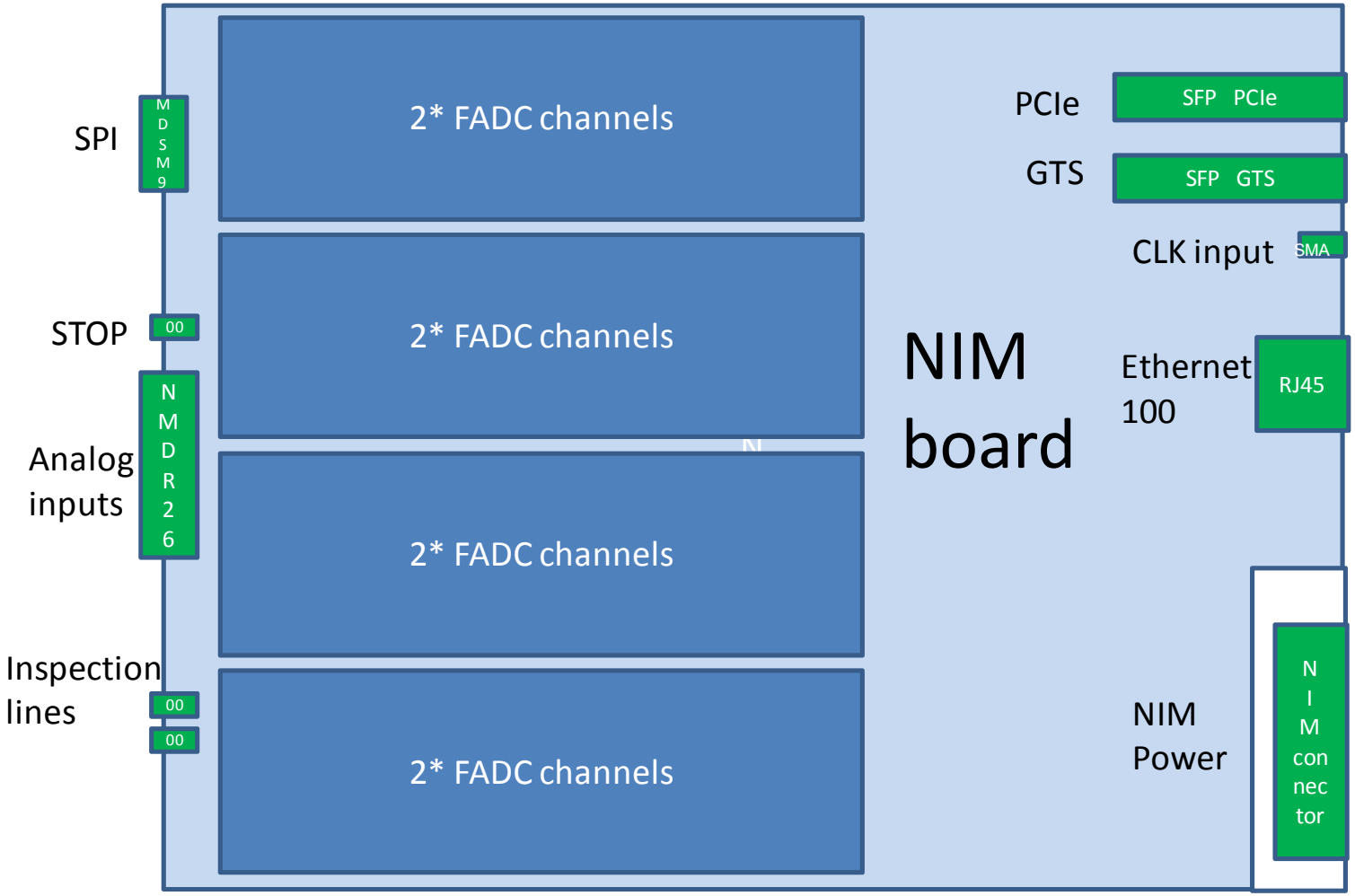
NUMEXO2
Block diagram of 8 FADC channels

One crystal = 7 detector channels



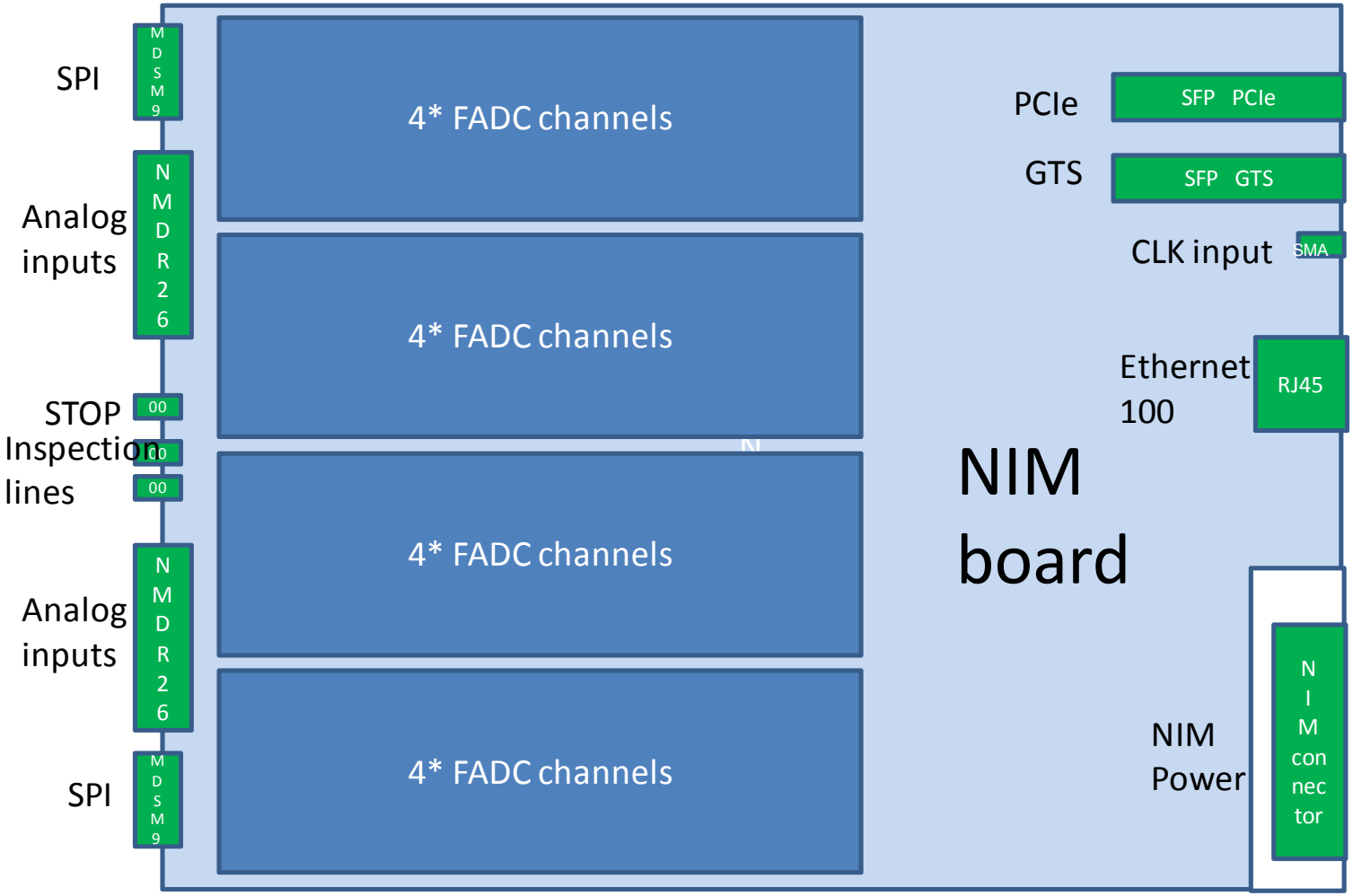
Option A : 8 FADC channels

NUMEXO2 phase 2: NIM module layout



Option B: 16 FADC channels

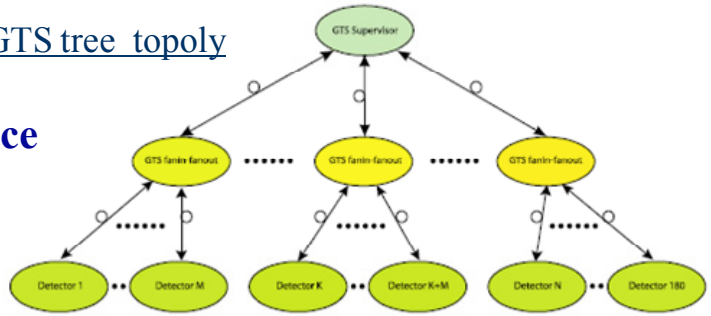
NUMEXO2 phase 2: 16 channels NIM module layout

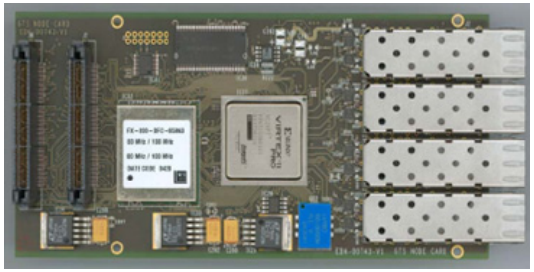


GTS implementation

3 main functions
- 200 MHz clock source
-Time stamping
- Trigger

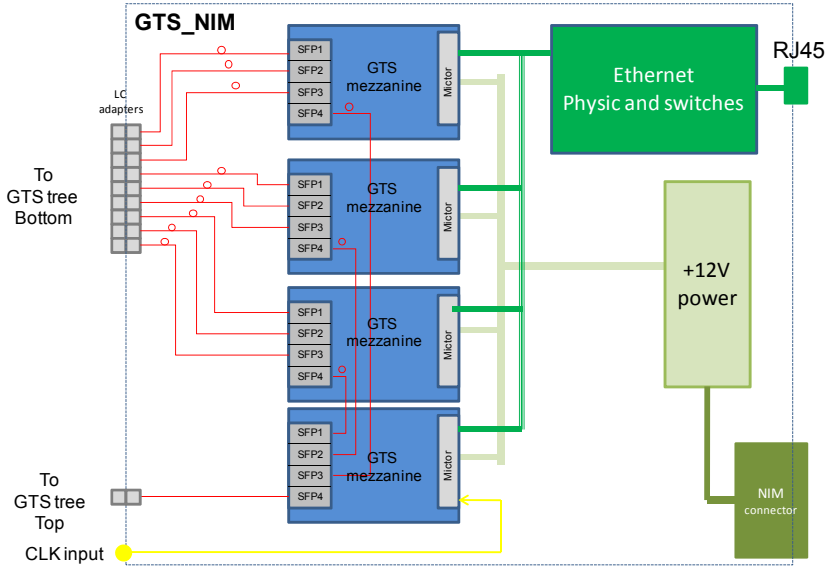
GTS tree topoly

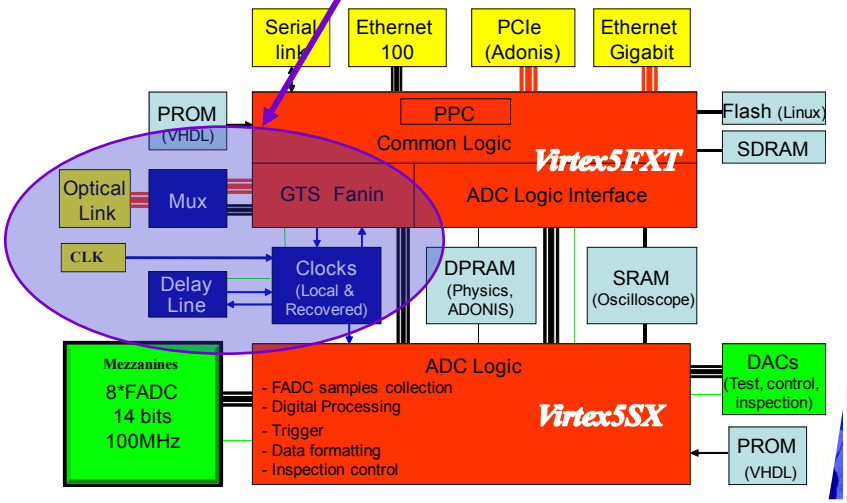




GTS V3 mezzanine

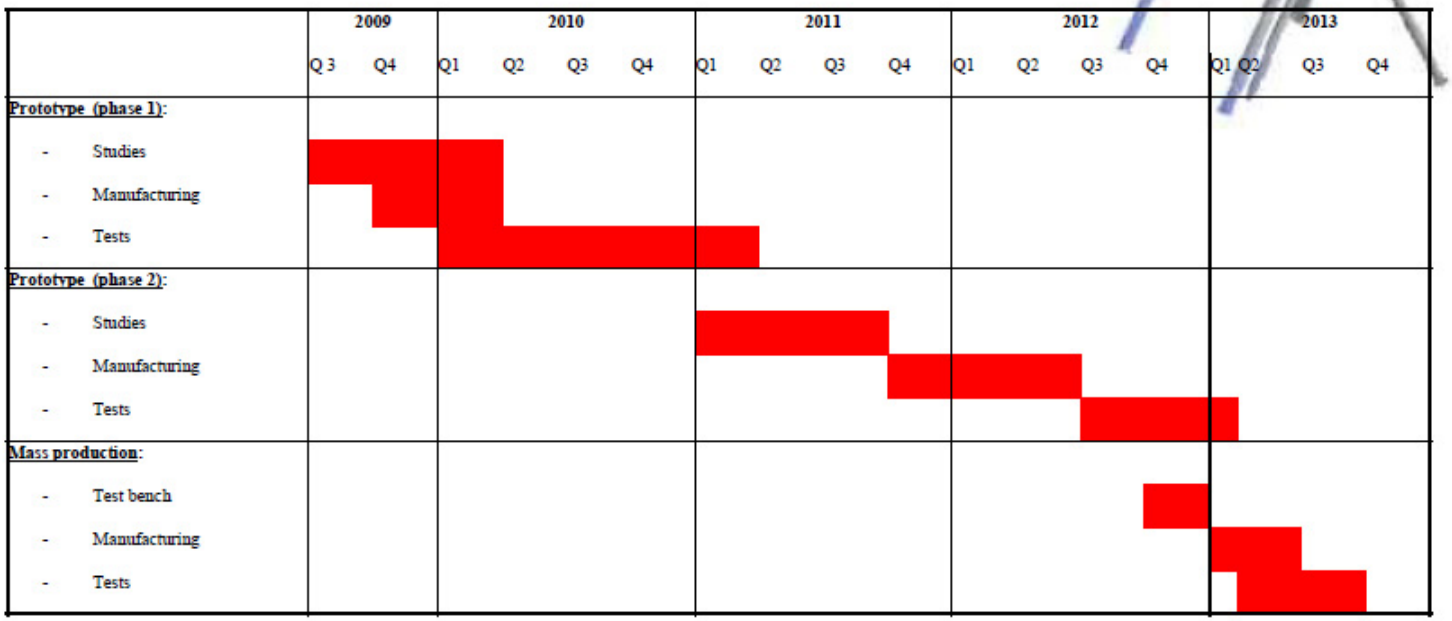
EXOGAM2 GTS tree : 4 GTS mezzanines in one NIM module





EXOGAM2

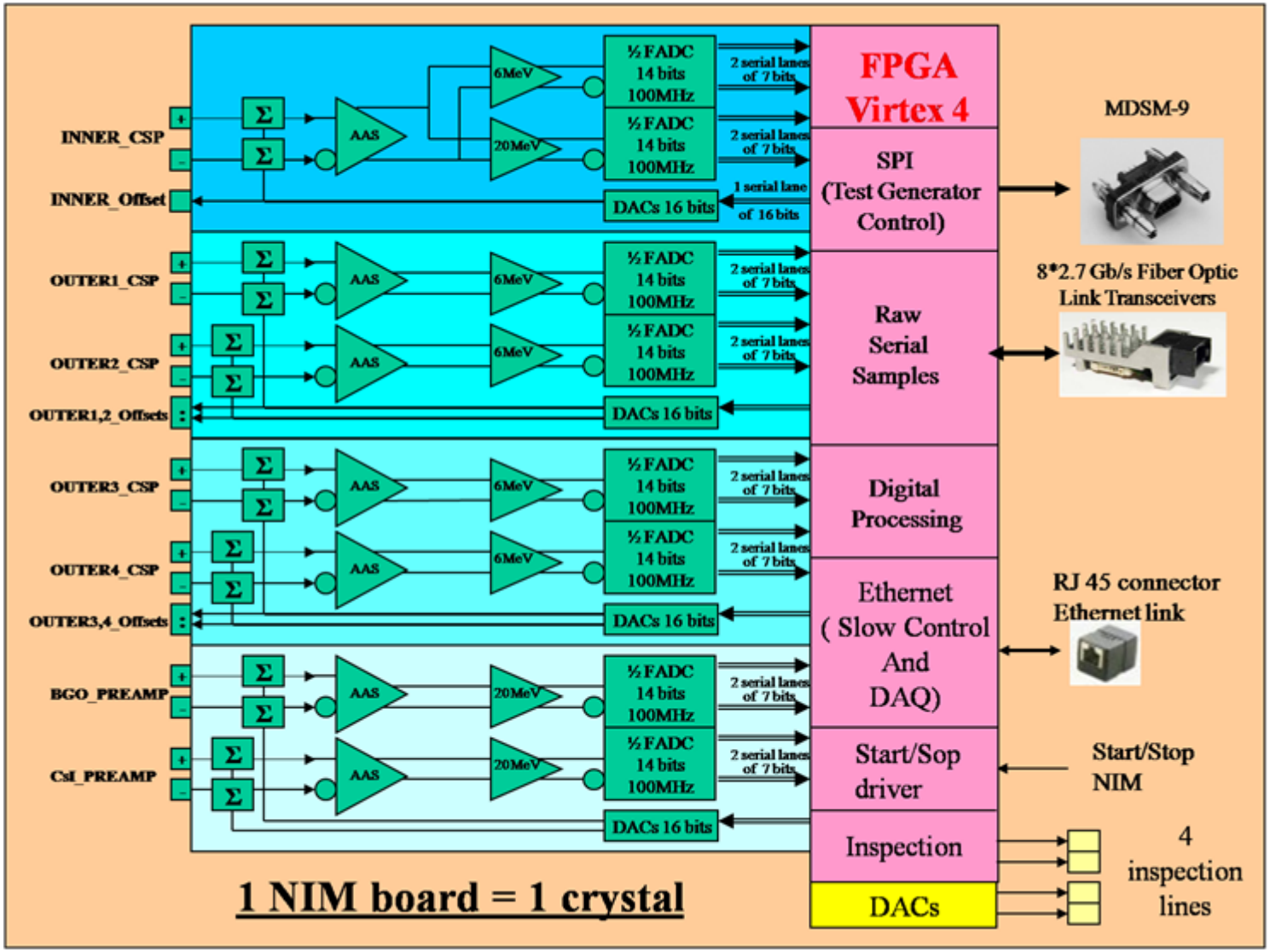
Schedule



Prototype phase 1 : digitizer (NIM) + connection box
Prototype phase 2 : digitizer + GTS + ADONIS + connection box
Studies : hardware design, VHDL and C files.

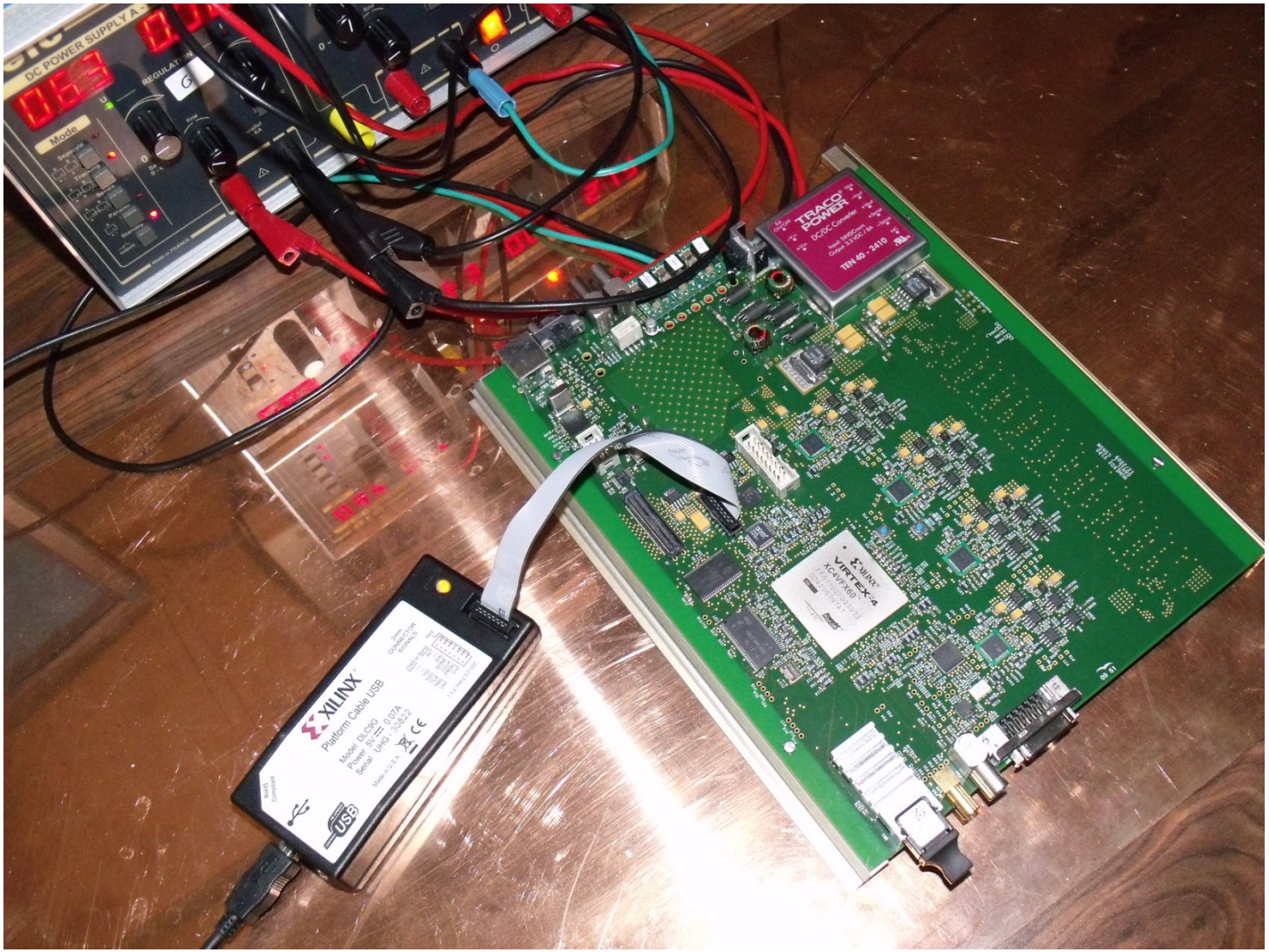
NUMEXO2, the NIM digitizer prototype (phase1)

Block diagram



NUMEXO2, the NIM digitizer prototype (phase1)

Picture of the NIM prototype

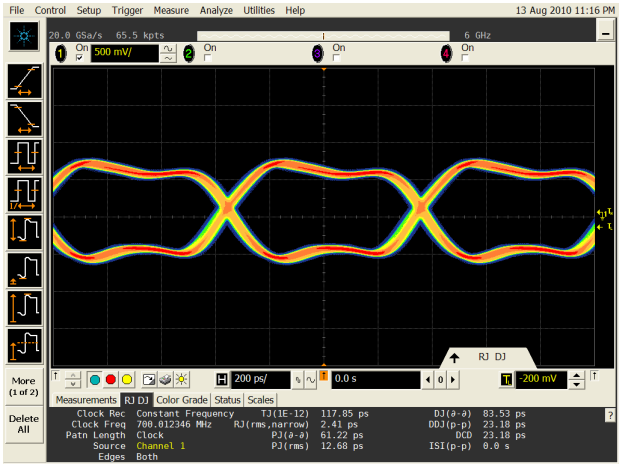


Current status (NUMEXO2 digitizer, phase 1)

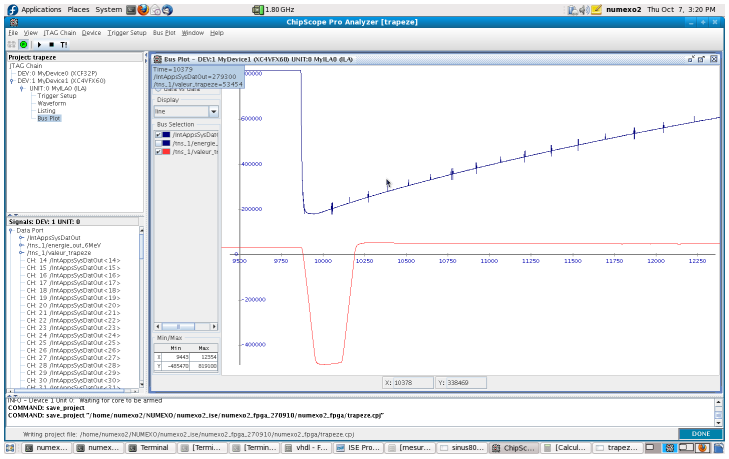
-Firmware
- Deserializer: 8 * (2 serial channels @ 700MB/s)
- Moving Window Deconvolution
- Discrimination
- FIFO interface

-Embedded software
- Linux 2.6.60
- TCP/IP protocol (Ethernet) @ 400Mb/s
- SPI driver and register server

-Software
- Characterization tools: traces, FFT, histograms, INL, DNL
- Generic user interface for slow control
- DAQ readout : FIFO readout process

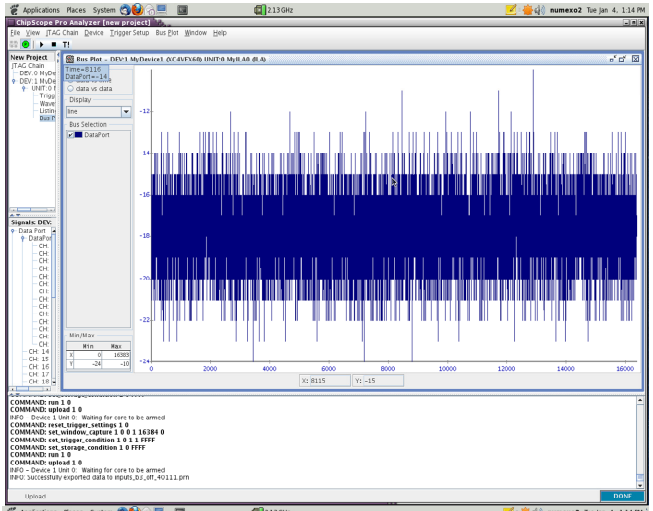


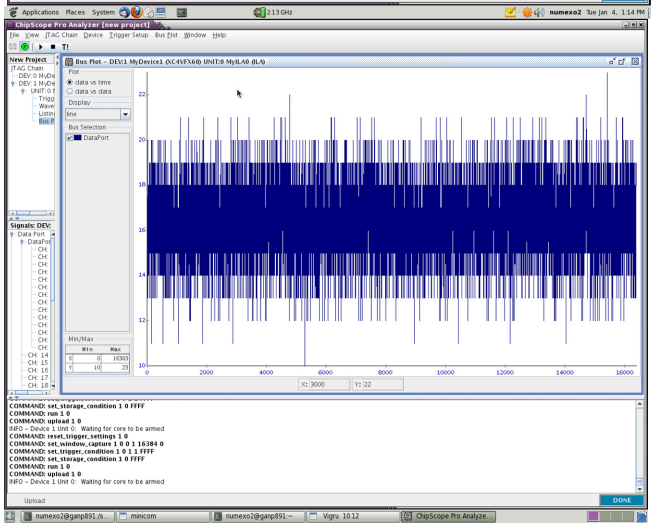
FADC serial output channel eye diagram



Moving Window Deconvolution processing

First results with NUMEXO2 phase1 : base line noise



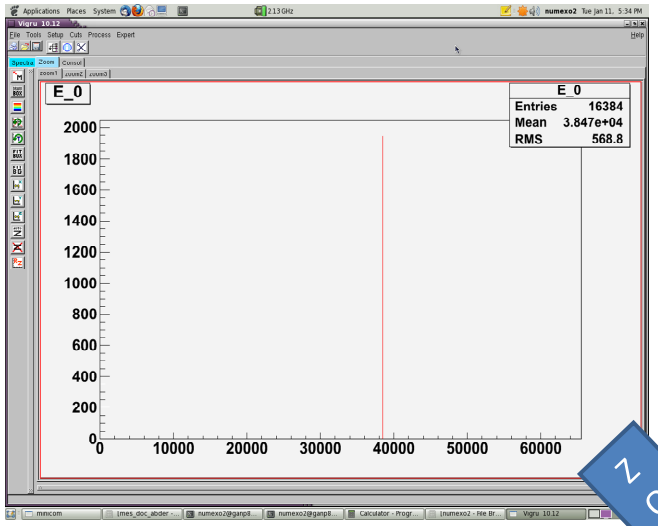


B3 and Numexo2 phase 1
(No inputs)
σ = 1.66 (1.43 KeV)

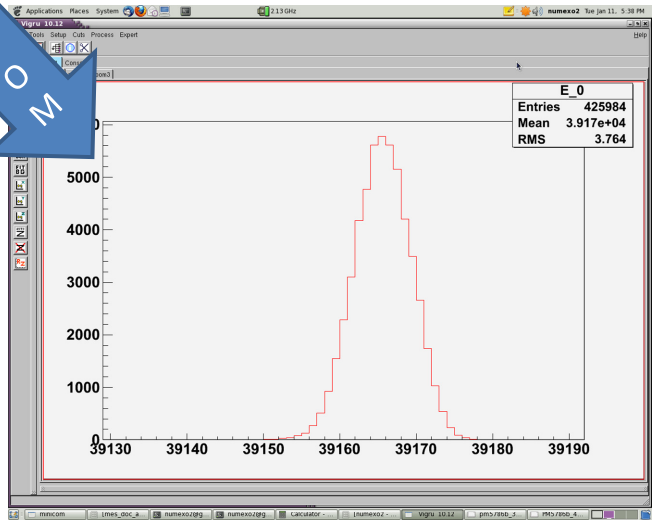
Numexo2 phase 1 (alone)
(No inputs)
σ = 1.51 (1.30 KeV)

A.Boujrad & C. Houarner

First results with NUMEXO2 phase 1: resolution from pulse generator



ZOOM



Energy spectrum (16 bits)
(from Pulse Generator)
$\sigma = 3.76$

A.Boujrad & C. Houarner

To do (NUMEXO2 digitizer, phase 1)

- **Characterisation of the digitizer with a generator**

- **Characterisation of the digitizer with a Ge clover and a source**

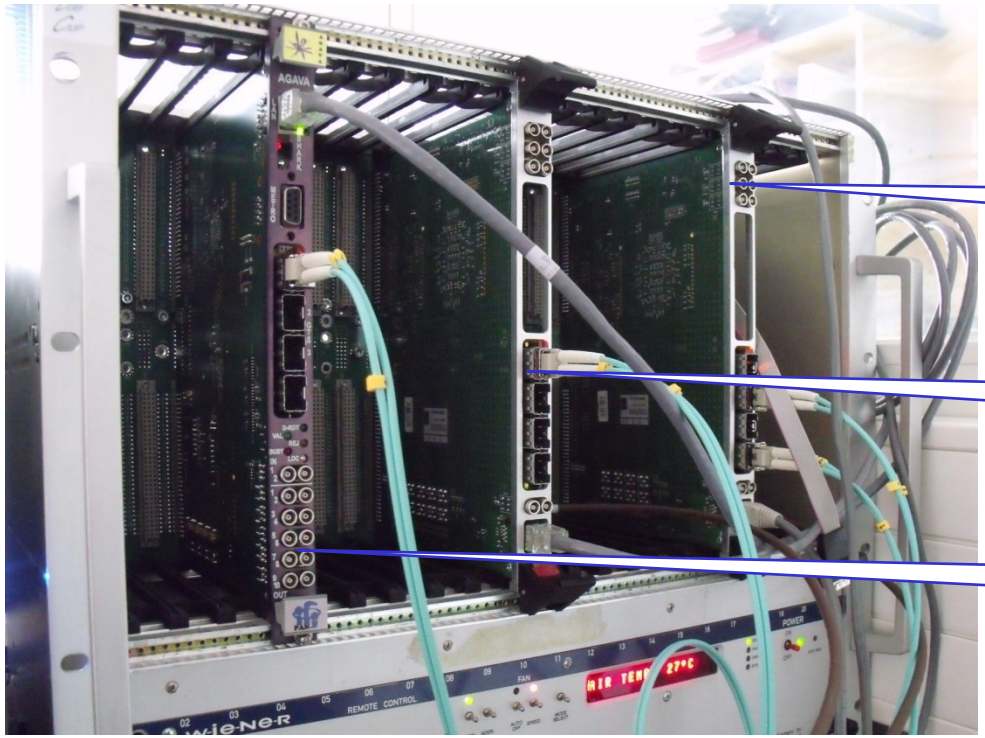
Collaboration to NUMEXO2 digitizer, phase 1):
CSNSM Orsay
IPN Orsay

GTS deployement at GANIL

- **Collaboration:**
  - **INFN Padova**
  - **IFJ PAN Krakow**
  - **IUAC New Delhi**

- **Tasks:**
  - **GTS tree deployment**
  - **GTS leaf implementation**

Current status: GTS tree deployment at GANIL:



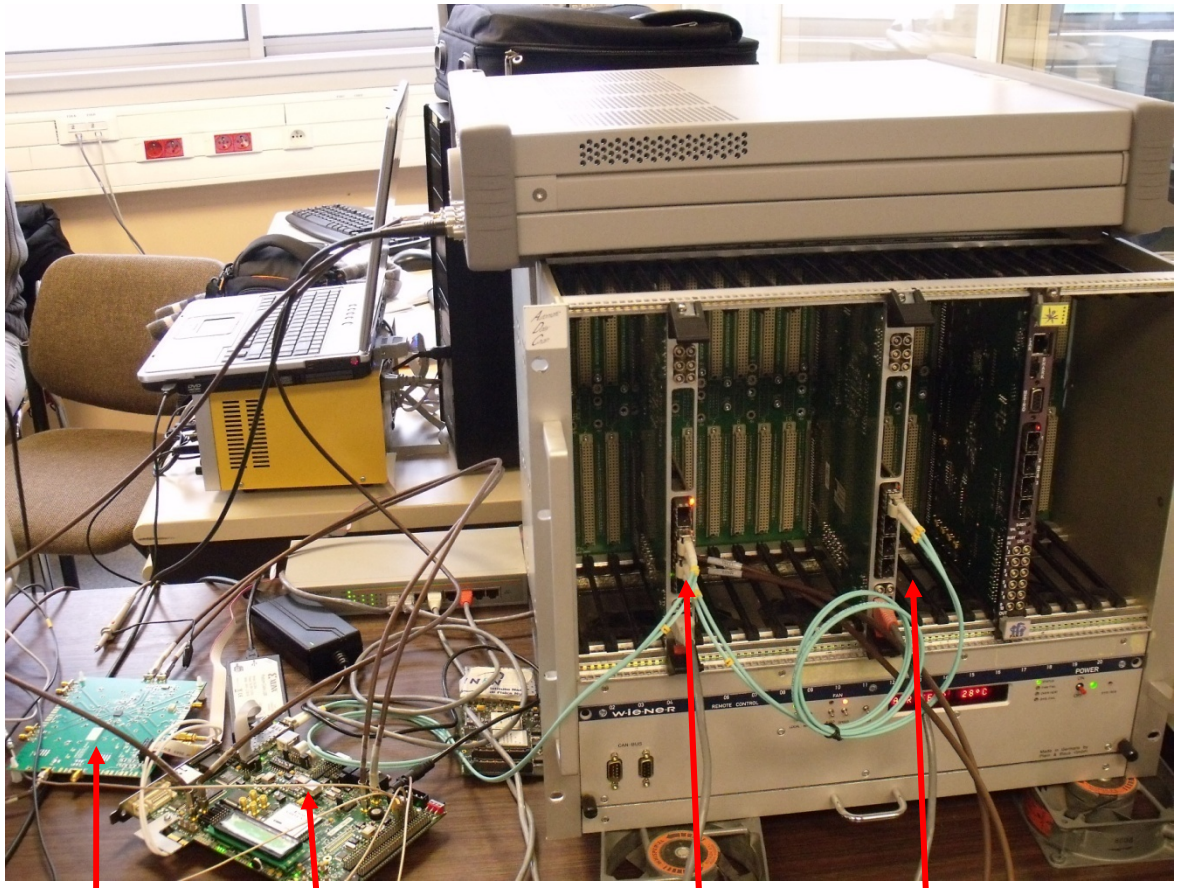
A) Training at Padova:

- GTS basics: functional blocks, tree setup, alignment
- Time stamp transmission: encoder/decoder, coarse delay implementation
- Trigger processing : packet transmission, trigger accept packets

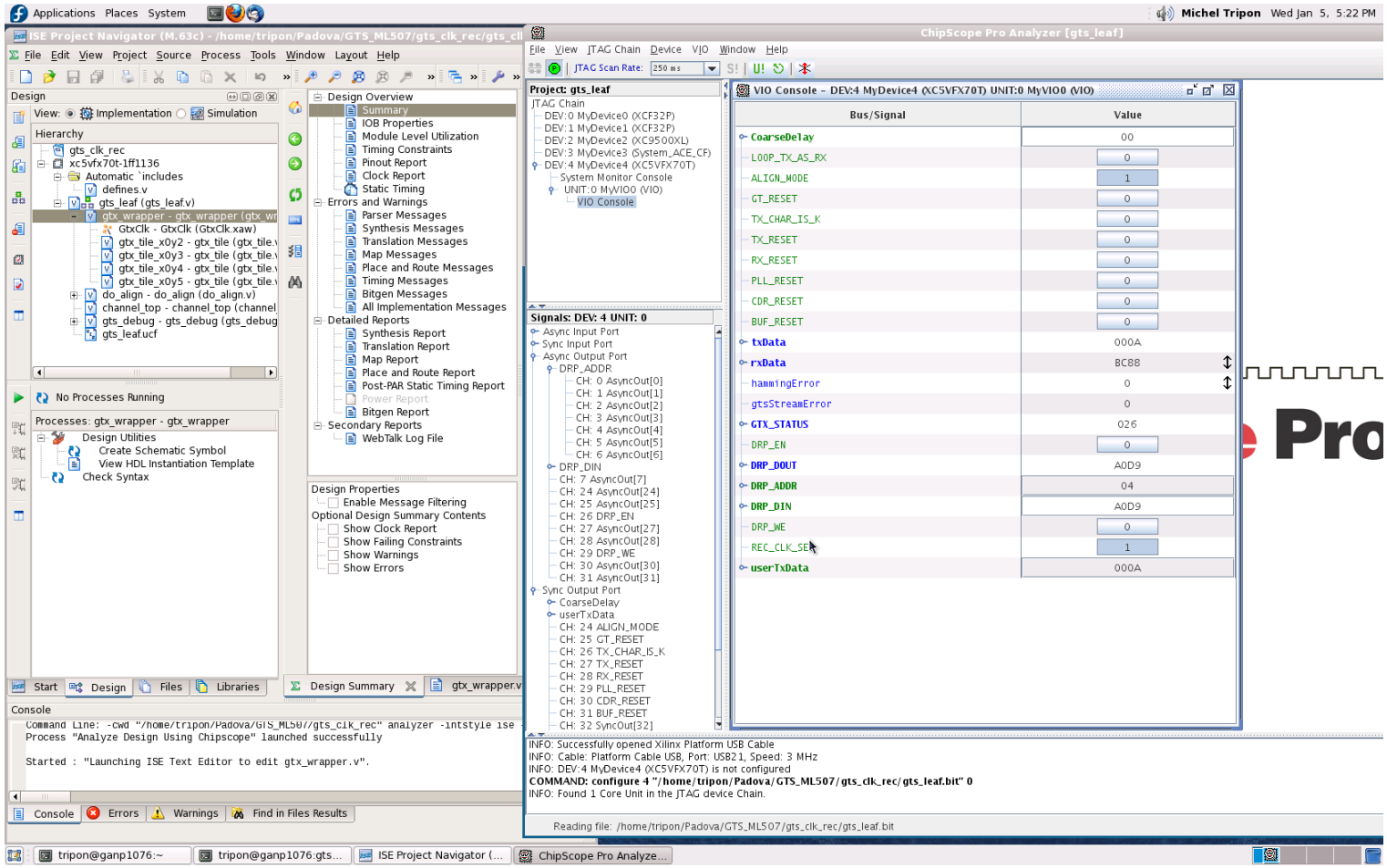
B) GTS Control System development:

- GUI : tree population, alignment, test
- UDP server/client

Current status: GTS leaf implementation



Current status: GTS leaf implementation



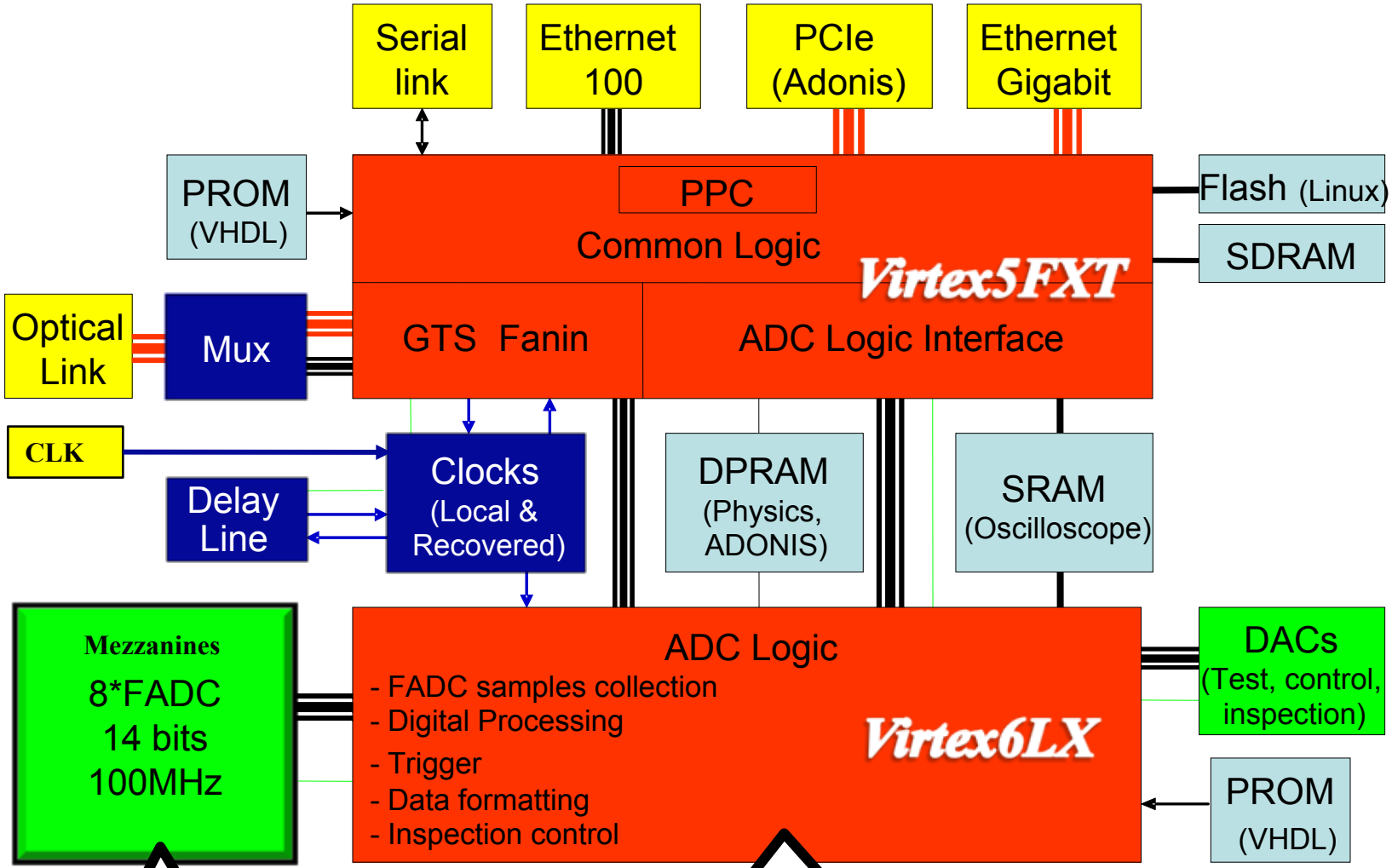
- GTS leaf ISE project on Viretx 5
- DRP registers are controlled by firmware

Current status: GTS leaf implementation

GTS recovered clock is locked :

100MHz clocks of the GTS root and leaves are synchronous

NUMEXO2 for NEDA and PARIS?

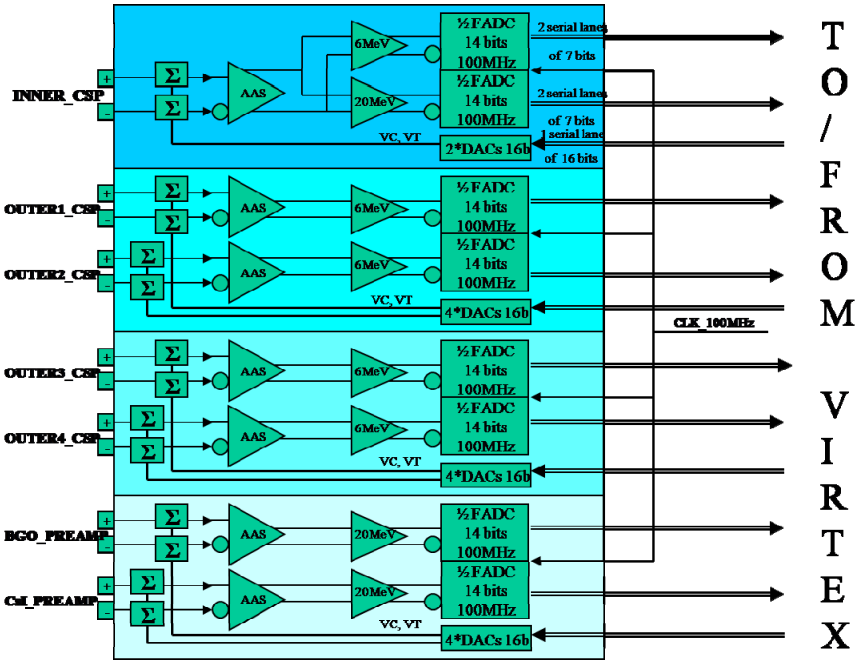


NUMEXO2 for NEDA and PARIS?

NUMEXO2 : 2*4 channnels FADC mezzanines block diagram

FADC: ADS6244, 14 bits, 100MHz, 2 binary samples serial lines @700Mb/s

Differential inputs



- Binary samples serial lines
- Clock line

⇒ **NEDA, PARIS:**

FADC mezzanines must be redesigned according to frequency bandwidth of inputs

- Sample frequency of FADC?
- Clock jitter?
- Number of binary samples serial lines?
- Power?
- MDR26 connector?
- SAMTEC connector?

NUMEXO2 for NEDA and PARIS?

3M™ Mini D Ribbon (MDR) Cable Assembly

.050" High Speed Digital Data Transmission System - 26 to 26 Pos. 14526-EZ8B-XXX-07C

- Solution for Digital Displays, Datacom and Telecom applications
- Supports LVDS FPD Link™, FlatLink™, ChannelLink™, PanelLink™/TMDS™ electrical interfaces
- Each differential twin-ax pair has a foil shield and drain
- Entire cable bundle is shielded with foil and braid for additional signal protection
- Rugged MDR ribbon type contact
- Quick release latches
- RoHS* compliant

Electrical

TS-0757-17
Sheet 1 of 4

Voltage Rating:	30 V
Current Rating:	1 A
Insulation Resistance:	$> 1 \times 10^{8}\Omega$ at @100 Vdc
Withstanding Voltage:	350 Vrms for 1 minute
Individually Shielded Twisted Pairs	
Characteristic Impedance:	$100 \pm 10^{\Omega}$
Conductor Size:	28 AWG Stranded
Propogation Velocity:	1.25 ns/ft [4.1 ns/m]

NEDA, PARIS:
MDR26 Cable and connector must be tested

Carrier-mezzanines connector: QFS-026-06-75-X-D-PC4

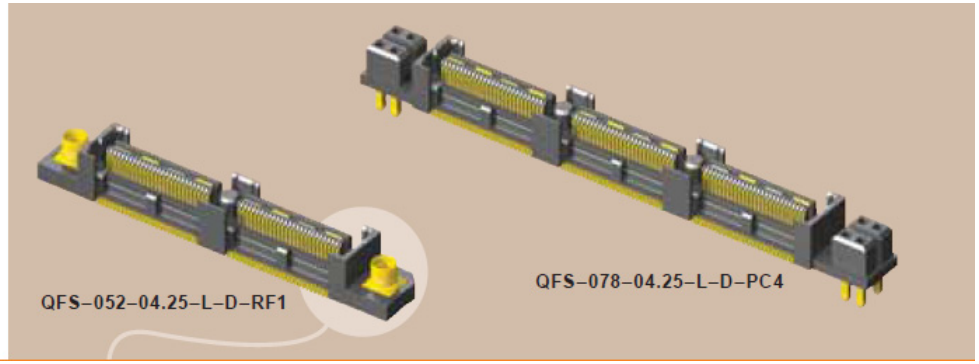
F-210-1

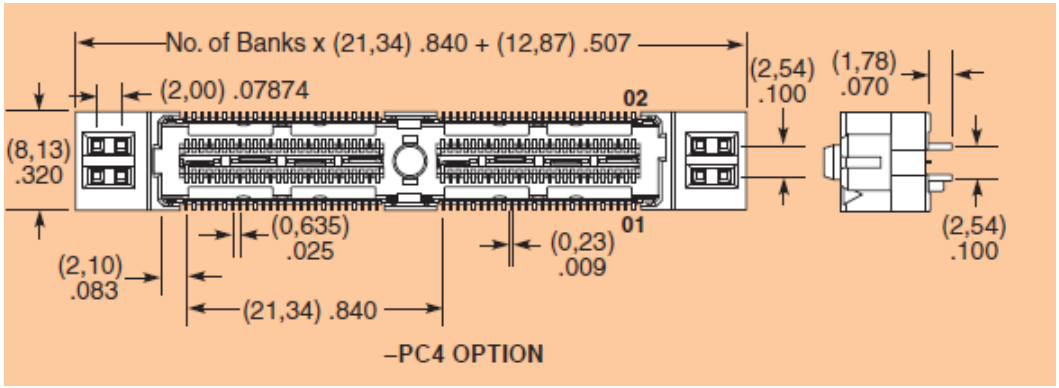
samtec

Q2™

(0,635mm) .025"

QFS-PC, QFS-RF SERIES





10mm Stack Height	Rated @ -3dB Insertion Loss
Single-Ended Signaling	9 GHz / 18 Gbps
Differential Pair Signaling	7.5 GHz / 15 Gbps

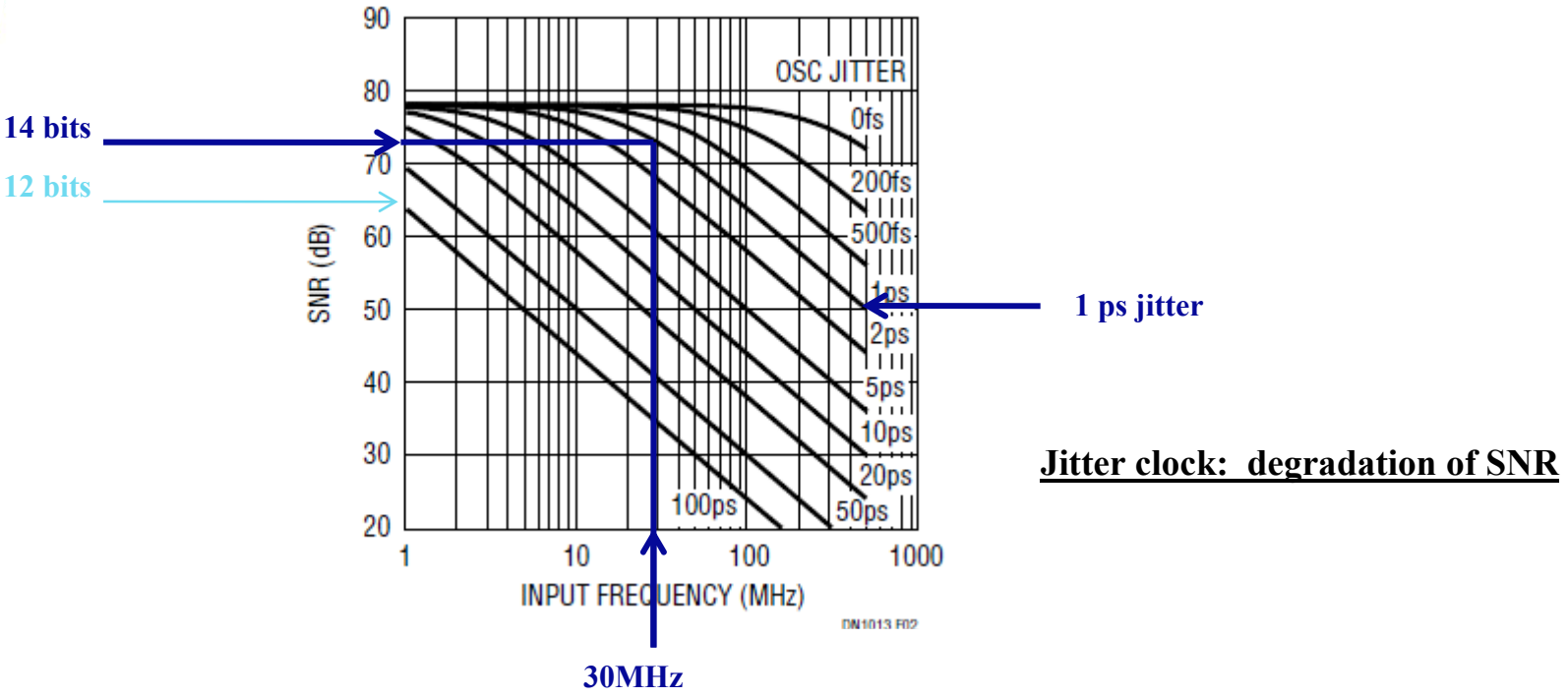
NEDA, PARIS: Does pins diagram fit?

FADC highlights

TI FADC	ADS6244	ADS62P49	ADS5463
Résolution (bits)	14	14	12
Sample rate (MSPS)	105	250	500
Input channels	2	2	1
Interface	LVDS serial // (2 LVDS lines)	LVDS serial // (7 LVDS lines)	LVDS // (12 LVDS lines)
Analog BW (MHz)	500	700	2300
SNR (dB)	73	73	65
ENOB (bits)	11.7	11.3	10.4
Power (W)	0.9	1.2	2.3

Clock jitter specifications

- FADC clock

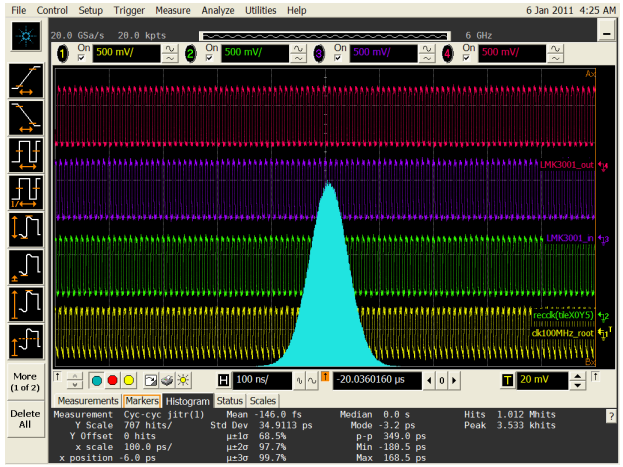


Jitter clock: degradation of SNR

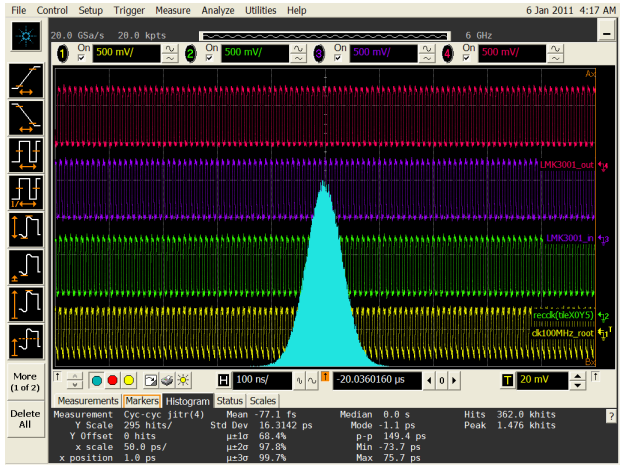
- High resolution timing

NUMEXO2 for NEDA and PARIS?

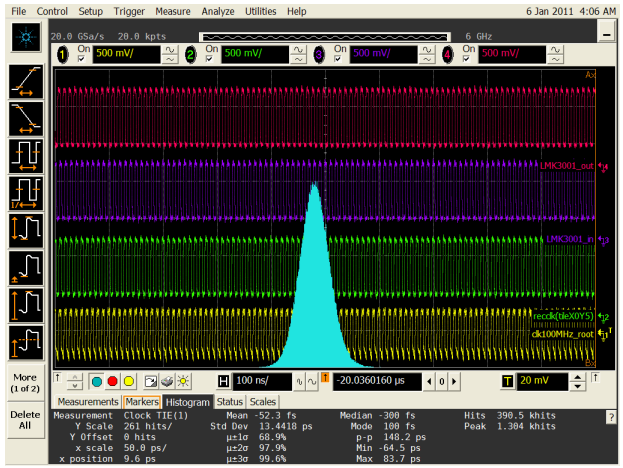
100MHz GTS clock jitter



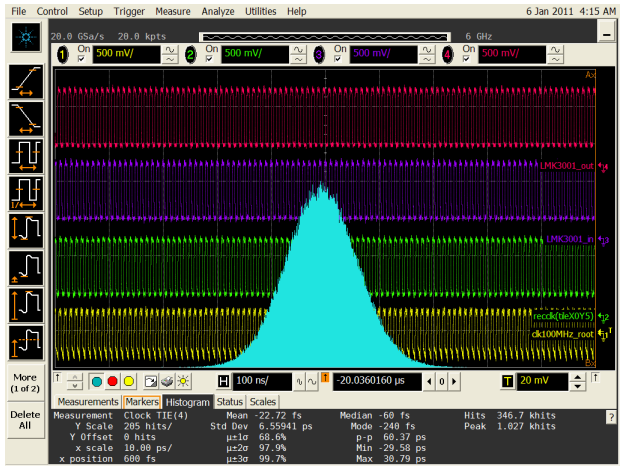
GTS ROOT: Std Dev (cycle to cycle)= 35ps



GTS leaf_like : Std Dev (leaf to leaf) = 16 ps



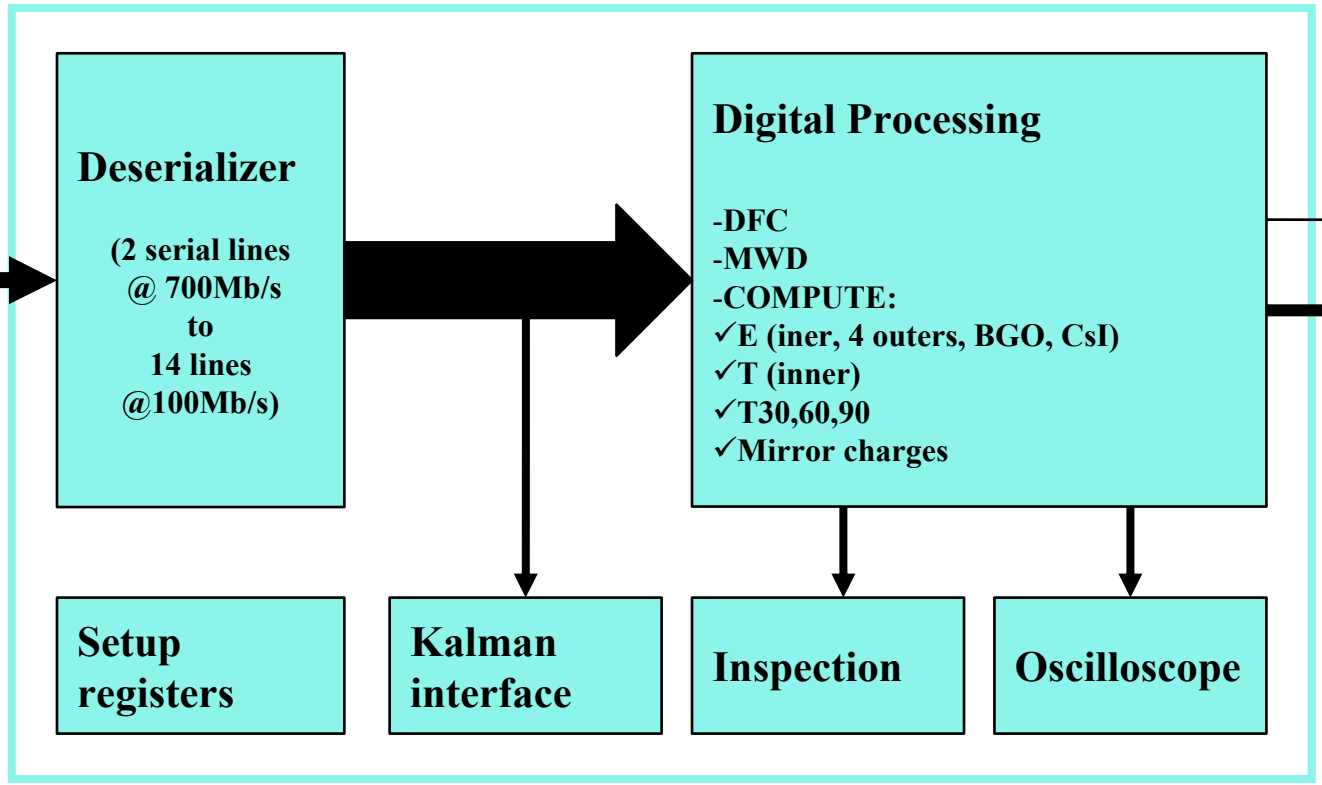
GTS ROOT: Std Dev (TIE)= 13ps



GTS leaf_like : Std Dev (TIE) = 6 ps

NUMEXO2 for NEDA and PARIS?

Block diagram of EXOGAM2 signal processing

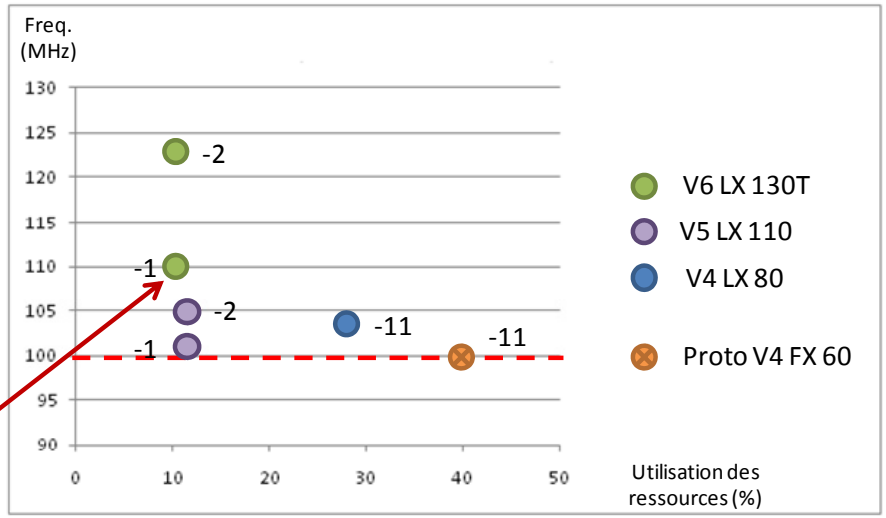


⇒NEDA, PARIS:
- Deserializer and Digital Processing IPs must be written
- Kalman interface suppressed
- Number of Trigger Request signals > 2
- Setup registers, Inspection and Oscilloscope IPs must be modified

FPGA target choice: Virtex 6 LX130T -1

PROJET EXOGAM2/NUMEXO2/FPGA TNS VIRTEX6

Quel composant VIRTEX4, 5, 6…



8 voies MWD

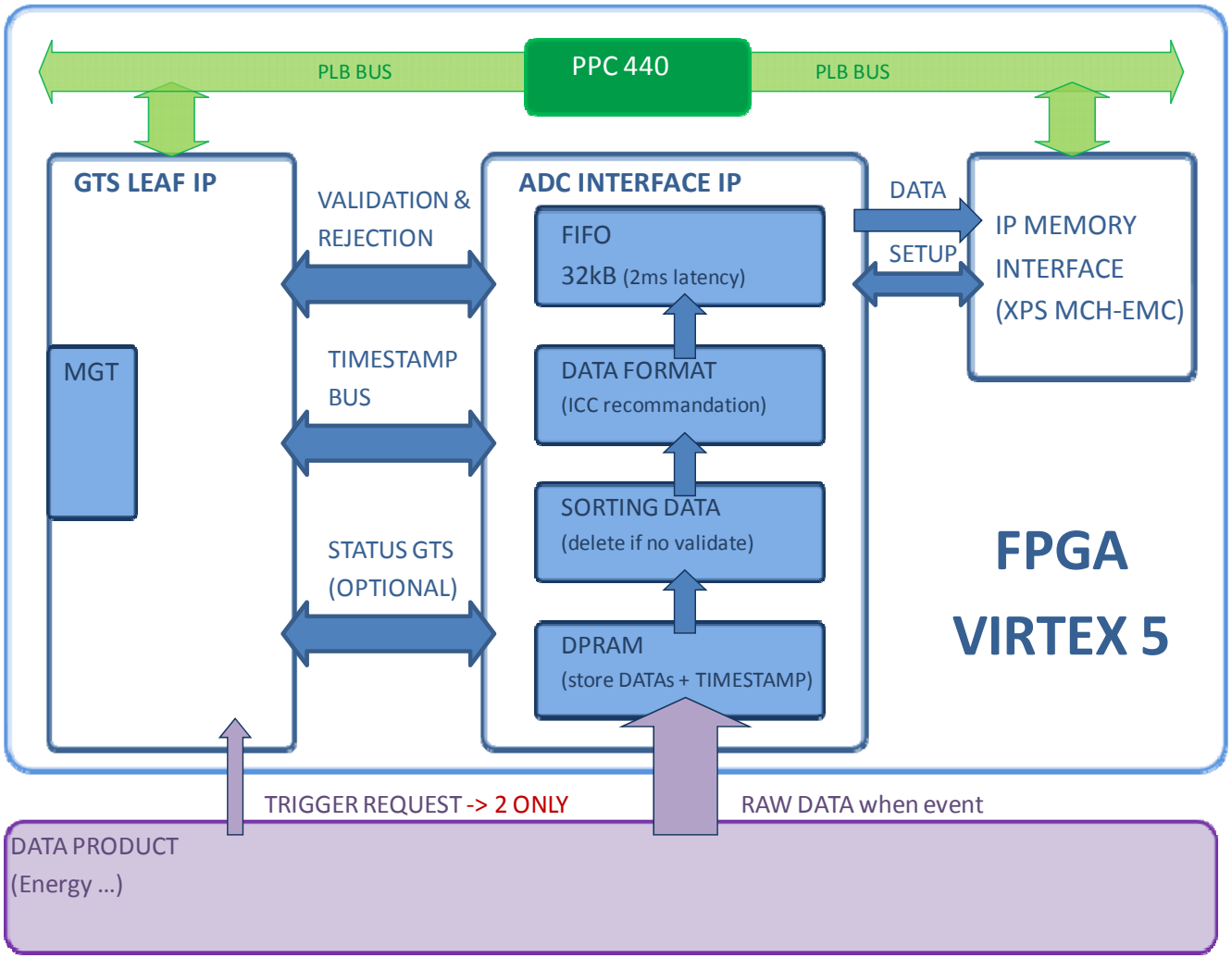
Cible choisie : Virtex 6 LX130T -1 *1094 $ - distributeur Avnet*

Marge de fréquence de 10% -> 40% désormais avec une optimisation plus poussée
Faible taux de remplissage

Is the Virtex 6 LX130T -1 powerfull enough for NEDA, PARIS signal processing?

NUMEXO2 for NEDA and PARIS?

Block diagram of EXOGAM2 GTS and ADC interfaces



⇒**NEDA, PARIS :**

- **DPRAM and FIFO depths?**
- **Data format?**