



CALOROC1C Datasheet



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CALOROC1C: ARCHITECTURAL OVERVIEW

The CALOROC1C ASIC (Application Specific Integrated Circuit) is made of 36 independent and autonomous channels to provide a measurement of the charge and of the arrival time (TOA) for the 36 input signals.

The overall block diagram is shown below (Figure I.1) and described after.

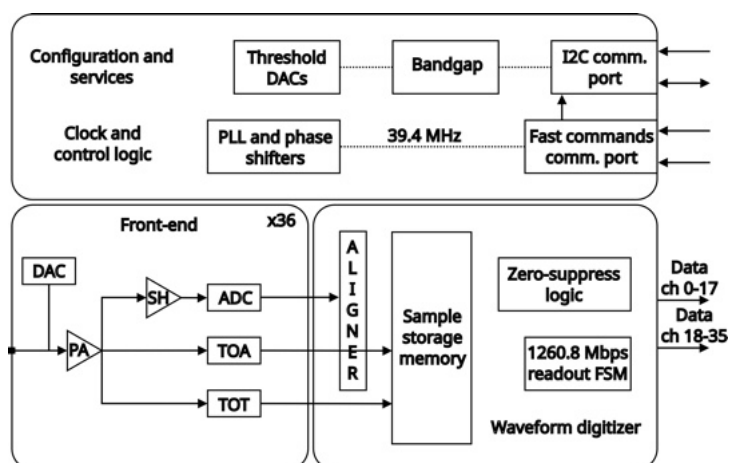


Figure I.1: The overall block diagram

The analog front-end part (Part II) amplifies and filters the input signals to allow the charge measurement thanks to a 10-bit SAR ADC (designed by AGH in Kraków) and the arrival time measurement thanks to a 10-bit TDC (designed by the CEA IRFU group in Saclay).

CALOROC1C was developed for ALLEGRO (A Lepton Lepton collider Experiment with Granular Read-Out) at FCC (Future Circular Collider), using Liquid Argon (LAr) as the active material. It could also be used for Silicon detectors of low capacitances (up to a few hundreds pF).

Two 1.28 Gbps links (18 channels per link) are dedicated to transmitting digitised event information (charge and time measurements). An internal 32-depth circular DRAM buffer stores this data (encoded with Hamming code for charge and time) until the serial link becomes available. An "almost full" indicator (Flag_AF) is provided via an output pin to inform the user of the buffer's status.

The Zero Suppression logic outputs data only from hit channels, transmitting it over dedicated links. It is enabled by status bits configured via slow control.

The I2C protocol is used to configure and monitor the chip parameters. This section is triplicated to provide robustness against Single Event Effects (SEE). The chip is controlled by the Fast Command block (Part III), which receives a 320 MHz clock and a 320 MHz command link. This block enables the transmission of commands for configuring specific operating modes, such as link synchronisation, reset, calibration, etc. It also generates the 40 MHz clock from the 320 MHz command link.

The 40 MHz clock is used by the digital part of the ASIC (digital processing, I2C interface) and by the PLL, which generates the additional clocks required by the ASIC. The PLL provides:

- a 640 MHz clock for the 1.28 Gbps links,
- a 40 MHz clock with adjustable phase for the ADCs,
- a 160 MHz clock with adjustable phase for the TDCs.

Phase adjustment is necessary to align the conversion blocks (ADC and TDC) with the phase of the physical signals, which depend on the rapidity angle.

All blocks (ADC, TDC, PLL) have proven to work with 40 MHz and its multiples before.

1 Analog front-end

The front-end can be divided in three main sub-parts (Fig. II.1):

- The **preamplifier** which converts the input charge coming from the electrode to an output voltage. It must provide the first amplification of the signal with the best noise performance. In the linear part of the amplifier, the feedback capacitors and feedback resistors provide the gain and the shape of the output signal which is sent to the shaper. From the saturation and above, the feedback discriminator triggers and provides the charge measurement by using the "Time Over Threshold" technique (ToT). Another discriminator allows to give the timing information. The preamplifier can be calibrated by injecting a voltage step through two channel-wise selectable capacitors (0.5pF and 10pF).
- The **shaper** part is composed of three stages: a Sallen-Key filter, a RC^2 filter and a unity gain amplifier to drive the ADC.
- The **two discriminators** providing the ToT and ToA (Time of Arrival) pulses, each one sent to a dedicated TDC.

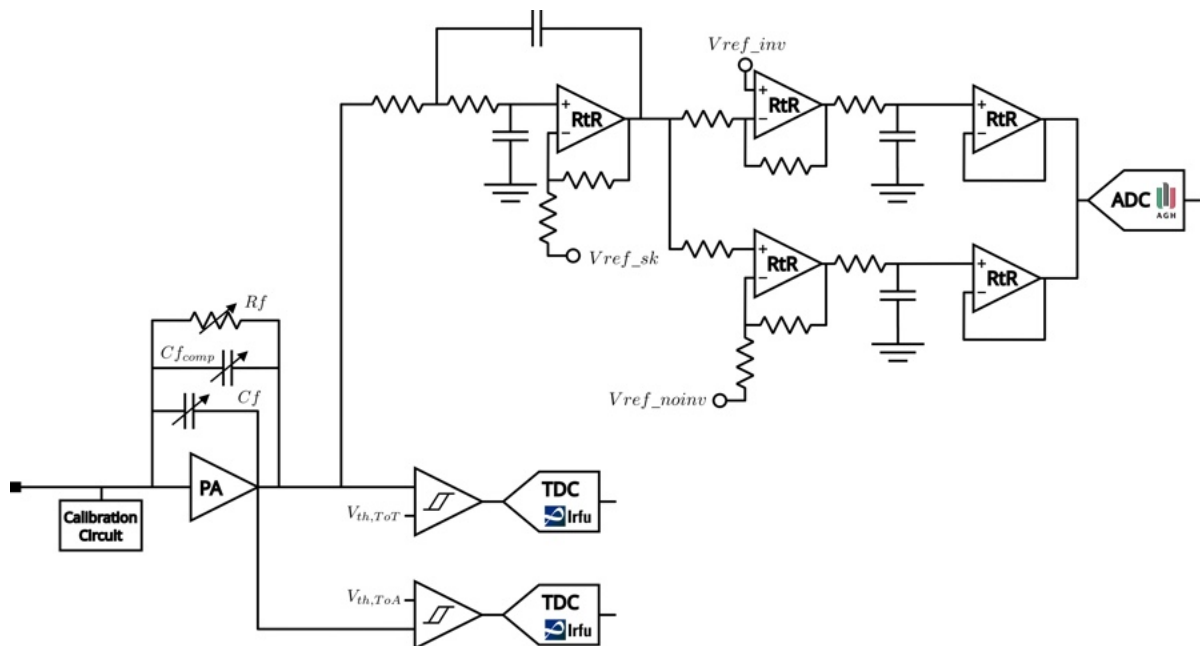


Figure II.1: CALOROC1C Analog Front-End

The image below (Fig. II.2) shows a layout view of the 4 channels block. The bump pads are placed above either large capacitors or I2C registers so that the area above the sensitive analog parts are kept free of bump pads.

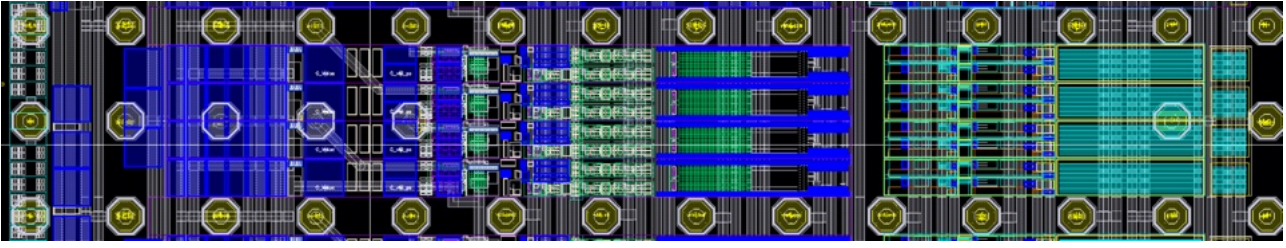


Figure II.2: Bump pads placement in CALOROC1C

In the following sections, more details are given for each blocks.

1.a Preamplifier

The preamplifier is DC coupled to the input and provides two outputs:

- outpa connected to the **shaper** and the **ToT discriminator**. Its DC operating point is the same as the preamplifier input (~ 200 mV).
- outCf_pa connected to the **ToA discriminator**. Its DC operating point is around outpa + V_{gs} (~ 500 mV).

A 8b-DAC is connected to the preamplifier input to absorb the leakage current coming from the sensor. And allow correction of the DC shift in temperature at the output of the preamplifier due to V_{gs} variations.

The purpose of the preamplifier is to convert the input charge to a voltage output with the best signal-to-noise ratio (SNR) and a gain adapted to the MIP signal. To meet all these requirements, the gain and the time constant must be adjustable (these parameters are global, not channel-wise). In the table below (Tab. II.1), all the possibilities are described:

Parameter	Possible values	Description
Rf (Ω)	100k, 1M	In parallel, these resistors provide 2 values to be adjusted with the Cf and Cf_comp values to get the desired decay time constant.
Cf (fF)	50, 100, 200, 400	Combined with the Cf_comp capacitors, provide the gain of the preamplifier.
Cf_comp (fF)	100, 200	Same purpose than Cf capacitors, but connected differently to improve the preamplifier stability. From gain point-of-view can be considered in parallel with Cf capacitors.

Table II.1: Rf, Cf and Cf_comp possibilities

The actual value of the feedback resistance depending on the slow control parameters is described in Tab. II.2. Note that even though Rf<1>, Rf<2> and Rf<3> are available in the slow control registers, they are unused in this ASIC. Only Rf<0> is useful to control the feedback resistance.

Rf code	Rf<0>	Rf value (Ω)	Description
0	0	1M	1M alone
1	1	90k	1M in parallel with 100k

Table II.2: Rf value depending on slow control parameter

The actual values of the feedback capacitances depending on the slow control parameters are described in Tab. II.3 and Tab. II.4.

Cf_comp code	Cf_comp<1>	Cf_comp<0>	Cf_comp value (fF)	Description
0	0	0	0	No capacitance
1	0	1	100	100 alone
2	1	0	200	200 alone
3	1	1	300	100 in parallel with 200

Table II.3: Cf_comp value depending on slow control parameter

Cf code	Cf<3>	Cf<2>	Cf<1>	Cf<0>	Cf value (fF)	Description
0	0	0	0	0	0	
1	0	0	0	1	50	
2	0	0	1	0	100	
3	0	0	1	1	150	50//100
4	0	1	0	0	200	
5	0	1	0	1	250	50//200
6	0	1	1	0	300	100//200
7	0	1	1	1	350	50//100//200
8	1	0	0	0	400	
9	1	0	0	1	450	50//400
10	1	0	1	0	500	100//400
11	1	0	1	1	550	50//100//400
12	1	1	0	1	650	50//200//400
13	1	1	0	0	600	400//200
14	1	1	1	0	700	100//200//400
15	1	1	1	1	750	50//100//200//400

Table II.4: Cf value depending on slow control parameter

The following plot (Fig. II.3) shows the preamplifier response to a 10 fC input charge for different choice of gain. The feedback resistor could not really be adjusted because the two values of Rf are too far apart, keeping the Rf*Cf product constant would make the "duration" of the signal constant as well and provide better comparison.

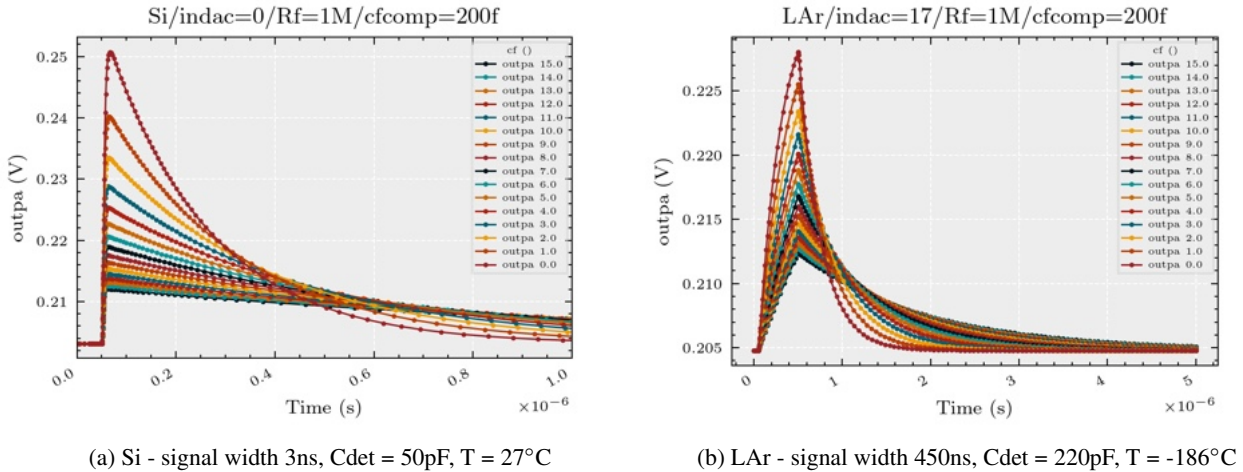


Figure II.3: Preamplifier response to 10 fC for multiple gains

The MIP in Allegro (FCC) is 2.25 fC, in order to have an ADC range of around 100 MIPs with a 10b ADC (meaning a LSB of around 0.1 MIP), the ADC range should be around 230 fC.

As said previously, this ASIC could also be used for Silicon detectors where the MIP is generally around 3-4 fC.

The tables below (Tab. II.5 for Si; Tab. II.6 for LAr) give the ADC dynamic range for each Cf and Cf_comp value, for Si and LAr detectors. The same tables are available with different temperatures and more Rf values in Annexe B. A column with the optimal MIP associated to the dynamic range is present; the ADC used is 10b (1023 ADC counts) and the wanted LSB is MIP/10, if the SNR wanted is different, the optimal MIP will change. The dynamic range is calculated from the simulated amplitude of the signal with an input charge of 10 fC, assuming that the maximum amplitude is 1 V (and 600 mV for signals at cryogenic temperatures with Rf = 90kΩ because the input DAC is unable to bring the DC level low enough). Note that the signal received by the ASIC and the temperature of the ASIC in the experiment are more or less independent; the main difference between Si and LAr signals is the width of the signal (around a few ns for Si and around a few hundred ns for LAr).

Rf code	Cf code	Cf_comp code	RfCf (ns)	Amplitude (mV)	Dynamic Range (fC)	MIP (fC)
---------	---------	--------------	-----------	----------------	--------------------	----------

0	0	1	100	206.9	48	0.47
0	0	2	200	132.5	75	0.73
0	0	3	300	98.66	101	0.99
0	1	0	50	276.8	36	0.35
0	1	1	150	153.9	65	0.64
0	1	2	250	109.6	91	0.89
0	1	3	350	85.66	117	1.14
0	2	0	100	184.7	54	0.53
0	2	1	200	123.4	81	0.79
0	2	2	300	93.61	107	1.05
0	2	3	400	75.73	132	1.29
0	3	0	150	141.6	71	0.69
0	3	1	250	103.4	97	0.95
0	3	2	350	81.83	122	1.19
0	3	3	450	67.91	147	1.44
0	4	0	200	115.5	87	0.85
0	4	1	300	89.09	112	1.09
0	4	2	400	72.76	137	1.34
0	4	3	500	61.55	162	1.58
0	5	0	250	97.8	102	1
0	5	1	350	78.37	128	1.25
0	5	2	450	65.51	153	1.5
0	5	3	550	56.33	178	1.74
0	6	0	300	84.94	118	1.15
0	6	1	400	69.99	143	1.4
0	6	2	500	59.59	168	1.64
0	6	3	600	51.94	193	1.89
0	7	0	350	75.13	133	1.3
0	7	1	450	63.25	158	1.54
0	7	2	550	54.65	183	1.79
0	7	3	650	48.17	208	2.03
0	8	0	400	67.43	148	1.45
0	8	1	500	57.72	173	1.69
0	8	2	600	50.5	198	1.94
0	8	3	700	44.93	223	2.18
0	9	0	450	61.18	163	1.59
0	9	1	550	53.12	188	1.84
0	9	2	650	46.97	213	2.08
0	9	3	750	42.07	238	2.33
0	10	0	500	55.95	179	1.75
0	10	1	600	49.19	203	1.98
0	10	2	700	43.88	228	2.23
0	10	3	800	39.62	252	2.46
0	11	0	550	51.62	194	1.9
0	11	1	650	45.8	218	2.13
0	11	2	750	41.17	243	2.38
0	11	3	850	37.39	267	2.61
0	12	0	600	47.92	209	2.04
0	12	1	700	42.84	233	2.28
0	12	2	800	38.77	258	2.52
0	12	3	900	35.43	282	2.76
0	13	0	650	44.71	224	2.19
0	13	1	750	40.29	248	2.42
0	13	2	850	36.67	273	2.67
0	13	3	950	33.66	297	2.9
0	14	0	700	41.9	239	2.34
0	14	1	800	37.98	263	2.57
0	14	2	900	34.75	288	2.82

0	14	3	1000	32.03	312	3.05
0	15	0	750	39.4	254	2.48
0	15	1	850	35.96	278	2.72
0	15	2	950	33.05	303	2.96
0	15	3	1050	30.6	327	3.2

Table II.5: Dynamic Range Si T = 27 °C

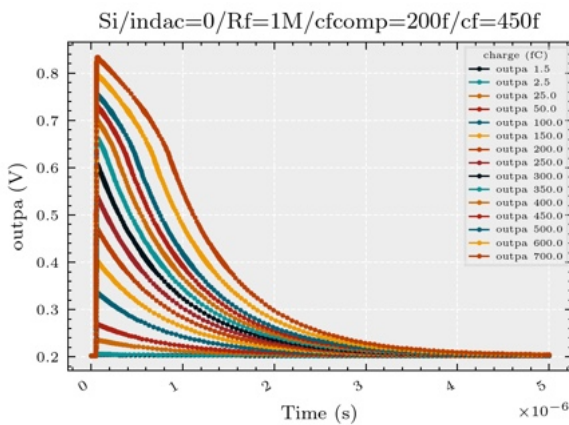
Rf code	Cf code	Cf_comp code	RfCf (ns)	Amplitude (mV)	Dynamic Range (fC)	MIP (fC)
0	0	1	100	106.3	94	0.92
0	0	2	200	86.8	115	1.12
0	0	3	300	71.55	140	1.37
0	1	0	50	113.1	88	0.86
0	1	1	150	94.11	106	1.04
0	1	2	250	76.93	130	1.27
0	1	3	350	64.47	155	1.52
0	2	0	100	102.1	98	0.96
0	2	1	200	83.09	120	1.17
0	2	2	300	68.86	145	1.42
0	2	3	400	58.62	171	1.67
0	3	0	150	89.99	111	1.09
0	3	1	250	73.89	135	1.32
0	3	2	350	62.24	161	1.57
0	3	3	450	53.74	186	1.82
0	4	0	200	79.57	126	1.23
0	4	1	300	66.34	151	1.48
0	4	2	400	56.73	176	1.72
0	4	3	500	49.55	202	1.97
0	5	0	250	71	141	1.38
0	5	1	350	60.13	166	1.62
0	5	2	450	52.15	192	1.88
0	5	3	550	45.98	217	2.12
0	6	0	300	64.02	156	1.52
0	6	1	400	55.02	182	1.78
0	6	2	500	48.2	207	2.02
0	6	3	600	42.89	233	2.28
0	7	0	350	58.22	172	1.68
0	7	1	450	50.65	197	1.93
0	7	2	550	44.82	223	2.18
0	7	3	650	40.19	249	2.43
0	8	0	400	53.37	187	1.83
0	8	1	500	46.93	213	2.08
0	8	2	600	41.87	239	2.34
0	8	3	700	37.81	264	2.58
0	9	0	450	49.24	203	1.98
0	9	1	550	43.7	229	2.24
0	9	2	650	39.29	255	2.49
0	9	3	750	35.71	280	2.74
0	10	0	500	45.71	219	2.14
0	10	1	600	40.9	244	2.39
0	10	2	700	37.04	270	2.64
0	10	3	800	33.85	295	2.88
0	11	0	550	42.64	235	2.3
0	11	1	650	38.43	260	2.54
0	11	2	750	35	286	2.8
0	11	3	850	32.12	311	3.04

0	12	0	600	39.97	250	2.44
0	12	1	700	36.27	276	2.7
0	12	2	800	33.18	301	2.94
0	12	3	900	30.62	327	3.2
0	13	0	650	37.63	266	2.6
0	13	1	750	34.36	291	2.84
0	13	2	850	31.54	317	3.1
0	13	3	950	29.19	343	3.35
0	14	0	700	35.53	281	2.75
0	14	1	800	32.58	307	3
0	14	2	900	30.06	333	3.26
0	14	3	1000	27.96	358	3.5
0	15	0	750	33.67	297	2.9
0	15	1	850	30.98	323	3.16
0	15	2	950	28.71	348	3.4
0	15	3	1050	26.76	374	3.66

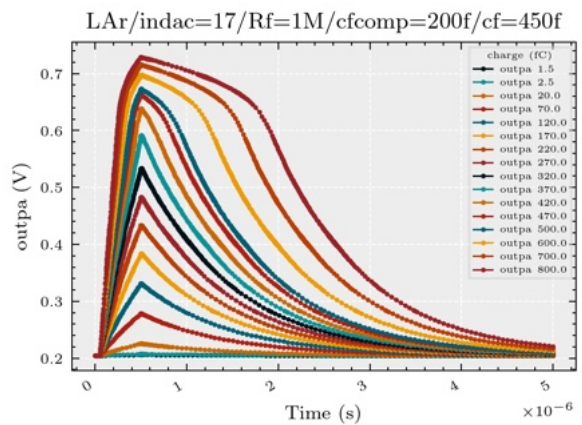
Table II.6: Dynamic Range LAr T = -186 °C

Since the preamplifier converts an input charge to an output voltage, its behaviour over the entire charge dynamic must be well known and characterised. That can be divided in three steps:

- The linear mode: the preamplifier provides an output amplitude proportional to the input charge. It is able to provide linear amplitude over ~300 mV dynamic range¹ (Fig. II.4). The ADC is used to measure the charge in this region which is named ADC range.
- The non-linear mode: this mode occurs in-between the linear and the saturated modes when the preamplifier is no longer linear but not still fully saturated. It is in this region that the ToT threshold has to be set in order to optimise the ADC range linearity. The preamplifier non-linear mode leads to the non-linearity of the ToT in the beginning of the ToT range, but the pile-up limitation is expected to be the best in this region (Fig. II.4 and Fig. II.5). The non-linear mode occurs for an output amplitude between 500 and 600 mV.
- The saturated mode: it occurs for an output amplitude above 600 mV (Fig. II.5). In this region, the preamplifier pulse width is proportional to the input charge and so well suited to use the Time-over-Threshold technics.



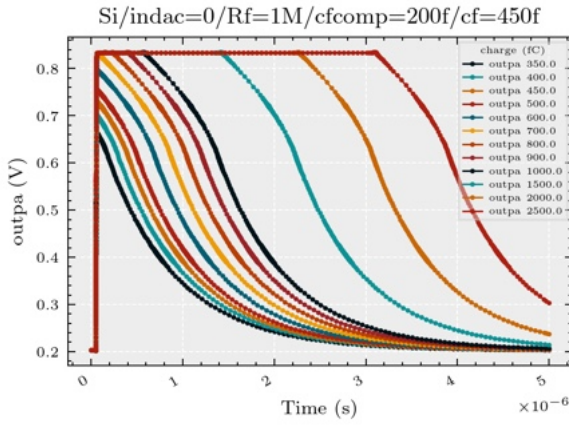
(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C



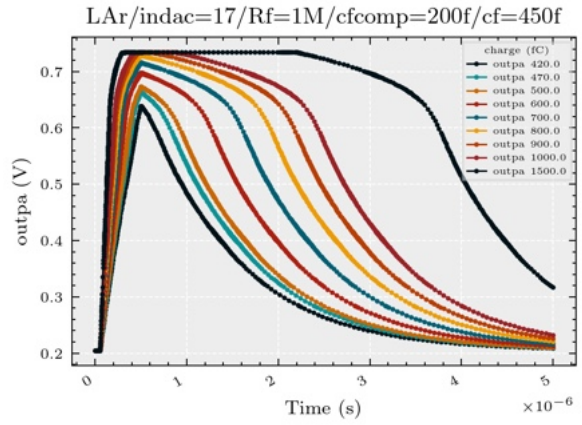
(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure II.4: Preamplifier response to different charges - no saturation

¹The linear dynamic range is limited to 300 mV because the first stage of the preamplifier is composed of four serial transistors needed to get a large open loop gain (90dB) what implies the first stage output amplitude is limited by a cascode transistor's Vds - Vds_sat voltage.



(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C



(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure II.5: Preamplifier response to different charges - saturation

1.b Input DAC

A DC shift at the input of the preamplifier at lower temperature is expected. The current causing the shift is actually provided by the front-end circuit itself, coming from the V_{gs} of the input transistor of the preamplifier. As a consequence, the DC level of the preamplifier output follows exactly the DC level of the preamplifier input and its dynamic range is limited by this effect. To withdraw the natural shift of the DC level due to the temperature shift, an input DAC is needed for providing the current compensation at the price of a degraded noise performance.

The input DAC could also be used to compensate the leakage current of the sensors in applications that do not deal with cryogenic temperatures like Allegro (FCC).

As the input DAC is needed to maintain the optimal preamplifier dynamic range (and so the ADC range), it has to be designed so that the noise performance are kept as good as possible. The figure of the architecture is shown below (Fig. II.6). The R-DAC is supposed to achieve better noise optimisation, but since the feedback resistance is relatively high by default (1 M Ω) is unusable in this ASIC, bringing this 8b DAC closer to a 5b DAC.

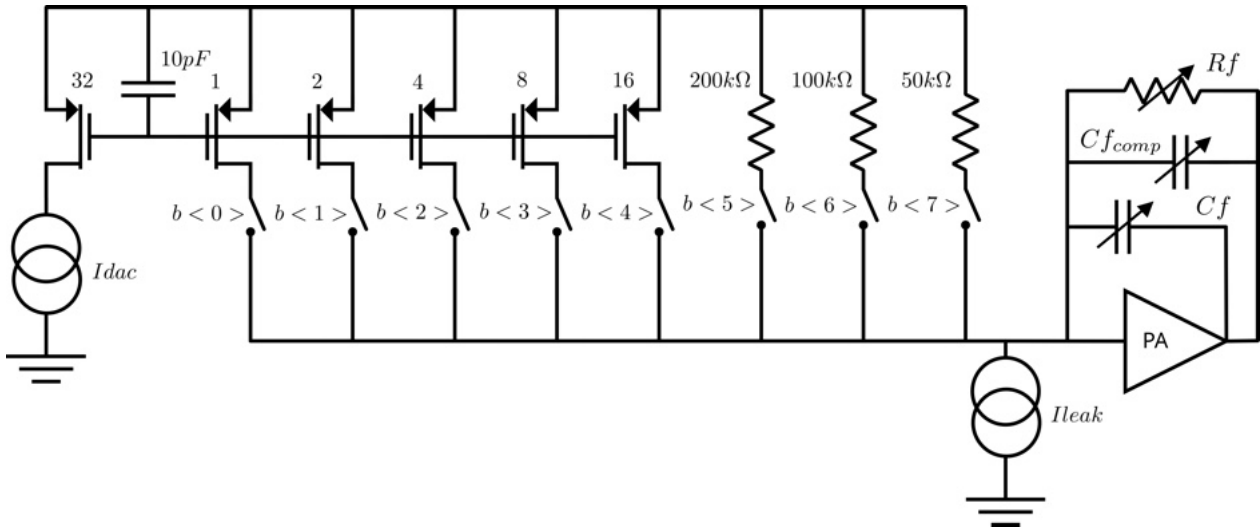


Figure II.6: Input DAC architecture

1.c Shapers

The shaper is divided in three stages:

- A Sallen-Key (S-K) shaper, gain 2,
- A RC² shaper, gain 2,
- Then a buffer to drive the ADC.

It is a 4th order RC shaper with the peaking time typically set around 600ns (shaping time ~150ns) for LAr and 200ns for Si. The purpose is to optimise the signal-to-noise ratio and use the full available dynamic range (~1 V). The shaping time is adjustable over 2 bits (rc) to mitigate for process variations, it can only correct a few nanoseconds.

The user has to set the `inv_vref` and `noinv_vref` 10b DACs to globally set the DC levels of respectively the inverter and non_inverter shapers, and so set the ADC pedestal. These 10b-DACs have typically 1mV LSB. In order to reduce the dispersion per channel, the user can play with a channel-wise trimming 6b-DAC (`trim_dac`).

The inverter shaper output's DC level is equal to:

$$3 \times (\text{inv_vref} < 9 : 0 > - \text{trim_dac} < 4 : 0 >) - 2 \times \text{Vinpa} \quad (\text{II.1})$$

The non_inverter shaper output's DC level is equal to:

$$2 \times \text{Vinpa} - \text{noinv_vref} < 9 : 0 > \quad (\text{II.2})$$

With Vinpa the preamplifier input's DC level (~200 mV).

The ADC converts the differential voltage ($\text{SH_noinv} - \text{SH_inv}$).

The following plots (Fig. II.7 and Fig. II.8) show respectively the non-inverted and the inverter shaper output. The curves show both the response to the signal in the ADC range and to small "ToT charges".

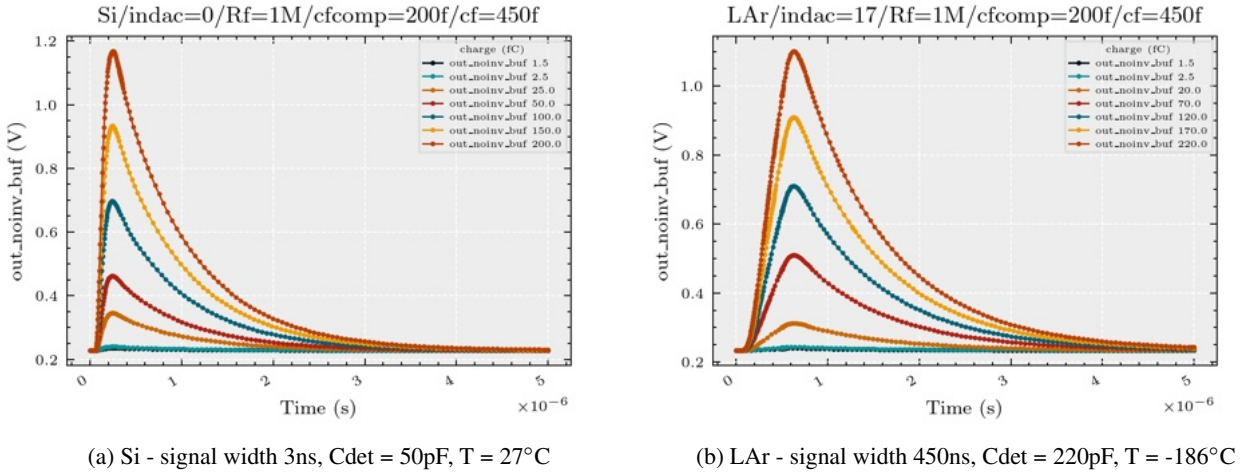


Figure II.7: Non-inverter shaper output - no saturation

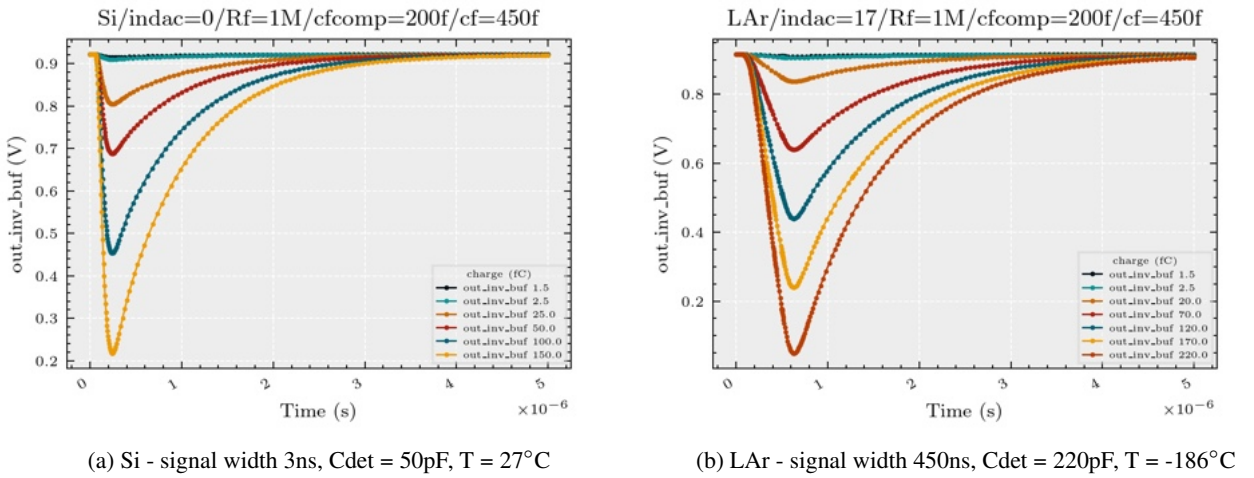


Figure II.8: Inverter shaper output - no saturation

Before saturation or a ToT triggering, the shaper outputs follow the equation below:

$$f(t) = \frac{1}{6\tau^4} e^{\frac{-t}{\tau_{pa}}} \left[e^{ct} \left(\frac{t^3}{c} - \frac{3t^2}{c^2} + \frac{6t}{c^3} - \frac{6}{c^4} \right) + \frac{6}{c^4} \right] \quad (\text{II.3})$$

With τ the shaper time constant, τ_{pa} the preamplifier time constant and $c = \frac{1}{\tau_{pa}} - \frac{1}{\tau}$.

The following plots (Fig. II.9 and Fig. II.10) show respectively the non-inverted and the inverter shaper output in ToT range. This ToT range is using the non-linear mode and the saturated mode of the preamplifier.

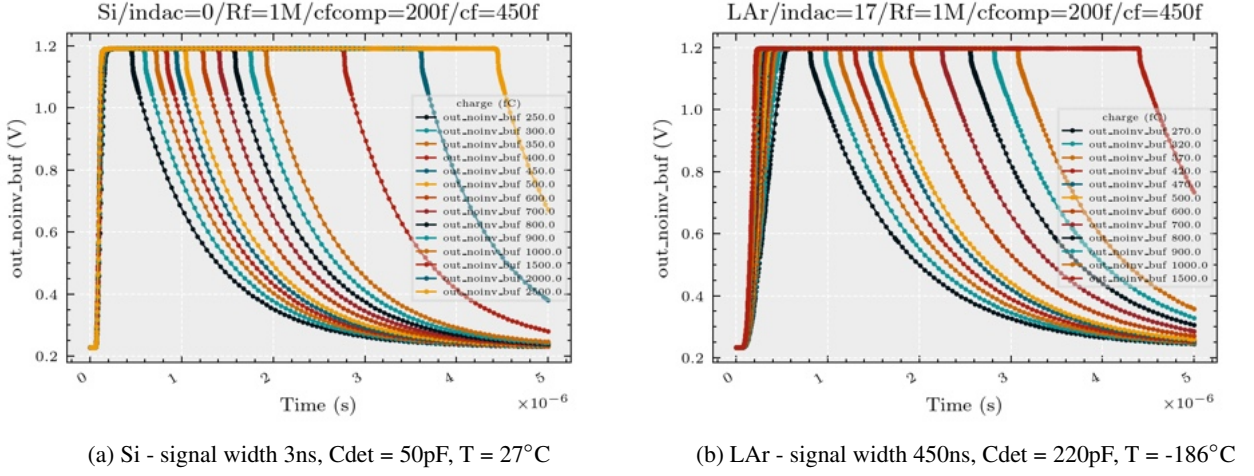


Figure II.9: Non-inverter shaper output - saturation

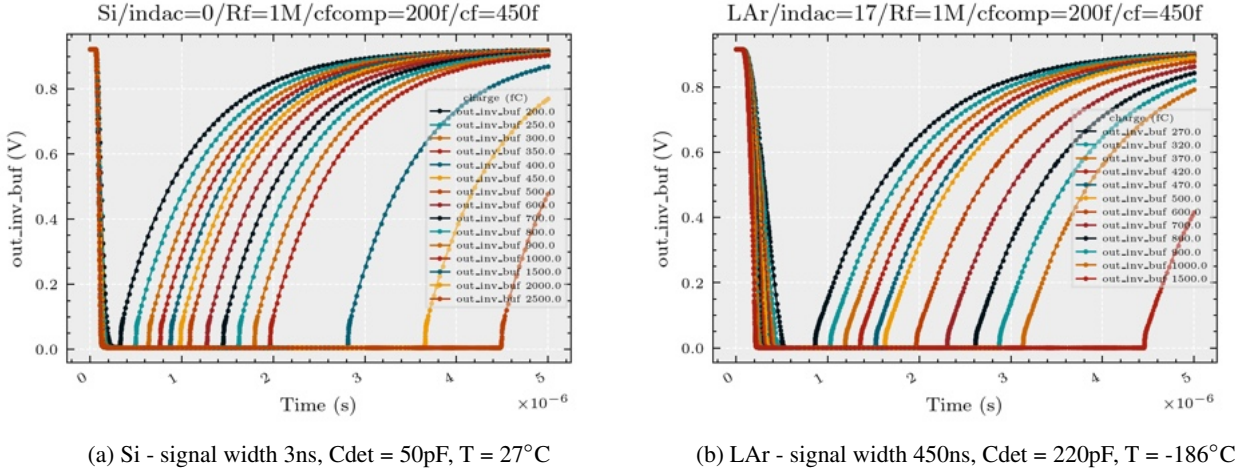


Figure II.10: Inverter shaper output - saturation

The next figure (Fig. II.11) presents the Equivalent Noise Charge (ENC) as a function of the detector capacitance.

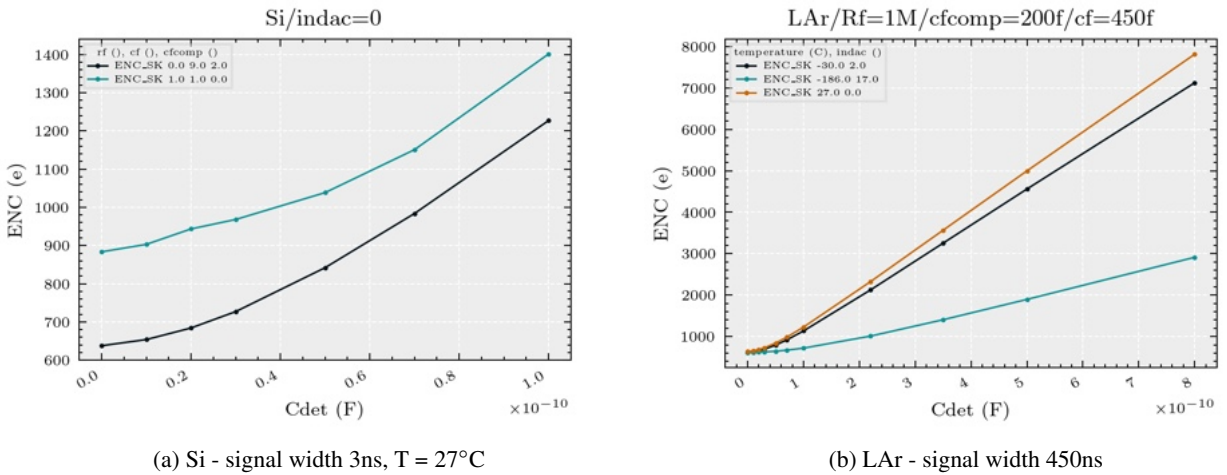


Figure II.11: ENC vs Cdet

The gain, the peaking time, the OOT (out-of-time) pileup vary with corners (PVT - process, voltage, temperature - variations)

and with the sensor capacitance. Therefore some parameters are available to tune these values: the shaping time over 2 bits (rc) and the bandwidth of the RtR amplifier.

The waveforms below (Fig. II.12) show the preamplifier and the shaper outputs as a function of the sensor capacitance Cdet.

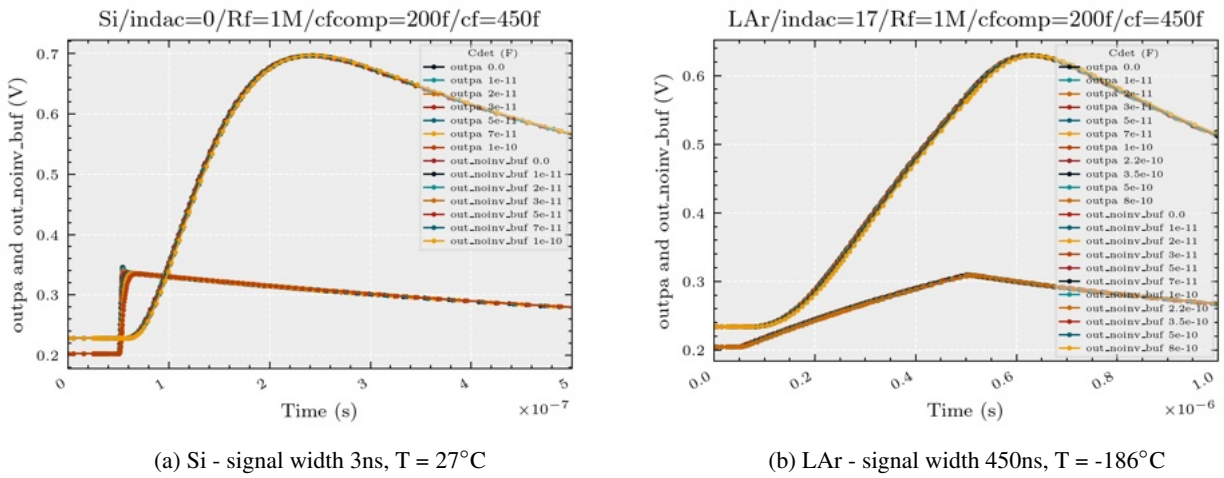


Figure II.12: PA and SH waveforms with different Cdet

The waveforms below (Fig. II.13) show the preamplifier and the shaper outputs as a function of the PVT variations.

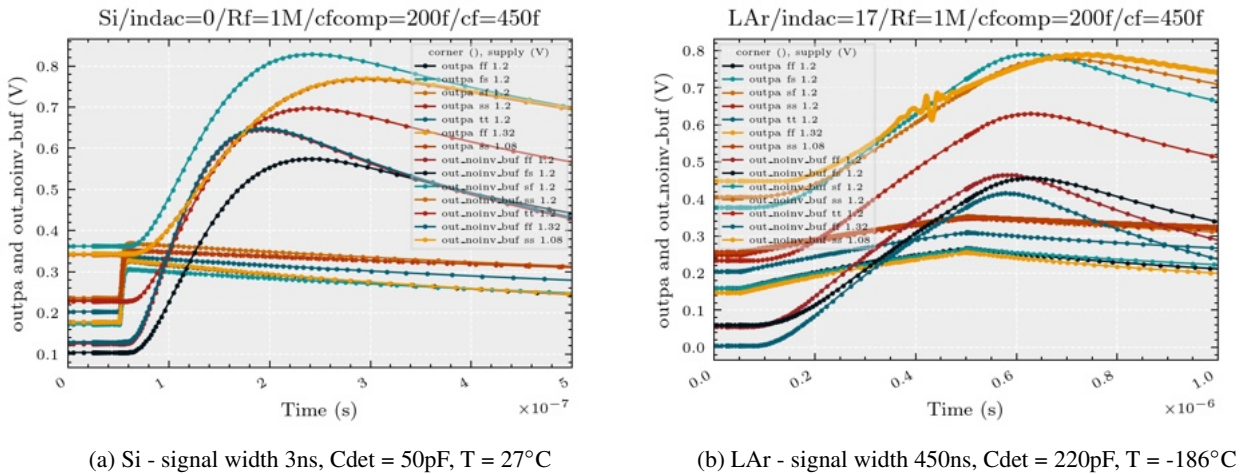
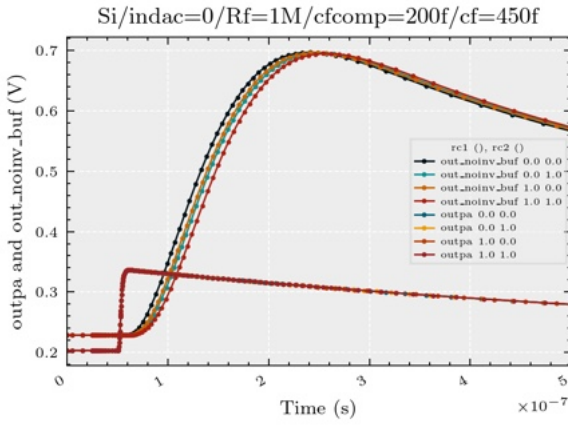
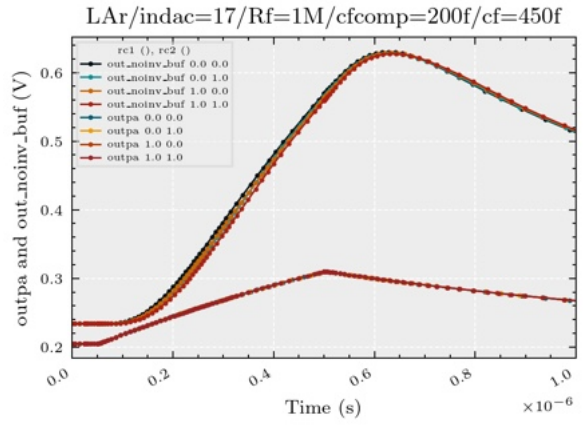


Figure II.13: PA and SH waveforms with different PVT

The shaping time parameter allow the user to tune the peaking time to remove the impact of the PVT variations on the shaping time (Fig. II.14)



(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C



(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure II.14: PA and SH waveforms - trimmed

If those parameters are not sufficient, the user can tune as well the bandwidth of the RtR amplifiers (2b bias of the input differential stage - Ibi_sk, Ibi_inv, Ibi_inv_buf, and Ibi_noinv_buf).

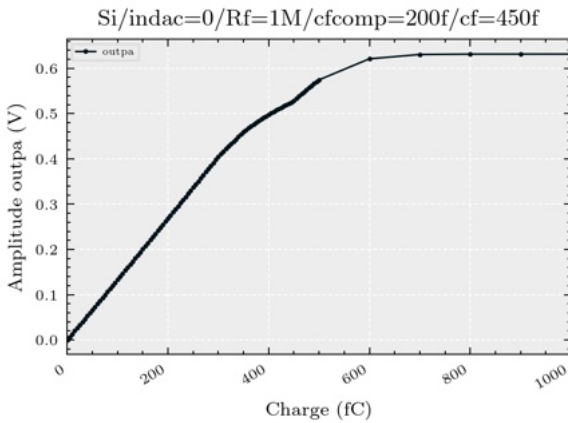
1.d Optimisation of the "ADC range"

A simple circuit has been introduced to automatically find out the best combination of both Vref_inv and Vref_noinv 10b DACs. The principle is to force one of the ADC input to 0.6 V, perform a scan of the Vref DAC of the other branch and set it to the value giving the code 256 (266 in fact to have some margin), and then redo the same operation but for the other branch. By construction, this procedure allows the optimisation of both the pedestal and the dynamic range.

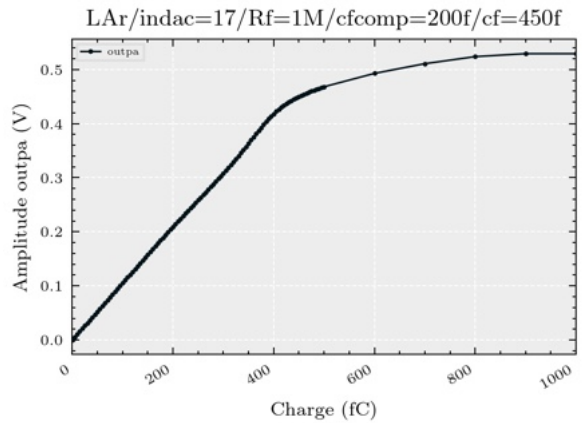
With Vref (≈ 1 V) the reference voltage of the ADC, Vdd (≈ 1.2 V) the power supply value, Inv and Noinv the inverted and non-inverted shaper outputs respectively, we have:

$$ADC = \left(1 - \frac{Inv - Noinv}{Vref}\right) \times \frac{1024}{2} \quad (II.4)$$

The figures below (Fig. II.15, Fig. II.16, Fig. II.17 and Fig. II.18) provide the dynamic range of the analog signals of the ASIC.

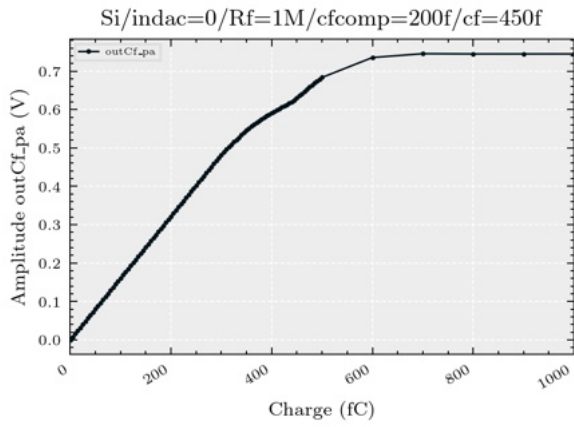


(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C

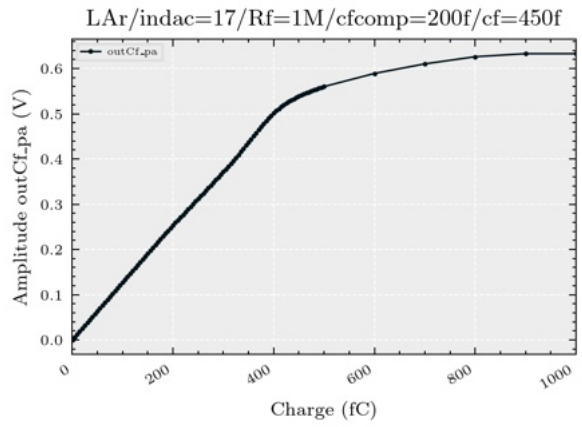


(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure II.15: outpa amplitude linearity

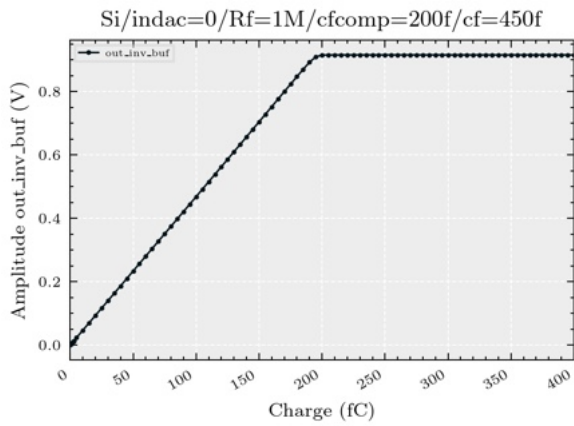


(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C

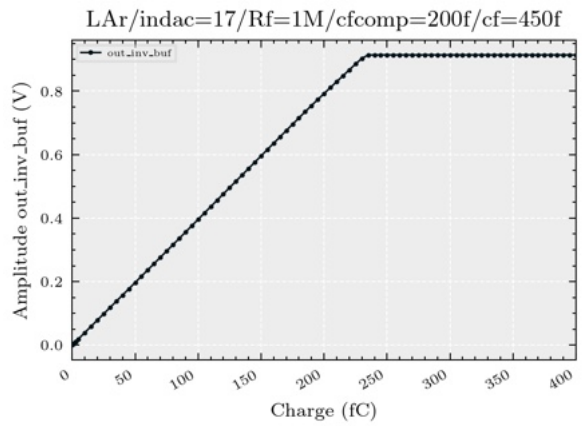


(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure II.16: outCf_pa amplitude linearity

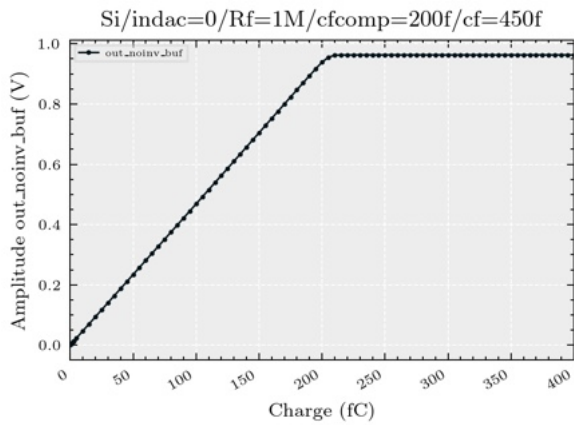


(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C

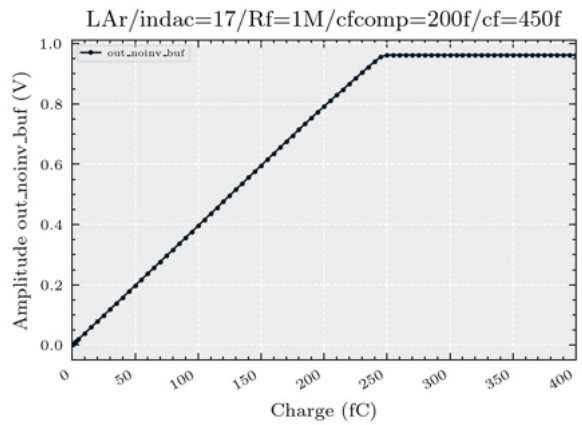


(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure II.17: out_inv_buf amplitude linearity



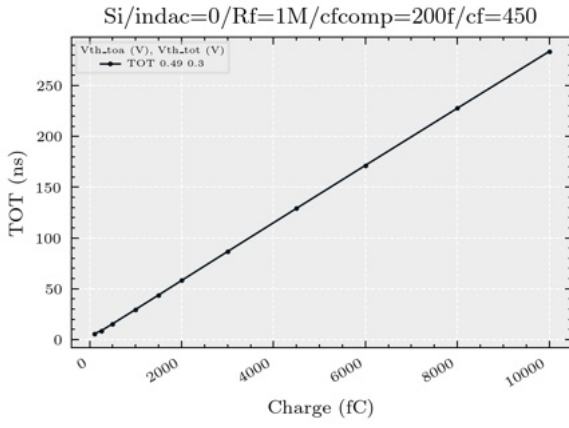
(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C



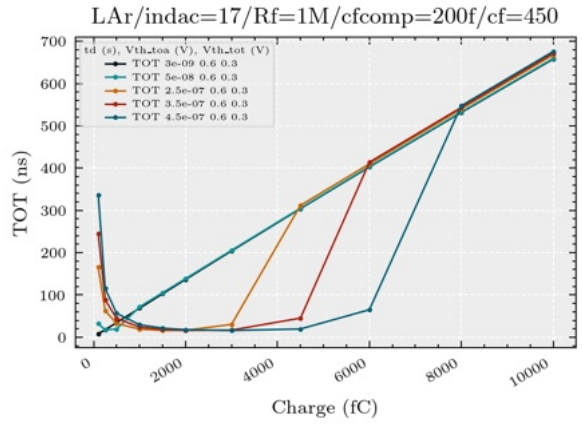
(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure II.18: out_noinv_buf amplitude linearity

The figures below (Fig. II.19 and Fig. II.20) highlights the linearity of the signal before ToT and the importance of using the current itot specifically for Liquid Argon where it isn't just a question of length of the signal like in Si but of integrity of the measurement. Figure II.21 present the signals at the input of the ToT discriminator for the same injected charge and different itot values.

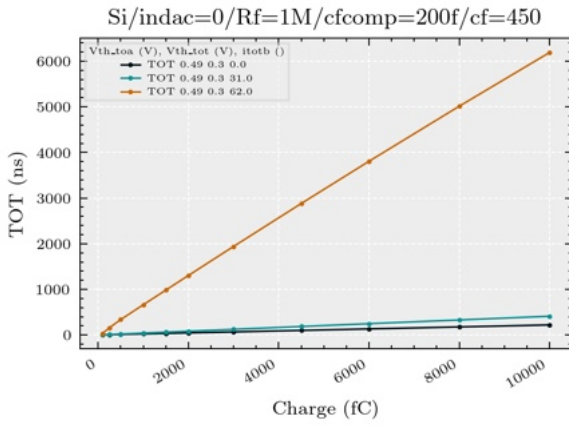


(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C

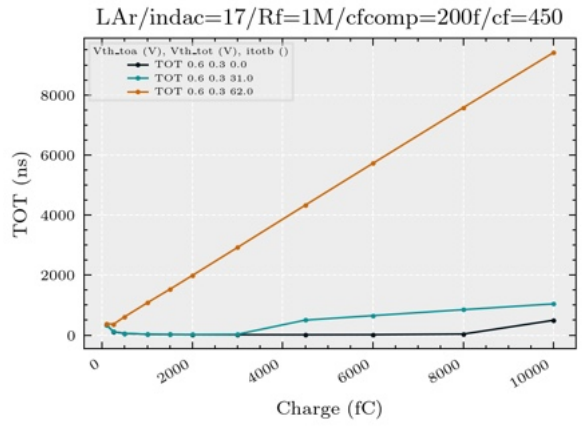


(b) LAr - signal width varying, Cdet = 220pF, T = -186°C

Figure II.19: ToT linearity

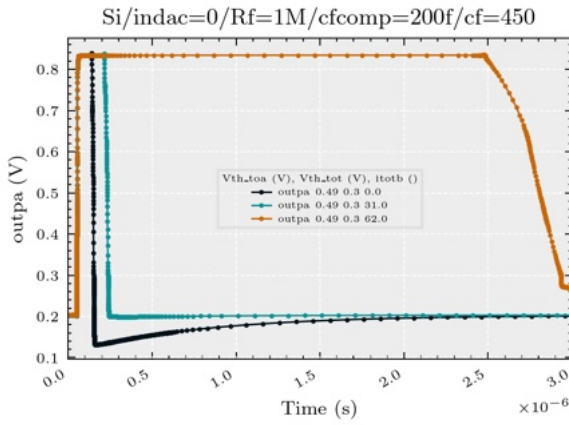


(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C

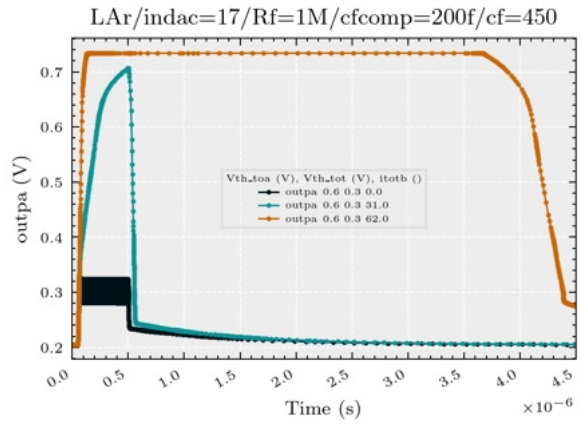


(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure II.20: ToT linearity with itot



(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C



(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure II.21: outpa signal with itot at 4.5 pC

The figures below (Fig. II.22) gives the simulated ToA.

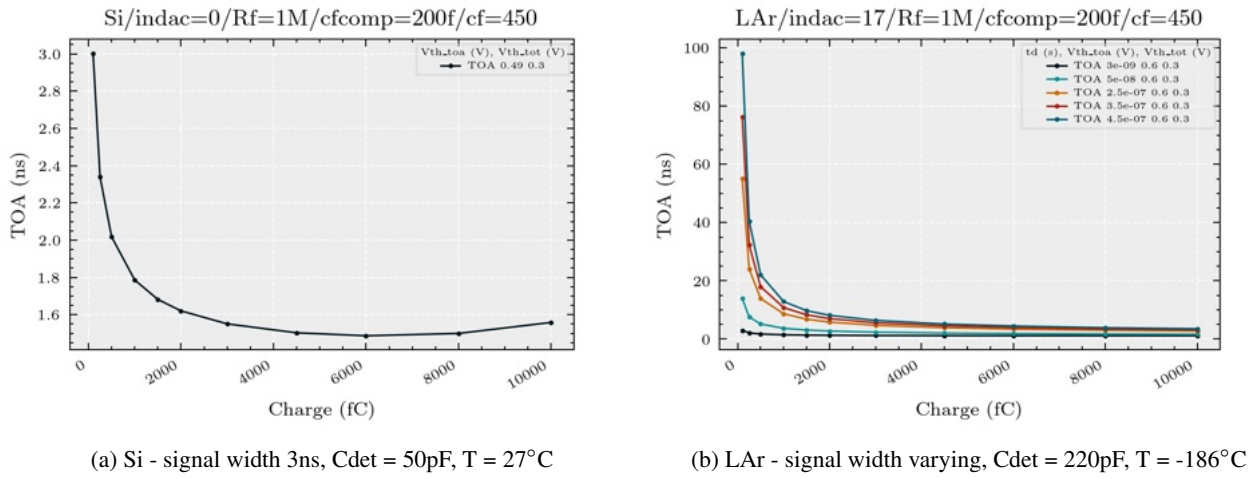


Figure II.22: ToA measurement

1.e Discriminators

There are two discriminators per channel, one for the ToT measurement, the other for the ToA.

The ToT discriminator is connected to the outpa output of the preamplifier (~200 mV). The ToA discriminator is connected to the outCf_pa output of the preamplifier (~500 mV). Two global 10b DACs allow the user to adjust the thresholds of the discriminators and two local trimming 5b-DACs allow to reduce the dispersion per channel. The 10b DAC have typically 1 mV LSB, the trimming 5b DAC have typically 0.25 mV LSB.

$$\begin{aligned} Toa_Threshold &= Toa_vref < 9 : 0 > - Trim_dac_toa < 4 : 0 > \\ Tot_Threshold &= Tot_vref < 9 : 0 > - Trim_dac_tot < 4 : 0 > \end{aligned} \quad (II.5)$$

There are two external trigger inputs available; typically, in the case when the user wants to calibrate the ToT and ToA, they can send a trigger for the ToA discriminator and the other for the ToT discriminator. They can also send a trigger for a channel, and the other for a neighbouring channel.

The two discriminators outputs can be masked per channel as well.

The following figure (Fig. II.23) shows the principle of the external trigger usage. The Trig1/2 are without effect when they are tied to 0: pull-down resistors have been placed to disable them by default. To send a trigger to a chosen channel, all the others must be masked.

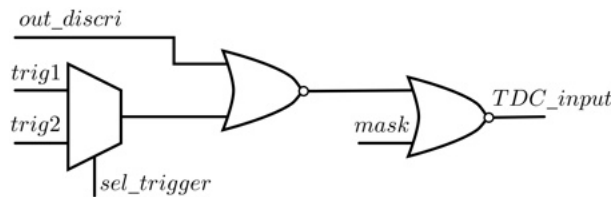
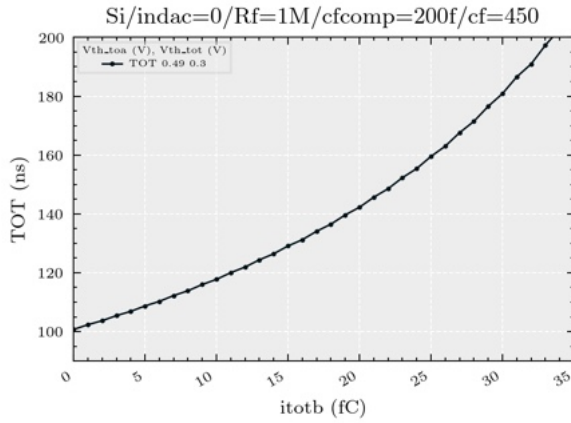


Figure II.23: External trigger

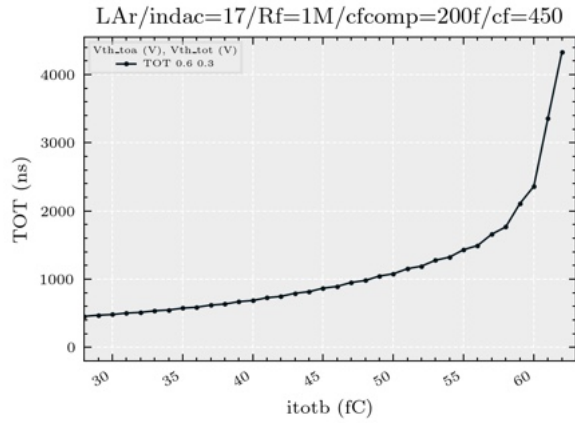
Regarding the ToT discriminator, when it is triggered (output at 0), it enables a constant current source which discharges the preamplifier so that the duration of the preamp signal is proportional to the input charge. This current source can be adjusted over 6 bits in order to adjust the width of the ToT.

The two discriminators outputs can be probed and looked at on a scope.

The following figure (Fig. II.24) shows the ToT duration at 4.5 pC injected charge as a function of the constant current itot.



(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C



(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure II.24: ToT as a function of itot

1.f Bias

All the bias are generated from the bandgap voltage so that the power consumption and DC values are less sensitive to temperature and power supply variations.

2 Mixed-signal blocks

2.a 10 bits ADC

The CALOROC1C ASIC contains a 10b SAR ADC (Fig. II.25) (successive-approximation ADC), designed by AGH in Kraków. The ADC's vrefm reference voltage is tied to ground.

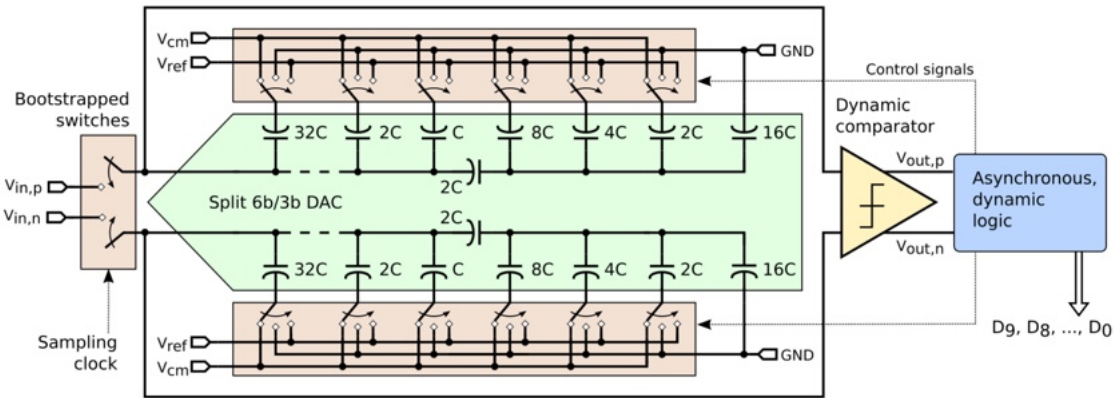


Figure II.25: Architecture of 10-bit SAR ADC

The 10 bits data provided by the ADC are sent to an Align Buffer to align them to the ToT and ToA data.

A mask can be applied channel-wise to the ADC which stops the clock. The asynchronous conversion delays can be globally adjusted over 3 bits.

2.b ToT and ToA TDCs

One TDC block handles the ToA and ToT measurements. It was designed by the CEA IRFU group in Saclay. The two following tables (Tab. II.7 and Tab. II.8) give the specifications respectively for the ToA and the ToT.

The architecture of the TDC is based on the time residue amplification method. It makes use of three main conversion blocks. A common **Gray counter** is used for the MSBs of all the channels. It is followed by a **Coarse TDC** (CTDC) based on an interpolator built using tapped delay line providing intermediate bits. The CTDC includes a pulse residue extractor. The residue is multiplied into a train of pulses by a **Pulse Replicator** (PR) and the resulting residual pulse train is sent to a residue integrator called **Fine TDC** (FTDC) that makes use of a DLL line to obtain the LSBs.

TDC ToA specifications	
Resolution	about 25 ps RMS
Range	10 bits over 25 ns
Conversion rate	> 40 MHz (bunch clock)
Power consumption	< 2 mW / channel (during conversion)
Area	Pitch 120 μm
Technology	TSMC 130 nm
Temperature	-40 to 40 $^{\circ}\text{C}$

Table II.7: TDC ToA specifications

TDC ToT specifications	
Resolution	< 50 ps RMS
Range	12 bits over 2-200 ns
Min time between hits	25 ns
Power consumption	< 2 mW / channel (during conversion)
Fixed latency	12 clock periods (200 + 100 ns)
Area	Pitch 120 μm
Technology	TSMC 130 nm
Temperature	-40 to 40 $^{\circ}\text{C}$

Table II.8: TDC ToT specifications

The schematic below (Fig. II.26) gives an overview of the TDC circuitry.

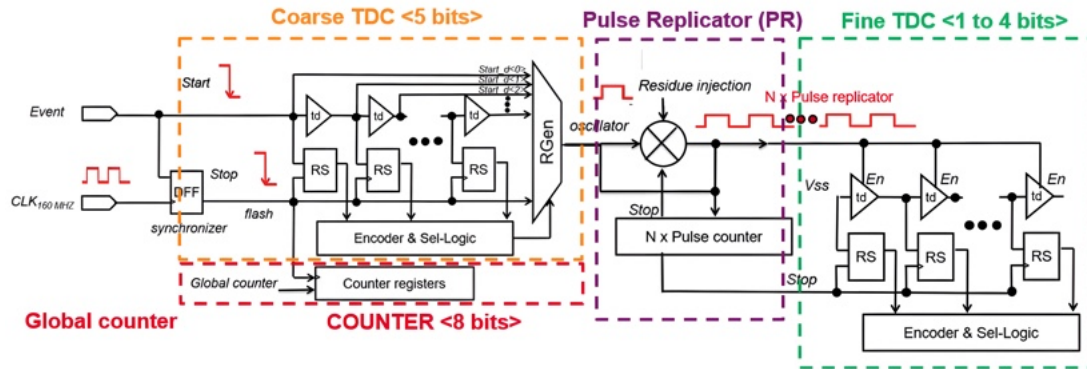


Figure II.26: TDC architecture

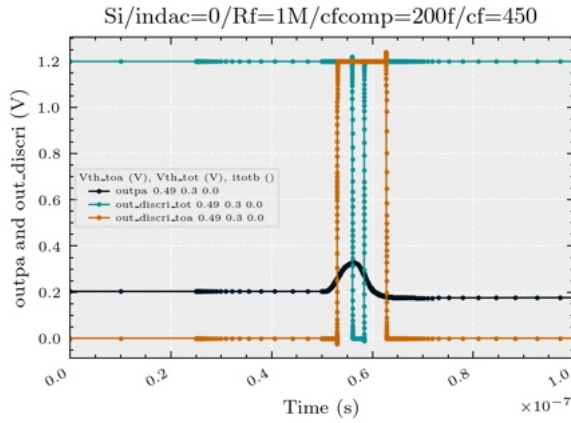
2.b.1 The Time of Arrival (ToA) TDC

For the ToA measurements, the start signal for the delay line of the CTDC is a digital signal generated by the discriminator of the analog front-end electronics (FEE) of the CALOROC1C chip. The propagation of the signal in the DLL is stopped with the next rising edge of the 160 MHz clock from the on-chip PLL. The thermometer code output obtained from the CTDC and the FTDC delay lines is then encoded and converted to the binary code.

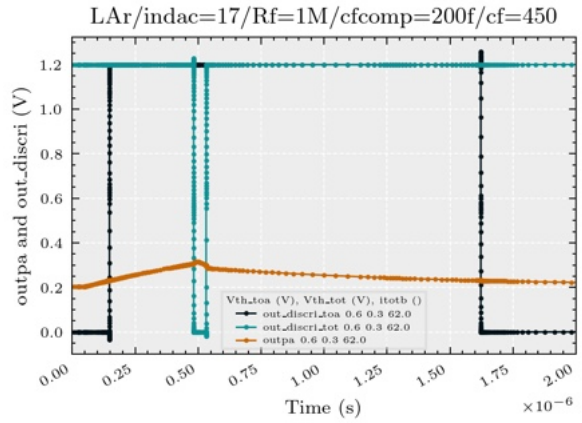
In principle, it can be available immediately after the conversion is finished. However, in the proposed architecture, it is required for the ToT measurement. To simplify overall design it is stored in the on-chip RAM memory when the ToT measurement is over.

2.b.2 The Time over Threshold (ToT) TDC

To measure ToT with a TDC, the analog input signal is compared with a programmable threshold (higher than the one used for the ToA) by the on-chip FEE. The pulse width of the resulting digital signal carries information about the deposited charge in the channel. The two following figures (Fig. II.27, Fig. II.28 and Fig. II.29) illustrate the ToT pulses respectively for 100 fC, 4.5 pC and 10 pC input charges.

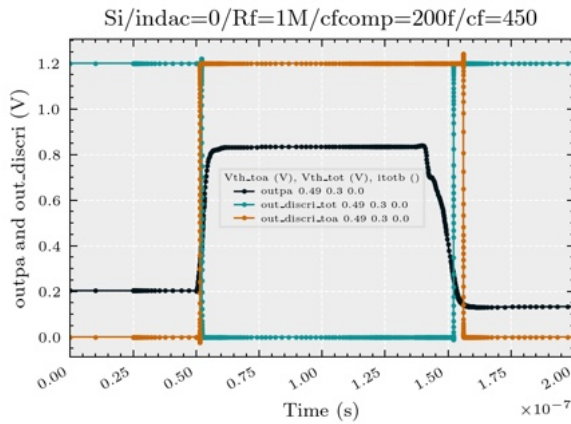


(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C

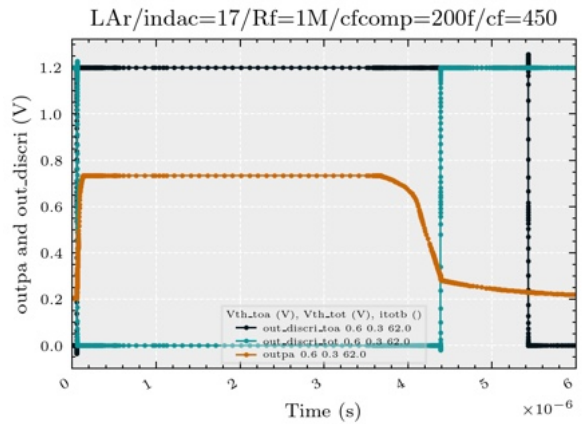


(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure II.27: ToT pulses - 100 fC

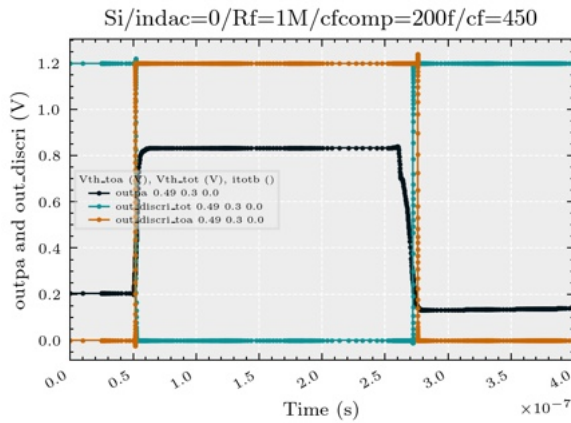


(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C

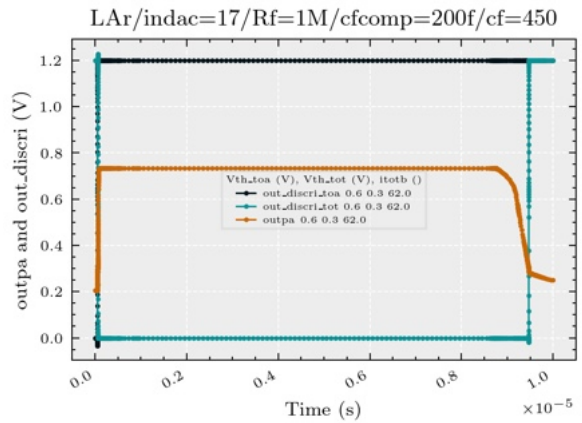


(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure II.28: ToT pulses - 4.5 pC



(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C



(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure II.29: ToT pulses - 10 pC

The shortest ToT interval to convert is about 2 ns. With an input charge up to 10 pC the duration of the longest ToT pulse is 200 ns. The conversion time of the ToA TDC is an order of magnitude longer than the specified 2 ns. Therefore, the same TDC cannot be used to convert arrival times of the leading and trailing edges of the ToT pulse.

The proposed solution for the ToT is to use the ToA measurement to mark the ToT rising edge and to use a dedicated TDC to measure the time of the falling edge of the ToT signal. The difference between the two times will give the ToT duration (Fig. II.30). The following figure (Fig. II.31) shows the proposed architecture for the ToA and ToT measurements.

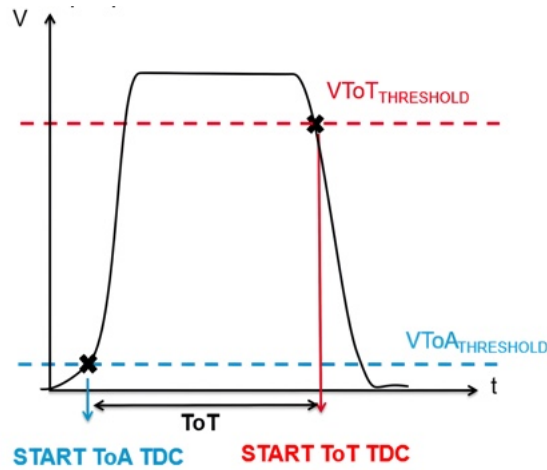


Figure II.30: Proposed method for the ToA and ToT measurements

Clearly, this architecture can be used only for a step rising edges of the input analog signals for which the time difference between the crossing points of the ToA and ToT thresholds can be neglected. According to the frontend simulations, this is the case for the typical charge deposits that generate ToT signals.

The rising edge of the ToA discriminator initiates ToA measurements. The second TDC, named ToT TDC, is activated only when the ToT discriminator detects the falling edge of the analog signal. Upon an active high signal from the discriminator, it measures the time of the falling edge of the signal delivered by the ToT discriminator.

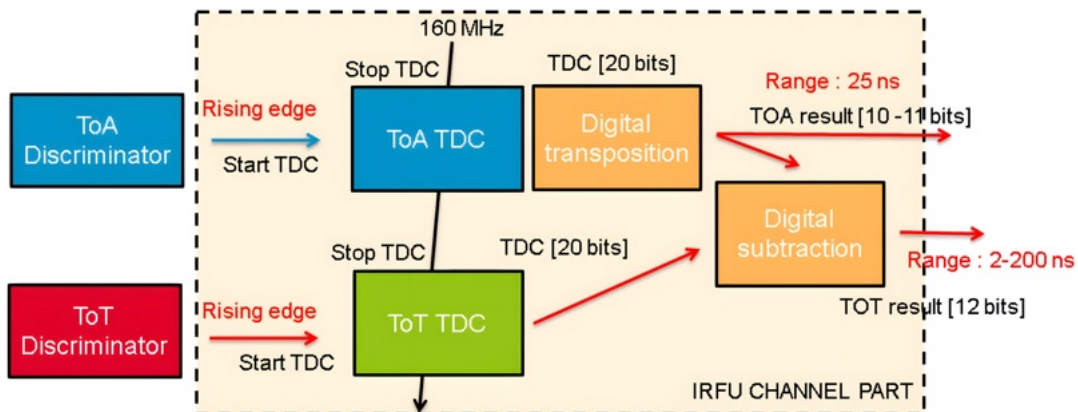


Figure II.31: Proposed architecture for the TOA and TOT measurements

The ToA value is obtained directly from the ToA TDC measurement after a digital transposition in 10 or 11 bits. The ToT value is obtained from the digital subtraction of the ToT TDC measurement from the ToA TDC measurement. Eventual overflows are detected and marked with all bits set in the ToT results.

The ToT result is valid during one 40 MHz clock period and is written to the on-chip RAM. For non-ToT events, the RAM is filled with the all-zero code.

2.b.3 Synchronisation

The ADC values are available immediately after conversion, as are those of the ToA TDC. However, as described above, the ToT interval may vary from 2 to 200 ns. The on-chip Trigger unit requires the ADC and the ToT measurements to be present simultaneously at the same rising edge of the on-chip PLL 40 MHz clock. To achieve the synchronisation, the ToT logic guaranties that the ToT measurement will be available after a fixed number of clock periods starting from the ToA discriminator rising edge. With today's assessment of the ToT logic performance, the fixed ToT latency is determined to be **200 ns + 100 ns corresponding to 12 (8+4) clock periods**.

2.b.4 Pileup effect

Taking into account the discharge time of the analog part, the minimal time between two consecutive ToT events can be as low as 50 ns. During the 300 ns ToT latency, several other charge deposits may occur within the same channel (Fig. II.32). The design guarantees that the ToT will be measured for all of them (Fig. II.33).

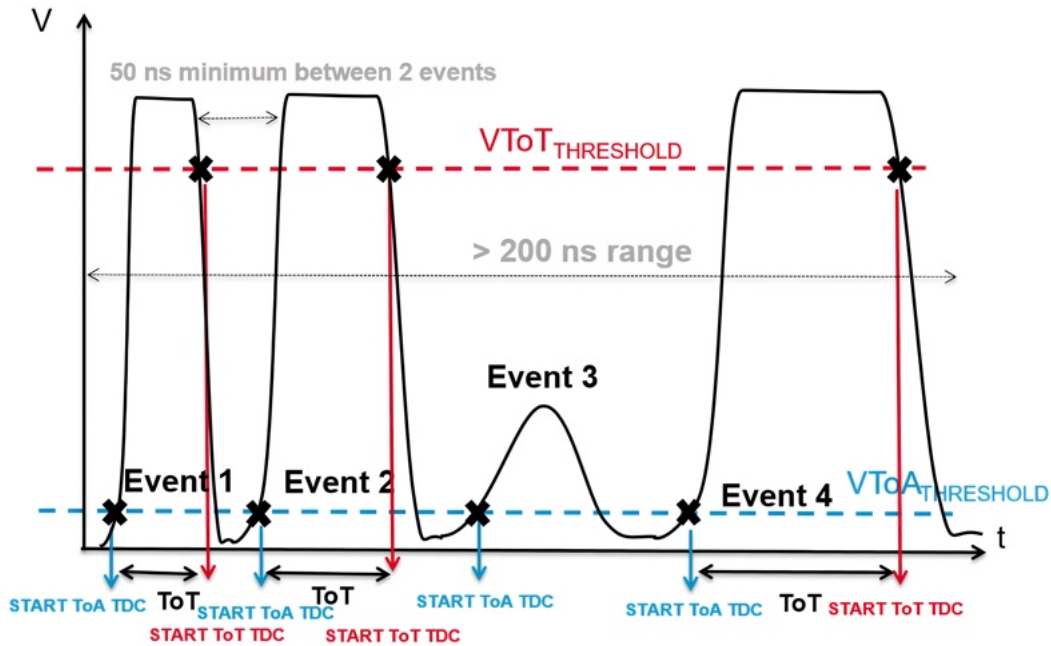


Figure II.32: Signal pileup during the ToT latency

According to the proposed design, after a ToA hit, the ToA is measured and stored into a ToA FIFO and a counter is started to count 12 40 MHz clock cycles. This creates a so-called ToA latency window to wait for a possible ToT discriminator signal, to measure its arrival time and to store it into the corresponding ToT FIFO. Note that this latency can be tuned by SC (0 to 15 clock cycles).

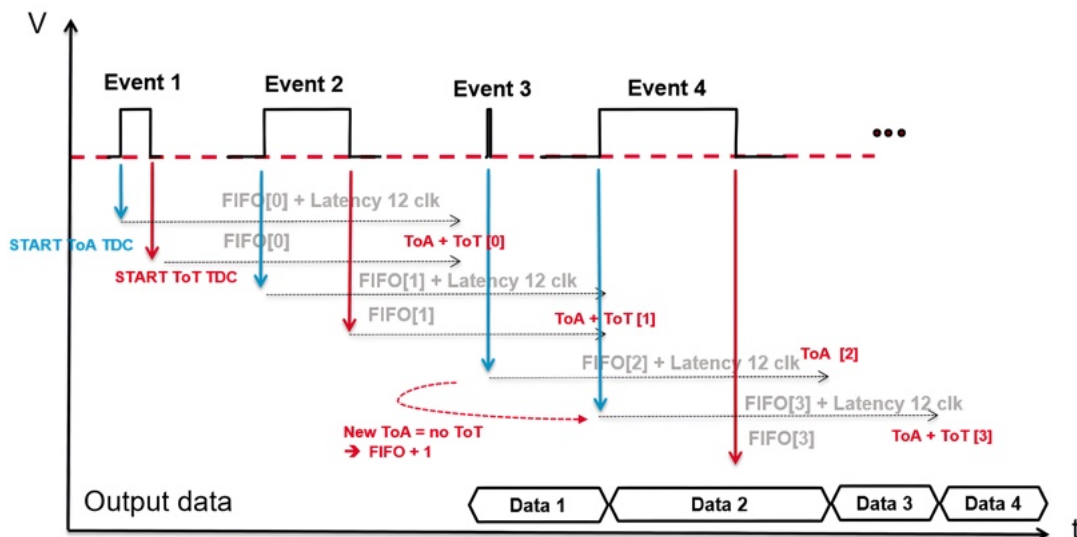


Figure II.33: Diagram demonstrating the overlap of multiple events in a sequence

At the end of the 12-cycle count, the ToT is obtained reading the ToA and ToT FIFOs and subtracting one from another. Per-channel subtraction logic is based on asynchronous gates that accomplish the operation within a 5-ns delay. After that, the ToA and ToT results are sent to the on-chip RAM where they are associated with the channel ADC measurement.

If there is no ToT hit during the ToA latency window, the ToT measurement logic is not activated and the ToA data is accompanied by a "0" code to indicate the absence of the ToT information.

If a new ToA/ToT event occurs during an active pending ToA[n-1] latency window, the new ToA[n] measurement is appended to the FIFOs, a new latency counter is started and the ToA[n] latency window is initiated.

If, within an active ToA[n-1] latency window, a ToA[n-1] hit is followed by another ToA[n] hit, rather than the ToT hit, this means that the charge deposit within the event [n-1] was not high enough to trigger the ToT discriminator. The "0" ToT code is appended to the ToT FIFO and the new ToA[n] latency window is started.

The ToA and ToT FIFO depth is determined by the fixed ToT latency of 300 ns and the 25 ns minimum time between the ToA: $300 \text{ ns} / 25 \text{ ns} = 12$. Ideally, the FIFOs need to store 12 ToA and ToT measurements and there should be 12 counters in the pool. However, with the expected channel occupancies, a long train of consecutive events has sufficiently low probability to reduce the FIFO depth. For simplification, a power of two logic is used and the 8-entry deep FIFOs implemented together with 8 counters. In case of overflows, events are lost without blocking of the ToA /ToT TDC circuitry.

The block diagram of the latency counter and FIFO architecture for the ToA and the ToT measurements is presented in the next figure (Fig. II.34).

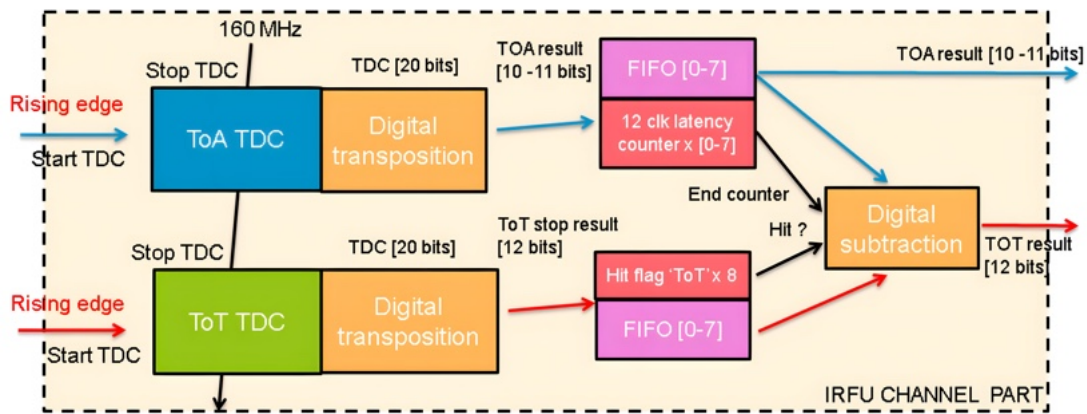


Figure II.34: block diagram of the latency counter and FIFO architecture for the ToA /ToT measurements

In addition, a data ToA/ToT debug mode is implemented. It allows reading of the 20-bit "raw" (non- transposed) data of the ToA and ToT TDCs.

2.b.5 Two consecutives TOT events

In case of high rate pileup, the preamplifier output signal may not return to its baseline after a ToT event when a new charge arrives. In this case, a second ToT may appear without the ToA threshold being crossed as shown on the next figure (Fig. II.35).

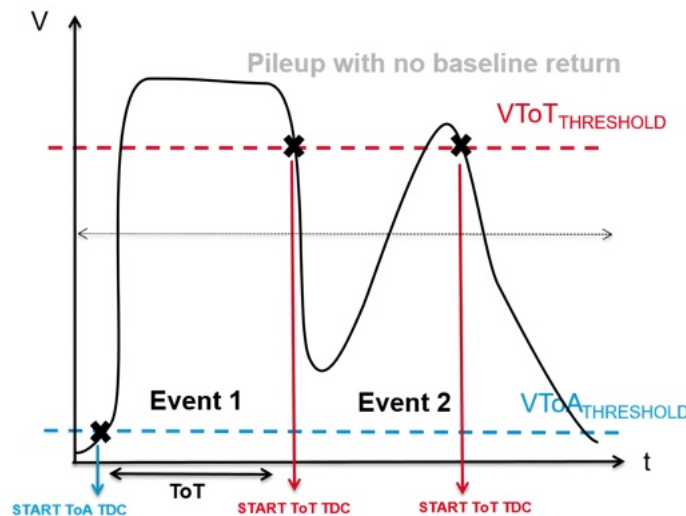


Figure II.35: Signal pileup during the ToT latency

In the current implementation the second ToT event, which does not have corresponding to its ToA event, will be ignored.

2.c Align Buffer

The 10 bits data provided by the ADC are sent to an Align Buffer to align them to the TOT and TOA data. Indeed, the TDCs providing the TOT measurement introduce a latency due to the duration of the TOT itself. The ADC + Align Buffer have a fixed latency of 11 Timestamp: sampling at Timestamp = 1, ADC data available at Timestamp = 2, data at the Align Buffer outputs at Timestamp = 11 (see next timing diagram II.36).

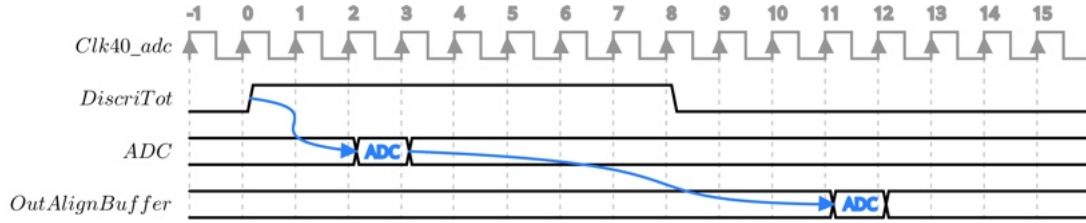


Figure II.36: Align Buffer timing diagram

The AlignBuffer block provides:

- The ADC raw data for the DAQ path.
- The Tot_in_progress flag for the DAQ path. It is equal to 1 as long as the analog shaper output is corrupted by a TOT event: saturation and undershoot.
- The pedestal subtracted ADC data for the Trigger path. The pedestal value is adjustable channel-wise.

The user can choose to force ADC data to 0 when the TOT pulse is at 1 (Clr_ADC = "1"), otherwise it provides the actual ADC values.

As after a TOT the shaper returns to the pedestal after a given time, the user can also choose to force ADC data to 0 for two next Timestamp after the end of the TOT pulse (Clr_ShaperTail = "1").

A mask is also available channel-wise to stop the clock and so the digital activity of the Align Buffer.

The edges of the "analog" 40 MHz clock can be selected and so the phase to send Align Buffer data to the RAM.

External ADC data can be forced, half-wise, configurable by slow-control, this mode is in particular interest for the DRAM tests.

The TDC block provides also the aligned TOA and TOT data with an internal align buffer.

3 Ancillary blocks

3.a PLL and clocks distribution

The main specifications of the PLL are described in the following table (Tab. II.9)

PLL specifications	
Input frequency	40 MHz (bunch clock)
Output frequencies	1.28 GHz and 640, 320, 160 MHz
Jitter cleaner	Low jitter < 15 ps RMS (for an input jitter of 30 ps RMS)
Power consumption	1.91 mW
Area	Pitch 120 μm
Technology	TSMC 130 nm
Temperature	-40 to 40 $^{\circ}\text{C}$

Table II.9: PLL specifications

The jitter cleaner and clock synthesiser PLL provides a set of on-chip clocks with frequencies varying from 40 MHz to 1.28 GHz, all phase aligned to its 40 MHz input clock. It consists of a low noise digital phase frequency detector (PFD), a precision charge pump, a loop filter, a voltage-controlled oscillator (VCO) and prescale dividers (Fig. II.37).

During the normal operation the 40 MHz PLL input clock is derived by the on-chip Fast Command unit receiving a 320 MHz clock on its fast command interface. For test purposes, the pinout of the DV1 version of the CALOROC1C ASIC foresees a pair of input pins dedicated to a differential 40 MHz clock. The chip can be programmed to feed this external

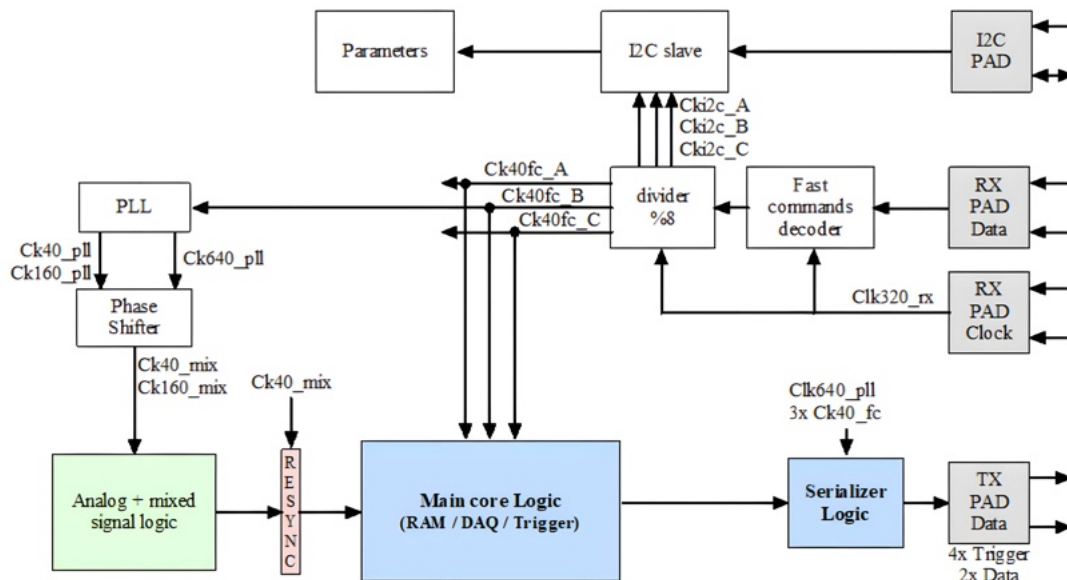


Figure II.37: PLL architecture

clock to the PLL. Also the chip pinout fixes a dedicated differential signalling output in order to evaluate the quality of the PLL generated clocks. For power supply, the PLL must have its own power supplies and reserved pads (VDD and VSS).

The chip only receives the Fast-Command link made of the 320 MHz fast command and the 320 MHz clock. The FastCommand block decodes the fast command and the 40 MHz clock. This 40 MHz clock is used for the I2C block, all the FSMs, the counters, the two RAMs, the wr/rd pointers and is the PLL reference clock. Only hard resets (ReHb and RESb) allows to stop or restart this clock by resetting the FastCommand block.

The FCU decodes the 40 MHz clock from the 320 MHz links. The 40 MHz clock for the I2C is directly divided from the 320 MHz clock input, so that the chip can be configurable even if it does not receive any fast commands. The 40 MHz clock for all the others parts (digital, PLL, mixed) are decode from both 320 MHz and FastCommand links, so that the chip needs correct fast command to provide this clock.

The PLL takes as reference the 40 MHz clock provided by the FastCommand block. The PLL can only be reset by the hard resets (ReHb and ReSb). The PLL generates three clocks: clk_40M_pll, clk_160M_pll, clk_640M_pll:

- clk_40M_pll: this clock comes in a Phase Shift block to achieve the ADCs clock.
- clk_160M_pll: this clock comes in a Phase Shift block to achieve the TDCs clock.
- clk_640M_pll: this clock comes in the SerDes of the E-links.

3.b Bandgap and voltage references

Typically, the bandgap provides an output voltage of around 280 mV. This value needs to be multiplied to get a usable voltage reference around 1 V. From the bandgap voltage, a V_{bg} -based current is provided as well (Fig. II.38).

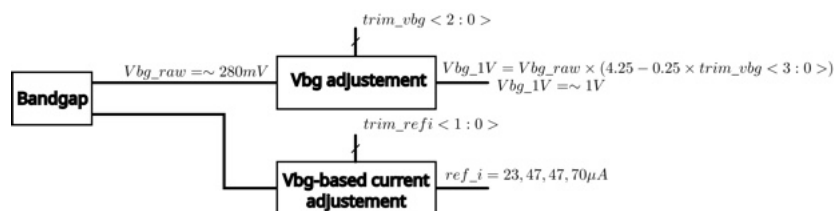


Figure II.38: Bandgap voltage and current

The Vbg_1V is used to generate the upper reference voltage of the Calibration 12b-DAC, the reference voltage of the ADCs, ref. voltage for the TDCs, bias. The ref_i reference current is used to generate the offset and the steps of the 10b-DACs.

Four global 10 bits DACs provide voltage references for the analog part: the two discriminator thresholds, the inverted and non-inverted references for the shaper.

The outputs voltage values of a preamplifier, similar to the PA of the classical channel (extra PA added in the Bias block), is used to give these voltage references. This is done to make the chip not sensitive to the temperature. So all the references follow the preamplifier input DC value.

3.c Calibration circuit

The following scheme (Fig. II.39) shows the circuitry of the CALOROC1C calibration DAC. It is a 12-bits DAC, the calibration DAC ground is connected to the preamplifier grounding to avoid offset due to current leakage. Moreover, another source of offset is the gate leakage current of the switches (HighRange and LowRange) into each channels, the offset should be lower than 1 fC for $N = 1$ and 2 fC for $N = 40$ (with N the number of enabled injection capacitances).

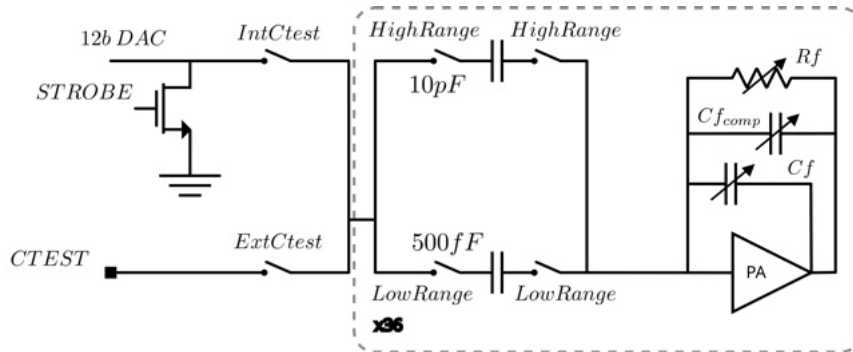


Figure II.39: Calibration circuit

Assuming the 12b-DAC provides a voltage up to around 1 V (the bandgap value), the user may set 0.5 pF and/or 10 pF injection capacitances in the chosen channels, to study the 0 – 0.5 pC range, the 0 – 10 pC range or, by setting both capacitances, the 0 – 10.5 pC range. To correctly calibrate the ADC/TOT behaviour, it is important to have an overlap between the available charge ranges.

The ctest node comes from an external pad and allows the user both to use an external pulser rather than the calibration DAC and also to calibrate the calibration 12b-DAC.

The calib fast command lasts 1 clock cycle but the STROBE pulse lasts more than 10-12 clock cycles to not inject the opposite charge at Timestamp+1. A counter (6 or 7 bits at 320 MHz) is implemented to achieve this.

The phase of the STROBE pulse with respect to the 40 MHz clock is adjustable by a delay of 1.56 ns.

A CalExt fast command sends a STROBE pulse to a pin.

A CalInt fast command sends a STROBE pulse to the internal CalibDAC.

3.d Monitoring

The internal DACs outputs (calibration, reference voltages and current DAC) are multiplexed as described in the figure (Fig. II.40). The signals will be sent to the ADC of the SCA chip. All the monitored points are in the 1.2 V range.

On probe_dc1, there are 64 available monitoring points.

If cmd_probe_dc1<0> is set, the next 32 voltages are accessible (Tab. II.10).

If cmd_probe_dc1<1> is set, the next 32 voltages are accessible (Tab. II.11).

If cmd_probe_dc1<1:0> are not set, the probe_dc1 is in high impedance so that several probes can be tied together on the modules.

If cmd_probe_dc2 is set, the calibration dac output is sent to probe_dc2.

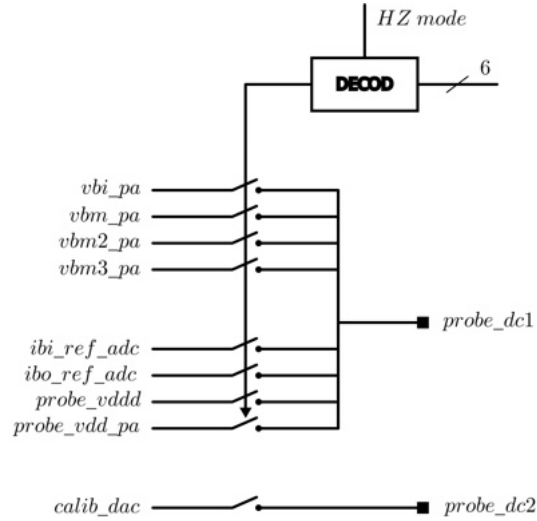


Figure II.40: Schematic of the monitoring scheme

Address	Probe Point	Nominal Value	Comment
0	vbi_pa	0.42	tunable over 4b (dac_vbi_pa)
1	vbm_pa	0.6	
2	vbm2_pa	0.4	
3	vbm3_pa	0.13	
4	vbo_pa	0.4	tunable over 3b (dac_vbo_pa)
5	vb_inputdac	0.3	tunable over 3b (indac)
6	vbi_discr_tot	0.8	
7	vbm_discr_tot	0.8	
8	vbo_discr_tot	0.16	
9	vbi_discr_toa	0.34	
10	vcasc_discr_toa	0.97	
11	vbm1_discr_toa	0.8	
12	vbm2_discr_toa	0.8	
13	vbo_discr_toa	0.44	
14	EXT_REF_TDC	0.1	
15	probe_VrefCf	0.43	equal to the ToA discr input DC
16	vcn	0.65	
17	VD_FTDC_P_EXT	0.07	
18	VD_CTDC_P_EXT	0.07	
19	probe_VrefPa	0.174	equal to the preamp output DC
20	vcp	0.65	
21	VD_FTDC_N_EXT	0.19	
22	VD_CTDC_N_EXT	0.19	
23	vb_hyst_tot	0.46	
24	vbi_itot_neg	0.65	ToT gain, tunable over 6b (dac_itot)
25	vbi_itot_pos	0.002	ToT gain, tunable over 6b (dac_itot)
26	vbiN_sk	0.3	tunable over 2b (ibi_sk)
27	vbiP_sk	0.81	tunable over 2b (ibi_sk)
28	vbFCN_sk	0.31	tunable over 6b (dac_sk)
29	vbFCP_sk	0.81	tunable over 6b (dac_sk)
30	vbiN_noinv	0.3	tunable over 2b (ibi_noinv)
31	vbiP_noinv	0.77	tunable over 2b (ibi_noinv)

Table II.10: Voltage accessible with cmd_probe_dc1<0>

Address	Probe Point	Nominal Value	Comment
0	VbFCP_noinv	0.3	tunable over 6b (dac_noinv)
1	VbFCN_noinv	0.81	tunable over 6b (dac_noinv)
2	vbiN_inv	0.3	tunable over 2b (ibi_inv)
3	vbiP_inv	0.81	tunable over 2b (ibi_inv)
4	vbFCN_inv	0.31	tunable over 6b (dac_inv)
5	vbFCP_inv	0.81	tunable over 6b (dac_inv)
6	vbiN_noinv_buf	0.33	tunable over 2b (ibi_noinv_buf)
7	vbiP_noinv_buf	0.77	tunable over 2b (ibi_noinv_buf)
8	vbFCN_noinv_buf	0.37	tunable over 6b (dac_noinv_buf)
9	vbFCP_noinv_buf	0.72	tunable over 6b (dac_noinv_buf)
10	vbiN_inv_inv_buf	0.33	tunable over 2b (ibi_inv_buf)
11	vbFCP_inv_buf	0.72	tunable over 6b (dac_inv_buf)
12	vbiP_inv_buf	0.77	tunable over 2b (ibi_inv_buf)
13	vbFCN_inv_buf	0.37	tunable over 6b (dac_inv_buf)
14	vb_5bdac_out_inv	0.68	tunable over 3b (idac_inv)
15	vb_5bdac_tot	0.72	tunable over 3b (idac_tot)
16	vb_5bdac_toa	0.72	tunable over 3b (idac_tot)
17	vcm_0p6_inv	0.58	
18	vcm_0p6_noinv	0.58	
19	vrefp_adc	1.15	
20	vcm_adc	0.56	
21	Vref_sk	0.173	
22	Vref_noinv	0.237	tunable over 10b (Vref_noinv)
23	Vref_inv	0.463	tunable over 10b (Vref_inv)
24	Vref_tot	0.392	tunable over 10b (Vref_tot)
25	Vref_toa	0.49	tunable over 10b (Vref_toa)
26	probe_vbg_1V	1.1	tunable over 3b (vbg_1V)
27	probe_center	0.5	VOUT_INIT_EXT
28	ibi_ref_adc	1.01	tunable over 2b (b_ref_adc)
29	ibo_ref_adc	0.79	
30	probe_vddd	0.58	
31	probe_vdd_pa	0.58	

Table II.11: Voltage accessible with cmd_probe_dc1<1>

If cmd_probe_dc1, cmd_probe_dc2, cmd_tes_D and cmd_test_G are set, the next 21 transistors can be tested (Tab. II.12), they are chosen with the address addr_test_t<4:0>. The drain (D) is sent to probe_dc2 and the gate (G) is sent to probe_dc1, those two probes should be enough to fully characterise the transistors.

For 21 transistors belong to:

Two types:

- PMOS (p-channel MOSFET): conducts when the gate voltage is low relative to the source.
- NMOS (n-channel MOSFET): conducts when the gate voltage is high relative to the source.

Four subtype:

- No special subtype (normal).
- lvt - Low-Voltage Threshold.
- hvt - High-Voltage Threshold.
- na - Native - Near-Zero Threshold.

Three sizes:

- small - $L = 130 \text{ nm}$ & $W = 2 \text{ }\mu\text{m}$ - usual size of the digital.
- medium - $L = 500 \text{ nm}$ & $W = 10 \text{ }\mu\text{m}$ - usual size of the analog.
- large - $L = 250 \text{ nm}$ & $W = 2 \text{ }\mu\text{m}$ & 10 fingers & $\times 150$ - usual size of the input transistor of the preamplifier.

Address	Type	Subtype	Size
0	pmos		small
1	pmos		medium
2	pmos		large
3	pmos	lvt	small
4	pmos	lvt	medium
5	pmos	lvt	large
6	pmos	hvt	small
7	pmos	hvt	medium
8	pmos	hvt	large
9	nmos		small
10	nmos		medium
11	nmos		large
12	nmos	lvt	small
13	nmos	lvt	medium
14	nmos	lvt	large
15	nmos	hvt	small
16	nmos	hvt	medium
17	nmos	hvt	large
18	nmos	na	small
19	nmos	na	medium
20	nmos	na	large

Table II.12: Transistors accessible with `cmd_test_D` and `cmd_test_G`

3.e eFuse

Serial number over 31 bits can be written inside each chip by burning e-fuses. Actually there are 32 e-fuses inside the chip, but the two last MSB, bit<31> and bit<30>, are hard-wired to 0 and to 1 respectively, furthermore the MSB, bit<31>, cannot be read. So in fact the range of the serial number goes from 0x4000 0000 to 0x7FFF FFFF (1 073 741 823 combinations).

The serial number has to be first written into registers R9[7..0], R11[7..0], R13[7..0] and R15[5..0] of Top sub-block before being burned bit per bit following the procedure described below (Fig. II.41, II.42, II.43, II.44 and II.45).

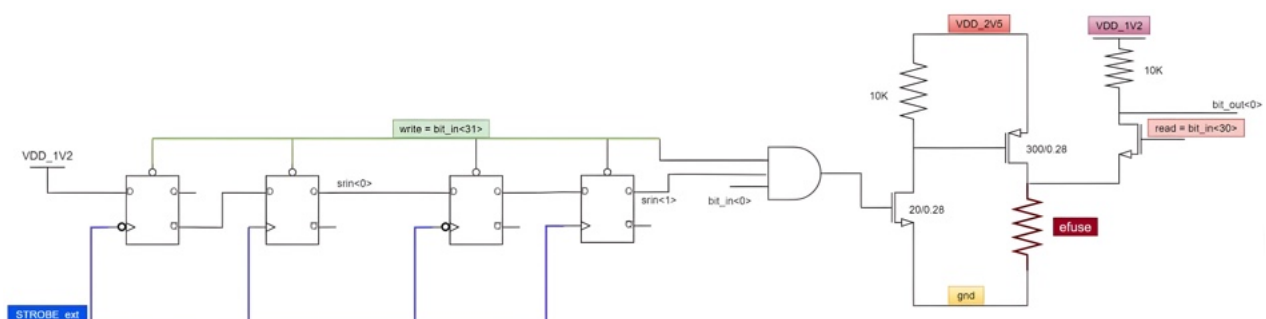
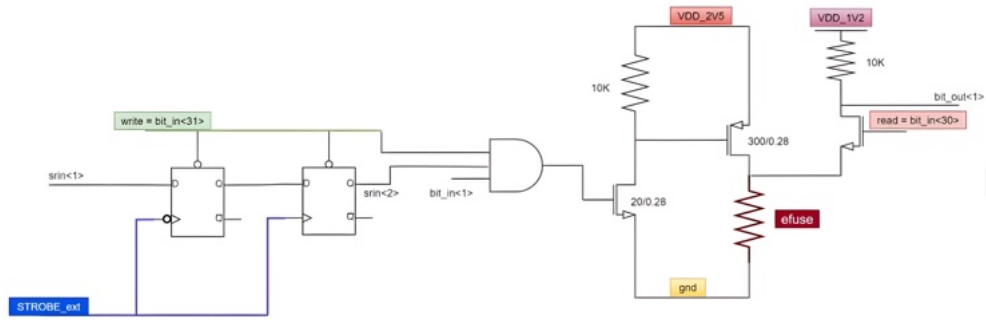
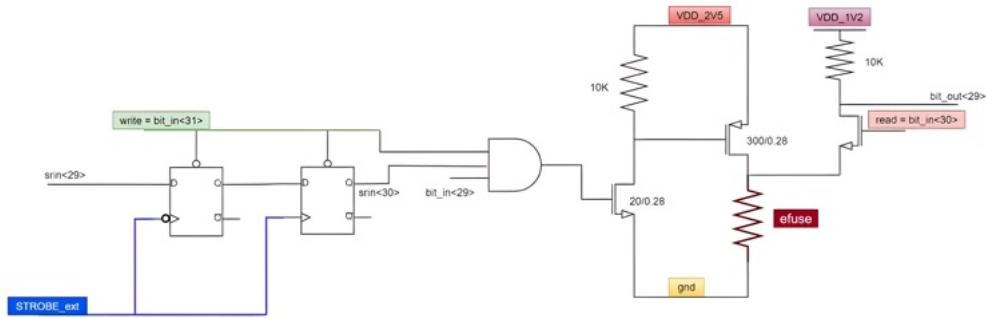
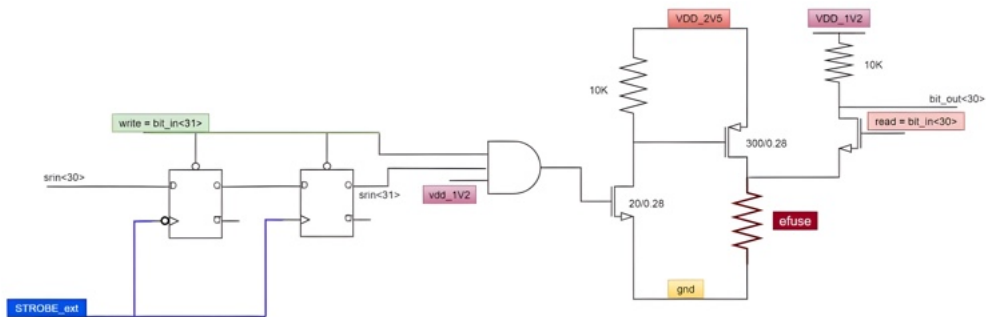
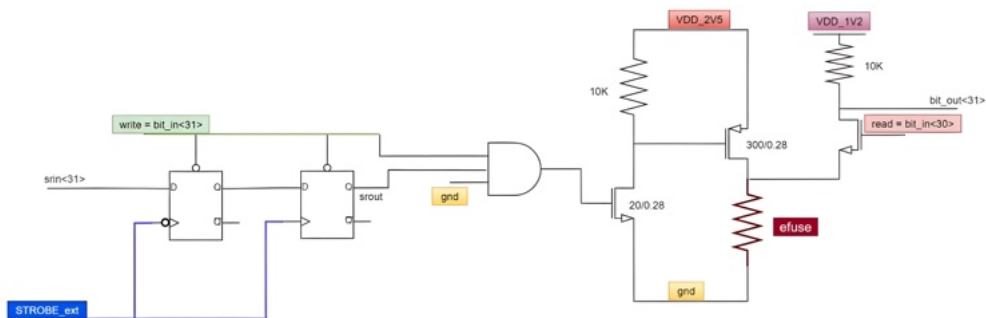


Figure II.41: eFuse procedure for *bit_out* < 0 >

Once the serial number is written inside registers R15[5..0], R13[7..0], R11[7..0], R9[7..0] of Top sub-block, R15[7] has to be set to 1 so that the write permission is enabled, 2.5 V has to be provided from the eFuse pin. And then a 33-pulses train has to be provided on the pin STROBE_ext which must start and finish to 0 as showed in the timing diagram below (Fig. II.46).

Figure II.42: eFuse procedure for $bit_out < 1 >$ Figure II.43: eFuse procedure for $bit_out < 29 >$ Figure II.44: eFuse procedure for $bit_out < 30 >$ Figure II.45: eFuse procedure for $bit_out < 31 >$

In order to read the serial number back, R15[6] of Top sub-block has to be set to 1 to enable the read permission, and then each bit is connected, LSB first, into R8[0..7], R10[0..7], R12[0..7] and R14[0..6]. No matter the value on the eFuse pin: 0 V, 2.5 V or floating. The bit R14[7] gives the state of the srout net of the figure above, only for debug purpose.

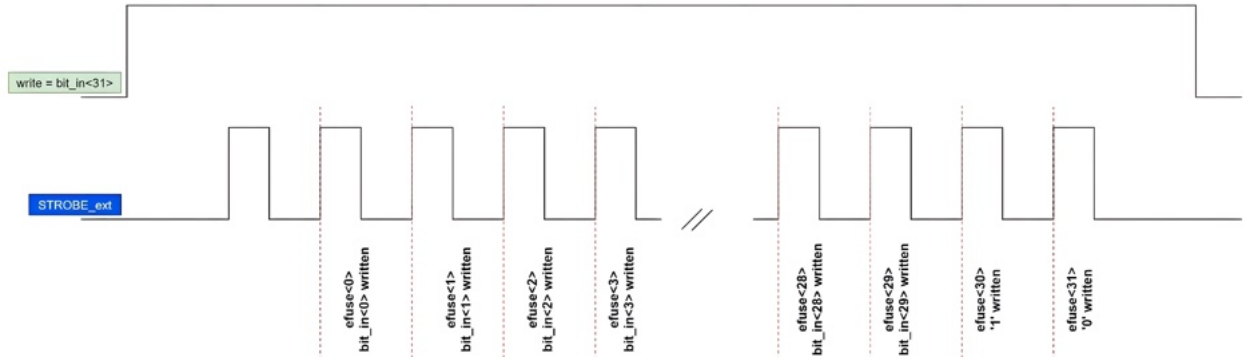


Figure II.46: Procedure to write the serial number

3.f Random Clock Generator (RCG)

A Random Clock Generator (Fig. II.47) has been implemented in order to calibrate the TDCs. This block generates a clock whose frequency is not synchronised with any clocks inside the chip so that the code distribution can be produced. From this code distribution, the INL and DNL can be extracted offline.

By default, the RCG is disabled and off.

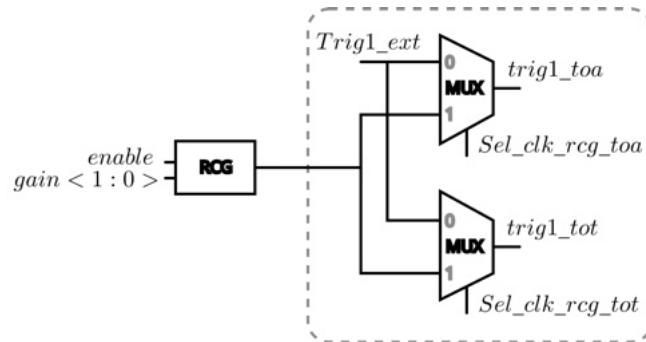


Figure II.47: RCG Slow Control

For triggering a TDC, the user has to select sel_trigger_toa/tot (channel_wise) of the channel, enable the RCG (Top sub-block) and select RCG as external trigger with Sel_clk_rcg_toa/tot parameter (MasterTDC sub-block).

PART III

DIGITAL PROCESSING

1 Overview

CALOROC integrates 36 channels with charge and time measurements. Digitised data are readout through 2 high speed serial links at 1.28 Gbps (each link readout 18 channels respectively).

As shown in the figure below (Fig. III.1), the ASIC has 3 main digital interfaces:

- 1x I2C interface to change the ASIC parameters,
- 1x Fast command interface which generate internal commands and clocks,
- 2x 1.28 Gbps serial data transmitter (ASIC outputs).

These interfaces are described in the next section (Section 2).

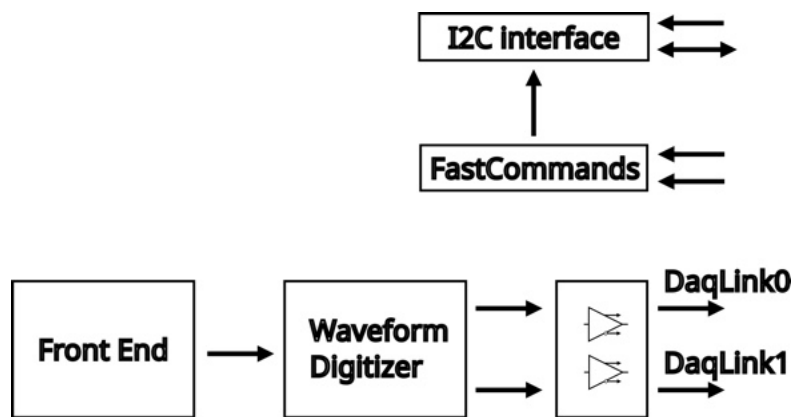


Figure III.1: The overview of the digital processing

2 Control interface blocks

2.a Fast Command

The Fast Command Unit (FCU) is responsible for generating internal fast commands. The table below (Tab. III.1) details each command along with its associated latency. Latency is defined as the delay between the reception of the last bit in the 320 Mbps bitstream and the issuance of the command to configure a specific operating mode of the system. Latency is expressed in clock cycles of the synchronised 40 MHz clock, which is generated internally by the FCU.

The FCU requires 3 clock cycles (at 40 MHz) to decode a command; therefore, the minimum achievable latency is 3 clock cycles.

Command	Code	Description	Total latency with FC
CMD_IDLE	00110110	Allow to generate the main internal 40MHz clock. It's derived from the 320MHz and aligned with bit 4 of incoming command.	
CMD_L1A	01001011	Acts as an internal triggering for all the channels: forcing timestamp and all ADCs-TOAs to be stored in the internal memories.	3+6 clock cycle at 40 MHz.
CMD_CALPULSEINT	00101101	Send a Calibration Pulse of 32 x 40 MHz clock period.	3+1 clock cycle at 40 MHz.
CMD_CALPULSEEXT	01111000	Send a Calibration Pulse of 4 x 40 MHz clock period.	3+1 clock cycle at 40 MHz.
CMD_CHIPSYNC	11010010	Reset all Digital FSM. Does not reset analog part (PLL) and the FCU.	3+1 clock cycles at 40 MHz to reset Startup FSM to idle state.
CMD_EBR	11010001	Reset the buffer pointer of FIFO and the event counter.	3+1 clock cycle at 40 MHz.
CMD_BCR	00011101	Reset the Timestamp to its default value (parameter TimeOffset).	3+1 clock cycle at 40 MHz.
CMD_PING	10011001	Replace an IDLE by an IDLE_ping.	Fixed
CMD_LINKRESETROCD	10011010	Link Sync: Upon completion of the current packet, 400 IDLEs are forced on the links.	The link is reset immediately if the readout is finished.
ROC_SERIALIZER_RESET	10011100	Link Reset: Reset all Serializers, it does a bit alignment for all of them. The chip loses links during 14 clock cycles at 40MHz.	1 clock cycle at 40 MHz to reset and 14 clock cycles at 40 MHz to recover links.
SlowControl_bit0 SC_0	01011010	Send 0 for the I2C over fast command module.	
SlowControl_bit1 SC_1	01011100	Send 1 for the I2C over fast command module.	
SlowControl_bit2 SC_2	10001011	Send 2 for the I2C over over fast command (reset if 2 consecutive).	

Table III.1: The Fast Command details

The fast command bit stream (command_rx Fig. III.2), clocked at 320 MHz, defines the phase relationship between internal 40 MHz lock and the 320 MHz clock as shown below.

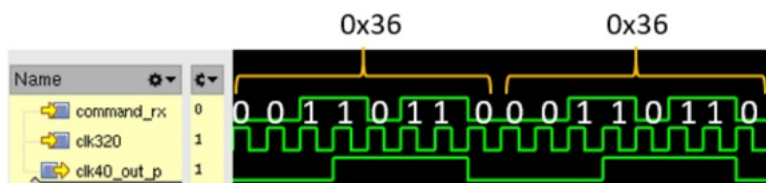


Figure III.2: Internal clock phase relationship with external clock

CMD_EBR (Fig. III.3) resets the memory RAM.

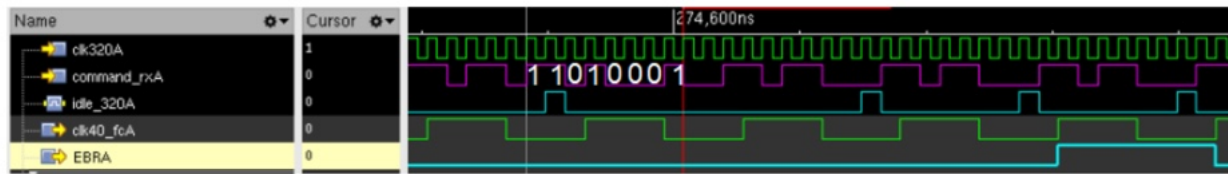


Figure III.3: Example of an internal fast commands decoding (CMD_EBR)

CMD_CALPULSEINT: send a STROBE pulse of 800 ns to the internal calibration DAC. The STROBE pulse phase depends on the main digital clock from Fast Commands module (clk40_fc) (Fig. III.4).



Figure III.4: Detail of the Calibration pulses fast commands: CMD_CALPULSEINT

CMD_CALPULSEEXT: send a STROBE pulse of 100 ns to the external pin SiPM_calibration. The STROBE pulse phase depends on the main digital clock from Fast Commands module (clk40_fc) (Fig. III.5).



Figure III.5: Detail of the Calibration pulses fast commands: CMD_CALPULSEEXT

2.b ASIC parameter access with I2C

I2C protocol is used to access ASIC parameters: SDA and SCL pins are dedicated to this. A standard I2C protocol is used the default frame to access parameters are given below. This block was originally designed by CERN and modified by OMEGA to bypass wishbone clock (internal stuff not seen outside).

A parameter can be accessed through its sub-block (cluster) number and its register number. The mapping is given in the section "ASIC parameters" (Part V).

The default frame to write a single parameter is given below (Fig. III.6):

S	CHIP ADR	W	A	SUB-ADR [15:8]	A	SUB-ADR [7:0]	A	DATA ADR [7:0]	A	P
---	----------	---	---	----------------	---	---------------	---	----------------	---	---

Figure III.6: Default frame to write a single parameter

S/P: START and STOP condition of a standard I2C protocol

CHIP ADDR: 7-bit chip address (MSB must be set to 1)

SUB-ADR [15:8]: sub-block (cluster) number (from 0 to 255)

SUB-ADR [7:0]: register number (from 0 to 31) – not used bits must be set to 0

DATA[7:0]: data to be written in the parameter

A: Acknowledge bit

The frame for a read operation is (Fig. III.7):

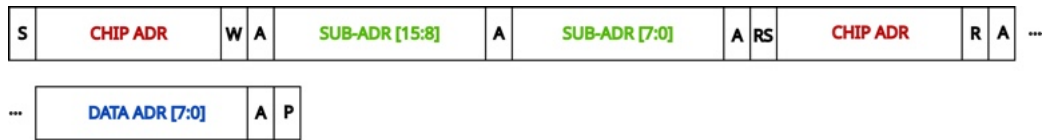


Figure III.7: Frame for a read operation

RS: RESTART condition (can be a STOP/START condition)

A: Acknowledge bit (except for the last one that need to be inverted)

The multibyte write and read can be handled with the following write (top) and read (bottom frames) (Fig. III.8). This operation is only allowed inside the same sub-block (cluster).

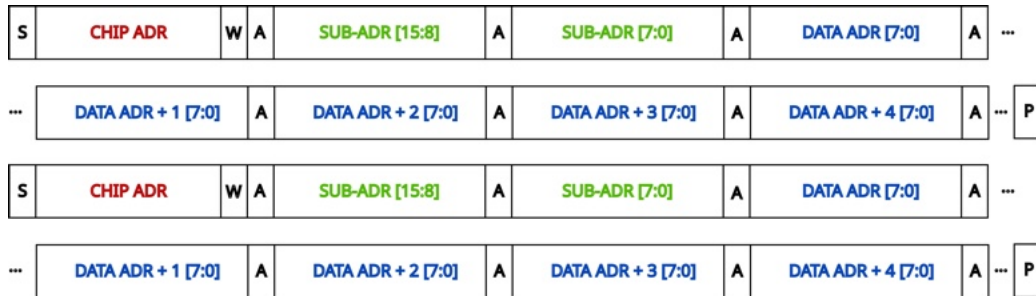


Figure III.8: Multibyte write and read frames

A broadcast address (hardcoded to 100 0000) is also available to write multiple chips at the same time.

2.c ASIC parameter access with fast commands

As an alternative, parameters can be accessed with 3 dedicated fast commands (sc1, sc0 and sc_Valid). It mimics simple or multibyte read and write actions (like I2C ones).

SC0 and SC1 are used to send respectively a 0 and 1. SC_V is used to validate a transaction.

A read transaction can be done by making the following frame (Fig. III.9). The effective read of the parameter is done through the first fast serial link.

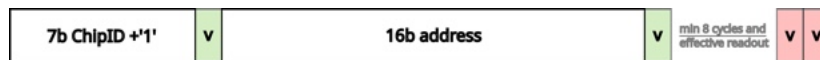


Figure III.9: Fast Command read transaction

A write transaction can be done by making the following frame (Fig. III.10).



Figure III.10: Fast Command write transaction

Sending 2 consecutive SC_V cancels the current transaction. When this method is used, the I2C port must remain in idle mode.

The read operation is done through the first high-speed data link (lowest number). This I2C readout has a lower priority than an event data readout and will be postponed until the ASIC has no event to readout.

If a read I2C is done, the output on link0, that reads channels 0 to 17 is (Fig. III.11):

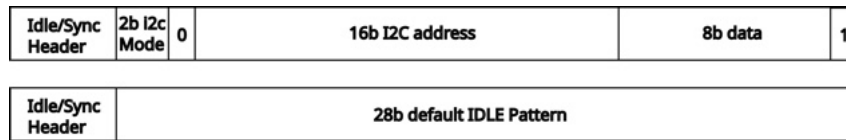


Figure III.11

2.d High speed serial links

The output differential links (aka eLinks) are composed of a serializer and a driver compatible with the LpGBT protocol (CLPS). The serializer converts parallel 32 bits words at 40 MHz to a serial train of bits send out at 1280 Mbps. In the table below (Tab. III.2), the electrical specifications of the driver are given.

Specification description	Value
Vcm (common voltage)	0.6 V
Vdiff (differential voltage)	100 to 200 mV
Pre-emphasis current	0.5 to 4 mA
Termination load	100 Ω

Table III.2: Electrical specification of the driver

The termination load resistor must be placed outside the chip.

3 Operating mode

3.a Resets

There are three ways to reset the chip.

- The hard reset pin `hard_resetsb` (CMOS input, active low) comes from an external pin and resets everything (analog + digital).
- The soft reset pin `soft_rstb` (CMOS input, active low) is same as `hard_resetsb` but leaves the SC parameters programmed.
- The fast command `ChipSync` is equivalent to an external soft reset (but only affects the digital part), it does not reset the Fast Command unit or analog part (like PLL). A `CMD_BCR` is needed after a `ChipSync` to resynchronise the time tagging counters with the whole system.

A Power-On-Reset has been implemented which performs a hard reset (`hard_resetsb`) while the chip is powered on. The Power-On-Reset is a very critical block of the chip. It has been simulated with the special gate-leakage models and furthermore with additional 1 μ A leakage current on the sensitive transistors. Moreover, its output is accessible on a spare pad (`Rstb_I2C`).

Some fast commands allow to reset specific parts of the chip, as described below:

- Bunch Crossing counter reset (BCR): issued via the fast command receiver, this command resets the internal timestamp counter to its default value (as defined by the corresponding parameter).
- Event Buffer Reset (EBR): issued via the fast command receiver, this command resets only the pointers of the Event Buffer (internal FIFO memory). After an EBR the ASIC can accept a new manual trigger from a fast command (L1A) on the next clock cycle. If an event readout is already in progress, it will complete normally.

3.b Startup procedure

CALOROC1C is able to read 1 detector per channel. The chip has 36 input-channels which are mapped to two 1.28 Gbps serial links (18 channels per link).

On start-up, the user resets the chip, this will force all chip parameters to default values. Once the reset is done, the user can configure the chip by using slow control parameters. The acquisition starts when the parameter named "Run" is equal to 1.

When the chip is powering on, the Power-On-Reset (POR) block applies a reset (like the `hard_resetsb`). The POR block can be disabled by a pin (Power-On disable).

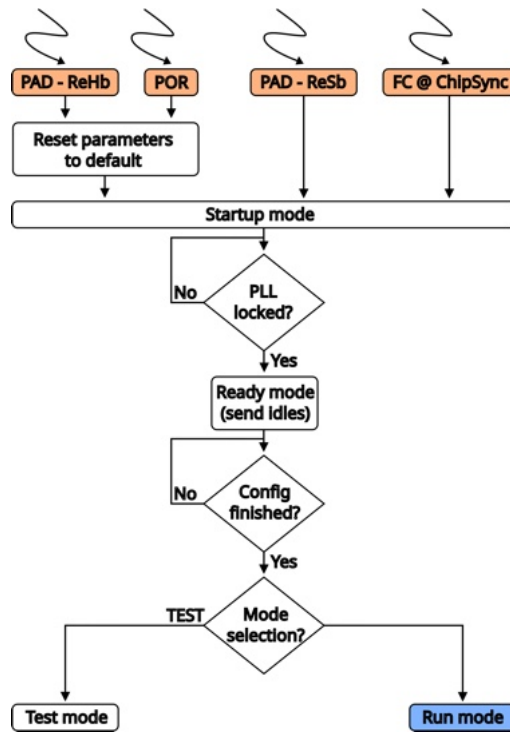


Figure III.12: State machine describing the ASIC operation

The following steps describe the state machine (Fig. III.12) or sequence the ASIC goes through after power-up and during operation. They are dynamic, meaning the ASIC transitions between them based on internal conditions or user actions:

1. Startup Mode

- Occurs immediately after reset or power-on.
- ASIC uses default configuration parameters.
- It stays here until the PLL locks.

2. Ready Mode

- The PLL is now locked, and the ASIC is ready for configuration.
- The user have to load operating parameters via I2C.
- Once configuration is done, a signal "Run" have to be set.
- ASIC starts sending a forced 32-bit IDLE pattern on the trigger links.

3. Run Mode

- The ASIC is fully configured and begins data acquisition.
- This is the default acquisition mode during system operation.

4. Test Mode

- Used to test the internal DRAM memory.
- Not part of normal acquisition, meant for diagnostics.

Low Power mode disables the chip's analog section, including the preamplifier, shaper, and discriminators. However, since the PLL remains active, the ADC, TDC, and AlignBuffer also remain operational.

3.c RUN mode

During normal operation, when all channels are active, the readout consists of **22 words of 32 bits each** (see Fig. III.13), when operating in zero-suppressed mode, the readout may contain fewer words than the nominal 3-20 word range.:

- **Words 1-2:** Contain the timestamp and hit channel information.
- **Words 3-20:** Depending on whether Zero Suppress is enabled, each word includes:
 - Tc - TOT complete, the second 10 bits packet corresponds to TOT, not ADC (Fig. III.15).
 - Tp - TOT in progress, A TOT occurred in a previous Timestamp and the ADC value can be "corrupted" (saturation or undershoot).
 - The remaining bits can contain the **Charge** (ADC and/or ADC - 1), **Time of Arrival (ToA)** data, and **Time over Threshold (TOT)** for each channel.
- **Word 21:** Contains the CRC for error checking.
- **Word 22:** Idle word.

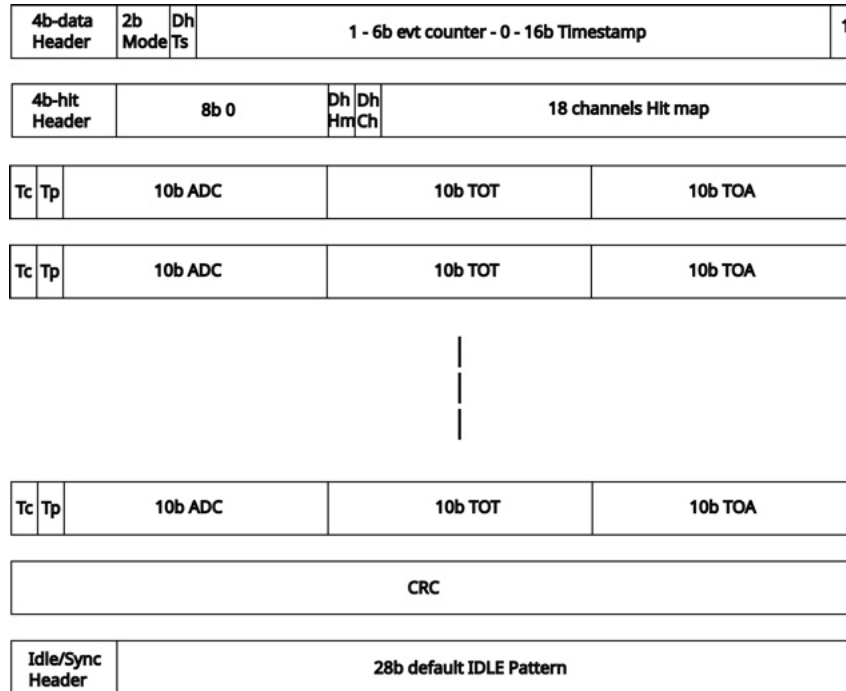


Figure III.13: Readout of the ASIC - with CalibrationSC = 1

Tc and Tp Interpretation:

- 0b00 : The TOT is not in operation (not busy), normal behaviour with ADC data.
- 0b01 : The TOT is busy (integration or undershoot), Tp highlights the fact that provided ADC correspond to saturation or undershoot.
- 0b10 : The TOT value is outputted, normal behaviour with TOT data (ADC value is between saturation and undershoot).
- 0b11 : The TOT value is outputted, normal behaviour with TOT data (ADC value is between saturation and undershoot).

The ADC and the TOA data are over 10 bits each and the TOT is natively in 12 bits. A first step of the digital processing is to compress the 12b TOT to 10b TOT. The figure below (Fig. III.14) shows the algorithm of the compression.

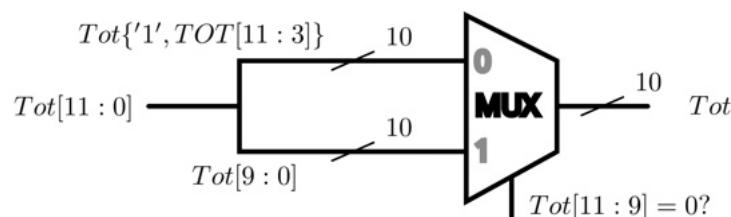


Figure III.14: ToT compression algorithm

Data Header (4 bits):

Identify the type of frame with dedicated header: 0x5.

Hit Header (4 bits):

Identify the type of frame with dedicated header: 0xF.

Mode (2 bits):

Indicates the ASIC mode:

- 00 → 1 ADC + 1 TOT (mode used in CALOROC1C).
- 01 → 2 ADCs mode with gain switching (not used in CALOROC1C).
- 10 → 1 ADC mode with gain switching (not used in CALOROC1C).
- 11 → Only appear in data readout to tag an I2C read through fast commands.

Dh (1 bit):

Double error flag — active high if a double error is detected during internal Hamming decoding.

- Dh Ts: double error for Hamming decoding Timestamp bits.
- Dh Ch: double error for Hamming decoding 18 channels data words.
- Dh Hm: double error for Hamming decoding HitMap bits.

Timestamp (16 bits):

Provides the timestamp corresponding to the detected event.

Event counter (6 bits):

Provides the sample event. First one is tagged 1.

HitMap (18 bits):

Regardless of whether Zero suppress mode is enabled or not, this bus indicates which channels were hit during the event. Data words for each channel are transmitted in ascending channel index order.

- For Link 0: (DATA(i) if HitMap(i) = 1, for i = 0 to 17).
- For Link 1: (DATA(i) if HitMap(i) = 1, for i = 18 to 35).

However, when the L1A fast command is enabled, all bits of HitMap are set to 1.

CRC (32 bits):

Cyclic Redundancy Check for data integrity verification.

3.d TEST mode

3.d.1 DRAM Self-Test via Memory BIST Module

The Test Mode is used to verify the integrity of the internal DRAM arrays using the integrated Memory BIST (Built-In Self-Test) module.

In the CALOROC ASIC, there are six DRAM instances, organised into two groups:

- Group 0: DRAM0, DRAM1, DRAM2.
- Group 1: DRAM3, DRAM4, DRAM5.

Each group is managed by a dedicated Memory BIST module.

3.d.2 Memory BIST Functionality

The Memory BIST module performs automated self-tests by:

- Writing a predefined set of test patterns to each DRAM instance.
- Applying a retention time (delay before readback).
- Reading back the stored data.
- Comparing the results to detect memory faults.

This module is clock-gated to minimise power consumption and operates exclusively in Test Mode.

3.d.3 Activation Conditions

Memory BIST tests are triggered automatically during startup if the following slow control parameters are set after reset:

- TestMode = 1
- Run = 0

In this case, the startup state machine enters DRAM test mode and executes the BIST sequence.

3.d.4 Interface Signals (Slow Control Registers)

The interface signals are summarised below (Fig. III.3):

Signal	Direction	Width	Description
Ret_time	Input	12	Retention time (wait cycles before readback)
BistRamErrors	Output	24	Error flags (4 bits per DRAM)
Bist_dones	Output	2	BIST completion flags (1 per DRAM group)

Table III.3: RAM I2C

3.d.5 Monitoring Test Progress

The Bist_dones signal provides status on BIST execution (Fig. III.4):

Signal Bit	DRAM Group	Description
Bist_dones[1]	DRAM3, DRAM4, DRAM5	Indicates BIST completion for upper group
Bist_dones[0]	DRAM0, DRAM1, DRAM2	Indicated BIST completion for lower group

Table III.4: RAM Tests

- While Bist_dones = 0, the BIST is in progress.
- When Bist_dones = 1, the test has completed for that group.

Each bit is set to "1" once the test finishes for the associated group.

3.d.6 Analysing Test Progress

The BistRamErrors signal provides a 24-bit error flag, organised as 4 bits per DRAM instance. A bit set to 1 indicates that a fault has been detected for a specific test pattern. Bits are grouped as follows:

- Bits [3:0] → DRAM0
- Bits [7:4] → DRAM1
- Bits [11:8] → DRAM2
- Bits [15:12] → DRAM3
- Bits [19:16] → DRAM4
- Bits [23:20] → DRAM5

Example: If BistRamErrors = 24'b0000_0100_0000_0000_1000_0001, then:

- Bit 0 = 1 → Fault in DRAM0.
- Bit 7 = 1 → Fault in DRAM1.

3 faults detected on DRAM0, DRAM1, and DRAM4.

3.e ASIC modes (functional configuration)

These are user-selectable configurations that determine how the ASIC internally processes analog signals. Set via a slow control register called AsicMode. They are static until changed by the user:

One ADC and One TOT Mode

- The ASIC uses one ADC and one TDC to digitise input channels, which one is used depends on the input charge.
- **Only mode used in CALOROC1C.**
- AsicMode = 00 → 1 ADC + 1 TOT mode.

Two ADCs Mode

- The ASIC uses two separate ADCs to digitise input channels.
- Likely for higher throughput or parallel processing.
- AsicMode = 01 → Two ADCs mode.

Single ADC with 4 Gain Stages Mode

- Uses one ADC, but with four selectable gain settings.
- Optimised for dynamic range adaptation and good when signals vary in amplitude.
- AsicMode = 10 → Single ADC mode.

The following picture (Fig. III.15) summarises the readout frame for different ASIC modes. Note that CALOROC1C only uses the mode 00 - 1 ADC and 1 TOT. The data content then depends if the TOT is available ($T_c = 1$, TOT complete) or if it is not ($T_c = 0$); and if the slow control parameter CalibrationSC is set to 0 or 1.

1 ADC + 1 TOT - CALOROC1C MODE

Tc	Tp	10b ADC-1	10b ADC	10b TOA	$T_c = 0$
Tc	Tp	10b ADC-1	10b TOT	10b TOA	$T_c = 1$
Tc	Tp	10b ADC	10b TOT	10b TOA	CalibrationSC = 1

2 ADCs

2b Gain	10b ADC - HG	10b ADC 3-gain	10b TOA
---------	--------------	----------------	---------

1 ADC

2b Gain	000000000	10b ADC 4-gain	10b TOA
---------	-----------	----------------	---------

Figure III.15: ASIC modes

3.f Idle word composition

The default word (Fig. III.16) sent over the high-speed links is defined as the idle word. It's a 32-bit word composed by 2 fields: a 4-bit header (defined in the next sections) and a 28-bit pattern (defined as a slow-control parameter with its LSB forced to 0).

Idle/Sync Header	28b default IDLE Pattern
------------------	--------------------------

Figure III.16: Default idle word

This idle word is automatically modified to carry the almost-full (AF) information (Fig. III.17). The bit 1 is set to 1 when the flag is internally active as it's shown below.

Idle/Sync Header	26b default IDLE Pattern	AF	0
------------------	--------------------------	----	---

Figure III.17: Idle word and AF information

In response to a ping fast command (CMD_PING), the chip will change this idle word to a ping-idle word (Fig. III.18). With a fixed latency the chip will output the following word containing the timestamp. The LSB is set to 1 to identify this ping-idle word.

Idle/Sync Header	4b default IDLE Pattern	16b Timestamp	6b default IDLE Pattern	AF	1
------------------	-------------------------	---------------	-------------------------	----	---

Figure III.18: Idle word, AF information and ping fast command

3.g Number of samples (N_value)

N_value is a 3 bits parameter. It specifies the desired number of charge samples per event. Its value must be greater than 0 (from 1 to 7). The next figure (Fig. III.19) illustrates the number of samples in normal mode. Red dots represent the acquired and transmitted samples, while the blue dot indicates the Time of Arrival (ToA).

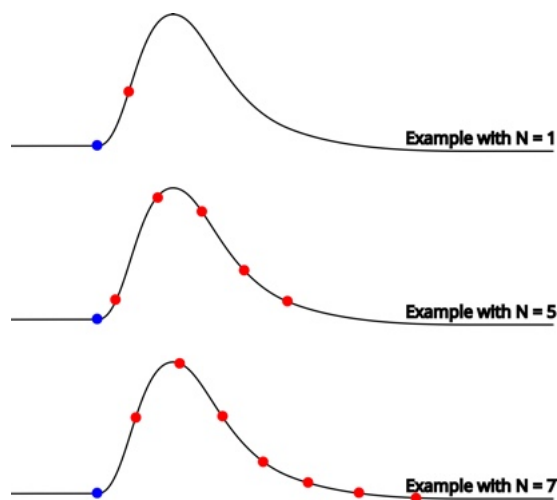


Figure III.19: Representation of different number of samples

3.h Synchronisation header (Time_trigger)

When the internal counter (16b Timestamps) of the chip crosses a defined value (parameter Time_trigger), the 4-bit header of the next readout 32-bit word will change according to table below (Tab. III.5).

4-bit header value	Signification
0x5	Data: first readout word (timestamp or I2C read)
0xF	Data: readout word is the event Hit Map
0xA	IDLE: default IDLE word
0x9	IDLE: idle word with synchronisation header

Table III.5: Synchronisation header summary

3.i Clocks

The only external clock needed to operate the ASIC is the 320MHz. All other needed clocks are generated internally. The state machines are clocked at 40MHz (which is generated by the fast command block). The chip embeds a PLL to provide the internal clocks.

3.j Almost full flag (Flag_AF)

Flag_AF is an output pin of the chip that notifies the user when the internal memory of the chip is almost full. Val_AF (value almost full) is a 6 bits parameter that contains the almost-full threshold (value from 1 to 32). If Val_AF is set to 32, Flag_AF will be active when the memory is full.

This information is almost available in the bit 1 of the idle word sent through the high-speed links.

PART **IV**

PACKAGING, I/OS AND POWERING SCHEME

1 Pin maps

The chip will be packaged in BGA. The BGA ballmap is given below (Fig. IV.1) (valid for all the CALOROC versions).

The figure below (Fig. IV.2) shows the pinout of the die bumps of CALOROC (to be used as a flip-chip). The view is from the TOP view of ASIC design tools. The black spots show location where bumps were removed.

	1	2	3	4	5	6	7	8	9	10
A	SDA	RSTB_I2C	HARD_RSTB	SOFT_RSTB	ERROR	CK_320_N	CK_320_P	FCMD_P	FCMD_N	ADD<4>
B	SCL	GND	GND	GND	GND	GND	VH10<0>	VH10<1>	FLAG_AF	ADD<4>
C	DACalido_daq0p	GND	GND	GND	GND	GND	NC	NC	FLAG_AF	NC
D	NC_daq0n	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD
E	NC_daq1p	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD
F	OUTff_daq1n	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD
G	SIPM_CALIB	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND
H	NC	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND
J	STROBE_EXT	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND
K	EFUSE	NC	GND	DVDD	VDD_PLL	VDD_PLL	AGND_PLL	GND	GND	AGND
L	TRIG_P	NC	GND	DVDD	VDD_SC	VDD_SC	AGND_PLL	GND	GND	AGND
M	TRIG_N	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND
N	DAQ2_P	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND
P	DAQ2_N	PLL_LOCK	GND	DVDD	VDD_SC	VDD_SC	GND	GND	GND	AGND
R	DAQ3_P	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD
T	DAQ3_N	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD
U	ADD<3>	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD
V	ADD<2>	GND	GND	GND	GND	GND	NC	NC	NC	NC
W	ADD<1>	GND	GND	GND	GND	GND	NC	VH10<2>	NC	NC
Y	ADD<0>	PROBE_TOT_PA	PROBE_TOA	PROBE_DC2	PROBE_DC1	PROBE_INV	VNEG	VH10<3>	PROBE_NOINV	TRIG2_EXT

	11	12	13	14	15	16	17	18	19	20
CHIP_R	AGND	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND	AGND
VREF_ADC	AGND	AGND	AVDD	AGND	IN<0>	AGND	IN<1>	AGND	NC	VDDA_PAD
VCM_ADC	AGND	AGND	AVDD	AGND	IN<2>	AGND	IN<3>	AGND	NC	VDDA_PAD
AVDD	AVDD	AVDD	AVDD	AGND	IN<4>	AGND	IN<5>	AGND	NC	VDDA_PAD
AVDD	AVDD	AVDD	AVDD	AGND	IN<6>	AGND	IN<7>	AGND	NC	VDDA_PAD
AVDD	AVDD	AVDD	AVDD	AGND	IN<8>	AGND	IN<9>	AGND	AGND	AGND
AGND	AGND	AGND	AGND	AGND	IN<10>	AGND	IN<11>	AGND	NC	VREF_SK_LP
AGND	AGND	AGND	AGND	AGND	IN<12>	AGND	IN<13>	AGND	AGND	AGND
AGND	AGND	AGND	AGND	AGND	IN<14>	AGND	IN<15>	AGND	NC	VREF_NOINV_SK
AGND	AGND	AGND	AGND	AGND	IN<16>	AGND	IN<17>	AGND	NC	VREFINV_VBM3PA
AGND	AGND	AGND	AGND	AGND	IN<18>	AGND	IN<19>	AGND	NC	VREFTOA_VBIIPA
AGND	AGND	AGND	AGND	AGND	IN<20>	AGND	IN<21>	AGND	NC	VREFTOT_VBM4PA
AGND	AGND	AGND	AGND	AGND	IN<22>	AGND	IN<23>	AGND	NC	VBC_1V
AGND	AGND	AGND	AGND	AGND	IN<24>	AGND	IN<25>	AGND	NC	PROBEPA_VBOPA
AGND	AGND	AGND	AGND	AGND	IN<26>	AGND	IN<27>	AGND	NC	INCTEST
AVDD	AVDD	AVDD	AVDD	AGND	IN<28>	AGND	IN<29>	AGND	NC	VDDA_PAD
AVDD	AVDD	AVDD	AVDD	AGND	IN<30>	AGND	IN<31>	AGND	NC	VDDA_PAD
AVDD	AVDD	AVDD	AVDD	AGND	IN<32>	AGND	IN<33>	AGND	NC	VDDA_PAD
VCM_ADC	AGND	AGND	AVDD	AGND	IN<34>	AGND	IN<35>	AGND	NC	VDDA_PAD
VREF_ADC	AGND	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND	AGND
TRIG1_EXT	AGND	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND	AGND

Figure IV.1: BGA ballmap

	1	2	3	4	5	6	7	8	9	10
A		gnd_dac	gnd_pa	in<1>	in<0>	gnd_pa	gnd_sk	gnd_buf	vcm_adc	gnd_adc
B	avss	vdd_dac	gnd_pa	in<3>	in<2>					
C	vdd_pad	gnd_dac	gnd_pa	in<5>	in<4>	vdd_pad	vdd_sk	vdd_buf	vref_adc	vdd_adc
D	Vref_sk	vdd_dac	gnd_pa	in<7>	in<6>					
E	vdd_pad	gnd_dac	gnd_pa	in<9>	in<8>	gnd_pa	gnd_sk	gnd_buf	vcm_adc	gnd_adc
F	Vref_noinv	vdd_dac	gnd_pa	in<11>	in<10>					
G	vdd_pad	gnd_dac	gnd_pa	in<13>	in<12>	vdd_pad	vdd_sk	vdd_buf	vref_adc	vdd_adc
H	Vref_inv	vdd_dac	gnd_pa	in<15>	in<14>					
J	avss	gnd_dac	gnd_pa	in<17>	in<16>	gnd_pa	gnd_sk	gnd_buf	vcm_adc	gnd_adc
K	Vref_toa	vdd_dac	gnd_pa	in<19>	in<18>					
L		gnd_dac	gnd_pa	gnd_pa	gnd_pa	vdd_pad	vdd_sk	vdd_buf	vref_adc	vdd_adc
M	Vref_tot	gnd_dac	gnd_pa	in<21>	in<20>	gnd_pa	gnd_sk	gnd_buf	vcm_adc	gnd_adc
N	avss	vdd_dac	gnd_pa	in<23>	in<22>					
P	vbg_1v	gnd_dac	gnd_pa	in<25>	in<24>	vdd_pad	vdd_sk	vdd_buf	vref_adc	vdd_adc
R	vdd_pad	vdd_dac	gnd_pa	in<27>	in<26>					
T	probe_pa	gnd_dac	gnd_pa	in<29>	in<28>	gnd_pa	gnd_sk	gnd_buf	vcm_adc	gnd_adc
U	vdd_pad	vdd_dac	gnd_pa	in<31>	in<30>					
V	in_ctest	gnd_dac	gnd_pa	in<33>	in<32>	vdd_pad	vdd_sk	vdd_buf	vref_adc	vdd_adc
W	vdd_pad	vdd_dac	gnd_pa	in<35>	in<34>					
Y		gnd_dac	gnd_pa	gnd_pa	gnd_pa	gnd_pa	gnd_sk	gnd_buf	vcm_adc	gnd_adc

	11	12	13	14	15	16	17	18	19	20
	gndd	gnd_tdc	gndd	vss	chip_R (100k)	add<4>	fcmd_p	clk320_p	soft_resetb	
	vddd	vdd_tdc	vddd	vddd2	flag_AF	VH10	fcmd_n	clk320_n	hard_resetb	SDA
			gndd	vss	vss	vss	vss	vss	error	SCL
	gndd	gnd_tdc	vddd	vddd2	vddd2	vddd2	vddd2	vddd1	NC0	NC1
			gndd	vss	vss	vss	vss	vss	gndd1	vddd1
	vddd	vdd_tdc	vddd	vddd2	vddd2	vddd2	vddd2	vddd1	NC	NC3
			gndd	vss	vss	vss	vss	vss	rstb_i2c	sipm_calib
	vddd	vdd_tdc	vddd	vddd2	vddd2	vddd2	vddd2	vddd1	efuse	strobe_ext
	gndd	gnd_tdc	gndd	vss	vss	vss	vss	vss	gnd_pil	vdd_pil
	vddd	vdd_tdc	vddd	vddd2	vddd2	vddd2	vddd2	vddd1	gnd_pil	vdd_pil
	gndd	gnd_tdc	gndd	vss	vss	vss	vss	vss	trig_n	trig_p
			vddd	vss	vss	vss	vss	vss	gndd1	vdd_sc
	vddd	vdd_tdc	vddd	vddd2	vddd2	vddd2	vddd2	vddd1	daq2_n (out0_n)	daq2_p (out0_p)
			gndd	vss	vss	vss	vss	vss	gndd1	vddd1
	gndd	gnd_tdc	vddd	vddd2	vddd2	vddd2	vddd2	vddd1	daq3_n (out1_n)	daq3_p (out1_p)
	vddd	vdd_tdc	gndd	vss	vss	vss	vss	vss	add<3>	add<2>
			vddd	vddd2	vddd2	vddd2	vddd2	vddd1	add<1>	add<0>
	vddd	vdd_tdc	gndd	vss	vss	vss	vss	vss	PLL_lock	vdd_sc
	gndd	gnd_tdc	vddd	vddd2	vddd2	vddd2	vddd2	VNEG	probe_toa	probe_tot
			trig1_ext	trig2_ext	probe_noinv	VH10	probe_inv	probe_dc1	probe_dc2	

Figure IV.2: Pinout of the die bumps

2 Pin list

Pin name	Pin type	I/O Type	Comments	Default value
VDDD	POWER		FIFO, ADC power supply	1.2 V
VDD_PAD	POWER		PAD power supply	1.2 V
VDD_TDC	POWER		TDC power supply	1.2 V
VDD_ADC	POWER		ADC power supply	1.2 V
VDD_BUF	POWER		BUFFER power supply	1.2 V
VDD_SK	POWER		Shaper power supply	1.2 V
VDD_DAC	POWER		DAC power supply	1.2 V
VDD_PLL	POWER		PLL power supply	1.2 V
VDD_SC	POWER		Slow Control power supply	1.2 V
VHI10	POWER		RAM positive power supply	1.2 V
VDD2	POWER		Digital power supply	1.2 V
VDD1	POWER		Digital power supply	1.2 V
VSS	GROUND		Digital ground	0 V
AVSS	GROUND		Analog ground	0 V
GNDD	GROUND		FIFO, ADC ground	0 V
GND_TDC	GROUND		TDC ground	0 V
GND_ADC	GROUND		ADC ground	0 V
GND_BUF	GROUND		BUFFER ground	0 V
GND_SK	GROUND		Shaper ground	0 V
GND_PA	GROUND		Preamplifier ground	0 V
GND_DAC	GROUND		DAC ground	0 V
GND_PLL	GROUND		PLL ground	0 V
GNDD1	GROUND		Digital ground	0 V

Table IV.1: Power/Grounds

Pin name	Pin type	I/O Type	Comments	Default value
Error	Open drain		Open collector; external resistor must be added. OR of all the slow-control cells' error signals. Errorb	
SCL	CMOS	Input	I2C clock	
SDA	Open drain	Input/Output	I2C data	
Out0_p	CLPS	Output	Data 0 link	
Out0_n	CLPS	Output	Data 0 link	
Out1_p	CLPS	Output	Data 1 link	
Out1_n	CLPS	Output	Data 1 link	
Trig_p	CLPS	Output	Analog Probe: Trigger_OR or PLL Probe (Clock) If SC EN_Probe_PLL=0 → Trigger_OR EN_trig=1	
Trig_n	CLPS	Output	Analog Probe: Trigger_OR or PLL Probe (Clock) If SC EN_Probe_PLL=0 → Trigger_OR EN_trig=1	
SiPM_Calib	CMOS	Output	Calibration signal for SiPM	
Rstb_I2C	CMOS	Input/Output	Output: Probe Power-On reset Input: Bypass Power-On reset Chip reset ACTIVE LOW	0 V
Hard_resetb	CMOS	Input	Global reset (PLL, I2C, FSM,SLOW CONTROL); ACTIVE LOW	0 V
Soft_rstb	CMOS	Input	Global reset (except SLOW CONTROL); ACTIVE LOW	0 V
Clk320_p	CLPS	Input	Fast command 320 MHz clock	
Clk320_n	CLPS	Input	Fast command 320 MHz clock	
Fcmd_p	CLPS	Input	Fast command data	
Fcmd_n	CLPS	Input	Fast command data	
Chip_R		Input	100k Ω resistor to gnd	
Strobe_ext	CMOS	Input	External calibration signal selectable by slow control	0 V
efuse	ANALOG		eFuse connection	
ADD<4:0>	I2C chip address		I2C chip address	
PLL_lock	CMOS	Output		
VNEG	POWER		RAM negative power supply	-100 mV
Flag_AF	Open drain	Output	Indicates internal almost full memory (active low)	0 V

Table IV.2: Common pins

Pin name	Pin type	I/O Type	Comments	Default value
IN<0:35>	ANALOG	Input	Analog inputs	200 mV
Trig1_ext	CMOS	Input	External trigger 1	
Trig2_ext	CMOS	Input	External trigger 2	
Vcm_ADC	ANALOG	Input/Output	Common mode reference voltage of the ADC.	500 mV
Vref_ADC	ANALOG	Input/Output	Reference voltage of the ADC.	1 V
Vref_SK	ANALOG	Input/Output	Reference voltage of the Shaper amplifier, value close to the preamp input voltage. By default must be kept free. Can be monitored/checked.	200 mV
Vref_noinv	ANALOG	Input/Output	Reference voltage of the non-inverted shaper. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	230 mV
Vref_inv	ANALOG	Input/Output	Reference voltage of the inverted shaper. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	460 mV
Vref_Toa	ANALOG	Input/Output	Reference voltage of the TOA shaper. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	500 mV
Vref_Tot	ANALOG	Input/Output	Reference voltage of the TOT shaper. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	400 mV
VBG_1V	ANALOG	Input/Output	BANDGAP voltage. Value can be tuned by slow-control.	1 V
In_ctest	ANALOG	Input	By default, external pin test, but possibility to connect the calibration DAC output to this pin by slow-control.	
Probe_noinv	CMOS	Output	Buffer noinv output probe. Channel-wise	
Probe_inv	CMOS	Output	Buffer inv output probe. Channel-wise	
Probe_Toa	CMOS	Output	TOA discr output probe. Channel-wise	
Probe_Tot	CMOS	Output	TOT discr output probe. Channel-wise	
Probe_pa	CMOS	Output	Preamplifier analog probe. Channel-wise	
Probe_DC1	ANALOG	Input/Output	DC analog probe	
Probe_DC2	ANALOG	Input/Output	DC analog probe	

Table IV.3: Analog and mixed part (channels 0 to 35)

The I2C slave has 4 internal registers (aka "Slim internal registers"): 2 read/write registers and 2 read-only status registers. These 4 registers are in the cluster 255 (register 0 to 3) and are described below.

Bit	Name	Default	Description
0	N.A.		
1	N.A.		
2	N.A.		
3	N.A.		
4	N.A.		
5	N.A.		
6	N.A.		
7	N.A.		

Table V.1: Cluster 255 - register 0 - read/write

Bit	Name	Default	Description
0	AutoReload	1	"1" = automatically correct SEU
1	N.A.		
2	N.A.		
3	N.A.		
4	N.A.		
5	N.A.		
6	N.A.		
7	N.A.		

Table V.2: Cluster 255 - register 1 - read/write

Bit	Name	Default	Description
0	ErrorOut_global		SEU error in slow control registers
1	ParityOut_global		Parity error in slow control registers
2	LOCK_PLL		
3	N.A.		
4	N.A.		
5	N.A.		
6	N.A.		
7	N.A.		

Table V.3: Cluster 255 - register 2 - read only (status)

Bit	Name	Default	Description
0	N.A.		
1	N.A.		
2	N.A.		
3	N.A.		
4	N.A.		
5	N.A.		
6	N.A.		
7	N.A.		

Table V.4: Cluster 255 - register 3 - read only (status)

1 I2C Addressing

The chip is divided in sub-blocks (aka clusters) containing a maximum of 32 registers. The 16-bit I2C address was divided in 2 parts:

- The 8 MSB of this address to encode the sub-block (cluster) number (from 0 to 255)
- The 8 LSB to encode the register number (from 0 to 31) of this sub-block (cluster)

The unused bits of the register number must be set to 0. The table below gives the address, the name and a short description of all the sub-blocks (clusters).

Sub-block name	Sub-block address	Description
Channel_0	0	
Channel_1	1	
Channel_2	2	
Channel_3	3	
Channel_4	4	
Channel_5	5	
Channel_6	6	
Channel_7	7	
Channel_8	8	
Channel_9	9	
Channel_10	10	
Channel_11	11	
Channel_12	12	
Channel_13	13	
Channel_14	14	
Channel_15	15	
Channel_16	16	
Channel_17	17	
Channel_18	18	Registers described in " channel wise " I2C parameters table
Channel_19	19	
Channel_20	20	
Channel_21	21	
Channel_22	22	
Channel_23	23	
Channel_24	24	
Channel_25	25	
Channel_26	26	
Channel_27	27	
Channel_28	28	
Channel_29	29	
Channel_30	30	
Channel_31	31	
Channel_32	32	
Channel_33	33	
Channel_34	34	
Channel_35	35	
UNUSED	36	
Reference_Voltage	37	Register described in " Reference Voltage " table
Global_Analog	38	Register described in " Global analog " table
Master_TDC	39	Register described in " Master TDC " table
Digital	40	Register described in " Digital " table
ChannelWise	41	Register described in " channel wise " I2C table
Top	42	Register described in " Top sub-block " table

Table V.5: Cluster 255 - register 3 - read only (status)

2 "Channel-wise" I2C parameters

Bit	Name	Default	Description
0	Inputdac<0>	0	Input-DAC for the leakage current compensation
1	Inputdac<1>	0	
2	Inputdac<2>	0	
3	Inputdac<3>	0	
4	Inputdac<4>	0	
5	Inputdac<5>	0	
6	Inputdac<6>	0	
7	Inputdac<7>	0	

Table V.6: Register #0

Bit	Name	Default	Description
0	mask_toa	0	TOA disci output mask ("1" = masked)
1	sel_trig_toa	0	External trigger selection for TOA ("0" = Ext Trig1; "1" = Ext Trig2)
2	trim_toa<0>	0	Local 6b-DAC for TOA threshold trimming
3	trim_toa<1>	0	
4	trim_toa<2>	0	
5	trim_toa<3>	0	
6	trim_toa<4>	0	
7	trim_toa<5>	0	

Table V.7: Register #1

Bit	Name	Default	Description
0	N.A.		
1	N.A.		
2	trim_tot<0>	0	Local 6b-DAC for TOT threshold trimming
3	trim_tot<1>	0	
4	trim_tot<2>	0	
5	trim_tot<3>	0	
6	trim_tot<4>	0	
7	trim_tot<5>	0	

Table V.8: Register #2

Bit	Name	Default	Description
0	probe_inv	0	Inverter shaper output probe ("1" = selected)
1	probe_noinv	0	Non-inverter shaper output probe ("1" = selected)
2	trim_inv<0>	0	Local 6b-DAC for pedestal trimming
3	trim_inv<1>	0	
4	trim_inv<2>	0	
5	trim_inv<3>	0	
6	trim_inv<4>	0	
7	trim_inv<5>	0	

Table V.9: Register #3

Bit	Name	Default	Description
0	probe_pa	0	Preamplifier output probe
1	LowRange	0	0.5pF injection cap
2	HighRange	0	10pF injection cap
3	Channel_off	0	"1" = preamplifier input tied to ground
4	sel_trig_tot	0	External trigger selection for TOT ("0" = Ext Trig1; "1" = Ext Trig2)
5	mask_tot	0	TOT discr output mask ("1" = masked)
6	probe_tot	0	TOT discr output probe
7	probe_toa	0	TOA discr output probe

Table V.10: Register #4

Bit	Name	Default	Description
0	DAC_CAL_CTDC_TOT<0>	0	Tune the fine gain of the TOT CTDC: 5 bits DAC <0:4> ($1\text{k}\Omega \times 32$) by the BIAS_CAL_DAC_P and the sign 1 bit <5> $\text{VD_P CAL} = \text{VD_P} + (\text{sign } <5> \times <0:4> \times$ $1\text{k}\Omega \times \text{BIAS_CAL_DAC_P})$
1	DAC_CAL_CTDC_TOT<1>	0	
2	DAC_CAL_CTDC_TOT<2>	0	
3	DAC_CAL_CTDC_TOT<3>	0	
4	DAC_CAL_CTDC_TOT<4>	0	
5	DAC_CAL_CTDC_TOT<5>	0	
6	N.A.		
7	mask_adc	0	"1" = ADC clock off

Table V.11: Register #5

Bit	Name	Default	Description
0	DAC_CAL_CTDC_TOA<0>	0	Tune the fine gain of the TOA CTDC: 5 bits DAC <0:4> ($1\text{k}\Omega \times 32$) by the BIAS_CAL_DAC_P and the sign 1 bit <5> $\text{VD_P CAL} = \text{VD_P} + (\text{sign } <5> \times <0:4> \times$ $1\text{k}\Omega \times \text{BIAS_CAL_DAC_P})$
1	DAC_CAL_CTDC_TOA<1>	0	
2	DAC_CAL_CTDC_TOA<2>	0	
3	DAC_CAL_CTDC_TOA<3>	0	
4	DAC_CAL_CTDC_TOA<4>	0	
5	DAC_CAL_CTDC_TOA<5>	0	
6	HZ_noinv	0	For making floating (high impedance) non-inverted shaper output
7	HZ_inv	0	For making floating (high impedance) inverted shaper output

Table V.12: Register #6

Bit	Name	Default	Description
0	DAC_CAL_FTDC_TOT<0>	0	Tune the fine gain of the TOT FTDC: 5 bits DAC <0:4> ($1\text{k}\Omega \times 32$) by the BIAS_CAL_DAC_P and the sign 1 bit <5> $\text{VD_P CAL} = \text{VD_P} + (\text{sign } <5> \times <0:4> \times$ $1\text{k}\Omega \times \text{BIAS_CAL_DAC_P})$
1	DAC_CAL_FTDC_TOT<1>	0	
2	DAC_CAL_FTDC_TOT<2>	0	
3	DAC_CAL_FTDC_TOT<3>	0	
4	DAC_CAL_FTDC_TOT<4>	0	
5	DAC_CAL_FTDC_TOT<5>	0	
6	N.A.		
7	N.A.		

Table V.13: Register #7

Bit	Name	Default	Description
0	DAC_CAL_FTDC_TOA<0>	0	Tune the fine gain of the TOA FTDC: 5 bits DAC <0:4> (1kΩ x 32) by the BIAS_CAL_DAC_P and the sign 1 bit <5> VD_P CAL = VD_P + (sign <5> x <0:4> x 1kΩ x BIAS_CAL_DAC_P)
1	DAC_CAL_FTDC_TOA<1>	0	
2	DAC_CAL_FTDC_TOA<2>	0	
3	DAC_CAL_FTDC_TOA<3>	0	
4	DAC_CAL_FTDC_TOA<4>	0	
5	DAC_CAL_FTDC_TOA<5>	0	
6	N.A.		
7	N.A.		

Table V.14: Register #8

Bit	Name	Default	Description
0	IN_FTDC_ENCODER_TOA<0>	0	Adjust the ToA FTDC offset by 5 bits <0:4> and the sign 1 bit <5> OFFSET = FTDC_TDC<0:5> + (sign <5> x DATA<0:4>)
1	IN_FTDC_ENCODER_TOA<1>	0	
2	IN_FTDC_ENCODER_TOA<2>	0	
3	IN_FTDC_ENCODER_TOA<3>	0	
4	IN_FTDC_ENCODER_TOA<4>	0	
5	IN_FTDC_ENCODER_TOA<5>	0	
6	N.A.		
7	N.A.		

Table V.15: Register #9

Bit	Name	Default	Description
0	IN_FTDC_ENCODER_TOT<0>	0	Adjust the ToT FTDC offset by 5 bits <0:4> and the sign 1 bit <5> OFFSET = FTDC_TDC<0:5> + (sign <5> x DATA<0:4>)
1	IN_FTDC_ENCODER_TOT<1>	0	
2	IN_FTDC_ENCODER_TOT<2>	0	
3	IN_FTDC_ENCODER_TOT<3>	0	
4	IN_FTDC_ENCODER_TOT<4>	0	
5	IN_FTDC_ENCODER_TOT<5>	0	
6	N.A.		
7	DIS_TDC	0	"1" = TDC clocks off

Table V.16: Register #10

Bit	Name	Default	Description
0	ExtData<8>	0	Forced ADC data, bits 9 & 8. When "SelExtADC" in GlobalAnalog register is set to 1
1	ExtData<9>	0	
2	N.A.		
3	N.A.		
4	N.A.		
5	N.A.		
6	N.A.		
7	mask_AlignBuffer	0	"1" = AlignBuffer clock off

Table V.17: Register #11

Bit	Name	Default	Description
0	Adc_pedestal<0>	0	ADC pedestal value. It is subtracted to ADC value for trigger path only
1	Adc_pedestal<1>	0	
2	Adc_pedestal<2>	0	
3	Adc_pedestal<3>	0	
4	Adc_pedestal<4>	0	
5	Adc_pedestal<5>	0	
6	Adc_pedestal<6>	0	
7	Adc_pedestal<7>	0	

Table V.18: Register #12

Bit	Name	Default	Description
0	ExtData<0>	0	Forced ADC data, bits 7 down to 0. When "SelExtADC" in GlobalAnalog register is set to 1
1	ExtData<1>	0	
2	ExtData<2>	0	
3	ExtData<3>	0	
4	ExtData<4>	0	
5	ExtData<5>	0	
6	ExtData<6>	0	
7	ExtData<7>	0	

Table V.19: Register #13

3 "Global analog" I2C parameters

Bit	Name	Default	Description
0	ON_pa	1	"1" = enable preamplifier bias
1	trim_vbo_pa<0>	0	3b-DAC for preamp output stage current tuning
2	trim_vbo_pa<1>	1	
3	trim_vbo_pa<2>	1	
4	trim_vbi_pa<0>	1	4b-DAC for preamp input stage current tuning
5	trim_vbi_pa<1>	1	
6	trim_vbi_pa<2>	1	
7	trim_vbi_pa<3>	0	

Table V.20: Register #0

Bit	Name	Default	Description
0	ON_rtr	1	"1" = enable shaper amplifiers bias
1	dac_pol	1	Leakage current Input-DAC polarity
2	range_tot<0>	0	3b-DAC for TOT threshold range tuning
3	range_tot<1>	1	
4	range_tot<2>	0	
5	range_indac<0>	0	3b-DAC for tot leakage dac range tuning
6	range_indac<1>	1	
7	range_indac<2>	0	

Table V.21: Register #1

Bit	Name	Default	Description
0	ON_toa	1	"1" = enable TOA discri bias
1	ON_tot	1	"1" = enable TOT discri bias
2	gain_tot<0>	0	6b-DAC for TOT gain tuning (0b000000 = no feedback current)
3	gain_tot<1>	0	
4	gain_tot<2>	0	
5	gain_tot<3>	0	
6	gain_tot<4>	1	
7	gain_tot<5>	1	

Table V.22: Register #2

Bit	Name	Default	Description
0	Ibi_sk<0>	0	S-K amplifier input stage current
1	Ibi_sk<1>	0	
2	Ibo_sk<0>	0	
3	Ibo_sk<1>	1	S-K amplifier output stage current
4	Ibo_sk<2>	0	
5	Ibo_sk<3>	1	
6	Ibo_sk<4>	0	
7	Ibo_sk<5>	0	

Table V.23: Register #3

Bit	Name	Default	Description
0	Ibi_inv<0>	0	Inverter and Non-inverter amplifier input stage current
1	Ibi_inv<1>	0	
2	Ibo_inv<0>	0	
3	Ibo_inv<1>	1	Inverter and Non-inverter amplifier output stage current
4	Ibo_inv<2>	0	
5	Ibo_inv<3>	1	
6	Ibo_inv<4>	0	
7	Ibo_inv<5>	0	

Table V.24: Register #4

Bit	Name	Default	Description
0	dac_hyst_toa<0>	0	6b-dac for TOA discriminator hysteresis tuning
1	dac_hyst_toa<1>	0	
2	dac_hyst_toa<2>	0	
3	dac_hyst_toa<3>	0	
4	dac_hyst_toa<4>	0	
5	dac_hyst_toa<5>	0	
6	N.A.		
7	en_deglitcher	0	Enable deglitcher of the TOA discri output

Table V.25: Register #5

Bit	Name	Default	Description
0	Ibi_inv_buf<0>	0	Inverter buffer input stage current
1	Ibi_inv_buf<1>	1	
2	Ibo_inv_buf<0>	0	
3	Ibo_inv_buf<1>	1	Inverter buffer output stage current
4	Ibo_inv_buf<2>	1	
5	Ibo_inv_buf<3>	0	
6	Ibo_inv_buf<4>	0	
7	Ibo_inv_buf<5>	1	

Table V.26: Register #6

Bit	Name	Default	Description
0	Ibi_noinv_buf<0>	0	Non Inverter buffer input stage current
1	Ibi_noinv_buf<1>	1	
2	Ibo_noinv_buf<0>	0	
3	Ibo_noinv_buf<1>	1	Non Inverter buffer output stage current
4	Ibo_noinv_buf<2>	1	
5	Ibo_noinv_buf<3>	0	
6	Ibo_noinv_buf<4>	0	
7	Ibo_noinv_buf<5>	1	

Table V.27: Register #7

Bit	Name	Default	Description
0	Rc<1>	1	Shaping time adjustment
1	Rc<0>	0	
2	En_hyst_toa	1	"1" = enable the TOA discri hysteresis
3	En_hyst_tot	1	"1" = enable the TOT discri hysteresis
4	Cf_comp<0>	0	Preamp feedback comp. cap. <0> = 100fF, <1> = 200fF
5	Cf_comp<1>	1	
6	neg	1	"1" = negative input polarity (Default)
7	pol_trig_toa	1	Polarity of the TOA discri output

Table V.28: Register #8

Bit	Name	Default	Description
0	Cf<0>	0	Preamp feedback cap. <0> = 50fF, <1> = 100fF, <2> = 200fF, <3> = 400fF
1	Cf<1>	0	
2	Cf<2>	1	
3	Cf<3>	0	
4	Rf<0>	0	Preamp feedback Res.
5	Rf<1>	0	
6	Rf<2>	0	Rf<0> = 1 : 90k
7	Rf<3>	0	Unconnected <1:3>

Table V.29: Register #9

Bit	Name	Default	Description
0	range_inv<0>	0	3b-DAC for pedestal range tuning
1	range_inv<1>	0	
2	range_inv<2>	1	
3	SelExtADC	0	"1" = Forced ADC data send to the DRAM
4	Clr_ADC	1	Force ADC to 0 when shaper saturates for the trigger path
5	S_sk<0>	0	S-K amp Miller cap. <0> = 50fF, <1> = 100fF, <2> = 200fF
6	S_sk<1>	1	
7	S_sk<2>	0	

Table V.30: Register #10

Bit	Name	Default	Description
0	Clr_ShaperTail	1	Force ADC to 0 when undershoot for the trigger path
1	SelRisingEdge	1	Select the rising edge as clock for the AlignBuffer
2	S_inv<0>	0	Inverter amp Miller cap. <0> = 50fF, <1> = 100fF, <2> = 200fF
3	S_inv<1>	1	
4	S_inv<2>	0	
5	S_noinv<0>	0	Non Inverter amp Miller cap. <0> = 50fF, <1> = 100fF, <2> = 200fF
6	S_noinv<1>	1	
7	S_noinv<2>	0	

Table V.31: Register #11

Bit	Name	Default	Description
0	N.A.		
1	N.A.		
2	S_inv_buf<0>	0	Inverter buffer Miller cap. <0> = 100fF, <1> = 200fF, <2> = 400fF
3	S_inv_buf<1>	1	
4	S_inv_buf<2>	0	
5	S_noinv_buf<0>	0	Non Inverter buffer Miller cap. <0> = 100fF, <1> = 200fF, <2> = 400fF
6	S_noinv_buf<1>	1	
7	S_noinv_buf<2>	0	

Table V.32: Register #12

Bit	Name	Default	Description
0	ref_adc<0>	0	Input stage current of the Ref ADC OTA
1	ref_adc<1>	0	
2	Delay40<0>	0	
3	Delay40<1>	1	Delay tuning for bits <4:0> "000" = faster conversion
4	Delay40<2>	0	
5	Delay65<0>	1	
6	Delay65<1>	1	Delay tuning for bits <6:5> "000" = faster conversion
7	Delay65<2>	0	

Table V.33: Register #13

Bit	Name	Default	Description
0	ON_ref_adc	1	"1" = enable ADC ref OTA
1	N.A.		
2	Delay87<0>	1	Delay tuning for bits <8:7> "000" = faster conversion
3	Delay87<1>	1	
4	Delay87<2>	0	
5	Delay9<0>	1	Delay tuning for bit <9> "000" = faster conversion
6	Delay9<1>	1	
7	Delay9<2>	0	

Table V.34: Register #14

4 "Reference Voltage" I2C parameters

Bit	Name	Default	Description
0	N.A.		
1	N.A.		
2	Refi<0>	0	Bandgap current tuning
3	Refi<1>	0	
4	Vbg_1v<0>	0	1V bandgap ref. tuning
5	Vbg_1v<1>	0	
6	Vbg_1v<2>	1	
7	ON_dac	1	"1" = enable DACs

Table V.35: Register #0

Bit	Name	Default	Description
0	Noinv_vref<0>	0	
1	Noinv_vref<1>	0	
2	Inv_vref<0>	0	
3	Inv_vref<1>	0	
4	Toa_vref<0>	0	
5	Toa_vref<1>	0	
6	Tot_vref<0>	0	
7	Tot_vref<1>	0	

Table V.36: Register #1

Bit	Name	Default	Description
0	Tot_vref<2>	0	10b-DAC TOT threshold global value
1	Tot_vref<3>	0	
2	Tot_vref<4>	1	
3	Tot_vref<5>	1	
4	Tot_vref<6>	0	
5	Tot_vref<7>	1	
6	Tot_vref<8>	1	
7	Tot_vref<9>	0	

Table V.37: Register #2

Bit	Name	Default	Description
0	Toa_vref<2>	0	10b-DAC TOA threshold global value
1	Toa_vref<3>	0	
2	Toa_vref<4>	1	
3	Toa_vref<5>	1	
4	Toa_vref<6>	1	
5	Toa_vref<7>	0	
6	Toa_vref<8>	0	
7	Toa_vref<9>	0	

Table V.38: Register #3

Bit	Name	Default	Description
0	Inv_vref<2>	1	10b-DAC Inverter shaper global reference
1	Inv_vref<3>	1	
2	Inv_vref<4>	1	
3	Inv_vref<5>	1	
4	Inv_vref<6>	0	
5	Inv_vref<7>	0	
6	Inv_vref<8>	0	
7	Inv_vref<9>	1	

Table V.39: Register #4

Bit	Name	Default	Description
0	Noinv_vref<2>	0	10b-DAC Non Inverter shaper global reference
1	Noinv_vref<3>	0	
2	Noinv_vref<4>	0	
3	Noinv_vref<5>	0	
4	Noinv_vref<6>	0	
5	Noinv_vref<7>	1	
6	Noinv_vref<8>	0	
7	Noinv_vref<9>	0	

Table V.40: Register #5

Bit	Name	Default	Description
0	Calib<0>	0	12b-DAC Calibration value
1	Calib<1>	0	
2	Calib<2>	0	
3	Calib<3>	0	
4	Calib<4>	0	
5	Calib<5>	0	
6	Calib<6>	0	
7	Calib<7>	0	

Table V.41: Register #6

Bit	Name	Default	Description
0	Calib<8>	0	Calibration DAC value
1	Calib<9>	0	
2	Calib<10>	0	
3	Calib<11>	0	
4	N.A.	0	
5	N.A.	0	
6	IntCtest	0	Selection of the Calibration DAC
7	ExtCtest	0	Selection of the external pulse test

Table V.42: Register #7

Bit	Name	Default	Description
0	probe_dc<0>	0	Selection among 32 probes to probe_dc1 pin
1	probe_dc<1>	0	
2	probe_dc<2>	0	
3	probe_dc<3>	0	
4	probe_dc<4>	0	
5	probe_dc1_0	0	Select the 32 first probes to probe_dc1 pin
6	probe_dc1_1	0	Select the 32 last probes to probe_dc1 pin
7	probe_dc2	0	Select calibration dac output to probe_dc2

Table V.43: Register #8

Bit	Name	Default	Description
0	addr_test_t<0>	0	Selection among 21 transistors to probe_dc1 and probe_dc2 pin
1	addr_test_t<1>	0	
2	addr_test_t<2>	0	
3	addr_test_t<3>	0	
4	addr_test_t<4>	0	
5	N.A.		
6	test_G	0	Enable the transistors testing
7	test_D	0	Enable the transistors testing

Table V.44: Register #9

5 "Master TDC" I2C parameters

Bit	Name	Default	Description
0	GLOBAL_TA_SELECT_GAIN_TOA<0>	1	ToA pulse replicator gain : "1000" : 2 pulses (TDC LSB : 97,6 ps) "1100" : 4 pulses (TDC LSB : 48,8 ps) "1110" : 8 pulses (TDC LSB : 24,4 ps) (Default) "1111" : 16 pulses (TDC LSB : 12,2 ps)
1	GLOBAL_TA_SELECT_GAIN_TOA<1>	1	
2	GLOBAL_TA_SELECT_GAIN_TOA<2>	1	
3	GLOBAL_TA_SELECT_GAIN_TOA<3>	0	
4	N.A.		
5	COUNTER_PHASE<0>	0	
6	COUNTER_PHASE<1>	0	
7	FIFO_DELL_40MHZ	0	

Table V.45: Register #0

Bit	Name	Default	Description
0	GLOBAL_SEU_TIME_OUT	1	Activate the SEU time-out in the control logic channel
1	N.A.		
2	N.A.		
3	N.A.		
4	N.A.		
5	N.A.		
6	N.A.		
7	N.A.		

Table V.46: Register #1

Bit	Name	Default	Description
0	BIAS_FOLLOWER_CAL_P_D<0>	0	Configure the VTC follower for the CTDC channel calibration follower bias P current: Current = DATA<0:3> Weight addition "base" : 50 nA <0>: 100 nA <1>: 500 nA <2>: 2,5 μ A <3>: 5 μ A
1	BIAS_FOLLOWER_CAL_P_D<1>	0	
2	BIAS_FOLLOWER_CAL_P_D<2>	0	
3	BIAS_FOLLOWER_CAL_P_D<3>	0	
4	BIAS_FOLLOWER_CAL_P_CTDC_EN	0	Enable the VTC follower for the CTDC channel calibration follower bias P
5	RST_COUNTER	0	
6	DISABLE_AUTO_REFRESH_COUNTER	1	
7	CALIB_CHANNEL_DLL	0	Activate the automatic calibration of all TDC channel

Table V.47: Register #2

Bit	Name	Default	Description
0	VD_CTDC_P_D<0>	0	5 bits DAC for the VD_CTDC_P voltage : "00000" = 0,2 V "11111" = 0,75 V
1	VD_CTDC_P_D<1>	0	
2	VD_CTDC_P_D<2>	0	
3	VD_CTDC_P_D<3>	0	
4	VD_CTDC_P_D<4>	0	
5	VD_CTDC_P_DAC_EN	0	Activate the DAC for the VD_CTDC_P voltage : "0" : external PAD "VD_CTDC_P_EXT" "1" : 5 bits DAC "VD_CTDC_P_D<0:4>"
6	EN_MASTER_CTDC_VOUT_INIT	0	Activate the voltage load in "VD_FTDC_P" of the master FTDC DLL pump charge output : "0" : High Z pump charge (Default) "1" : FTDC_P INIT voltage load "VD_FTDC_P_DAC MODE"
7	EN_MASTER_CTDC_DLL	1	Activate the CTDC master DLL to provide master CLKs and global channel calibration : "0" : OFF : No CLKs "power off channels" "1" : ON : MASTER TDC activated (Default)

Table V.48: Register #3

Bit	Name	Default	Description
0	BIAS_CAL_DAC_CTDC_P_D<0>	0	Configure the VTC BIAS_CAL_DAC_CTDC_P bias of the current calibration channel: Current = DATA<0:5> Weight addition <0>: 100 nA <1>: 500 nA <2>: 1 μ A <3>: 4 μ A
1	BIAS_CAL_DAC_CTDC_P_D<1>	0	
2	CTDC_CALIB_FREQUENCY<0>	0	CTDC Master DLL calibration period : "000000" : 32 ns "100000" : 50 ns "010000" : 100 ns "001000" : 200 ns "000100" : 400 ns "000010" : 800 ns "000001" : 1600 ns "111111" : 3200 ns
3	CTDC_CALIB_FREQUENCY<1>	1	
4	CTDC_CALIB_FREQUENCY<2>	0	
5	CTDC_CALIB_FREQUENCY<3>	0	
6	CTDC_CALIB_FREQUENCY<4>	0	
7	CTDC_CALIB_FREQUENCY<5>	0	

Table V.49: Register #4

Bit	Name	Default	Description
0	GLOBAL_MODE_TOA_DIRECT_OUTPUT	0	The output of the ToA TDC are directly connected to the ToA & ToT output
1	BIAS_I_CTDC_D<0>	0	Configure the VTC the bias CTDC BIAS_N_CTDC bias (pump charge injection current) : Current = DATA<0:5> Weight addition (default 30 μ A) "base" : 50 nA <0>: 100 nA <1>: 500 nA <2>: 2,5 μ A <3>: 5 μ A <4>: 25 μ A <5>: 50 μ A
2	BIAS_I_CTDC_D<1>	0	
3	BIAS_I_CTDC_D<2>	0	
4	BIAS_I_CTDC_D<3>	1	
5	BIAS_I_CTDC_D<4>	1	
6	BIAS_I_CTDC_D<5>	0	
7	FOLLOWER_CTDC_EN	1	Activate the VTC for the bias MASTER CTDC BIAS_N_CTDC bias (pump charge injection): "0" : OFF "1" : VTC 6 bits "BIAS_I_CTDC_D<0:5>"

Table V.50: Register #5

Bit	Name	Default	Description
0	GLOBAL_EN_BUFFER_CTDC	0	Enable the BUFFER of the calibration FTDC channel "0" : OFF "1" : "VTC 6 bits "BIAS_CAL_DAC_FTDC_P_D<0:3>"
1	VD_CTDC_N_FORCE_MAX	1	Force the VD_CTDC_N voltage to 1.2 V
2	N.A.		
3	VD_CTDC_N_D<0>	0	5 bits DAC for the VD_CTDC_N voltage : "00000" = 0,6 V "11111" = 1 V
4	VD_CTDC_N_D<1>	0	
5	VD_CTDC_N_D<2>	0	
6	VD_CTDC_N_D<3>	0	
7	VD_CTDC_N_DAC_EN	0	Activate the DAC for the VD_CTDC_N voltage : "0" : external PAD "VD_CTDC_N_EXT" "1" : 5 bits DAC "VD_CTDC_N_D<0:4>"

Table V.51: Register #6

Bit	Name	Default	Description
0	EN_MASTER_CTDC_START_UP	0	
1	CTRL_IN_CTDC_P_SIG	0	
2	N.A.		
3	N.A.		
4	N.A.		
5	N.A.		
6	BIAS_CAL_DAC_CTDC_P_D<2>	0	Configure the VTC BIAS_CAL_DAC_CTDC_P bias of the current calibration channel: Current = DATA<0:5> Weight addition <0>: 100 nA <1>: 500 nA <2>: 1 μ A <3>: 4 μ A
7	BIAS_CAL_DAC_CTDC_P_D<3>	0	

Table V.52: Register #7

Bit	Name	Default	Description
0	CTRL_IN_SIG_CTDC_P_D<0>	0	5 bits DAC for the CTRL_SIG_CTDC calibration voltage : "00000" = 0,2 V "11111" = 0,8 V
1	CTRL_IN_SIG_CTDC_P_D<1>	0	
2	CTRL_IN_SIG_CTDC_P_D<2>	0	
3	CTRL_IN_SIG_CTDC_P_D<3>	0	
4	CTRL_IN_SIG_CTDC_P_D<4>	0	
5	CTRL_IN_SIG_CTDC_P_EN	0	Activate the DAC for CTRL_SIG_CTDC calibration voltage : "0" : DAC OFF 0 V output "1" : DAC 5 bits "CTRL_IN_SIG_CTDC_P_D<0:4>"
6	GLOBAL_INIT_DAC_B_CTDC	0	Load the channel calibration registers by DAC_CAL_CTDC_TOA <0:5> and DAC_CAL_CTDC_TOT <0:5> "0" : LOAD by SC registers "1" : Adjustment in automatic calibration mode
7	BIAS_CAL_DAC_CTDC_P_EN	0	Activate the VTC for the bias BIAS_CAL_DAC_CTDC_P bias of the current calibration channel "0" : OFF "1" : VTC 6 bits "BIAS_CAL_DAC_CTDC_P_D<0:3>"

Table V.53: Register #8

Bit	Name	Default	Description
0	VD_FTDC_P_D<0>	0	5 bits DAC for the VD_FTDC_P voltage : "00000" = 0,4 V "11111" = 0,9 V
1	VD_FTDC_P_D<1>	0	
2	VD_FTDC_P_D<2>	0	
3	VD_FTDC_P_D<3>	0	
4	VD_FTDC_P_D<4>	0	
5	VD_FTDC_P_DAC_EN	0	Activate the DAC for the VD_FTDC_P voltage : "0" : external PAD "VD_FTDC_P_EXT" "1" : 5 bits DAC "VD_FTDC_P_D<0:4>"
6	EN_MASTER_FTDC_VOUT_INIT	0	Activate the voltage load in "VD_FTDC_P" of the master FTDC DLL pump charge output : "0" : High Z pump charge "1" : FTDC_P INIT voltage load "VD_FTDC_P_DAC MODE"
7	EN_MASTER_FTDC_DLL	1	Activate the FTDC master DLL to provide master CLKs and global channel calibration : "0" : OFF : No CLKs "power off channels" "1" : ON : MASTER TDC activated (Default)

Table V.54: Register #9

Bit	Name	Default	Description
0	N.A.		
1	BIAS_FOLLOWER_CAL_P_FTDC_EN	0	Activate the VTC for the bias MASTER FTDC BIAS_N_FTDC bias (pump charge injection): "0" : OFF "1" : VTC 6 bits "BIAS_I_FTDC_D<0:5>"
2	FTDC_CALIB_FREQUENCY<0>	0	FTDC Master DLL calibration period : "000000" : 32 ns "100000" : 50 ns "010000" : 100 ns "001000" : 200 ns "000100" : 400 ns "000010" : 800 ns "000001" : 1600 ns "111111" : 3200 ns
3	FTDC_CALIB_FREQUENCY<1>	1	
4	FTDC_CALIB_FREQUENCY<2>	0	
5	FTDC_CALIB_FREQUENCY<3>	0	
6	FTDC_CALIB_FREQUENCY<4>	0	
7	FTDC_CALIB_FREQUENCY<5>	0	

Table V.55: Register #10

Bit	Name	Default	Description
0	EN_REF_BG	1	Activate the BANDGAP source 1V to the calibration part "0" : External PAD "EXT_REF_TDC" "1" : Internal 1V Bandgap "BG_1V"
1	BIAS_I_FTDC_D<0>	0	Configure the VTC the bias PLL BIAS_N_PLL bias (pump charge injection current) : Current = DATA<0:5> Weight addition (default 30 μ A) "base" : 50 nA <0>: 100 nA <1>: 500 nA <2>: 2,5 μ A <3>: 5 μ A <4>: 25 μ A <5>: 50 μ A
2	BIAS_I_FTDC_D<1>	0	
3	BIAS_I_FTDC_D<2>	0	
4	BIAS_I_FTDC_D<3>	1	
5	BIAS_I_FTDC_D<4>	1	
6	BIAS_I_FTDC_D<5>	0	
7	FOLLOWER_FTDC_EN	1	Activate the VTC for the bias MASTER FTDC BIAS_N_FTDC bias (pump charge injection): "0" : OFF "1" : VTC 6 bits "BIAS_I_FTDC_D<0:5>"

Table V.56: Register #11

Bit	Name	Default	Description
0	GLOBAL_EN_BUFFER_FTDC	0	Enable the BUFFER of the calibration FTDC channel "0" : OFF "1" : "VTC 6 bits "BIAS_CAL_DAC_FTDC_P_D<0:3>"
1	VD_FTDC_N_FORCE_MAX	1	Force the VD_FTDC_N voltage to 1.2 V
2	N.A.		
3	VD_FTDC_N_D<0>	0	5 bits DAC for the VD_FTDC_N voltage : "00000" = 0,4 V "11111" = 0,9 V
4	VD_FTDC_N_D<1>	0	
5	VD_FTDC_N_D<2>	0	
6	VD_FTDC_N_D<3>	0	
7	VD_FTDC_N_DAC_EN	0	Activate the DAC for the VD_FTDC_N voltage : "0" : external PAD "VD_FTDC_N_EXT" "1" : 5 bits DAC "VD_FTDC_N_D<0:4>"

Table V.57: Register #12

Bit	Name	Default	Description
0	CTRL_IN_SIG_FTDC_P_D<0>	0	5 bits DAC for the VD_FTDC_N voltage : "00000" = 0,4 V "11111" = 0,9 V
1	CTRL_IN_SIG_FTDC_P_D<1>	0	
2	CTRL_IN_SIG_FTDC_P_D<2>	0	
3	CTRL_IN_SIG_FTDC_P_D<3>	0	
4	CTRL_IN_SIG_FTDC_P_D<4>	0	
5	CTRL_IN_SIG_FTDC_P_EN	0	Activate the DAC for CTRL_SIG_FTDC calibration voltage : "0" : DAC OFF 0 V output "1" : DAC 5 bits "CTRL_IN_SIG_FTDC_P_D<0:4>"
6	BIAS_FOLLOWER_CAL_P_FTDC_D<0>	0	Configure the VTC follower for the FTDC channel calibration follower bias P current : Current = DATA<0:3> Weight addition " base " : 50 nA <0>: 100 nA <1>: 500 nA <2>: 2,5 μ A <3>: 5 μ A
7	BIAS_FOLLOWER_CAL_P_FTDC_D<1>	0	

Table V.58: Register #13

Bit	Name	Default	Description
0	EN_MASTER_FTDC_START_UP	0	
1	CTRL_IN_FTDC_P_SIG	0	
2	N.A.		
3	N.A.		
4	N.A.		
5	N.A.		
6	BIAS_FOLLOWER_CAL_P_FTDC_D<2>	0	Configure the VTC follower for the FTDC channel calibration follower bias P current : Current = DATA<0:3> Weight addition " base " : 50 nA <0>: 100 nA <1>: 500 nA <2>: 2,5 μ A <3>: 5 μ A
7	BIAS_FOLLOWER_CAL_P_FTDC_D<3>	0	

Table V.59: Register #14

Bit	Name	Default	Description
0	GLOBAL_SYNC_OUT	0	Sync the output data synchronisation with the edge of the 40 MHz "0" : rising edge
1	GLOBAL_FORCE_EN_CLK	0	Force the output data transfer clk (always clock gating) "0" : 2 clk cycles dedicated to 1 data transfer (1 for the data & 1 for the 0 after) (low power mode) "1" : clk is always present for the data transfer (40 MHz power consumption)
2	GLOBAL_FORCE_EN_OUTPUT_DATA	0	Force the En flag event to "1" (always read ToA)
3	GLOBAL_FORCE_EN_TOA<0>	0	ToA pulse replicator gain : S0 & S1 for the digital : "00" : 2 pulses (TDC LSB : 97,6 ps) "10" : 4 pulses (TDC LSB : 48,8 ps) "01" : 8 pulses (TDC LSB : 24,4 ps) (Default) "11" : 16 pulses (TDC LSB : 12,2 ps)
4	GLOBAL_FORCE_EN_TOA<1>	1	
5	GLOBAL_EN_TUNE_GAIN_DAC	0	Load the FTDC channel calibration registers by DAC_CAL_FTDC_TOA <0:5>: "0" : OFF "1" : LOAD by SC registers
6	Sel_clk_rcg_toa	0	"1": select clk_rcg to trig1_tot
7	Sel_clk_rcg_tot	0	"1": select clk_rcg to trig1_toa

Table V.60: Register #15

6 "Digital part" I2C parameters

Bit	Name	Default	Description
0	IdleFrame<0>	0	Default 28 LSB "1100 — 1100" data readout on output links when no readout request – or at startup
1	IdleFrame<1>	0	
2	IdleFrame<2>	1	
3	IdleFrame<3>	1	
4	IdleFrame<4>	0	
5	IdleFrame<5>	0	
6	IdleFrame<6>	1	
7	IdleFrame<7>	1	

Table V.61: Register #0

Bit	Name	Default	Description
0	IdleFrame<8>	0	Default 28 LSB "1100 — 1100" data readout on output links when no readout request – or at startup
1	IdleFrame<9>	0	
2	IdleFrame<10>	1	
3	IdleFrame<11>	1	
4	IdleFrame<12>	0	
5	IdleFrame<13>	0	
6	IdleFrame<14>	1	
7	IdleFrame<15>	1	

Table V.62: Register #1

Bit	Name	Default	Description
0	IdleFrame<16>	0	Default 28 LSB "1100 — 1100" data readout on output links when no readout request – or at startup
1	IdleFrame<17>	0	
2	IdleFrame<18>	1	
3	IdleFrame<19>	1	
4	IdleFrame<20>	0	
5	IdleFrame<21>	0	
6	IdleFrame<22>	1	
7	IdleFrame<23>	1	

Table V.63: Register #2

Bit	Name	Default	Description
0	IdleFrame<24>	0	Default 28 LSB "1100 — 1100" data readout on output links when no readout request – or at startup
1	IdleFrame<25>	0	
2	IdleFrame<26>	1	
3	IdleFrame<27>	1	
4	LAT_ADC<0>	1	needed ADC Latency from 0 to 3
5	LAT_ADC<1>	1	
6	AsicMode<0>	1	00 → H2GEIC 01 → CALO3g (2 ADCs) 10 → CALO4g (1 ADC, 4 gains) 11 → STATUS (not an input mode; used for I2C-read output only)
7	AsicMode<1>	0	

Table V.64: Register #3

Bit	Name	Default	Description
0	SC_testRAM_data<0>	1	Default test RAM pattern
1	SC_testRAM_data<0>	0	
2	SC_testRAM_data<0>	1	
3	SC_testRAM_data<0>	0	
4	SC_testRAM_data<0>	1	
5	SC_testRAM_data<0>	0	
6	SC_testRAM_data<0>	1	
7	SC_testRAM_data<0>	0	

Table V.65: Register #4

Bit	Name	Default	Description
0	SC_testRAM_data<0>	1	Default test RAM pattern
1	SC_testRAM_data<0>	0	
2	SC_testRAM_data<0>	1	
3	SC_testRAM_data<0>	0	
4	SC_testRAM_data<0>	1	
5	SC_testRAM_data<0>	0	
6	SC_testRAM_data<0>	1	
7	SC_testRAM_data<0>	0	

Table V.66: Register #5

Bit	Name	Default	Description
0	SC_testRAM_data<0>	1	Default test RAM pattern
1	SC_testRAM_data<0>	0	
2	SC_testRAM_data<0>	1	
3	SC_testRAM_data<0>	0	
4	SC_testRAM_data<0>	1	
5	SC_testRAM_data<0>	0	
6	SC_testRAM_data<0>	1	
7	SC_testRAM_data<0>	0	

Table V.67: Register #6

Bit	Name	Default	Description
0	SC_testRAM_data<0>	1	Default test RAM pattern
1	SC_testRAM_data<0>	0	
2	SC_testRAM_data<0>	1	
3	SC_testRAM_data<0>	0	
4	SC_testRAM_data<0>	1	
5	SC_testRAM_data<0>	0	
6	SC_testRAM_data<0>	1	
7	SC_testRAM_data<0>	0	

Table V.68: Register #7

Bit	Name	Default	Description
0	OFF_LDO	0	
1	N.A.		
2	N.A.		
3	N.A.		
4	N.A.		
5	N.A.		
6	N.A.		
7	N.A.		

Table V.69: Register #8

Bit	Name	Default	Description
0	N.A.		
1	N.A.		
2	N.A.		
3	N.A.		
4	N.A.		
5	N.A.		
6	N.A.		
7	N.A.		

Table V.70: Register #9

Bit	Name	Default	Description
0	N.A.		
1	N.A.		
2	N.A.		
3	N.A.		
4	N.A.		
5	N.A.		
6	N.A.		
7	N.A.		

Table V.71: Register #10

Bit	Name	Default	Description
0	Ret_time<0>	0	Time RETENTION SC parameter for test Ram RETENTION time
1	Ret_time<1>	0	
2	Ret_time<2>	0	
3	Ret_time<3>	0	
4	Ret_time<4>	1	
5	Ret_time<5>	0	
6	Ret_time<6>	0	
7	Ret_time<7>	1	

Table V.72: Register #11

Bit	Name	Default	Description
0	Ret_time<8>	1	Time RETENTION SC parameter for test Ram RETENTION time
1	Ret_time<9>	0	
2	Ret_time<10>	0	
3	Ret_time<11>	0	
4	ZeroSuppressEn	1	SC: If =1 -> DaqData out with zero suppress, only hit channels will be output, If=0 -> DaqData all CH will be output on link
5	CharacterisationSC	0	"calibration" mode
6	TestMode	0	Test mode to enter BIST (test of DRAM)
7	RUN	0	Run mode

Table V.73: Register #12

Bit	Name	Default	Description
0	TimeOffset<0>	1	After reset, the time counter starts from this offset value.
1	TimeOffset<1>	0	
2	TimeOffset<2>	0	
3	TimeOffset<3>	0	
4	TimeOffset<4>	0	
5	TimeOffset<5>	0	
6	TimeOffset<6>	0	
7	TimeOffset<7>	0	

Table V.74: Register #13

Bit	Name	Default	Description
0	TimeOffset<8>	0	After reset, the time counter starts from this offset value.
1	TimeOffset<9>	0	
2	TimeOffset<10>	0	
3	TimeOffset<11>	0	
4	TimeOffset<12>	0	
5	TimeOffset<13>	0	
6	TimeOffset<14>	0	
7	TimeOffset<15>	0	

Table V.75: Register #14

Bit	Name	Default	Description
0	TimeOffset<16>	0	After reset, the time counter starts from this offset value.
1	TimeOffset<17>	0	
2	TimeOffset<18>	0	
3	TimeOffset<19>	0	
4	TimeOffset<20>	0	
5	TimeOffset<21>	0	
6	TimeOffset<22>	0	
7	TimeOffset<23>	0	

Table V.76: Register #15

Bit	Name	Default	Description
0	N_VALUE<0>	0	N consecutive snapshot of the digitised data normal op = 5
1	N_VALUE<1>	0	
2	N_VALUE<2>	1	
3	ADCsampleR	1	ADC -> 1: Sample on rising edge, 0: Sample on falling edge
4	SC_testRAM_cmd	0	Bit set to test/fill RAM with specific pattern
5	EdgeSel_T1A	0	Selection clock edge of the fast command unit
6	In_inv_cmd_rx	0	Invert fast command decoding
7	n_counter_rst	1	Reset SEU counter of the serializer

Table V.77: Register #16

Bit	Name	Default	Description
0	Time_trigger<0>	1	Generate Special header on links @ time = Time_trigger
1	Time_trigger<1>	1	
2	Time_trigger<2>	1	
3	Time_trigger<3>	1	
4	Time_trigger<4>	0	
5	Time_trigger<5>	0	
6	Time_trigger<6>	0	
7	Time_trigger<7>	0	

Table V.78: Register #17

Bit	Name	Default	Description
0	Time_trigger<8>	0	Generate Special header on links @ time = Time_trigger
1	Time_trigger<9>	0	
2	Time_trigger<10>	0	
3	Time_trigger<11>	0	
4	Time_trigger<12>	0	
5	Time_trigger<13>	0	
6	Time_trigger<14>	0	
7	Time_trigger<15>	0	

Table V.79: Register #18

Bit	Name	Default	Description
0	Time_trigger<16>	0	Generate Special header on links @ time = Time_trigger
1	Time_trigger<17>	0	
2	Time_trigger<18>	0	
3	Time_trigger<19>	0	
4	Time_trigger<20>	0	
5	Time_trigger<21>	0	
6	Time_trigger<22>	0	
7	Time_trigger<23>	0	

Table V.80: Register #19

Bit	Name	Default	Description
0	Val_AF <0>	1	Fixed Almost full value for Ram
1	Val_AF <1>	1	
2	Val_AF <2>	0	
3	Val_AF <3>	1	
4	Val_AF <4>	1	
5	Val_AF <5>	0	
6	TOAsampleR	1	TOA -> 1: Sample on rising edge, 0: Sample on falling edge
7	TOTsampleR	1	TOT -> 1: Sample on rising edge, 0: Sample on falling edge

Table V.81: Register #20

7 "Top sub-block" I2C parameters

Bit	Name	Default	Description
0	HF_test_TSPFF	0	Frequency for testing TSPFF: "0" = 40MHz, "1" = 640MHz
1	ON_Test_TSPFF	0	"1" = enable the TSPFF test circuit
2	N.A.		
3	N.A.		
4	N.A.		
5	N.A.		
6	N.A.		
7	N.A.		

Table V.82: Register #0

Bit	Name	Default	Description
0	EN_START_UP	1	Enable PLL
1	DIV_PLL_A	1	Choose the "OUT_CLK_SEL_READ" output frequency <A:B>: "00" : 40 MHz "10" : 160 MHz "01" : 320 MHz "11" : 1280 MHz
2	DIV_PLL_B	1	
3	FOLLOWER_PLL_EN	1	Activate the VTC for the bias PLL bias (pump charge injection): "0" : OFF "1" : VTC 6 bits "BIAS_I_PLL_D<0:5>
4	Sel_strobe_ext	0	"0": CalPulseInt; "1": Strobe_ext pin
5	N.A.		
6	Sel_error	0	"0": I2C error; "1": fast command error
7	Sel_lock	0	"0": PLL lock; "1": fast command lock

Table V.83: Register #1

Bit	Name	Default	Description
0	VOUT_INIT_EXT_EN	0	Activate the DAC for V_PUMP_P voltage : "0" : external PAD "VOUT_INIT_EXT PLL" "1" : 5 bits DAC "VOUT_INIT_EXT_D<0:4>"
1	VOUT_INIT_EXT_D<0>	0	5 bits DAC for VOUT_INIT PLL voltage : "00000" = 0 V "11111" = 1.2 V
2	VOUT_INIT_EXT_D<1>	0	
3	VOUT_INIT_EXT_D<2>	0	
4	VOUT_INIT_EXT_D<3>	0	
5	VOUT_INIT_EXT_D<4>	0	
6	EN_REF_BG	1	Activate the BANDGAP source 1V to the calibration part "0" : External PAD "EXT_REF_TDC" "1" : Internal 1V Bandgap "BG_1V"
7	VOUT_INIT_EN	0	Activate the voltage load in "V_PUMP_P" of the PLL pump charge output : "0" : High Z pump charge (Default) "1" : VOUT_INIT voltage load "VOUT_INIT MODE"

Table V.84: Register #2

Bit	Name	Default	Description
0	EN_HIGH_CAPA	1	Add another large capacitor in the PLL LPF
1	BIAS_I_PLL_D<0>	0	Configure the VTC the bias PLL BIAS_N_PLL bias (pump charge injection current) : Current = DATA<0:5> Weight addition (default 30 μA) "base" : 50 nA <0>: 100 nA <1>: 500 nA <2>: 2,5 μ A <3>: 5 μ A <4>: 25 μ A <5>: 50 μ A
2	BIAS_I_PLL_D<1>	0	
3	BIAS_I_PLL_D<2>	0	
4	BIAS_I_PLL_D<3>	1	
5	BIAS_I_PLL_D<4>	1	
6	BIAS_I_PLL_D<5>	0	
7	EN_RCG	0	Active the RCG: "0" : OFF "1" : ON : RCG activated

Table V.85: Register #3

Bit	Name	Default	Description
0	INIT_DAC_EN	0	Activate the DAC for the VCO voltage : "0" : external PAD "INIT_EXT" "1" : 5 bits DAC "INIT_D<0:4>"
1	INIT_D<0>	0	Tune VCO frequency of the RCG: 5 bits DAC <0:4> (1kΩ x 32)
2	INIT_D<1>	0	
3	INIT_D<2>	0	
4	INIT_D<3>	0	
5	INIT_D<4>	0	
6	Rcg_gain<0>	0	Choose the "OUT_CLK_RCG" output frequency <A:B>: "00" : /4096 "10" : /512 "01" : /32 "11" : pure
7	Rcg_gain<1>	0	

Table V.86: Register #4

Bit	Name	Default	Description
0	EN<0>	1	Current value of the CLPS drivers (Data/Trigger)
1	EN<1>	1	
2	EN<2>	0	
3	ENpE<0>	0	Current value of the CLPS pre-emphasis driver (Data/Trigger)
4	ENpE<1>	0	
5	ENpE<2>	0	
6	S<0>	0	Delay value of the CLPS pre-emphasis driver (Data/Trigger)
7	S<1>	0	

Table V.87: Register #5

Bit	Name	Default	Description
0	EN_LOCK_CONTROL	1	Active the PLL lock detector : "0" : OFF "1" : ON : PLL lock detector activated
1	ERROR_LIMIT_SC<0>	0	Configure the maximal error limit between EXT 40 MHz & PLL 40 MHz : "000" : 0 difference "100" : 1 difference ... "111" : 7 difference
2	ERROR_LIMIT_SC<1>	1	
3	ERROR_LIMIT_SC<2>	0	
4	EN_trig	0	
5	PLL_Lockec_sc	0	Slow-control lock pll signal
6	EN_probe_pll	0	Enable probe PLL
7	EN_PhaseShift	1	Enable phase shifter

Table V.88: Register #6

Bit	Name	Default	Description
0	Phase_ck<0>	0	Phase shifter value for 40M & 160M clocks
1	Phase_ck<1>	0	
2	Phase_ck<2>	0	
3	Phase_ck<3>	0	
4	Phase_strobe<0>	0	Phase shifter value for calibration pulse
5	Phase_strobe<1>	0	
6	Phase_strobe<2>	0	
7	Phase_strobe<3>	0	

Table V.89: Register #7

Bit	Name	Default	Description
0	B_out<0>	0	Read e-fuse values
1	B_out<1>	0	
2	B_out<2>	0	
3	B_out<3>	0	
4	B_out<4>	0	
5	B_out<5>	0	
6	B_out<6>	0	
7	B_out<7>	0	

Table V.90: Register #8 - read only

Bit	Name	Default	Description
0	B_in<0>	0	Write e-fuse values
1	B_in<1>	0	
2	B_in<2>	0	
3	B_in<3>	0	
4	B_in<4>	0	
5	B_in<5>	0	
6	B_in<6>	0	
7	B_in<7>	0	

Table V.91: Register #9

Bit	Name	Default	Description
0	B_out<8>	0	Read e-fuse values
1	B_out<9>	0	
2	B_out<10>	0	
3	B_out<11>	0	
4	B_out<12>	0	
5	B_out<13>	0	
6	B_out<14>	0	
7	B_out<15>	0	

Table V.92: Register #10 - read only

Bit	Name	Default	Description
0	B_in<8>	0	Write e-fuse values
1	B_in<9>	0	
2	B_in<10>	0	
3	B_in<11>	0	
4	B_in<12>	0	
5	B_in<13>	0	
6	B_in<14>	0	
7	B_in<15>	0	

Table V.93: Register #11

Bit	Name	Default	Description
0	B_out<16>	0	Read e-fuse values
1	B_out<17>	0	
2	B_out<18>	0	
3	B_out<19>	0	
4	B_out<20>	0	
5	B_out<21>	0	
6	B_out<22>	0	
7	B_out<23>	0	

Table V.94: Register #12 - read only

Bit	Name	Default	Description
0	B_in<16>	0	Write e-fuse values
1	B_in<17>	0	
2	B_in<18>	0	
3	B_in<19>	0	
4	B_in<20>	0	
5	B_in<21>	0	
6	B_in<22>	0	
7	B_in<23>	0	

Table V.95: Register #13

Bit	Name	Default	Description
0	B_out<24>	0	Read e-fuse values
1	B_out<25>	0	
2	B_out<26>	0	
3	B_out<27>	0	
4	B_out<28>	0	
5	B_out<29>	0	
6	B_out<30>	0	
7	SROUT	0	Srout read

Table V.96: Register #14 - read only

Bit	Name	Default	Description
0	B_in<24>	0	Write e-fuse values
1	B_in<25>	0	
2	B_in<26>	0	
3	B_in<27>	0	
4	B_in<28>	0	
5	B_in<29>	0	
6	B_in<30>	0	E-fuse read signal
7	B_in<31>	0	E-fuse write signal

Table V.97: Register #15

Bit	Name	Default	Description
0	BistRamErrors<16>	0	Error Count per DRAM (4 bits): Each bit represents a possible error in one of four test patterns (bit set to "1" indicates an error). With 6 DRAM blocks, this yields a total of 24 bits of error information.
1	BistRamErrors<17>	0	
2	BistRamErrors<18>	0	
3	BistRamErrors<19>	0	
4	BistRamErrors<20>	0	
5	BistRamErrors<21>	0	
6	BistRamErrors<22>	0	
7	BistRamErrors<23>	0	

Table V.98: Register #16 - read only

Bit	Name	Default	Description
0	BistRamErrors<8>	0	Error Count per DRAM (4 bits): Each bit represents a possible error in one of four test patterns (bit set to "1" indicates an error). With 6 DRAM blocks, this yields a total of 24 bits of error information.
1	BistRamErrors<9>	0	
2	BistRamErrors<10>	0	
3	BistRamErrors<11>	0	
4	BistRamErrors<12>	0	
5	BistRamErrors<13>	0	
6	BistRamErrors<14>	0	
7	BistRamErrors<15>	0	

Table V.99: Register #17 - read only

Bit	Name	Default	Description
0	BistRamErrors<0>	0	Error Count per DRAM (4 bits): Each bit represents a possible error in one of four test patterns (bit set to "1" indicates an error). With 6 DRAM blocks, this yields a total of 24 bits of error information.
1	BistRamErrors<1>	0	
2	BistRamErrors<2>	0	
3	BistRamErrors<3>	0	
4	BistRamErrors<4>	0	
5	BistRamErrors<5>	0	
6	BistRamErrors<6>	0	
7	BistRamErrors<7>	0	

Table V.100: Register #18 - read only

Bit	Name	Default	Description
0	Status<0>	0	FSM state from global startup state machine
1	Status<1>	0	
2	Status<2>	0	
3	Bist_dones<0>	0	Flags indicates Bists complete verifications and remain in Finish state until reset
4	Bist_dones<1>	0	
5	vss	0	Always "0"
6	vss	0	
7	vss	0	

Table V.101: Register #19 - read only

Bit	Name	Default	Description
0	Lock_count<0>	0	Running count of number of times the phase lock is successful: no-wrap,cleared on reset
1	Lock_count<1>	0	
2	Lock_count<2>	0	
3	Lock_count<3>	0	
4	Lock_count<4>	0	
5	Lock_count<5>	0	
6	Lock_count<6>	0	
7	Lock_count<7>	0	

Table V.102: Register #20 - read only

Bit	Name	Default	Description
0	Fc_error_count<0>	0	Running count of number of times the phase lock is successful: no-wrap,cleared on reset
1	Fc_error_count<1>	0	
2	Fc_error_count<2>	0	
3	Fc_error_count<3>	0	
4	Fc_error_count<4>	0	
5	Fc_error_count<5>	0	
6	Fc_error_count<6>	0	
7	Fc_error_count<7>	0	

Table V.103: Register #21 - read only

Bit	Name	Default	Description
0	Err_count0<0>	0	Number of pll_lock loss seen by the serializer
1	Err_count0<1>	0	
2	Err_count0<2>	0	
3	Err_count0<3>	0	
4	Err_count0<4>	0	
5	Err_count0<5>	0	
6	Err_count0<6>	0	
7	Err_count0<7>	0	

Table V.104: Register #22 - read only

APPENDIX **A**

PROCEDURES

1 Preamplifier gain

Parameters:

- Cf_comp<0:1>
- Cf<0:3>
- Rf<0:3>

Procedure:

- Determine the MIP.
- Determine the SNR wanted for the MIP.
- Find the ADC range associated with those values:

$$range = 1024 \times \frac{MIP}{SNR} \quad (A.1)$$

- Lookup Tab. B.1 and B.2 for Si; Tab. B.3, B.4 and B.5 for LAr, for the correct Cf_comp, Cf and Rf values.

Recommended values based on simulations (for both Si at 27°C and LAr at -186°C):

- Cf_comp = 200 fF = 2.
- Cf = 450 fF = 9.
- Rf = 1 MΩ = 0.

2 DC outpa

Parameter:

- Inputdac<0:7>
- dac_pol

Procedure:

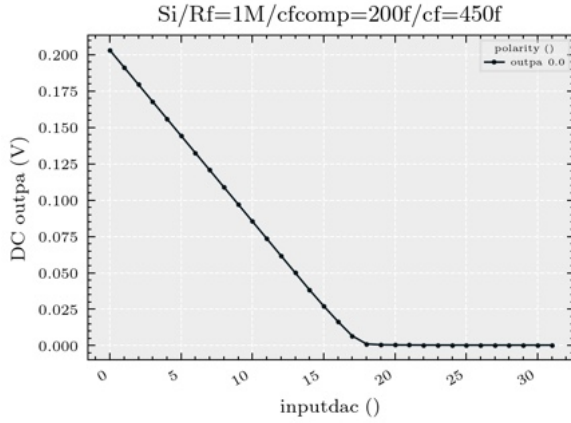
- Monitor outpa (probe_VrefPa accessible through probe_dc1_0 address 19).
- Change Inputdac until outpa is closest to 200mV.

Recommended value based on simulations:

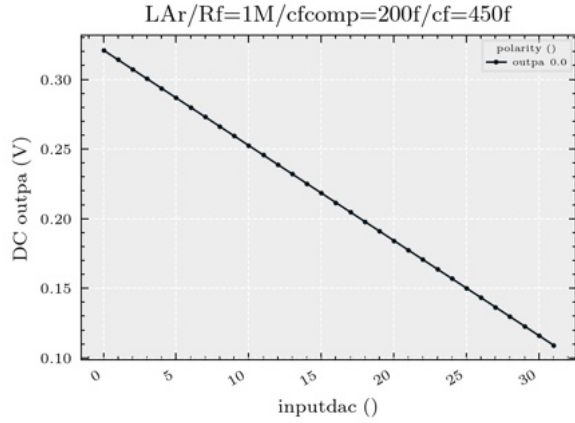
- dac_pol = 0

- Inputdac<0:7> = 0 at 27°C for Rf = 0.
- Inputdac<0:7> = 2 at -30°C for Rf = 0.
- Inputdac<0:7> = 17 at -186°C for Rf = 0.
- Inputdac<0:7> = 0 at 27°C for Rf = 1.
- Inputdac<0:7> = 27 at -30°C for Rf = 1.
- Inputdac<0:7> = 31 at -186°C for Rf = 1 (not sufficient to bring outpa to the desired value).

The figures below (Fig. A.1 and Fig. A.2), respectively present the DC level of the output of the preamplifier with different values of Inputdac, and different dac polarities.

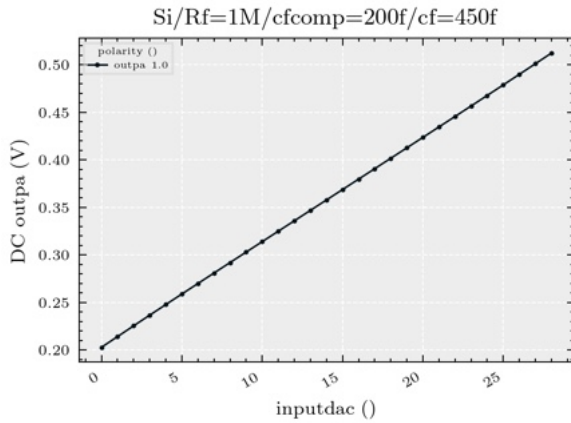


(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C

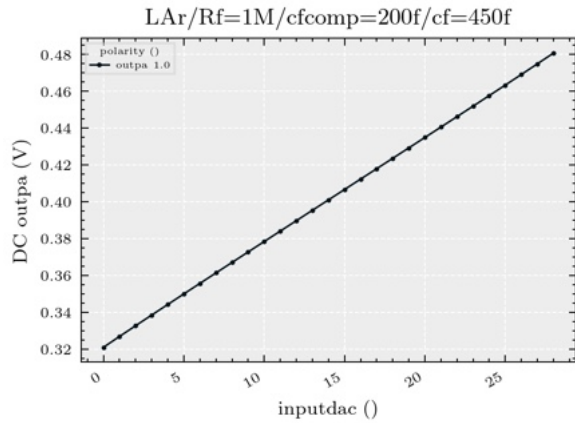


(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure A.1: outpa DC for different values of Inputdac - negative polarity



(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C



(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure A.2: outpa DC for different values of Inputdac - positive polarity

Obviously, Inputdac can also be used to trim channel per channel and compensate for leakage current.

3 Vref_sk

Parameter:

- Refi<0:1>

Procedure:

- Monitor Vref_sk (Vref_sk accessible through probe_dc1_1 address 21).
- Change Refi to have Vref_sk closest to 170mV.

Recommended value based on simulations:

- $\text{Refi}_{<0:1>} = 0$ for Si at 27°C
- $\text{Refi}_{<0:1>} = 3$ for LAr at -186°C

The figures below (Fig. A.3) shows the voltage reference $V_{\text{ref_sk}}$ as a function of Refi . The impact of Refi at cryogenic temperature might very be inaccurate.

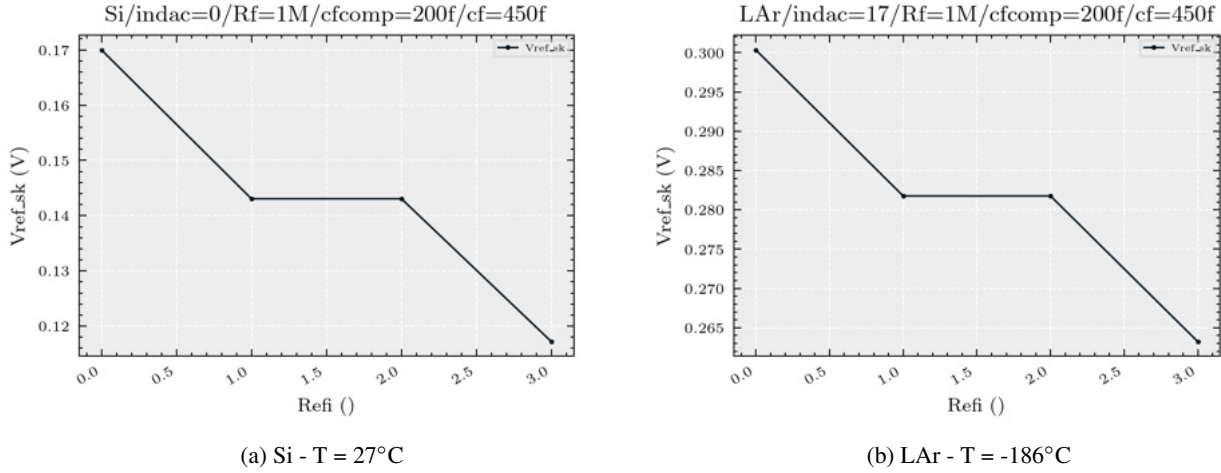


Figure A.3: $V_{\text{ref_sk}}$ for different Refi

4 Threshold ToA and ToT

Parameters:

- $\text{Toa_vref}_{<0:9>}$
- $\text{trim_toa}_{<0:5>}$
- $\text{Tot_vref}_{<0:9>}$
- $\text{trim_tot}_{<0:5>}$

Procedure:

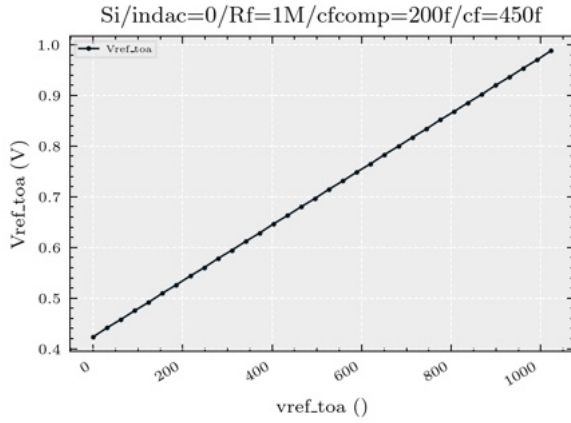
- Sweep Toa_vref and read the ToA occupancy for each sweep value (while injecting a charge).
- Pick the appropriate value for Toa_vref (lowest value for which all the channel see ToA).
- Sweep trim_toa and read the ToA occupancy for each sweep value.
- Pick the appropriate value for trim_toa per channel (this is the value for which all channel have the same toa occupancy).
- If the first sweep is done again after Toa_vref is globally set and the trimming of the channel is done, the S-curves should be aligned.
- Do the same for Tot_vref and trim_tot .

Recommended values based on simulations:

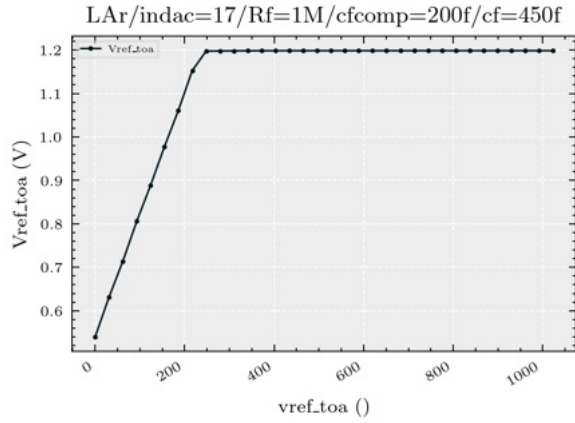
- $\text{Toa_vref}_{<0:9>} = 128$ at 27°C .
- $\text{Tot_vref}_{<0:9>} = 256$ at 27°C .
- $\text{Toa_vref}_{<0:9>} = 32$ at -186°C .
- $\text{Tot_vref}_{<0:9>} = 64$ at -186°C .
- No recommendation for $\text{trim_toa}_{<0:5>}$, depends on the channels disparities.
- No recommendation for $\text{trim_tot}_{<0:5>}$, depends on the channels disparities.

The figures below (Fig. A.4) show the impact of the slow control parameter Toa_vref on the global threshold value of the

ToA. Figure A.6 shows the same for the ToT.



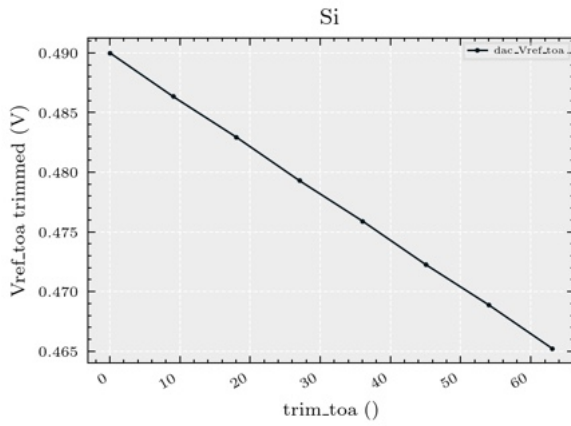
(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C



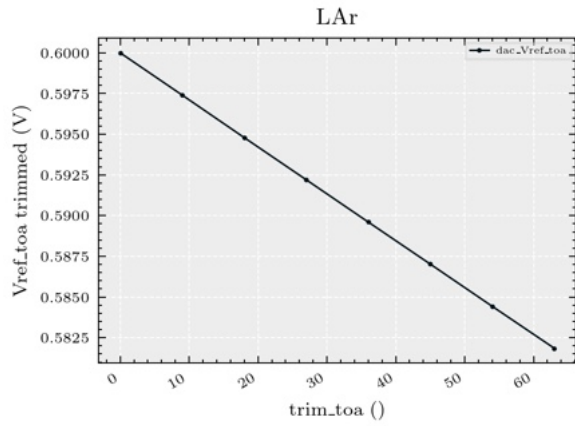
(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure A.4: ToA threshold for different Toa_vref

The figures below (Fig. A.5) show the impact of the channel wise trimming trim_toa on the ToA threshold, this parameter is meant to be used to correct for process and mismatch variations between channels. The same can be said for Fig. A.7 with respect to ToT.

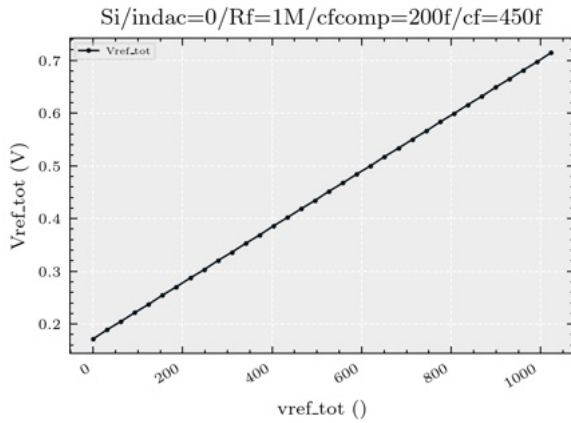


(a) Si - T = 27°C

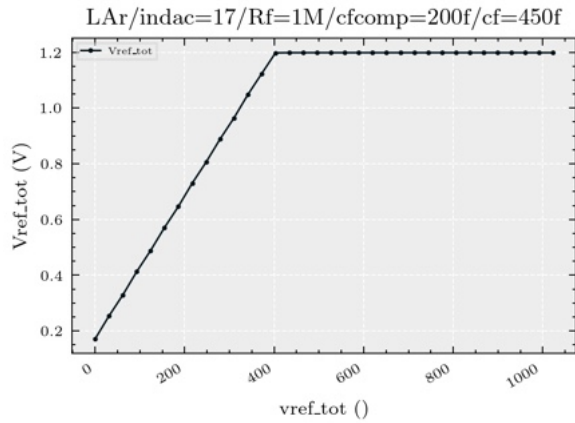


(b) LAr - T = -186°C

Figure A.5: ToA threshold for different trim_toa with Vref_toa constant



(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C



(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure A.6: ToT threshold for different Tot_vref

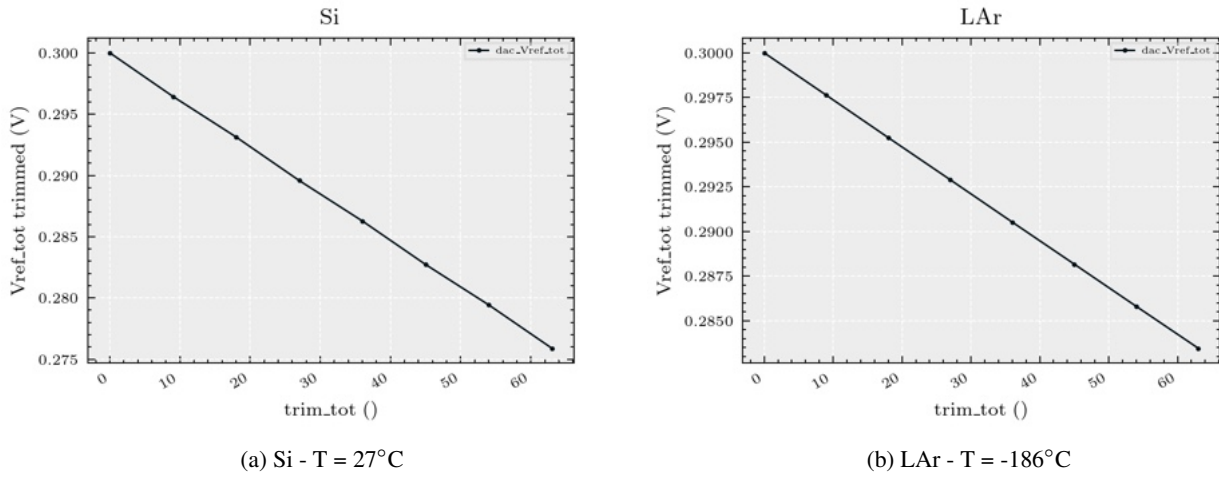


Figure A.7: ToT threshold for different trim_tot with Vref_tot constant

5 Vref_noinv

Parameter:

- Noinv_vref<0:9>

Procedure:

- Monitor Vref_noinv (Vref_noinv accessible through probe_dc1_1 address 22).
- Change Noinv_vref to have Vref_noinv closest to 230mV.

Recommended value based on simulations:

- Noinv_vref<0:9> = 128 at 27°C.
- Noinv_vref<0:9> = 32 at -186°C.

The figures below (Fig. A.8) present the impact of the slow control parameter Noinv_vref on Vref_noinv, the voltage reference of the RtR outputting out_noinv.

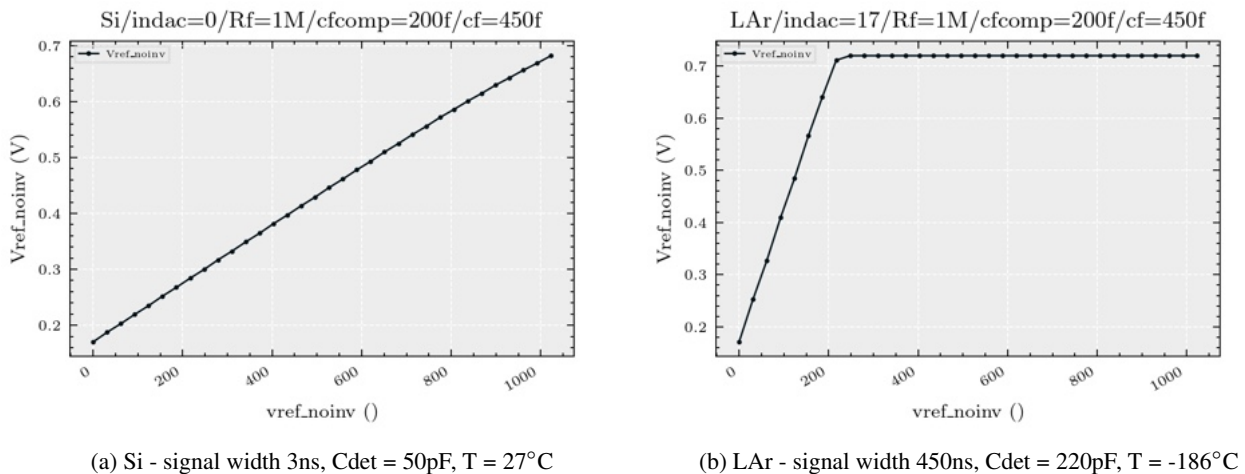


Figure A.8: Vref_noinv (out_noinv bias) for different Noinv_vref

6 Vref_inv

Parameter:

- Inv_vref<0:9>

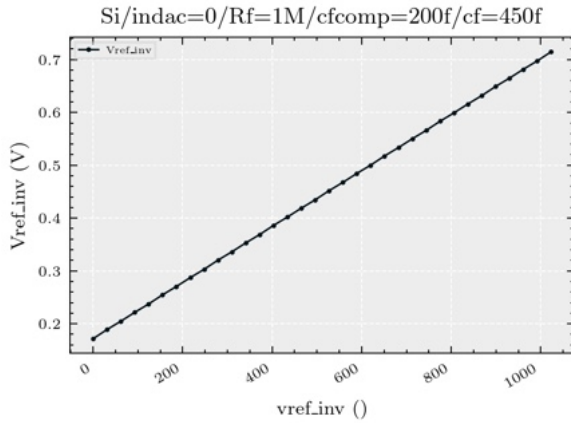
Procedure:

- Monitor Vref_inv (Vref_inv accessible through probe_dc1_1 address 23).
- Change Inv_vref to have Vref_inv closest to 460mV.

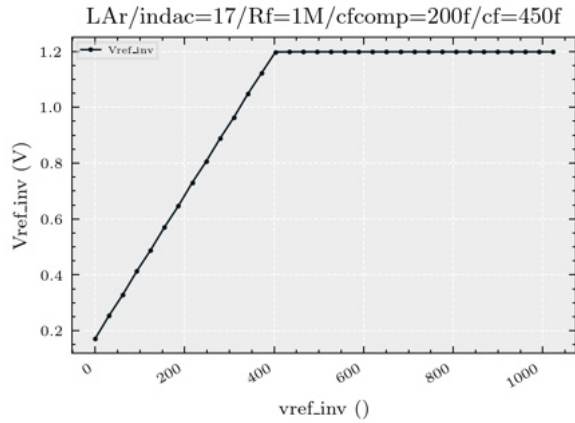
Recommended value based on simulations:

- Inv_vref<0:9> = 512 at 27°C.
- Inv_vref<0:9> = 128 at -186°C.

The figures below (Fig. A.9) present the impact of the slow control parameter Inv_vref on Vref_inv, the voltage reference of the RtR outputting out_inv.



(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C



(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure A.9: Vref_inv (out_inv bias) for different Inv_vref

7 Pedestal trimming

Parameter:

- trim_inv<0:5>

Procedure:

- Sweep the trim_inv values.
- Read the pedestal of each channel for each sweep value.
- Pick a pedestal value common to all channel and find the correct associated trim_inv per channel.

Recommended value based on simulations:

- No recommendation, depends on the channel variations and the desired pedestal value.

The figure below (Fig. A.10) highlights the impact of the slow control parameter trim_inv on the voltage reference of the RtR outputting out_inv, this is the reason for the pedestal trimming.

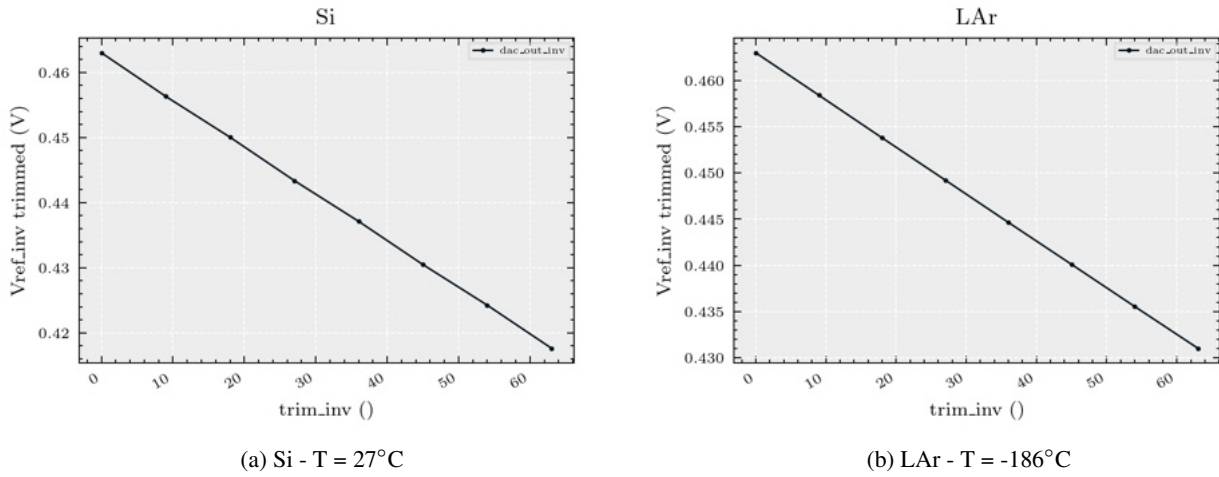


Figure A.10: out_inv bias for different trim_inv with Vref_inv constant

8 Power consumption versus Noise

Parameter:

- trim_vbi_pa<0:3>

Procedure:

- Know the MIP and the SNR wanted for this MIP.
- Know the detector capacitance used.
- Set a noise limit in electron at a given detector capacitance.
- Look at Fig. A.16 and choose a trim_vbi_pa (in the plot trim_vbi_pa is the inverse of dacb_vbi_pa).

Recommended value based on simulations:

- No recommendation, depends on personal priorities (power or noise).

The figure below (Fig. A.11) shows the impact of the inverse of trim_vbi_pa on the power consumption of the analog part per channel. Obviously the trend is the same for the complete power consumption per channel, with an offset taking into account the digital, the ADC, the TDCs and the PLL (see Tab. A.1 for the complete power consumption estimate).

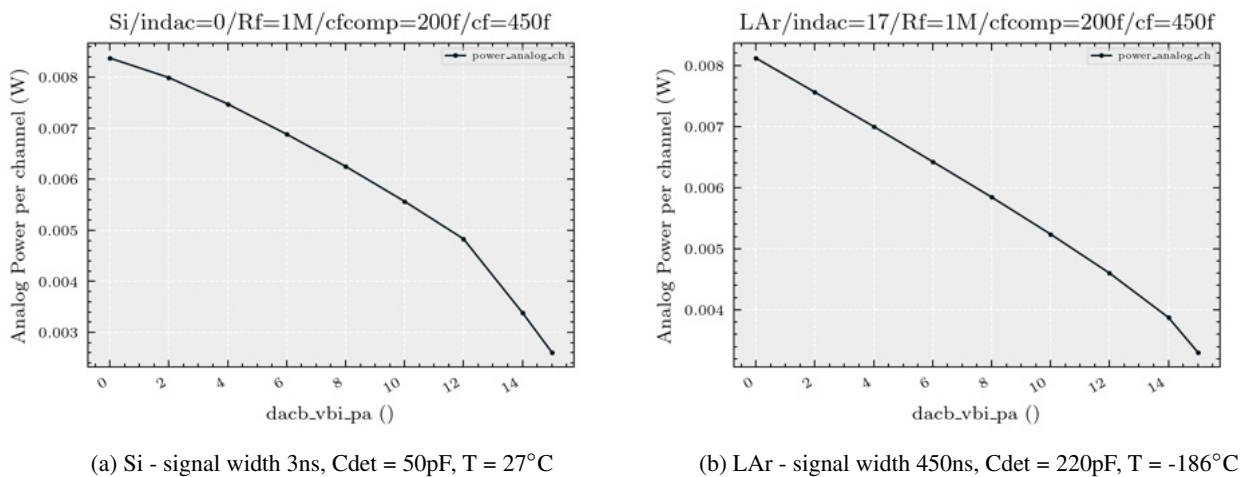
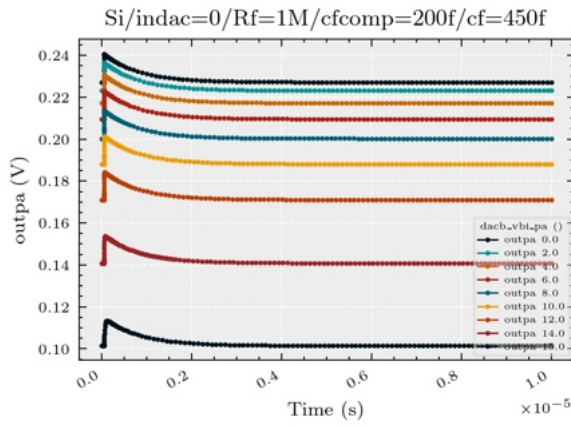
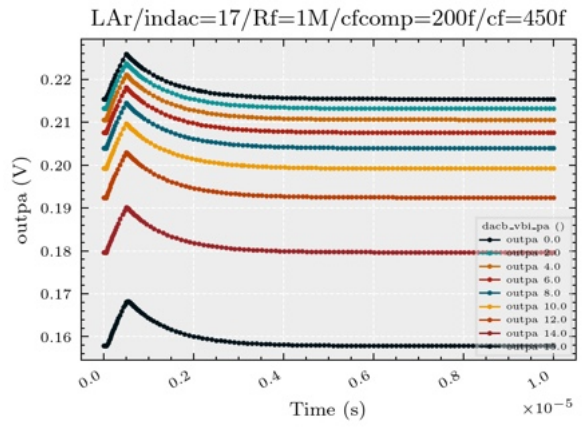


Figure A.11: Power as a function of trim_vbi_pa

The figures below (Fig. A.12 and Fig. A.13) represent the output of the preamplifier and of the non-inverted buffer (right before the ADC). The DC level shifts, this could in theory be compensated by the Inputdac.

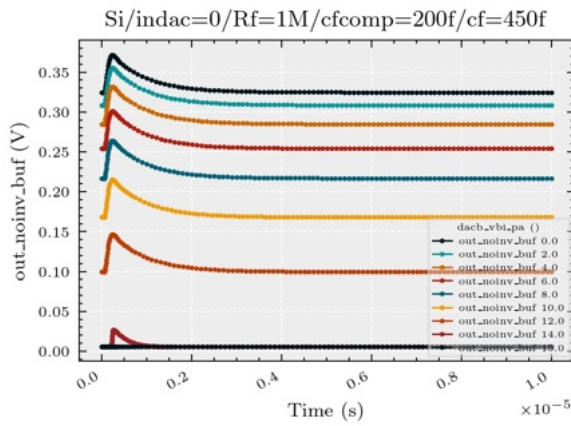


(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C

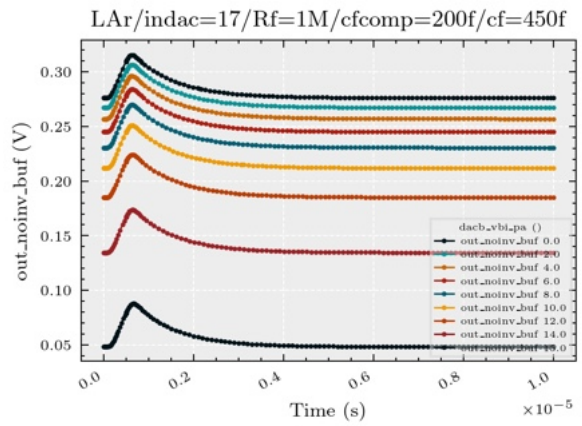


(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure A.12: Signal outpa for different trim_vbi_pa



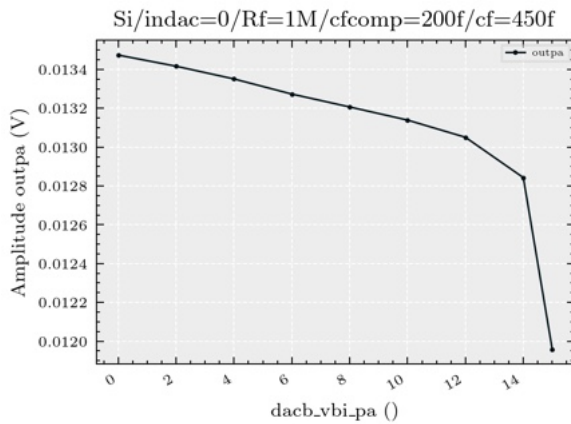
(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C



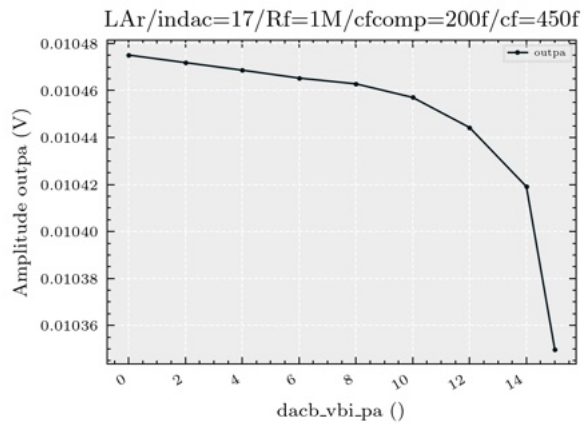
(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure A.13: Signal out_noinv_buf for different trim_vbi_pa

The figures below (Fig. A.14 and Fig. A.15) represent the amplitude of the output of the preamplifier and of the non-inverted buffer (right before the ADC). The amplitude at the output of the preamplifier changes, but the amplitude right before the ADC is somewhat constant. Since the ENC is calculated before the ADC and takes into account both the amplitude and the noise, it can be assumed that any increase in the ENC would be directly linked to noise increase.

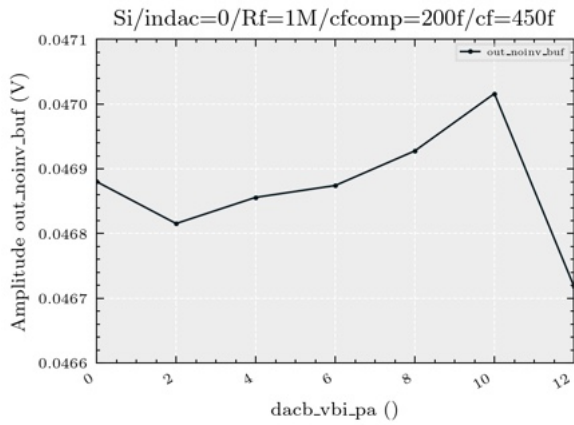


(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C

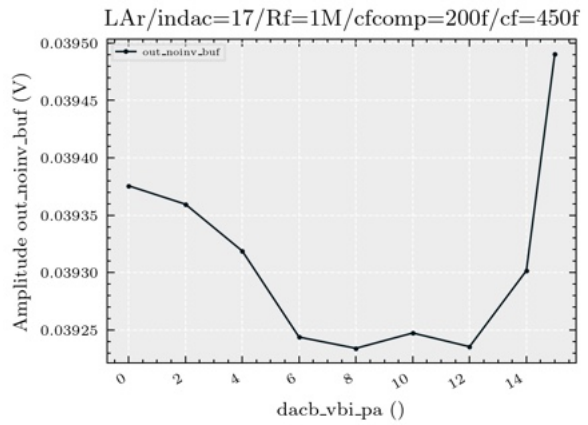


(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure A.14: Amplitude of the signal outpa for different trim_vbi_pa



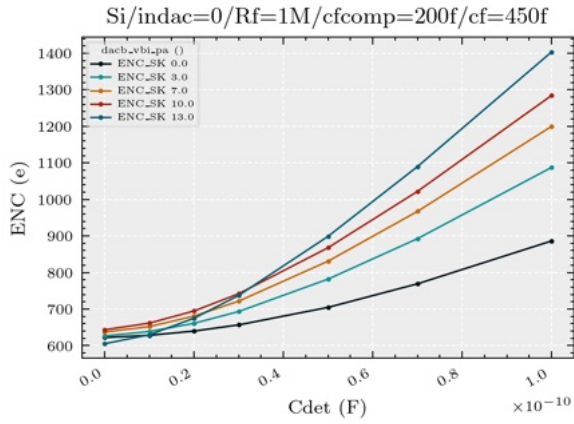
(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C



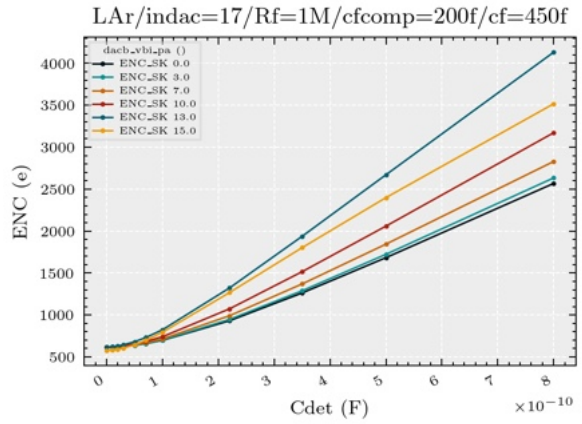
(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure A.15: Amplitude of the signal out_noinv_buf for different trim_vbi_pa

The figure below (Fig. A.16) present the ENC before the ADC as a function of the detector capacitance for different trim_vbi_pa (inverse of dacb_vbi_pa). In general, it seems that the noise increase when trim_vbi_pa decreases. Note that by default trim_vb_pa is at 7 (so dacb_vbi_pa by default is 8).



(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C



(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure A.16: ENC vs Cdet for different trim_vbi_pa

	Power (mW/ch)	Comments
Analog Channel	2.6 - 8.4	FE - Bias - DAC - Reference Voltages (6.7 by default)
Digital	82/36	Digital Processing - DRAM - Align Buffer - Fast Command
ADC	0.881	At 40 MHz. At 10 MHz, it would be 0.22 mW
ToA TDC	0.101 - 2.2	Depends on the hit rate. TDC is off when unused.
ToT TDC	0.101 - 2.2	Depends on the hit rate. TDC is off when unused.
PLL	1.91/36	
Serializer + E-Link	2 × 6/36	Data ch 0-17 and Data ch 18-35.
Total	6.35 - 16.35	With reasonable values for the ToT and ToA power consumption (respectively max×0.1 and max×0.5): 7.47 - 13.27 mW/ch depending on the required noise.

Table A.1: Power simulations of the entire ASIC

9 ToT gain

Parameter:

- gain_tot (often also called itot)

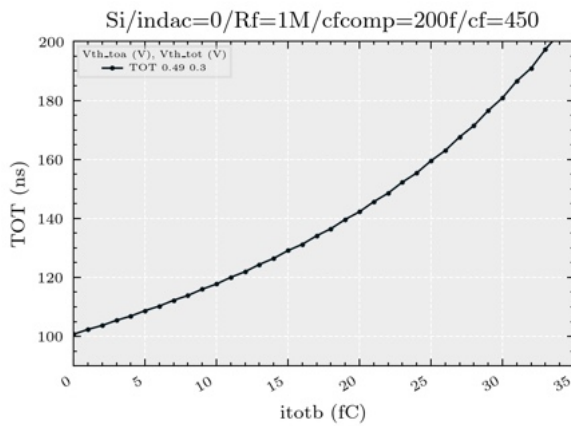
Procedure:

- Measure the ToT for the highest charge.
- Change gain_tot until the ToT is not saturated by this charge.
- If no value of gain_tot can make the ToT unsaturated (the max ToT is 200 ns), then pick the highest gain_tot.

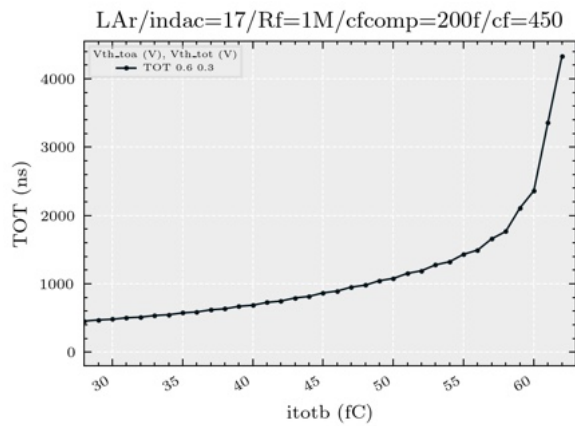
Recommended value based on simulations:

- gain_tot = 48-63 for Si at 27°C.
- gain_tot = 35 for LAr at -186°C.

The figure below (Fig. A.17) shows the importance of setting gain_tot (the inverse of itotb) correctly in order to see the entire ToT range.



(a) Si - signal width 3ns, Cdet = 50pF, T = 27°C



(b) LAr - signal width 450ns, Cdet = 220pF, T = -186°C

Figure A.17: ToT as a function of itot

10 Other Important Parameters

10.a Zero suppression

Parameter:

- ZeroSuppressEn = 1 (if zero suppression is wanted)

10.b Necessary for the ASIC to be used

Parameter:

- AsicMode<0:1> = 00.
- CharacterisationSC = 1 (if both ADC and ToT need to be seen at the same time).
- RUN = 1.

10.c Internal calibration

Parameter:

- Calib<0:11>
- IntCtest
- ExtCtest
- LowRange
- HighRange

The slow control parameter Calib is used with IntCTest enabled and ExtCTest disabled, to inject internally. The figure below (Fig. A.18) shows the ramp created when Calib is swept, this is then injected in the capacitance chosen with the parameters HighRange (10 pF) and LowRange (500fF) (at least one needs to be enabled).

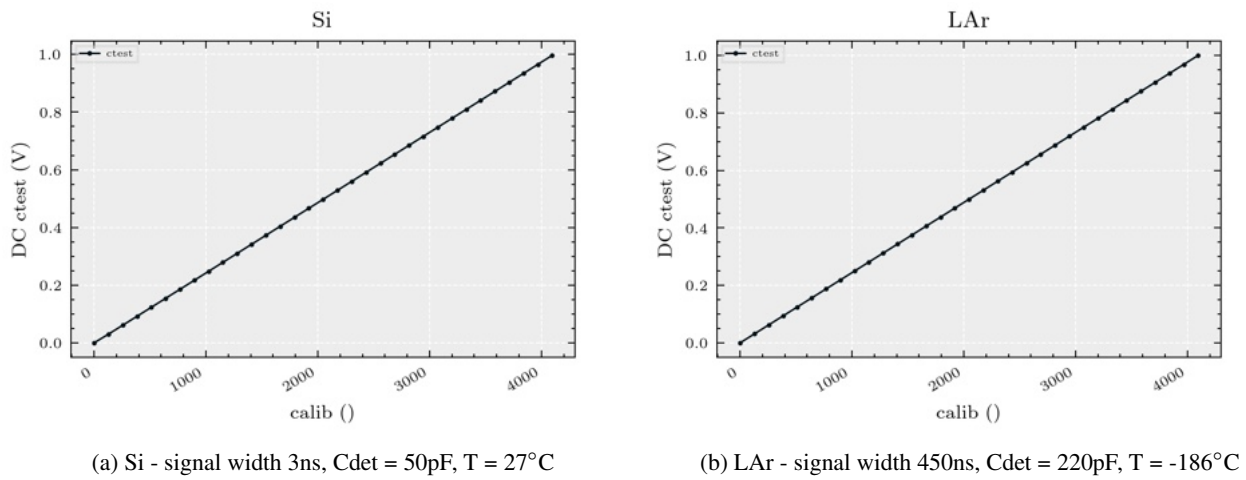


Figure A.18: Linearity of the internal injection

APPENDIX B

PREAMPLIFIER GAIN - DYNAMIC RANGE

Rf code	Cf code	Cf_comp code	RfCf (ns)	Amplitude (mV)	Dynamic Range (fC)	MIP (fC)
0	0	1	100	206.9	48	0.47
0	0	2	200	132.5	75	0.73
0	0	3	300	98.66	101	0.99
0	1	0	50	276.8	36	0.35
0	1	1	150	153.9	65	0.64
0	1	2	250	109.6	91	0.89
0	1	3	350	85.66	117	1.14
0	2	0	100	184.7	54	0.53
0	2	1	200	123.4	81	0.79
0	2	2	300	93.61	107	1.05
0	2	3	400	75.73	132	1.29
0	3	0	150	141.6	71	0.69
0	3	1	250	103.4	97	0.95
0	3	2	350	81.83	122	1.19
0	3	3	450	67.91	147	1.44
0	4	0	200	115.5	87	0.85
0	4	1	300	89.09	112	1.09
0	4	2	400	72.76	137	1.34
0	4	3	500	61.55	162	1.58
0	5	0	250	97.8	102	1
0	5	1	350	78.37	128	1.25
0	5	2	450	65.51	153	1.5
0	5	3	550	56.33	178	1.74
0	6	0	300	84.94	118	1.15
0	6	1	400	69.99	143	1.4
0	6	2	500	59.59	168	1.64
0	6	3	600	51.94	193	1.89
0	7	0	350	75.13	133	1.3
0	7	1	450	63.25	158	1.54
0	7	2	550	54.65	183	1.79
0	7	3	650	48.17	208	2.03
0	8	0	400	67.43	148	1.45
0	8	1	500	57.72	173	1.69
0	8	2	600	50.5	198	1.94
0	8	3	700	44.93	223	2.18
0	9	0	450	61.18	163	1.59
0	9	1	550	53.12	188	1.84
0	9	2	650	46.97	213	2.08

0	9	3	750	42.07	238	2.33
0	10	0	500	55.95	179	1.75
0	10	1	600	49.19	203	1.98
0	10	2	700	43.88	228	2.23
0	10	3	800	39.62	252	2.46
0	11	0	550	51.62	194	1.9
0	11	1	650	45.8	218	2.13
0	11	2	750	41.17	243	2.38
0	11	3	850	37.39	267	2.61
0	12	0	600	47.92	209	2.04
0	12	1	700	42.84	233	2.28
0	12	2	800	38.77	258	2.52
0	12	3	900	35.43	282	2.76
0	13	0	650	44.71	224	2.19
0	13	1	750	40.29	248	2.42
0	13	2	850	36.67	273	2.67
0	13	3	950	33.66	297	2.9
0	14	0	700	41.9	239	2.34
0	14	1	800	37.98	263	2.57
0	14	2	900	34.75	288	2.82
0	14	3	1000	32.03	312	3.05
0	15	0	750	39.4	254	2.48
0	15	1	850	35.96	278	2.72
0	15	2	950	33.05	303	2.96
0	15	3	1050	30.6	327	3.2
1	0	1	9	34.85	287	2.81
1	0	2	18	31.92	313	3.06
1	0	3	27	29.39	340	3.32
1	1	0	4.5	38.08	263	2.57
1	1	1	13.5	33.18	301	2.94
1	1	2	22.5	30.4	329	3.22
1	1	3	31.5	28.01	357	3.49
1	2	0	9	34.69	288	2.82
1	2	1	18	31.52	317	3.1
1	2	2	27	28.99	345	3.37
1	2	3	36	26.73	374	3.66
1	3	0	13.5	32.86	304	2.97
1	3	1	22.5	30.02	333	3.26
1	3	2	31.5	27.65	362	3.54
1	3	3	40.5	25.58	391	3.82
1	4	0	18	31.15	321	3.14
1	4	1	27	28.56	350	3.42
1	4	2	36	26.37	379	3.7
1	4	3	45	24.43	409	4
1	5	0	22.5	29.56	338	3.3
1	5	1	31.5	27.21	368	3.6
1	5	2	40.5	25.21	397	3.88
1	5	3	49.5	23.45	426	4.16
1	6	0	27	28.17	355	3.47
1	6	1	36	26.02	384	3.75
1	6	2	45	24.12	415	4.06
1	6	3	54	22.5	444	4.34
1	7	0	31.5	26.83	373	3.65
1	7	1	40.5	24.83	403	3.94
1	7	2	49.5	23.12	433	4.23
1	7	3	58.5	21.62	463	4.53
1	8	0	36	25.62	390	3.81
1	8	1	45	23.79	420	4.11

1	8	2	54	22.18	451	4.41
1	8	3	63	20.86	479	4.68
1	9	0	40.5	24.47	409	4
1	9	1	49.5	22.82	438	4.28
1	9	2	58.5	21.34	469	4.58
1	9	3	67.5	20.15	496	4.85
1	10	0	45	23.44	427	4.17
1	10	1	54	21.89	457	4.47
1	10	2	63	20.61	485	4.74
1	10	3	72	19.5	513	5.01
1	11	0	49.5	22.5	444	4.34
1	11	1	58.5	21.06	475	4.64
1	11	2	67.5	19.93	502	4.91
1	11	3	76.5	18.88	530	5.18
1	12	0	54	21.62	463	4.53
1	12	1	63	20.37	491	4.8
1	12	2	72	19.28	519	5.07
1	12	3	81	18.33	546	5.34
1	13	0	58.5	20.8	481	4.7
1	13	1	67.5	19.71	507	4.96
1	13	2	76.5	18.72	534	5.22
1	13	3	85.5	17.81	561	5.48
1	14	0	63	20.15	496	4.85
1	14	1	72	19.07	524	5.12
1	14	2	81	18.14	551	5.39
1	14	3	90	17.32	577	5.64
1	15	0	67.5	19.46	514	5.02
1	15	1	76.5	18.52	540	5.28
1	15	2	85.5	17.64	567	5.54
1	15	3	94.5	16.81	595	5.82

Table B.1: Dynamic Range Si T = 27 °C

Rf code	Cf code	Cf_comp code	RfCf (ns)	Amplitude (mV)	Dynamic Range (fC)	MIP (fC)
0	0	1	100	203.3	49	0.48
0	0	2	200	130.9	76	0.74
0	0	3	300	97.79	102	1
0	1	0	50	269.4	37	0.36
0	1	1	150	151.7	66	0.65
0	1	2	250	108.4	92	0.9
0	1	3	350	84.9	118	1.15
0	2	0	100	181.5	55	0.54
0	2	1	200	122	82	0.8
0	2	2	300	92.77	108	1.06
0	2	3	400	75.11	133	1.3
0	3	0	150	139.7	72	0.7
0	3	1	250	102.3	98	0.96
0	3	2	350	81.15	123	1.2
0	3	3	450	67.38	148	1.45
0	4	0	200	114.2	88	0.86
0	4	1	300	88.24	113	1.1
0	4	2	400	72.17	139	1.36
0	4	3	500	61.13	164	1.6
0	5	0	250	96.85	103	1.01
0	5	1	350	77.66	129	1.26

0	5	2	450	65	154	1.51
0	5	3	550	55.94	179	1.75
0	6	0	300	84.18	119	1.16
0	6	1	400	69.41	144	1.41
0	6	2	500	59.16	169	1.65
0	6	3	600	51.56	194	1.9
0	7	0	350	74.52	134	1.31
0	7	1	450	62.79	159	1.55
0	7	2	550	54.29	184	1.8
0	7	3	650	47.85	209	2.04
0	8	0	400	66.91	149	1.46
0	8	1	500	57.32	174	1.7
0	8	2	600	50.19	199	1.95
0	8	3	700	44.61	224	2.19
0	9	0	450	60.71	165	1.61
0	9	1	550	52.74	190	1.86
0	9	2	650	46.66	214	2.09
0	9	3	750	41.84	239	2.34
0	10	0	500	55.59	180	1.76
0	10	1	600	48.83	205	2
0	10	2	700	43.6	229	2.24
0	10	3	800	39.37	254	2.48
0	11	0	550	51.28	195	1.91
0	11	1	650	45.48	220	2.15
0	11	2	750	40.88	245	2.39
0	11	3	850	37.16	269	2.63
0	12	0	600	47.6	210	2.05
0	12	1	700	42.6	235	2.3
0	12	2	800	38.56	259	2.53
0	12	3	900	35.22	284	2.78
0	13	0	650	44.41	225	2.2
0	13	1	750	40.03	250	2.44
0	13	2	850	36.43	274	2.68
0	13	3	950	33.45	299	2.92
0	14	0	700	41.61	240	2.35
0	14	1	800	37.75	265	2.59
0	14	2	900	34.53	290	2.83
0	14	3	1000	31.87	314	3.07
0	15	0	750	39.19	255	2.49
0	15	1	850	35.74	280	2.74
0	15	2	950	32.87	304	2.97
0	15	3	1050	30.41	329	3.22
1	0	1	9	33.41	299	2.92
1	0	2	18	31.04	322	3.15
1	0	3	27	28.66	349	3.41
1	1	0	4.5	35.67	280	2.74
1	1	1	13.5	32.13	311	3.04
1	1	2	22.5	29.65	337	3.29
1	1	3	31.5	27.39	365	3.57
1	2	0	9	33.35	300	2.93
1	2	1	18	30.69	326	3.19
1	2	2	27	28.3	353	3.45
1	2	3	36	26.21	382	3.73
1	3	0	13.5	31.78	315	3.08
1	3	1	22.5	29.26	342	3.34
1	3	2	31.5	27.01	370	3.62
1	3	3	40.5	25.05	399	3.9
1	4	0	18	30.23	331	3.24

1	4	1	27	27.88	359	3.51
1	4	2	36	25.83	387	3.78
1	4	3	45	24.01	416	4.07
1	5	0	22.5	28.81	347	3.39
1	5	1	31.5	26.65	375	3.67
1	5	2	40.5	24.71	405	3.96
1	5	3	49.5	22.99	435	4.25
1	6	0	27	27.49	364	3.56
1	6	1	36	25.41	394	3.85
1	6	2	45	23.67	422	4.13
1	6	3	54	22.12	452	4.42
1	7	0	31.5	26.21	382	3.73
1	7	1	40.5	24.35	411	4.02
1	7	2	49.5	22.7	441	4.31
1	7	3	58.5	21.28	470	4.59
1	8	0	36	25.09	399	3.9
1	8	1	45	23.33	429	4.19
1	8	2	54	21.82	458	4.48
1	8	3	63	20.47	489	4.78
1	9	0	40.5	23.99	417	4.08
1	9	1	49.5	22.41	446	4.36
1	9	2	58.5	21	476	4.65
1	9	3	67.5	19.83	504	4.93
1	10	0	45	22.97	435	4.25
1	10	1	54	21.52	465	4.55
1	10	2	63	20.23	494	4.83
1	10	3	72	19.2	521	5.09
1	11	0	49.5	22.1	452	4.42
1	11	1	58.5	20.73	482	4.71
1	11	2	67.5	19.61	510	4.99
1	11	3	76.5	18.61	537	5.25
1	12	0	54	21.22	471	4.6
1	12	1	63	20.01	500	4.89
1	12	2	72	18.98	527	5.15
1	12	3	81	18.04	554	5.42
1	13	0	58.5	20.46	489	4.78
1	13	1	67.5	19.39	516	5.04
1	13	2	76.5	18.42	543	5.31
1	13	3	85.5	17.51	571	5.58
1	14	0	63	19.79	505	4.94
1	14	1	72	18.76	533	5.21
1	14	2	81	17.84	561	5.48
1	14	3	90	17.05	587	5.74
1	15	0	67.5	19.17	522	5.1
1	15	1	76.5	18.22	549	5.37
1	15	2	85.5	17.36	576	5.63
1	15	3	94.5	16.6	602	5.88

Table B.2: Dynamic Range Si T = -30 °C

Rf code	Cf code	Cf_comp code	RfCf (ns)	Amplitude (mV)	Dynamic Range (fC)	MIP (fC)
0	0	1	100	94.33	106	1.04
0	0	2	200	80.89	124	1.21
0	0	3	300	68.4	146	1.43
0	1	0	50	114	88	0.86

0	1	1	150	86.51	116	1.13
0	1	2	250	73.02	137	1.34
0	1	3	350	62.35	160	1.56
0	2	0	100	92.2	108	1.06
0	2	1	200	78.16	128	1.25
0	2	2	300	66.23	151	1.48
0	2	3	400	57.16	175	1.71
0	3	0	150	83.75	119	1.16
0	3	1	250	70.55	142	1.39
0	3	2	350	60.46	165	1.61
0	3	3	450	52.71	190	1.86
0	4	0	200	75.46	133	1.3
0	4	1	300	64.15	156	1.52
0	4	2	400	55.54	180	1.76
0	4	3	500	48.87	205	2
0	5	0	250	68.24	147	1.44
0	5	1	350	58.67	170	1.66
0	5	2	450	51.31	195	1.91
0	5	3	550	45.54	220	2.15
0	6	0	300	62.15	161	1.57
0	6	1	400	53.99	185	1.81
0	6	2	500	47.66	210	2.05
0	6	3	600	42.62	235	2.3
0	7	0	350	56.95	176	1.72
0	7	1	450	49.97	200	1.96
0	7	2	550	44.47	225	2.2
0	7	3	650	40.05	250	2.44
0	8	0	400	52.51	190	1.86
0	8	1	500	46.49	215	2.1
0	8	2	600	41.68	240	2.35
0	8	3	700	37.77	265	2.59
0	9	0	450	48.68	205	2
0	9	1	550	43.44	230	2.25
0	9	2	650	39.21	255	2.49
0	9	3	750	35.73	280	2.74
0	10	0	500	45.37	220	2.15
0	10	1	600	40.77	245	2.39
0	10	2	700	37.02	270	2.64
0	10	3	800	33.9	295	2.88
0	11	0	550	42.46	236	2.31
0	11	1	650	38.41	260	2.54
0	11	2	750	35.06	285	2.79
0	11	3	850	32.35	309	3.02
0	12	0	600	39.9	251	2.45
0	12	1	700	36.3	275	2.69
0	12	2	800	33.28	300	2.93
0	12	3	900	30.74	325	3.18
0	13	0	650	37.63	266	2.6
0	13	1	750	34.41	291	2.84
0	13	2	850	31.7	315	3.08
0	13	3	950	29.38	340	3.32
0	14	0	700	35.61	281	2.75
0	14	1	800	32.7	306	2.99
0	14	2	900	30.25	331	3.24
0	14	3	1000	28.13	355	3.47
0	15	0	750	33.79	296	2.89
0	15	1	850	31.17	321	3.14
0	15	2	950	28.92	346	3.38

0	15	3	1050	26.99	371	3.63
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Table B.3: Dynamic Range LAr T = 27 °C

Rf code	Cf code	Cf_comp code	RfCf (ns)	Amplitude (mV)	Dynamic Range (fC)	MIP (fC)
0	0	1	100	97.73	102	1
0	0	2	200	82.83	121	1.18
0	0	3	300	69.63	144	1.41
0	1	0	50	114.5	87	0.85
0	1	1	150	89	112	1.09
0	1	2	250	74.42	134	1.31
0	1	3	350	63.27	158	1.54
0	2	0	100	95.3	105	1.03
0	2	1	200	79.81	125	1.22
0	2	2	300	67.31	149	1.46
0	2	3	400	57.83	173	1.69
0	3	0	150	85.87	116	1.13
0	3	1	250	71.85	139	1.36
0	3	2	350	61.26	163	1.59
0	3	3	450	53.22	188	1.84
0	4	0	200	76.95	130	1.27
0	4	1	300	65.1	154	1.51
0	4	2	400	56.13	178	1.74
0	4	3	500	49.26	203	1.98
0	5	0	250	69.4	144	1.41
0	5	1	350	59.38	168	1.64
0	5	2	450	51.76	193	1.89
0	5	3	550	45.88	218	2.13
0	6	0	300	62.99	159	1.55
0	6	1	400	54.52	183	1.79
0	6	2	500	48.02	208	2.03
0	6	3	600	42.91	233	2.28
0	7	0	350	57.58	174	1.7
0	7	1	450	50.37	199	1.95
0	7	2	550	44.79	223	2.18
0	7	3	650	40.31	248	2.42
0	8	0	400	52.99	189	1.85
0	8	1	500	46.83	214	2.09
0	8	2	600	41.95	238	2.33
0	8	3	700	38	263	2.57
0	9	0	450	49.06	204	1.99
0	9	1	550	43.74	229	2.24
0	9	2	650	39.45	253	2.47
0	9	3	750	35.93	278	2.72
0	10	0	500	45.69	219	2.14
0	10	1	600	41.03	244	2.39
0	10	2	700	37.24	269	2.63
0	10	3	800	34.07	294	2.87
0	11	0	550	42.74	234	2.29
0	11	1	650	38.64	259	2.53
0	11	2	750	35.26	284	2.78
0	11	3	850	32.41	309	3.02
0	12	0	600	40.15	249	2.43
0	12	1	700	36.51	274	2.68
0	12	2	800	33.47	299	2.92

0	12	3	900	30.88	324	3.17
0	13	0	650	37.85	264	2.58
0	13	1	750	34.59	289	2.83
0	13	2	850	31.85	314	3.07
0	13	3	950	29.51	339	3.31
0	14	0	700	35.8	279	2.73
0	14	1	800	32.87	304	2.97
0	14	2	900	30.38	329	3.22
0	14	3	1000	28.25	354	3.46
0	15	0	750	33.96	294	2.87
0	15	1	850	31.31	319	3.12
0	15	2	950	29.05	344	3.36
0	15	3	1050	27.08	369	3.61

Table B.4: Dynamic Range LAr T = -30 °C

Rf code	Cf code	Cf_comp code	RfCf (ns)	Amplitude (mV)	Dynamic Range (fC)	MIP (fC)
0	0	1	100	106.3	94	0.92
0	0	2	200	86.8	115	1.12
0	0	3	300	71.55	140	1.37
0	1	0	50	113.1	88	0.86
0	1	1	150	94.11	106	1.04
0	1	2	250	76.93	130	1.27
0	1	3	350	64.47	155	1.52
0	2	0	100	102.1	98	0.96
0	2	1	200	83.09	120	1.17
0	2	2	300	68.86	145	1.42
0	2	3	400	58.62	171	1.67
0	3	0	150	89.99	111	1.09
0	3	1	250	73.89	135	1.32
0	3	2	350	62.24	161	1.57
0	3	3	450	53.74	186	1.82
0	4	0	200	79.57	126	1.23
0	4	1	300	66.34	151	1.48
0	4	2	400	56.73	176	1.72
0	4	3	500	49.55	202	1.97
0	5	0	250	71	141	1.38
0	5	1	350	60.13	166	1.62
0	5	2	450	52.15	192	1.88
0	5	3	550	45.98	217	2.12
0	6	0	300	64.02	156	1.52
0	6	1	400	55.02	182	1.78
0	6	2	500	48.2	207	2.02
0	6	3	600	42.89	233	2.28
0	7	0	350	58.22	172	1.68
0	7	1	450	50.65	197	1.93
0	7	2	550	44.82	223	2.18
0	7	3	650	40.19	249	2.43
0	8	0	400	53.37	187	1.83
0	8	1	500	46.93	213	2.08
0	8	2	600	41.87	239	2.34
0	8	3	700	37.81	264	2.58
0	9	0	450	49.24	203	1.98
0	9	1	550	43.7	229	2.24
0	9	2	650	39.29	255	2.49

0	9	3	750	35.71	280	2.74
0	10	0	500	45.71	219	2.14
0	10	1	600	40.9	244	2.39
0	10	2	700	37.04	270	2.64
0	10	3	800	33.85	295	2.88
0	11	0	550	42.64	235	2.3
0	11	1	650	38.43	260	2.54
0	11	2	750	35	286	2.8
0	11	3	850	32.12	311	3.04
0	12	0	600	39.97	250	2.44
0	12	1	700	36.27	276	2.7
0	12	2	800	33.18	301	2.94
0	12	3	900	30.62	327	3.2
0	13	0	650	37.63	266	2.6
0	13	1	750	34.36	291	2.84
0	13	2	850	31.54	317	3.1
0	13	3	950	29.19	343	3.35
0	14	0	700	35.53	281	2.75
0	14	1	800	32.58	307	3
0	14	2	900	30.06	333	3.26
0	14	3	1000	27.96	358	3.5
0	15	0	750	33.67	297	2.9
0	15	1	850	30.98	323	3.16
0	15	2	950	28.71	348	3.4
0	15	3	1050	26.76	374	3.66

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V.40 Register #5	63
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V.42 Register #7	64
V.43 Register #8	64
V.44 Register #9	64
V.45 Register #0	64
V.46 Register #1	65
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V.51 Register #6	66
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