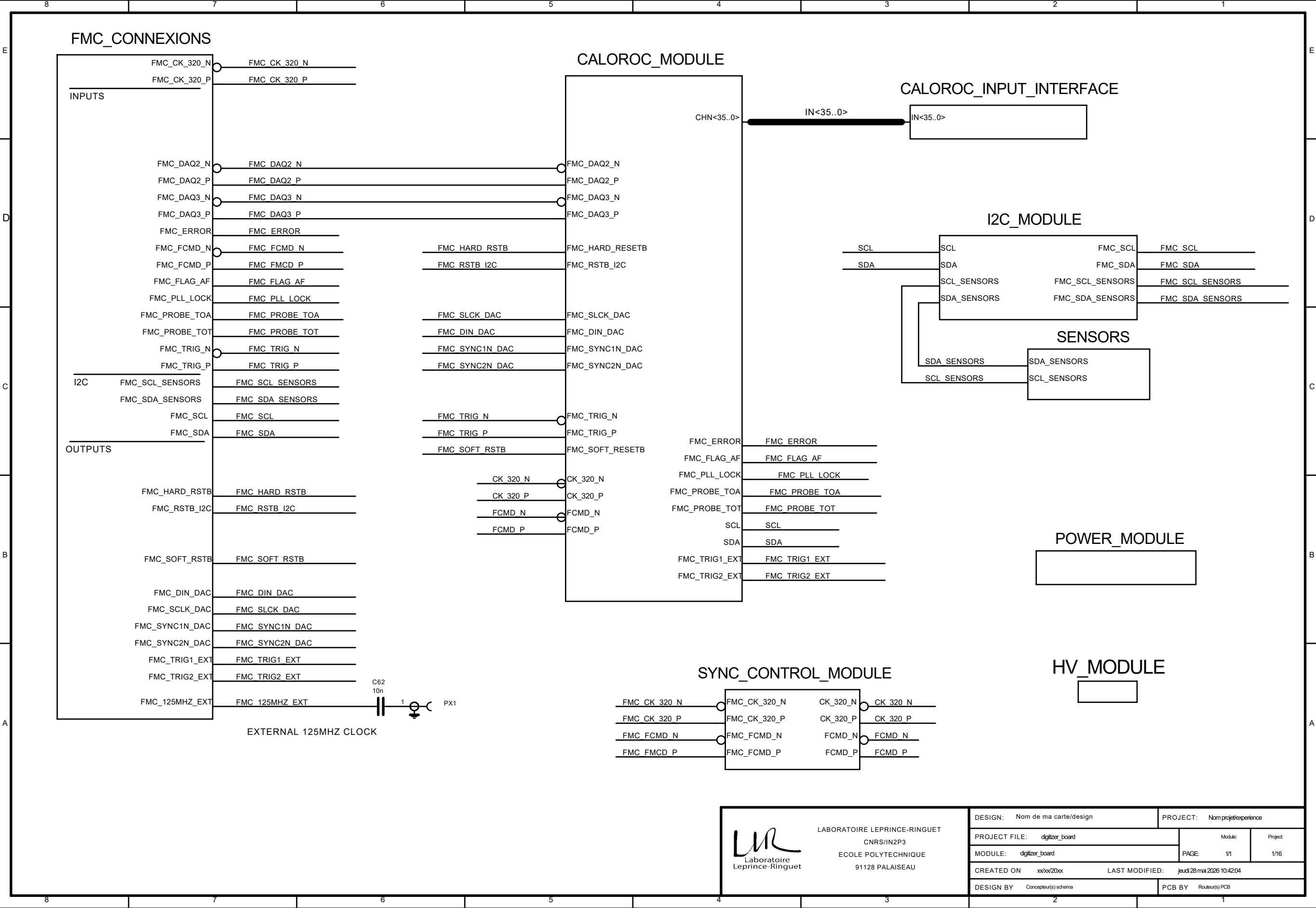




FMC_CONNEXIONS

FMC_CK_320_N FMC CK 320 N
FMC_CK_320_P FMC CK 320 P

INPUTS

FMC_DAQ2_N FMC DAQ2 N
FMC_DAQ2_P FMC DAQ2 P
FMC_DAQ3_N FMC DAQ3 N
FMC_DAQ3_P FMC DAQ3 P
FMC_ERROR FMC ERROR
FMC_FCMD_N FMC FCMD N
FMC_FCMD_P FMC FCMD P
FMC_FLAG_AF FMC FLAG AF
FMC_PLL_LOCK FMC PLL LOCK
FMC_PROBE_TOA FMC PROBE TOA
FMC_PROBE_TOT FMC PROBE TOT
FMC_TRIG_N FMC TRIG N
FMC_TRIG_P FMC TRIG P

I2C

FMC_SCL_SENSORS FMC SCL SENSORS
FMC_SDA_SENSORS FMC SDA SENSORS
FMC_SCL FMC SCL
FMC_SDA FMC SDA

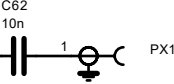
OUTPUTS

FMC_HARD_RSTB FMC HARD RSTB
FMC_RSTB_I2C FMC RSTB I2C

FMC_SOFT_RSTB FMC SOFT RSTB

FMC_DIN_DAC FMC DIN DAC
FMC_SCLK_DAC FMC SLCK DAC
FMC_SYNC1N_DAC FMC SYNC1N DAC
FMC_SYNC2N_DAC FMC SYNC2N DAC
FMC_TRIG1_EXT FMC TRIG1 EXT
FMC_TRIG2_EXT FMC TRIG2 EXT
FMC_125MHZ_EXT FMC 125MHZ EXT

EXTERNAL 125MHZ CLOCK



CALOROC_MODULE

FMC_HARD_RSTB FMC_HARD_RESETB
FMC_RSTB_I2C FMC_RSTB_I2C

FMC_SLCK_DAC FMC_SLCK_DAC
FMC_DIN_DAC FMC_DIN_DAC
FMC_SYNC1N_DAC FMC_SYNC1N_DAC
FMC_SYNC2N_DAC FMC_SYNC2N_DAC

FMC_TRIG_N FMC_TRIG_N
FMC_TRIG_P FMC_TRIG_P
FMC_SOFT_RSTB FMC_SOFT_RESETB

CK_320_N CK_320_N
CK_320_P CK_320_P
FCMD_N FCMD_N
FCMD_P FCMD_P

CHN<35..0>

IN<35..0>

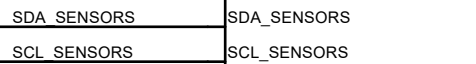
CALOROC_INPUT_INTERFACE



I2C_MODULE

SCL SCL FMC_SCL FMC_SCL
SDA SDA FMC_SDA FMC_SDA
SCL_SENSORS FMC_SCL_SENSORS FMC_SCL_SENSORS
SDA_SENSORS FMC_SDA_SENSORS FMC_SDA_SENSORS

SENSORS



POWER_MODULE



HV_MODULE



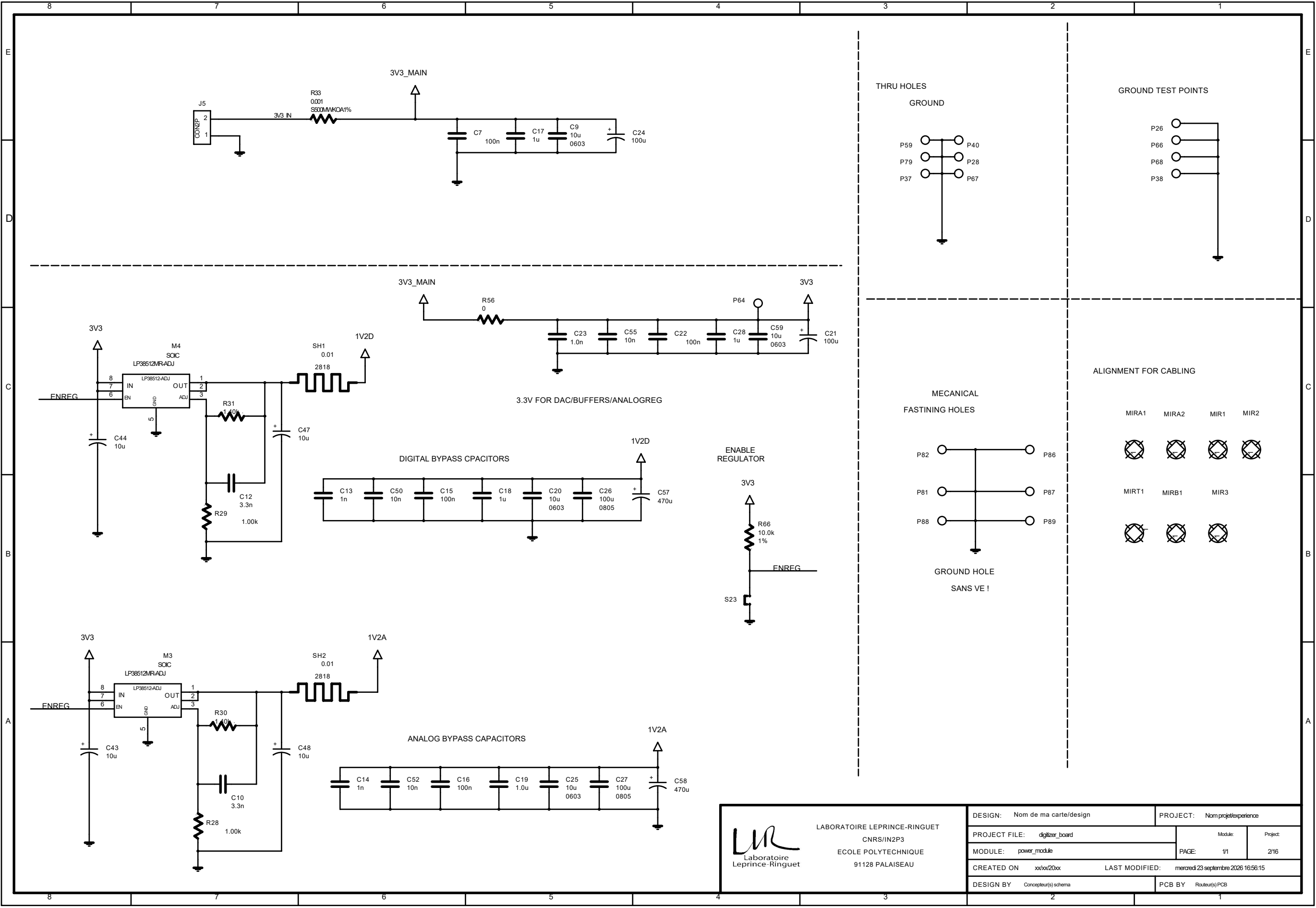
SYNC_CONTROL_MODULE

FMC_CK_320_N FMC_CK_320_N CK_320_N CK_320_N
FMC_CK_320_P FMC_CK_320_P CK_320_P CK_320_P
FMC_FCMD_N FMC_FCMD_N FCMD_N FCMD_N
FMC_FCMD_P FMC_FCMD_P FCMD_P FCMD_P



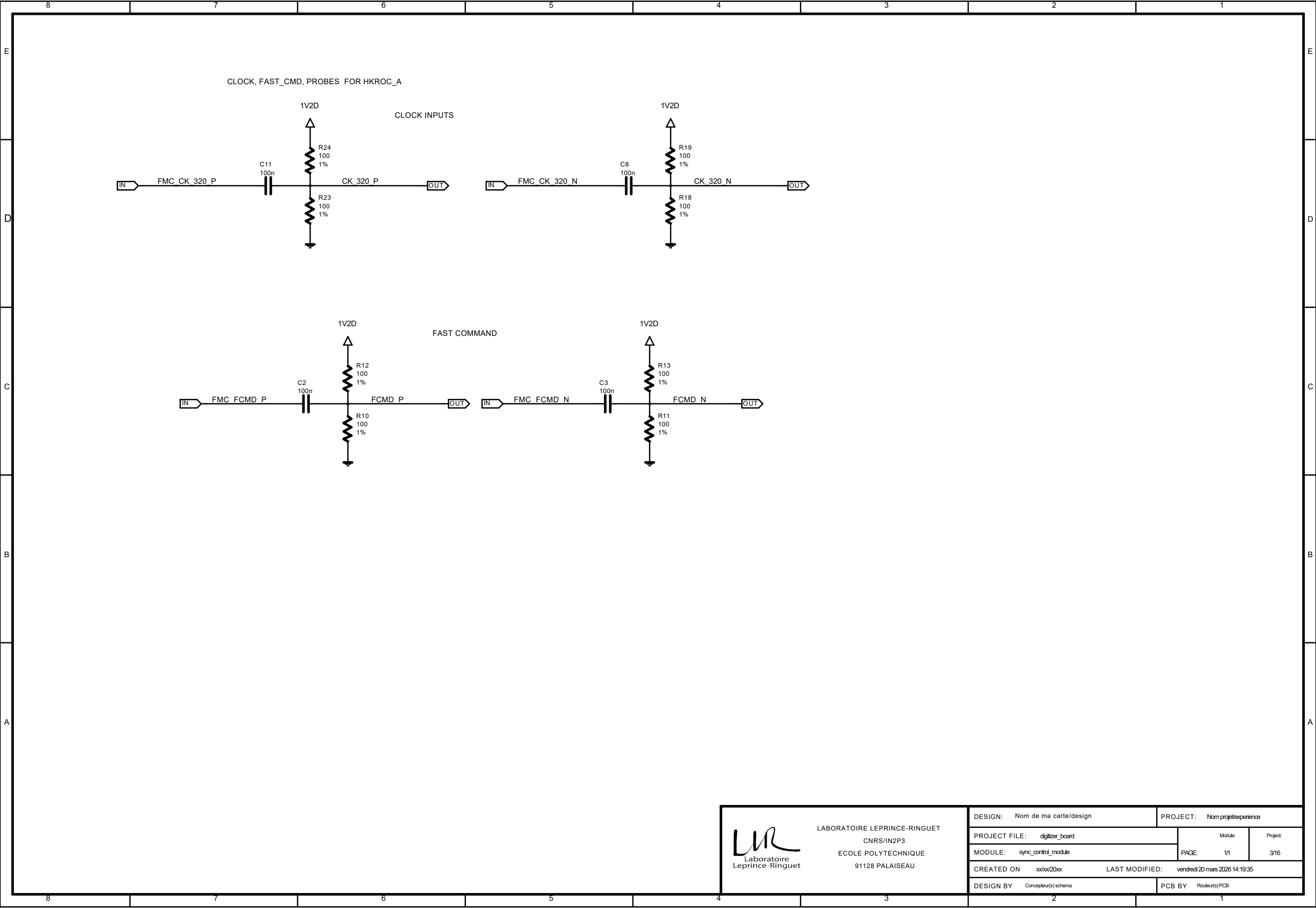
LABORATOIRE LEPRINCE-RINGUET
CNRS/IN2P3
ECOLE POLYTECHNIQUE
91128 PALAISEAU

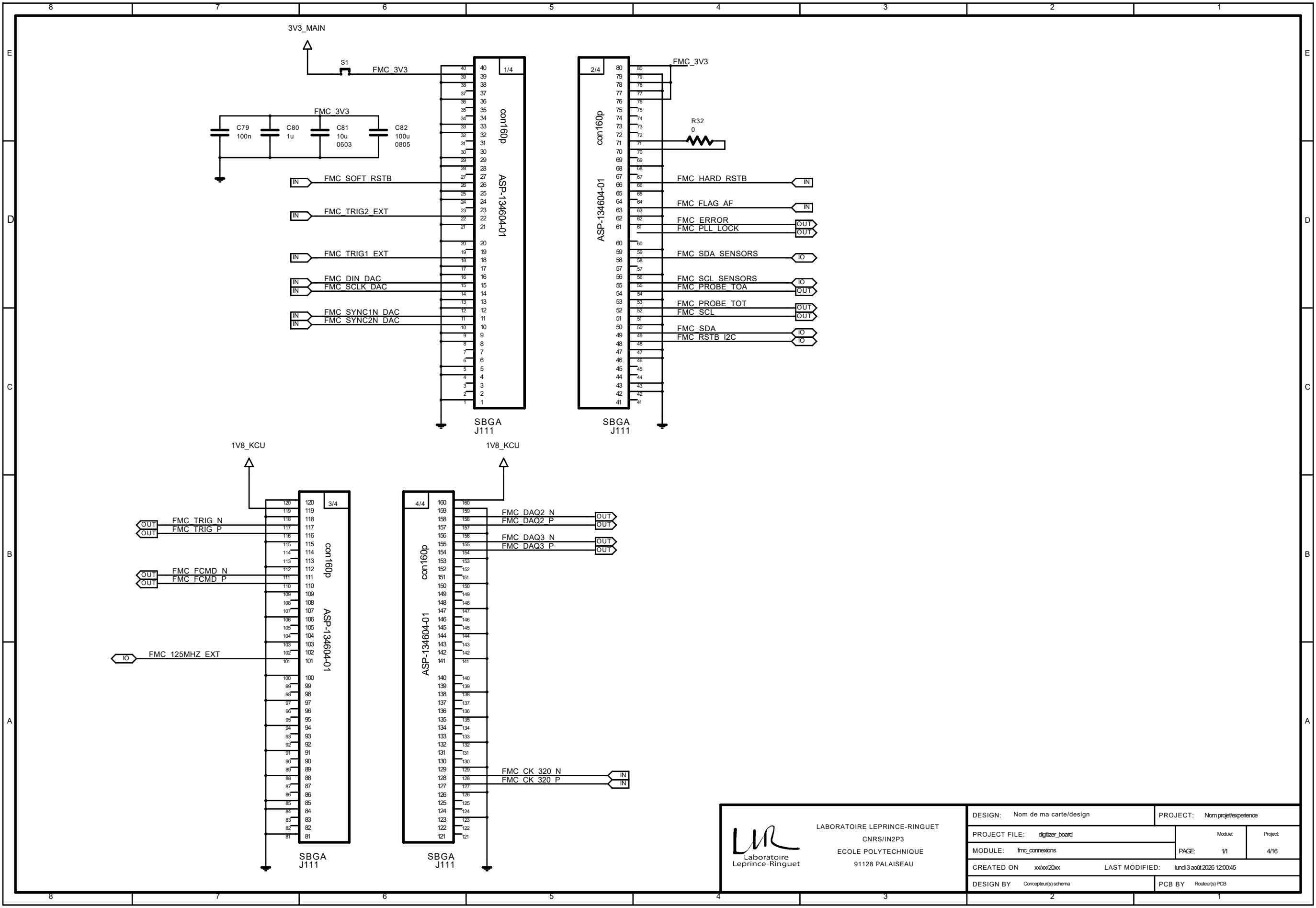
DESIGN: Nom de ma carte/design		PROJECT: Nom projet/experience	
PROJECT FILE: digitizer_board		Module:	Project:
MODULE: digitizer_board		PAGE: 1/1	1/16
CREATED ON xx/xx/20xx		LAST MODIFIED: jeudi 28 mai 2026 10:42:04	
DESIGN BY Concepteur(s) schema		PCB BY Routeur(s) PCB	



LABORATOIRE LEPRINCE-RINGUET
CNRS/IN2P3
ECOLE POLYTECHNIQUE
91128 PALAISEAU

DESIGN: Nom de ma carte/design		PROJECT: Nom projet/experience	
PROJECT FILE: digitizer_board		Module:	Project:
MODULE: power_module		PAGE: 1/1	2/16
CREATED ON xx/xx/20xx		LAST MODIFIED: mercredi 23 septembre 2026 16:56:15	
DESIGN BY Concepteur(s) schema		PCB BY Routeur(s) PCB	

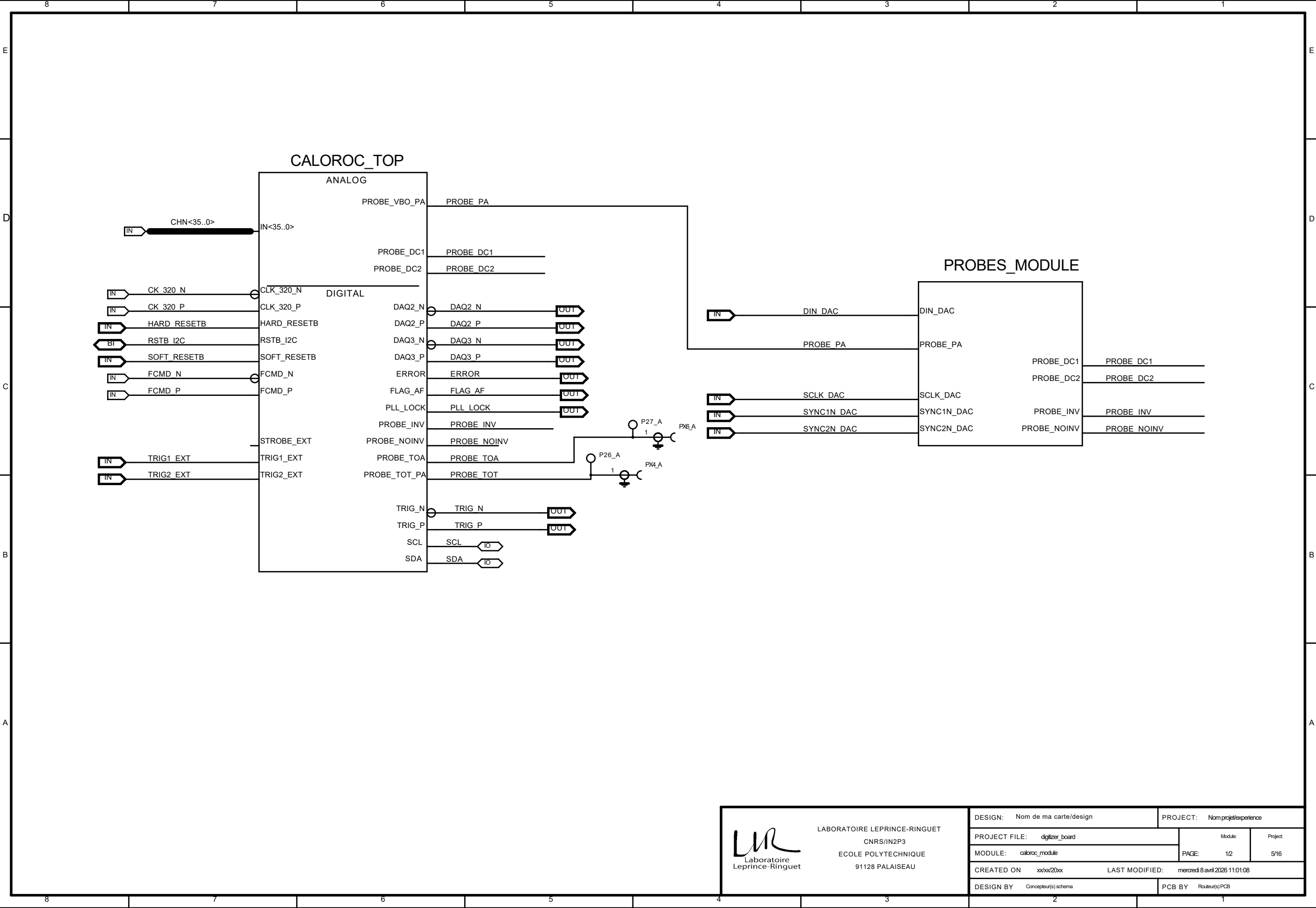


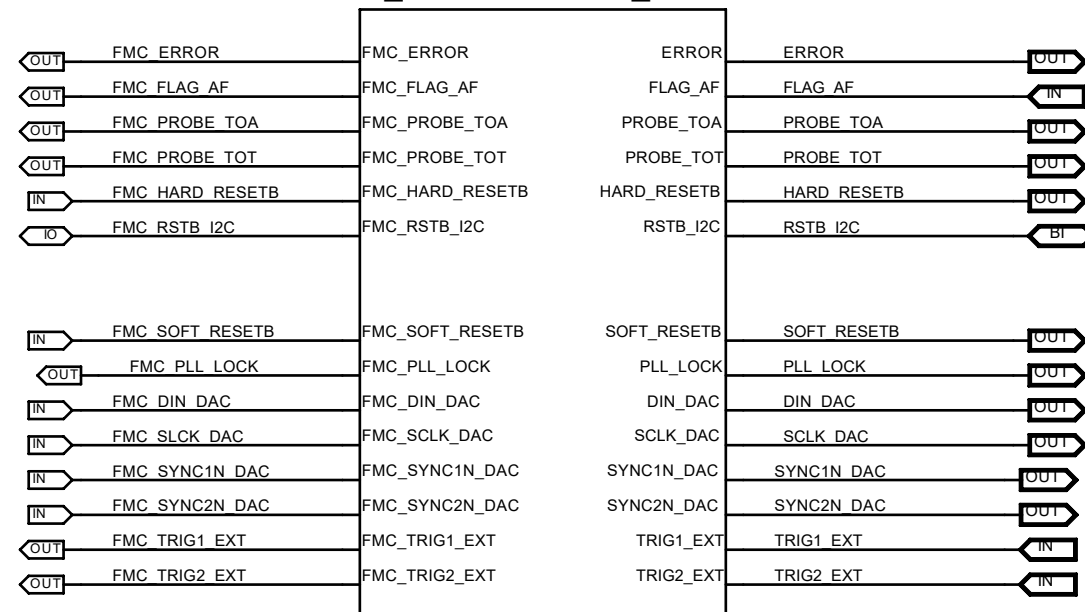


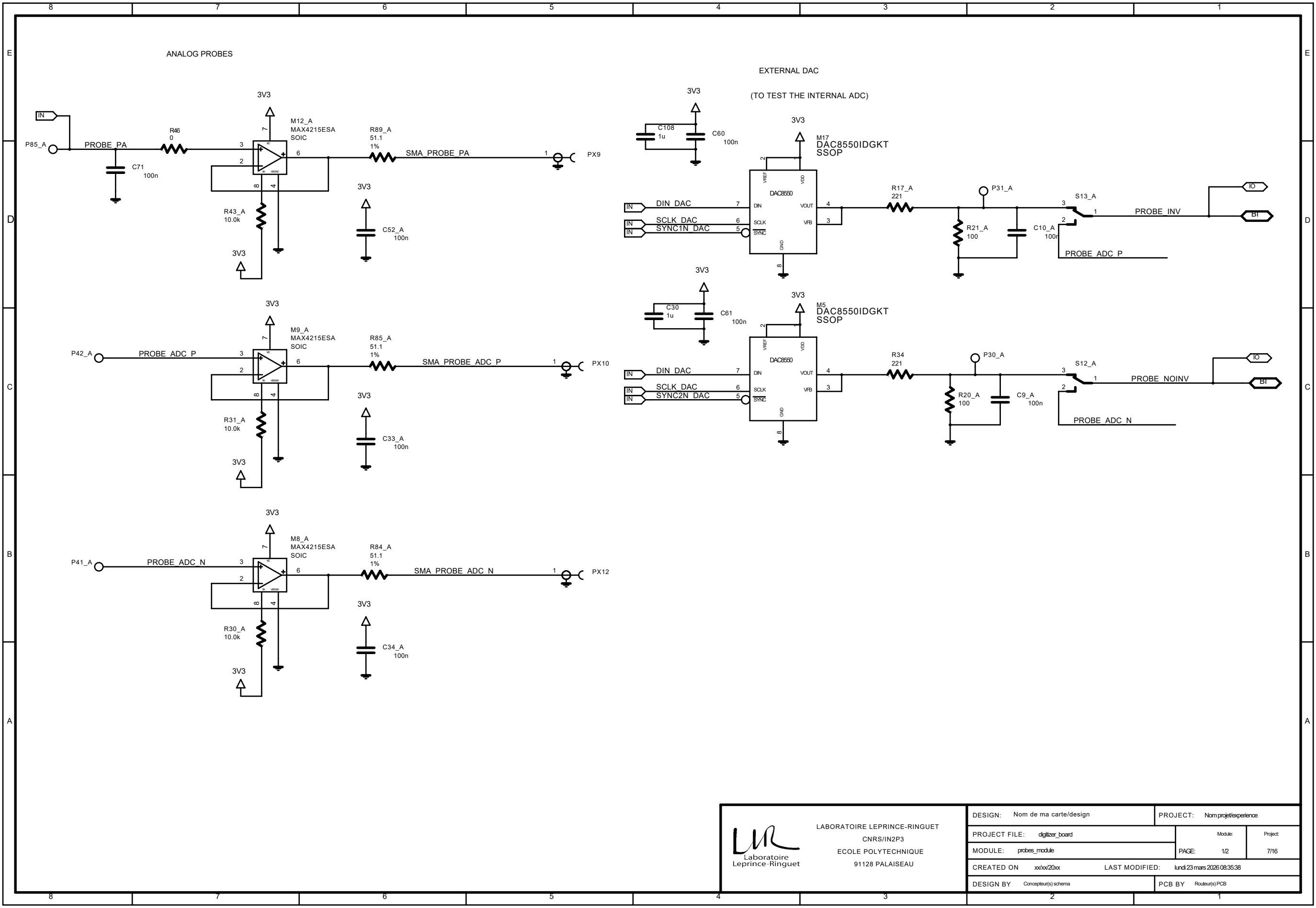


LABORATOIRE LEPRINCE-RINGUET
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91128 PALAISEAU

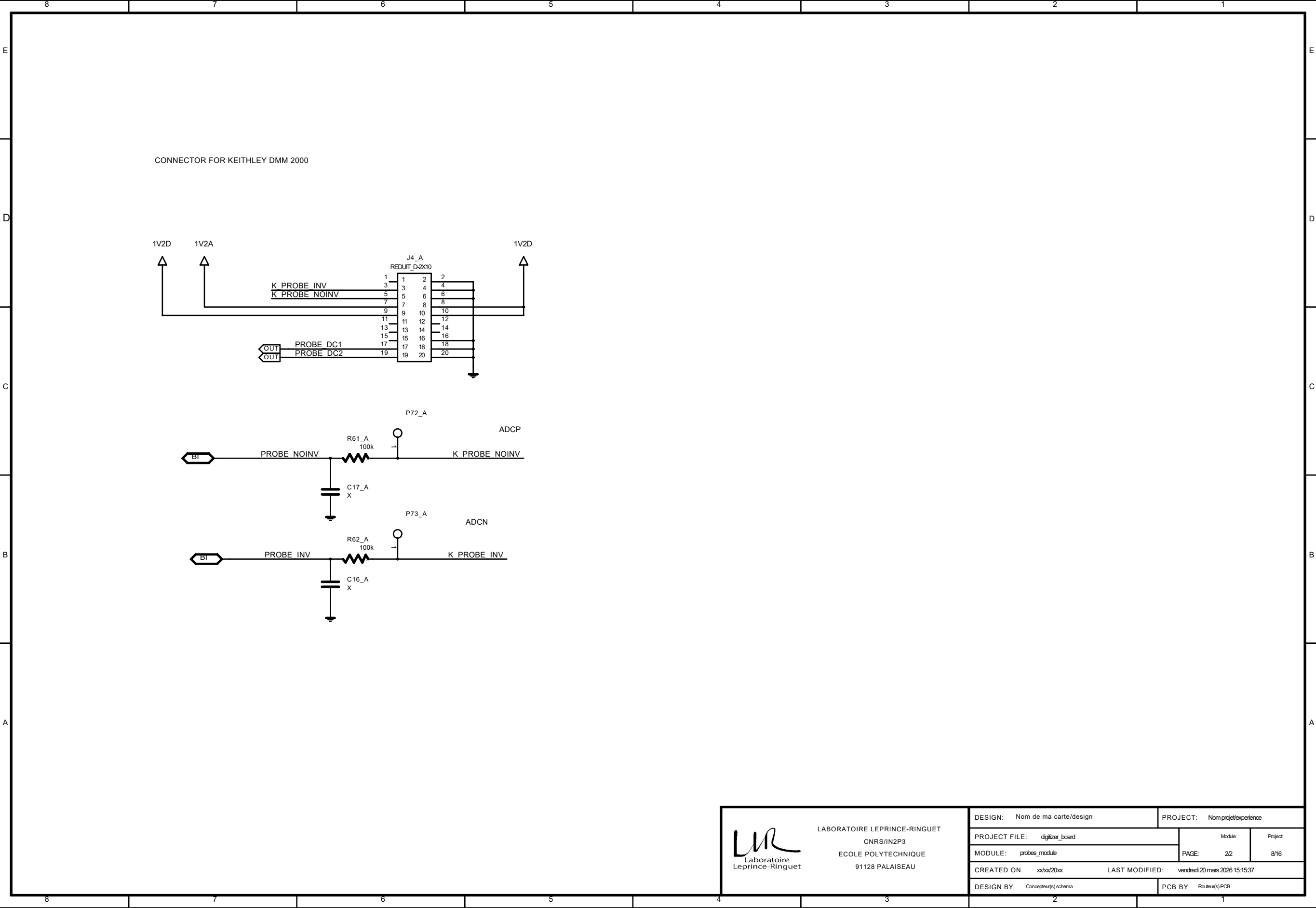
DESIGN: Nom de ma carte/design	PROJECT: Nom projet/experience	
PROJECT FILE: digitizer_board	Module:	Project:
MODULE: fmc_connexions	PAGE: 1/1	4/16
CREATED ON: xx/xx/20xx	LAST MODIFIED: lundi 3 août 2026 12:00:45	
DESIGN BY: Concepteur(s) schema	PCB BY: Routeur(s) PCB	

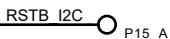
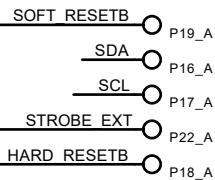






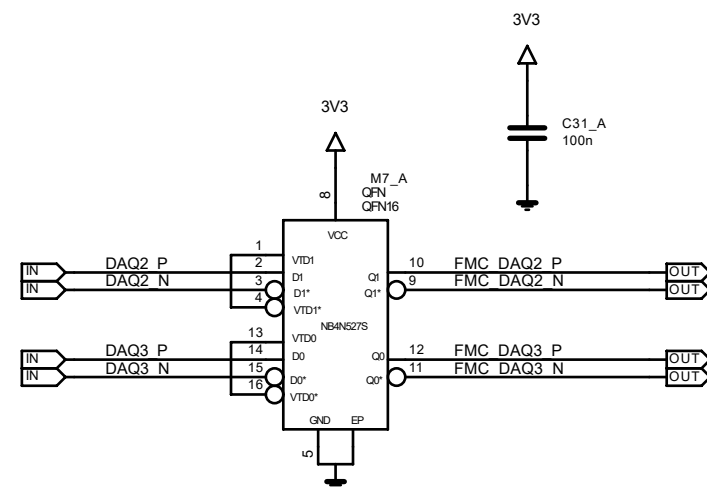
LNR Laboratoire Leprince-Ringuet	LABORATOIRE LEPRINCE-RINGUET		DESIGN: Nom de ma carte/design		PROJECT: Nom projet/experience	
	CNRS/IN2P3		PROJECT FILE: digitizer_board		Module:	Project:
	ECOLE POLYTECHNIQUE		MODULE: probes_module			
	91128 PALAISEAU				PAGE: 1/2	7/16
			CREATED ON xx/xx/20xx		LAST MODIFIED: lundi 23 mars 2026 08:35:38	
		DESIGN BY Concepteur(s) schema		PCB BY Routeur(s) PCB		



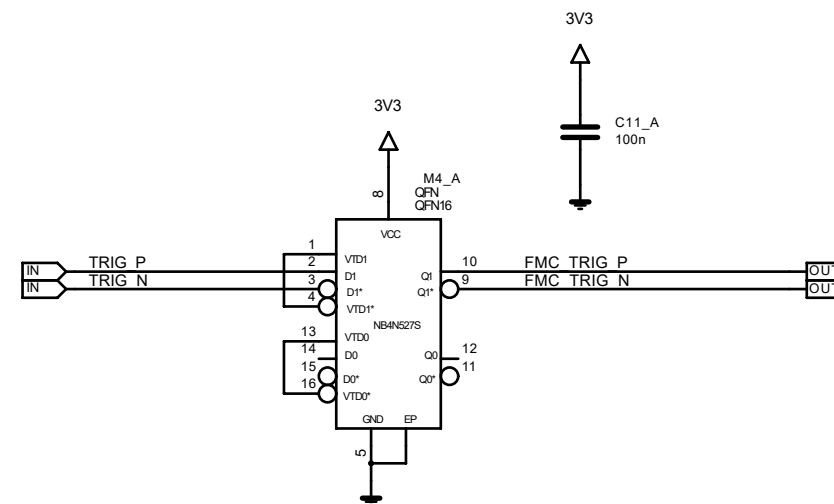


LABORATOIRE LEPRINCE-RINGUET
CNRS/IN2P3
ECOLE POLYTECHNIQUE
91128 PALAISEAU

DESIGN: Nom de ma carte/design		PROJECT: Nom projet/experience	
PROJECT FILE: digitizer_board		Module:	Project:
MODULE: caloroc_top		PAGE: 1/2	9/16
CREATED ON xx/xx/20xx		LAST MODIFIED: jeudi 28 mai 2026 10:42:04	
DESIGN BY Concepteur(s) schema		PCB BY Routeur(s) PCB	

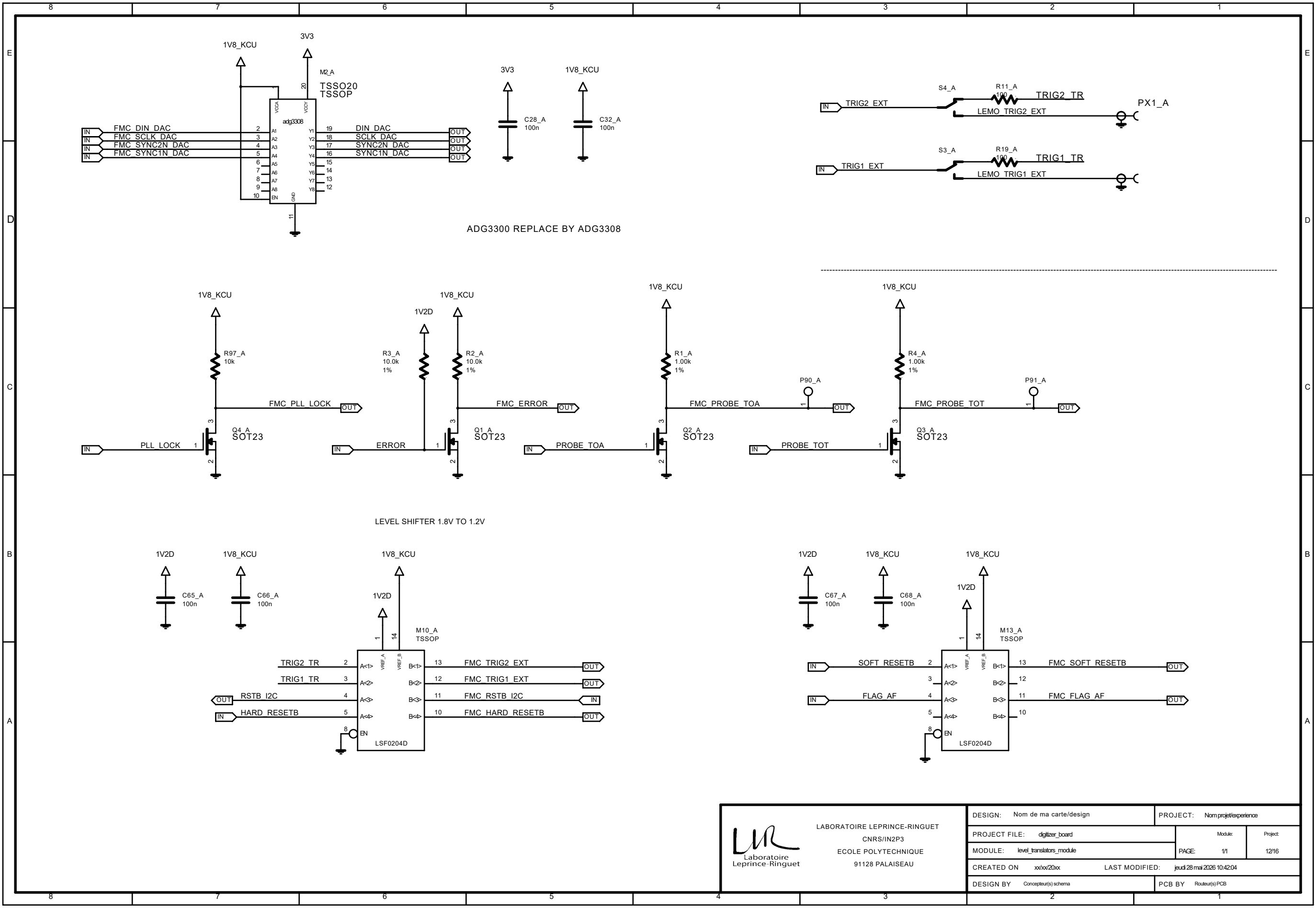


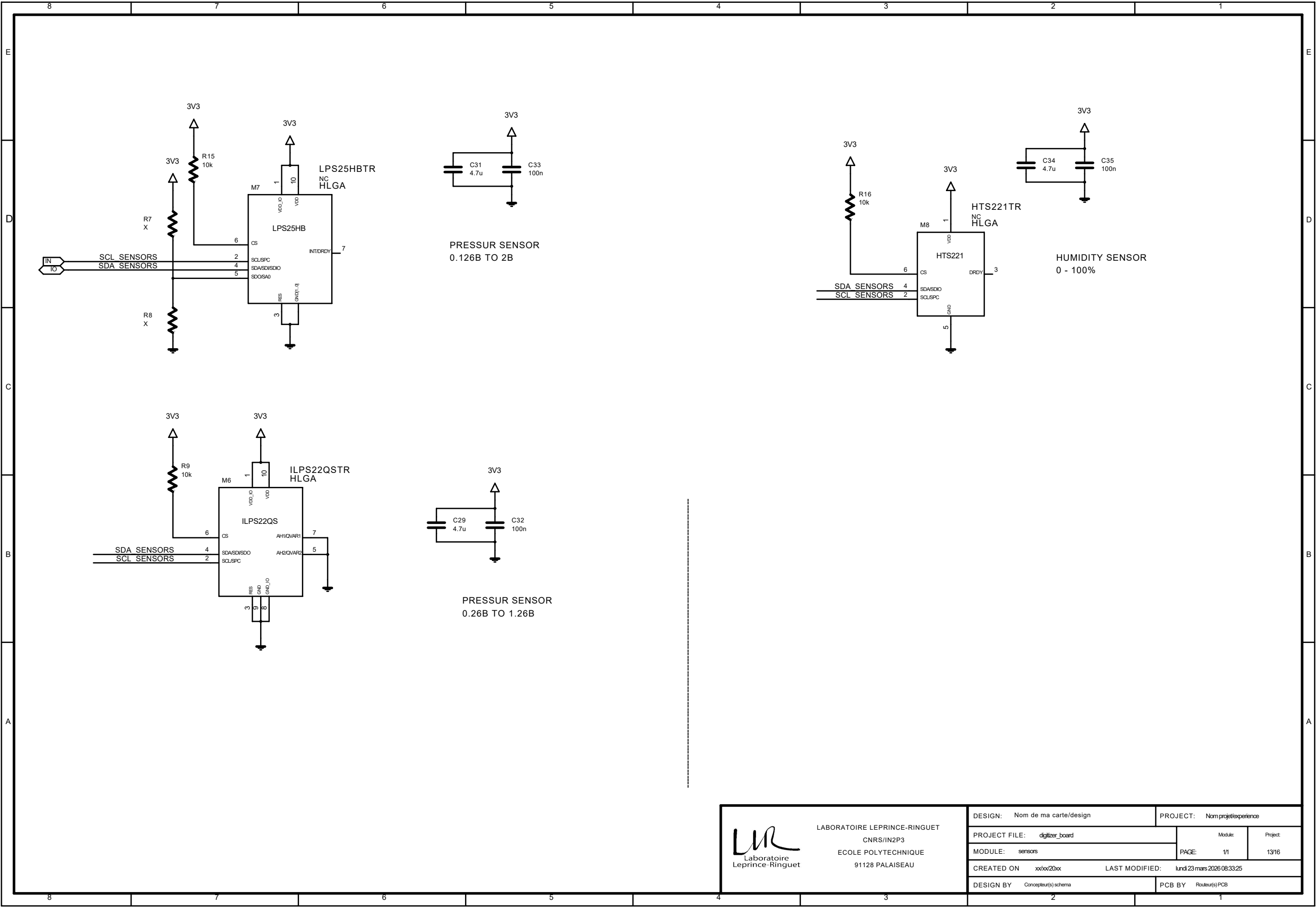
LEVEL ADAPTER FOR HKROC DATA



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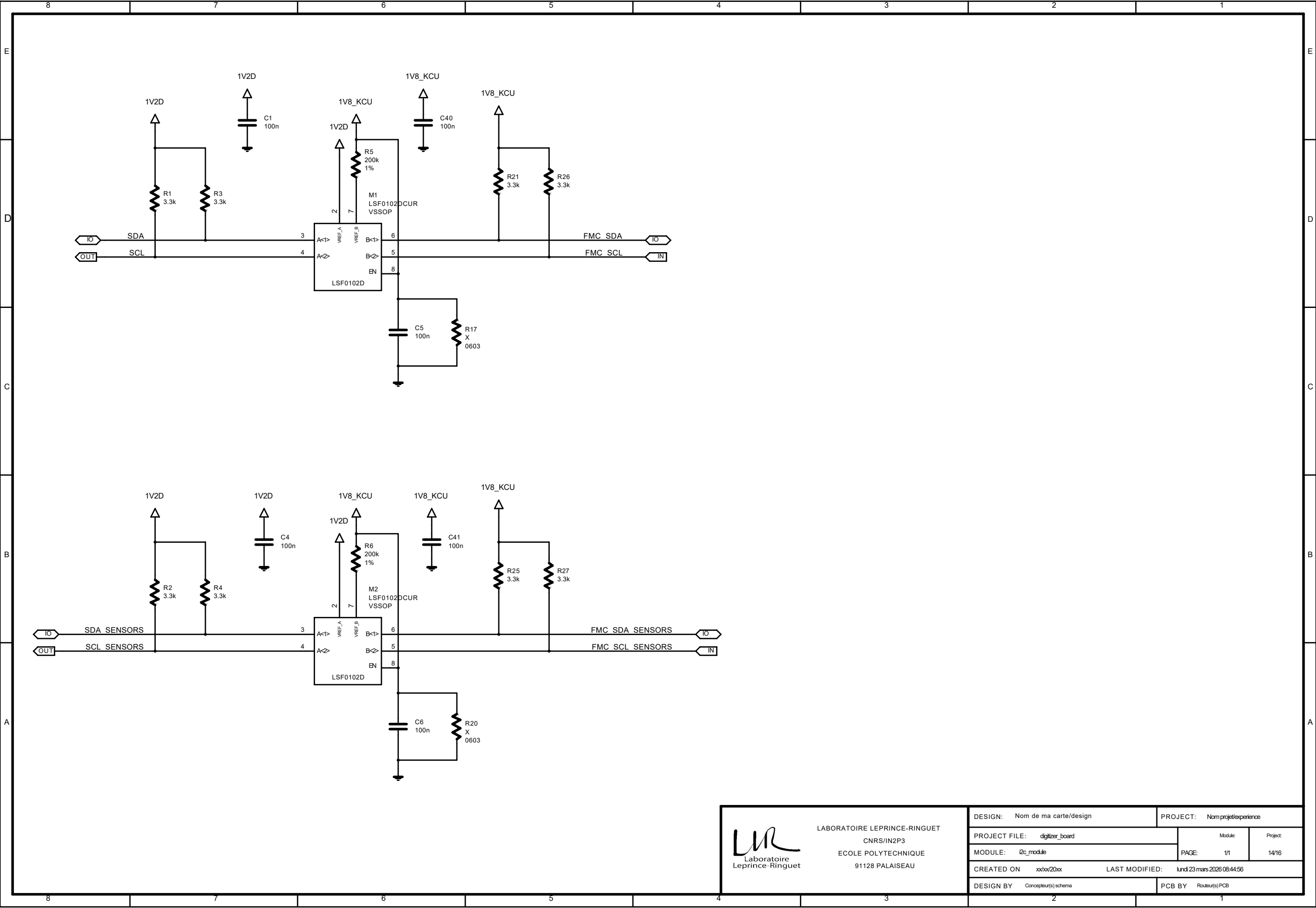
DESIGN: Nom de ma carte/design		PROJECT: Nom projet/experience	
PROJECT FILE: digitizer_board		Module:	Project:
MODULE: data_module			
		PAGE: 1/1	11/16
CREATED ON xx/xx/20xx		LAST MODIFIED: vendredi 20 mars 2026 14:19:35	
DESIGN BY Concepteur(s) schema		PCB BY Routeur(s) PCB	





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DESIGN: Nom de ma carte/design	PROJECT: Nom projet/experience	
PROJECT FILE: digitizer_board	Module:	Project:
MODULE: sensors	PAGE: 1/1	13/16
CREATED ON xx/xx/20xx	LAST MODIFIED: lundi 23 mars 2026 08:33:25	
DESIGN BY Concepteur(s) schema	PCB BY Routeur(s) PCB	



LNR Laboratoire Leprince-Ringuet LABORATOIRE LEPRINCE-RINGUET CNRS/IN2P3 ECOLE POLYTECHNIQUE 91128 PALAISEAU	DESIGN: Nom de ma carte/design	PROJECT: Nom projet/experience	
	PROJECT FILE: digitizer_board	Module:	Project:
	MODULE: i2c_module	PAGE: 1/1	14/16
	CREATED ON: xx/xx/20xx	LAST MODIFIED: lundi 23 mars 2026 08:44:56	
DESIGN BY: Concepteur(s) schema		PCB BY: Routeur(s) PCB	

