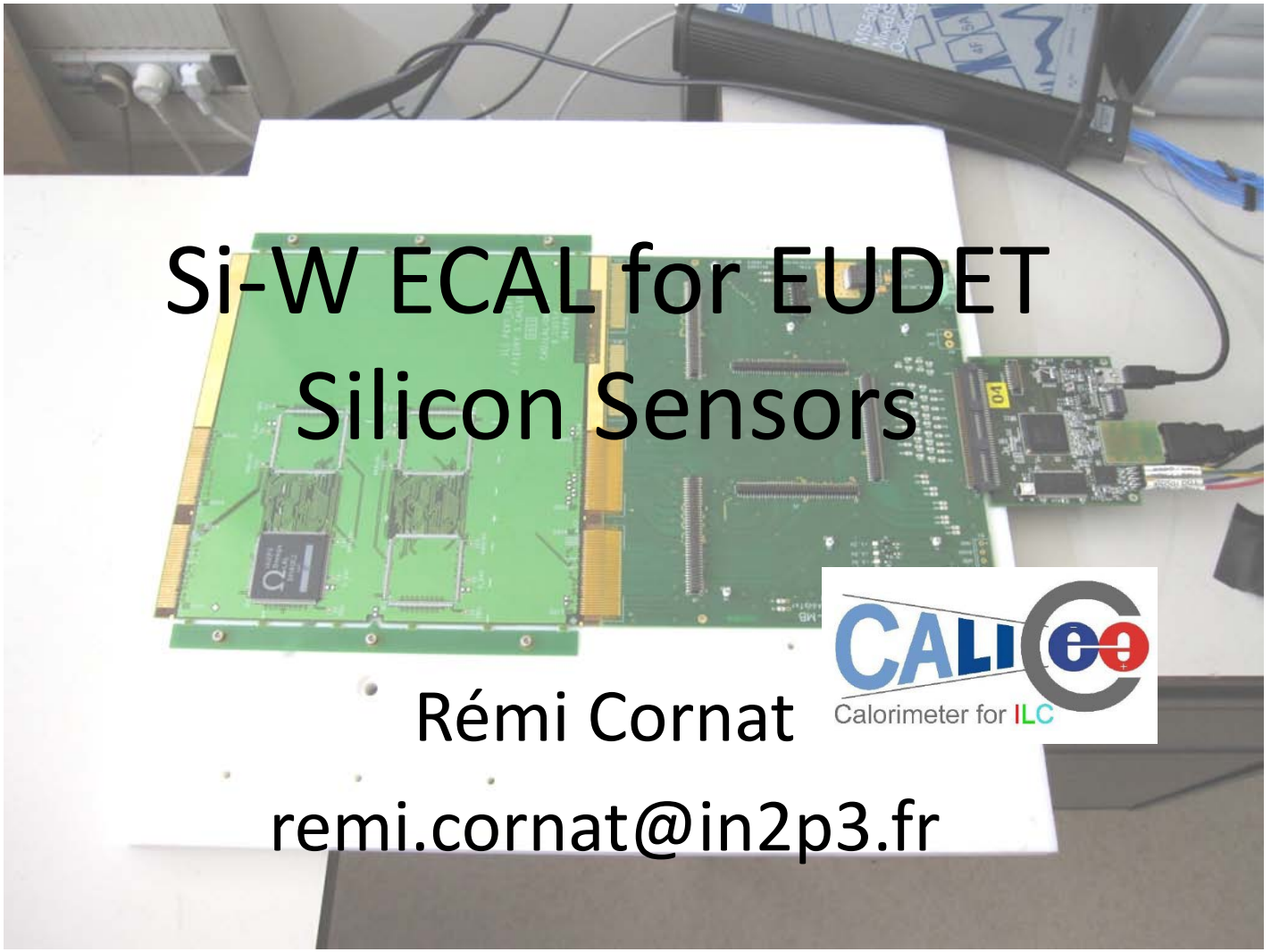
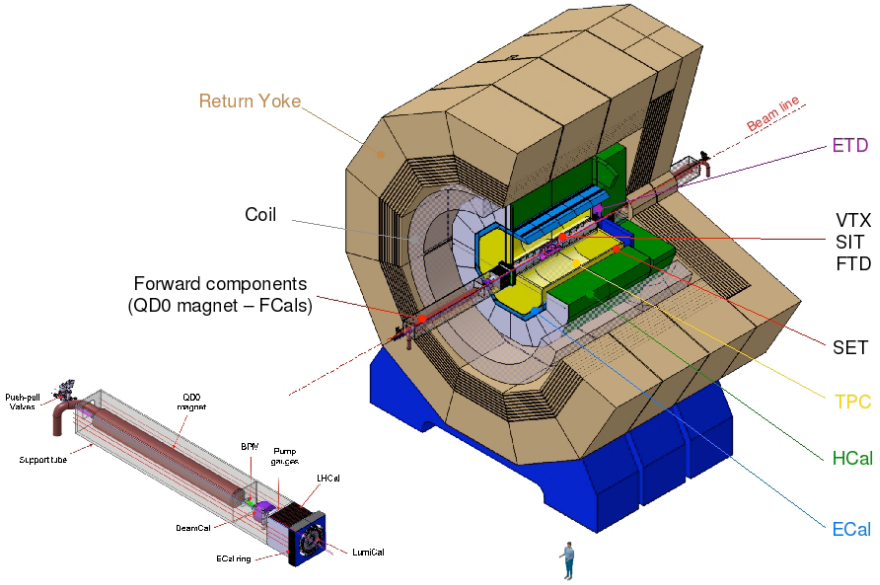


Si-W ECAL for EUDET Silicon Sensors

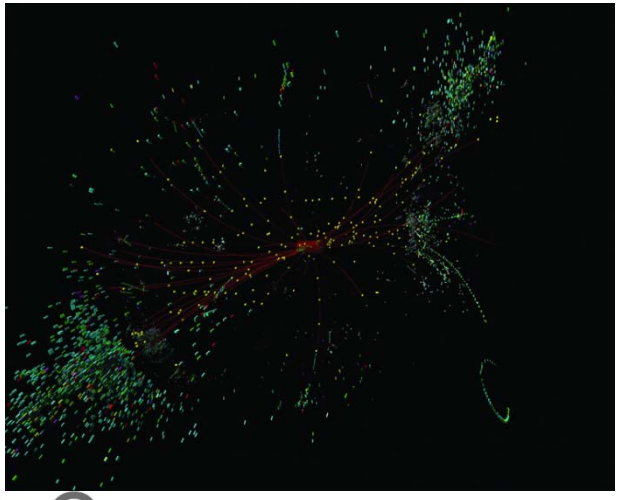
Rémi Cornat

remi.cornat@in2p3.fr

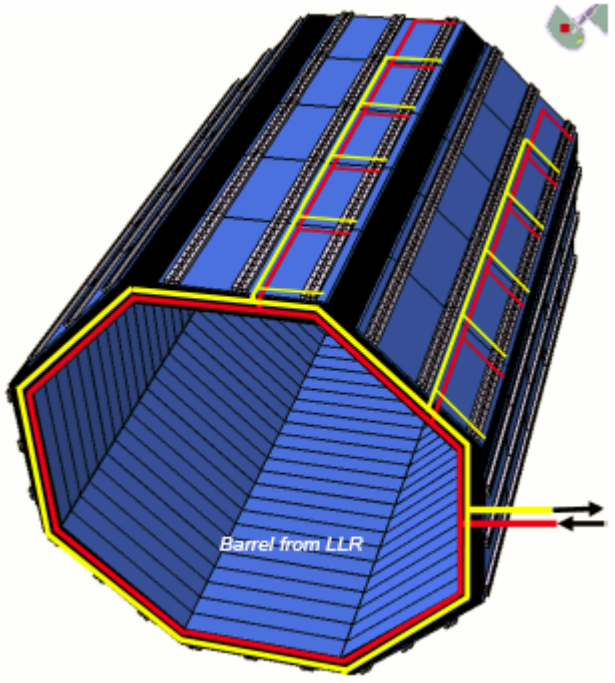
ILD concept detector



Orienté “particle flow”
Détecteurs à l’intérieur du solénoide

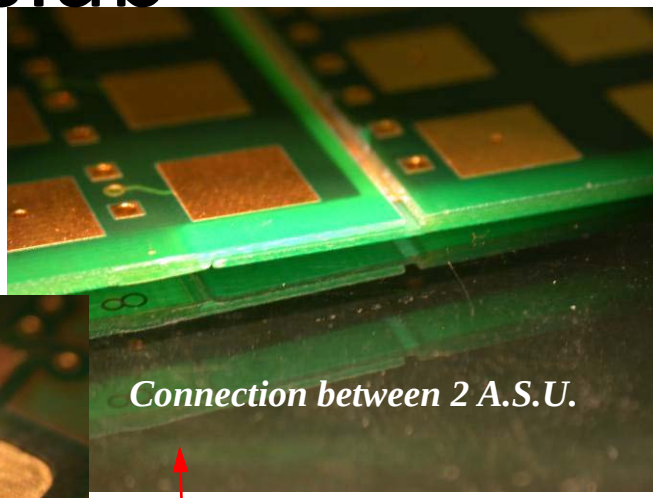


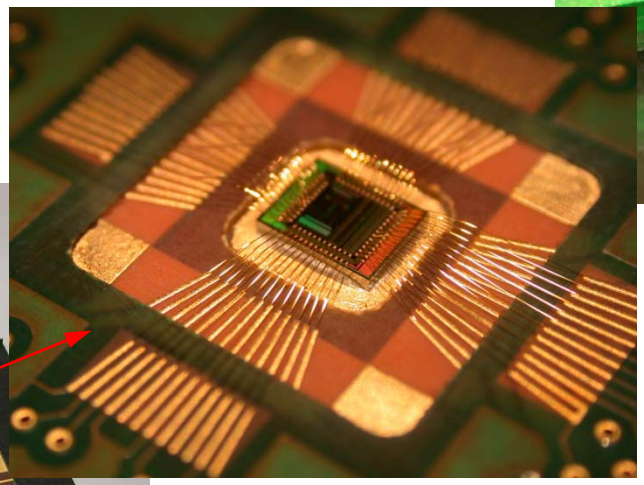
« Imaging calorimetry »
10000 voies / dm^3



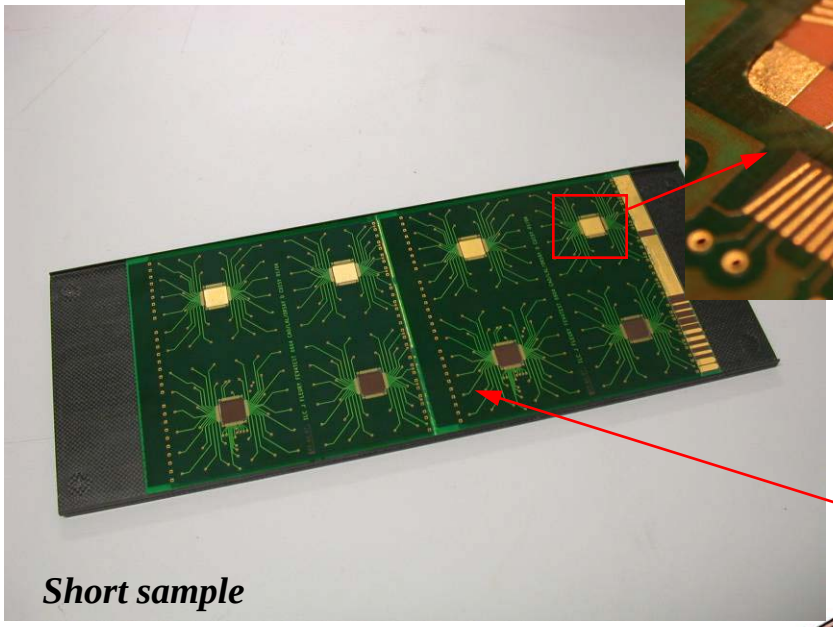
ECAL detector slab

Slightly relaxed mechanical constraints : ILD + 0.4 mm





Chip embedded



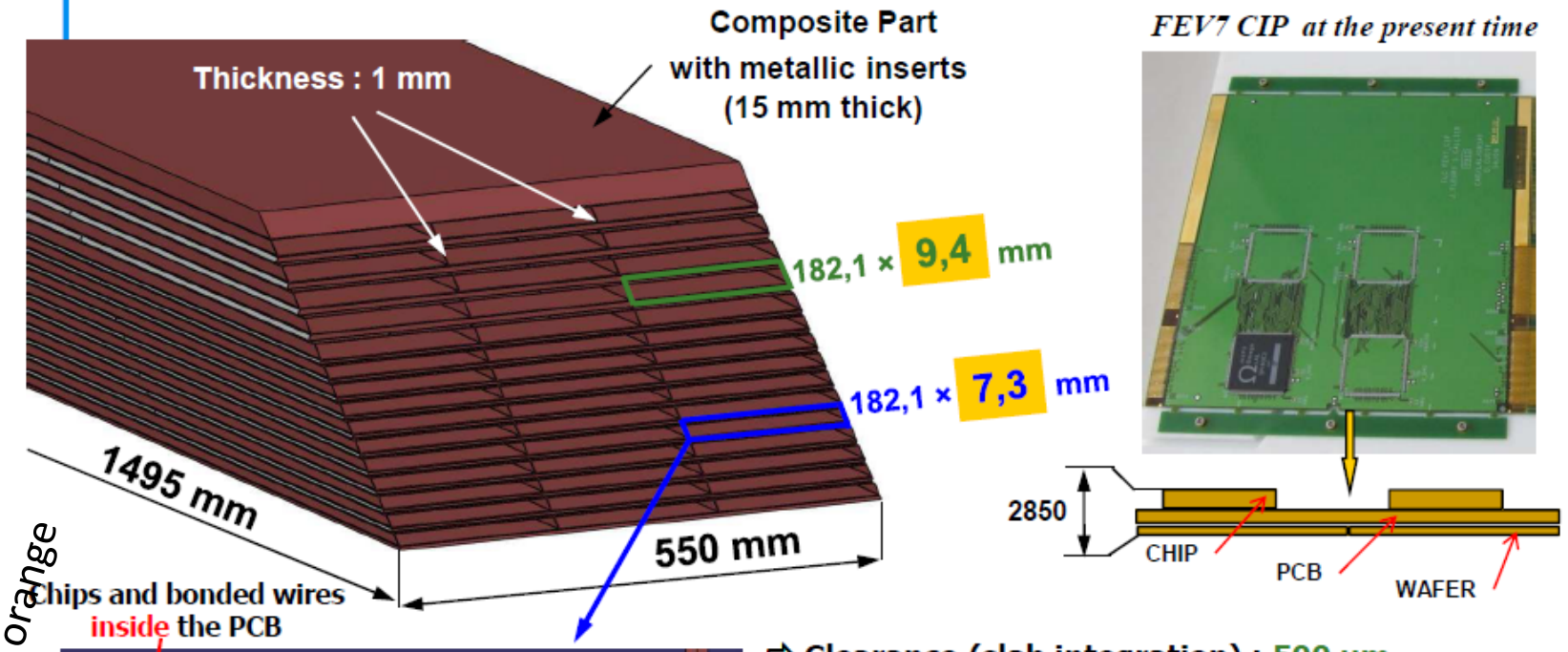
Short sample

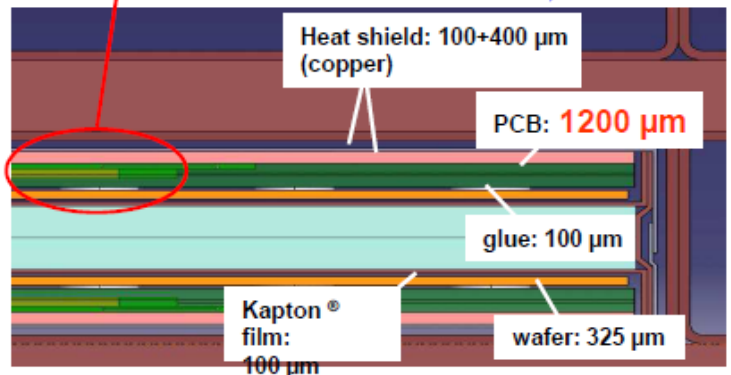
A long SLAB and a tower made up of short SLABs (30 layers)

Detector design

Sandwich made up of tungsten PCB and silicon. Slide into a Composite carbon fibre structure

EUDET design



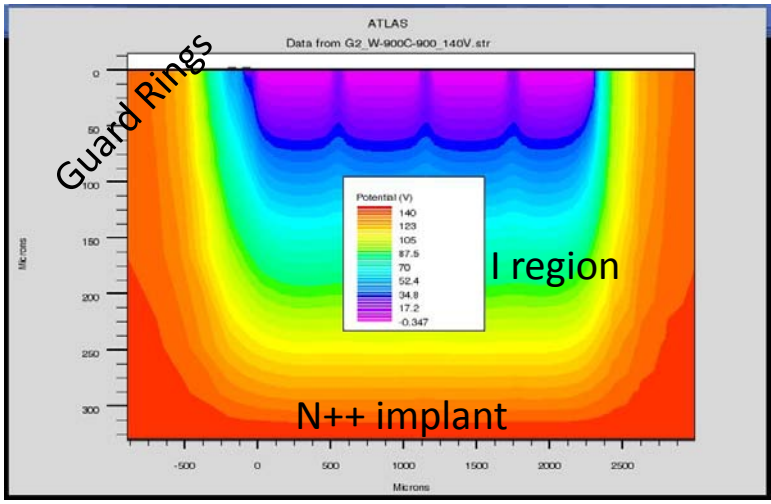


- ⇨ Clearance (slab integration) : 500 µm
- ⇨ Heat shield : 500 µm → Thermal demonstrator
- ⇨ PCB : 1200 µm → but 1100 µm used
- ⇨ Thickness of glue : 100 µm
- ⇨ Thickness of wafer : 325 µm
- ⇨ Kapton® film HV : 100 µm ? → tests
- ⇨ Thickness of W : 2100/4200 µm (± 80 µm)

Sensor Design

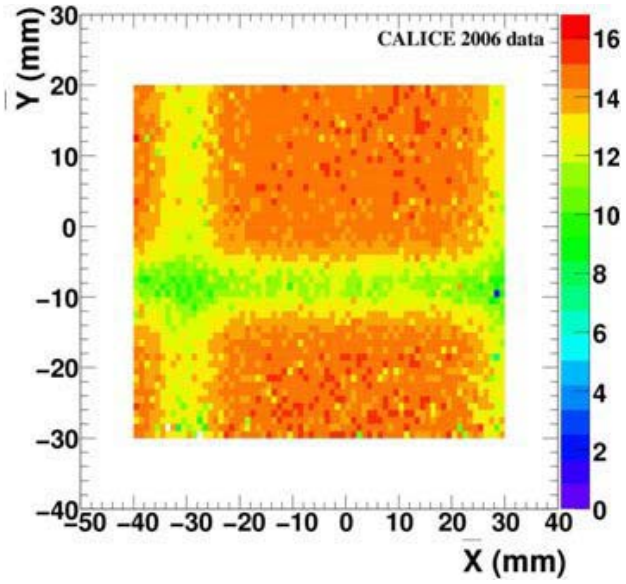
- The simplest design to control the cost
  - Few thousands of m² needed for ILD
  - Minimize the number of steps of the processing procedure
  - Guard rings = same as pixels
  - Glued on PCB : Floating GR
- Drawbacks : lack of optimization
  - Large dead zone at the edges: efficiency loss
  - Crosstalk between GR & pixels (Square Events)
- But…cost is still too high
  - 70 keur (including NRE) for 40 pcs of this hamamatsu prototype = 22 € / cm2 (14 w/o NRE)
  - Cost limit for feasibility of ILD : ~3 € /cm²

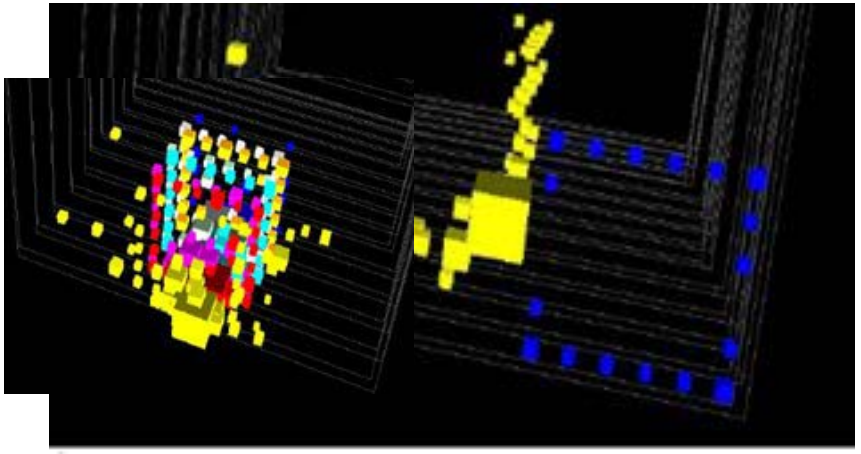
P++ implants (pixels)



9x9 cm², 324 pixels

2 défauts





Zone “morte” à la périphérie : -20% d’efficacité de détection

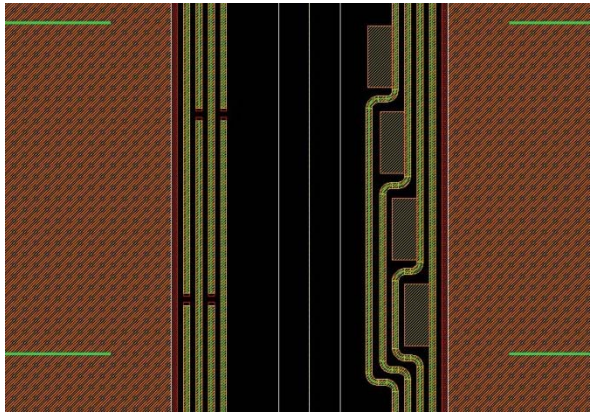
Peut être compensé off-line

Evénements carrés : diaphonie guard-rings – pixels périphériques

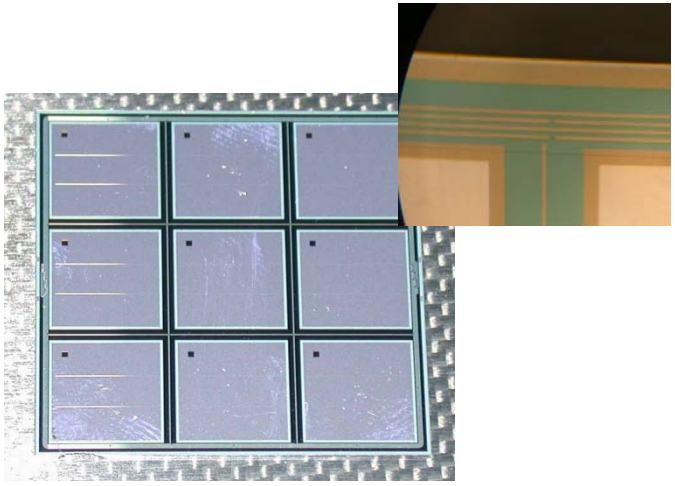
A minimiser par un facteur 50 à 100

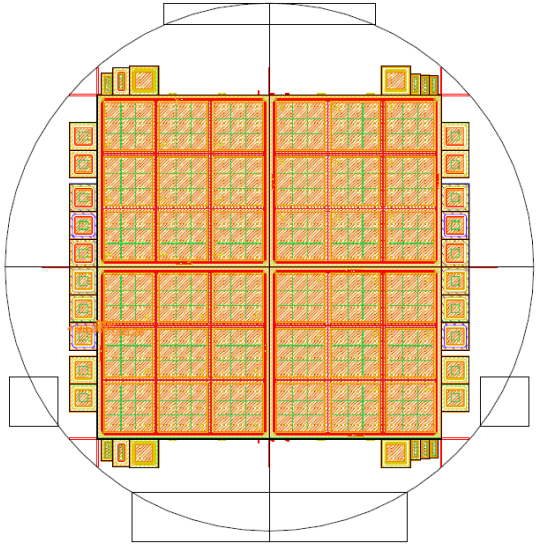
Segmented guard ring

- Should avoid the signal propagation along the border of the wafer



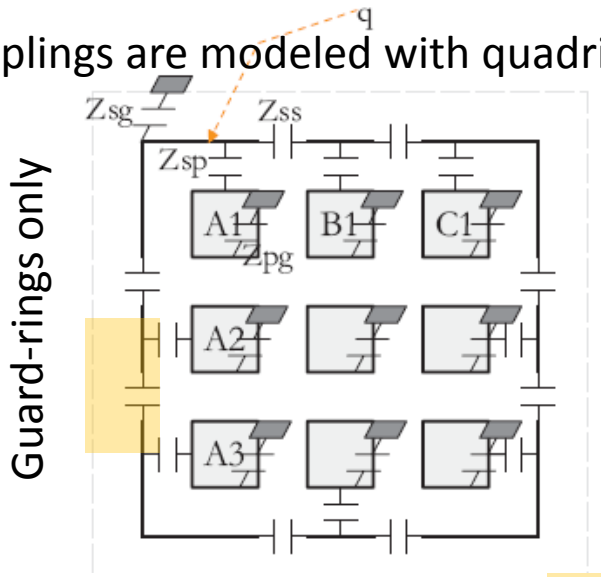
- Prototype wafers have been manufactured (LLR made layout)
  - OnSemi/Institute of Physics (Prague), Cz
  - BhaBha Atomic Research Centre, India
  - Tests are ongoing





Modélisation

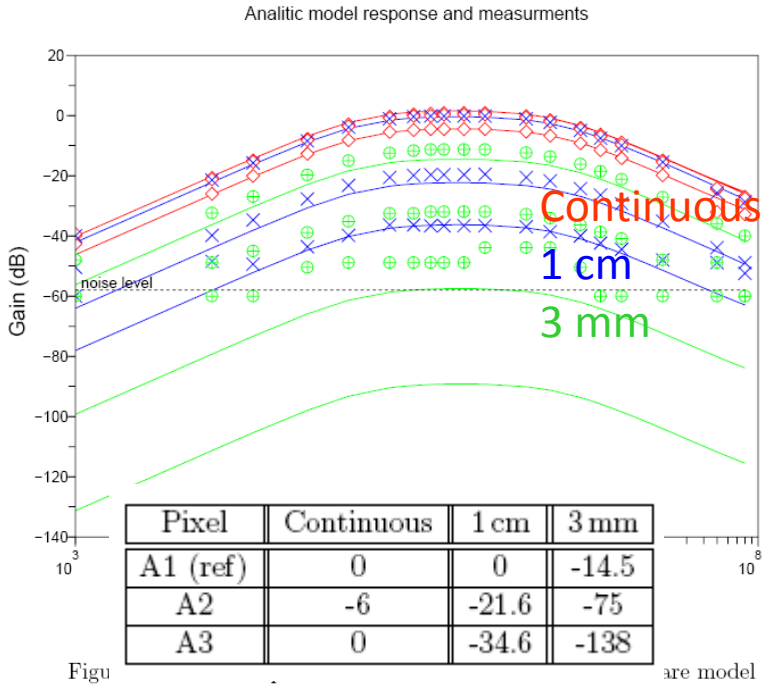
Couplings are modeled with quadripoles filters



$$T = T_{elec} \times T_{pix} \times (T_{seg} \times T_{ss})^{N_{seg}} \times T_{seg} \times T_{inj}$$

Measurement electronics — Crosstalk — Charge injector

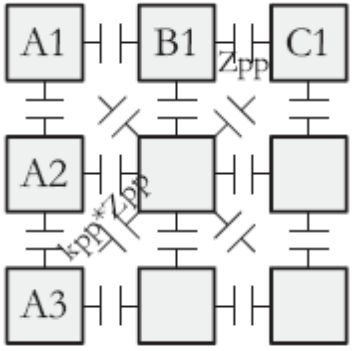
Mesures :



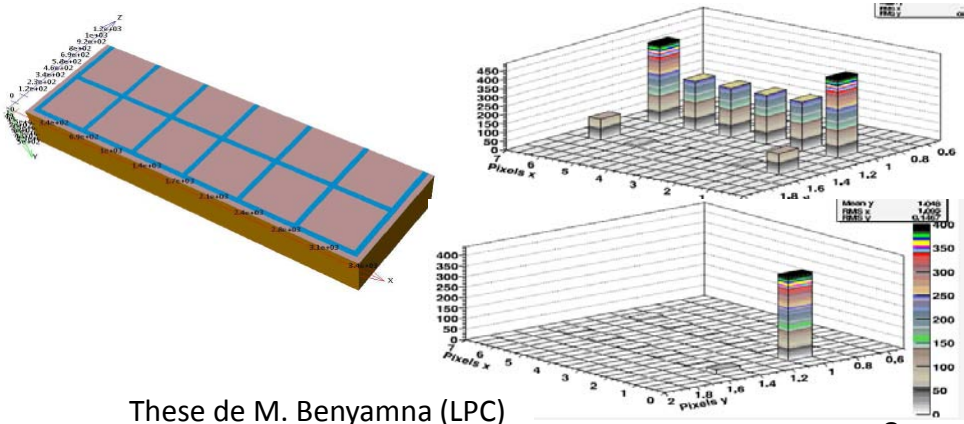
Pixel	Continuous	1 cm	3 mm
A1 (ref)	0	0	-14.5
A2	-6	-21.6	-75
A3	0	-34.6	-138

Figu … are model

Additional electrical simulations (SPICE) including the pixel to pixel crosstalk

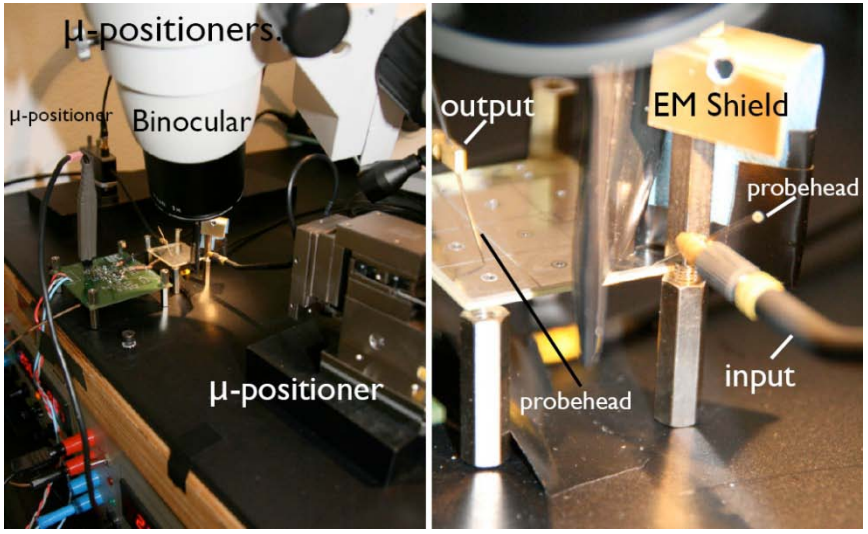


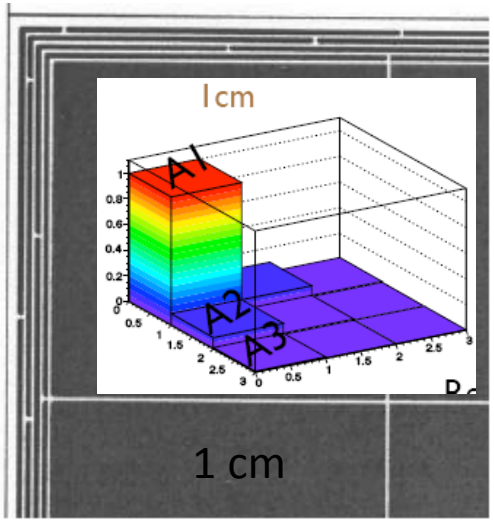
TCAD simulation (Silvaco)

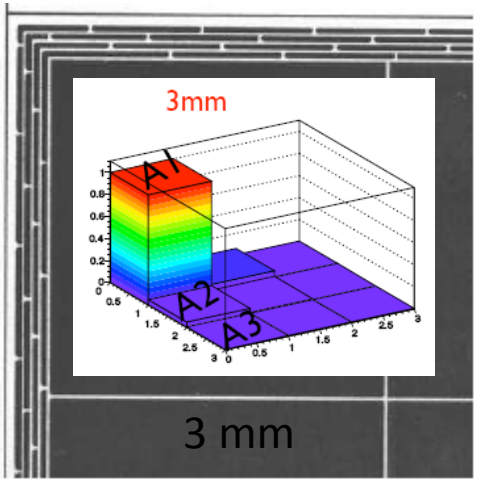


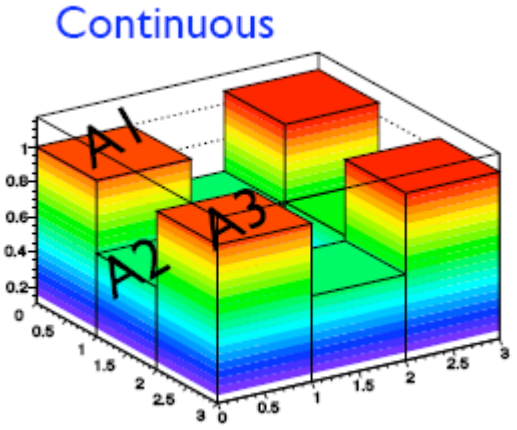
These de M. Benyamna (LPC)

Mesures

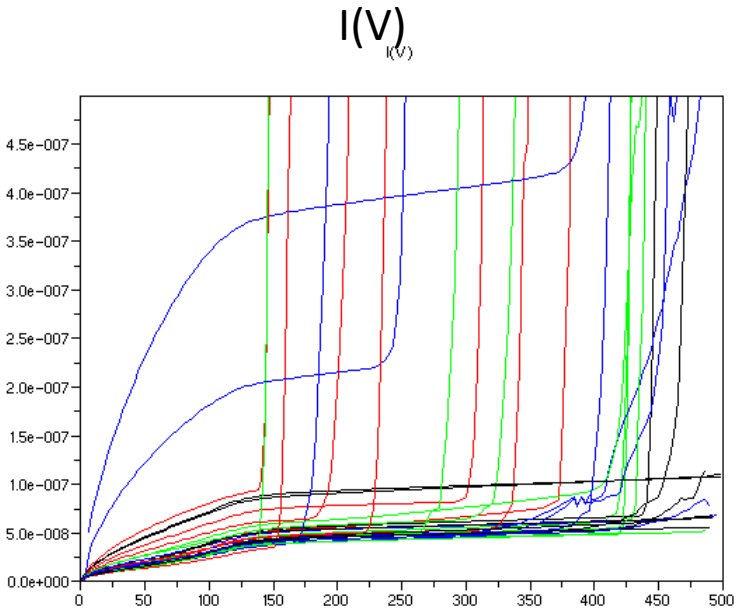

µ-positioners
µ-positioner
Binocular
µ-positioner
output
EM Shield
probehead
probehead
input


1cm
A1
A2
A3
1 cm


3mm
A1
A2
A3
3 mm


Continuous
A1
A2
A3

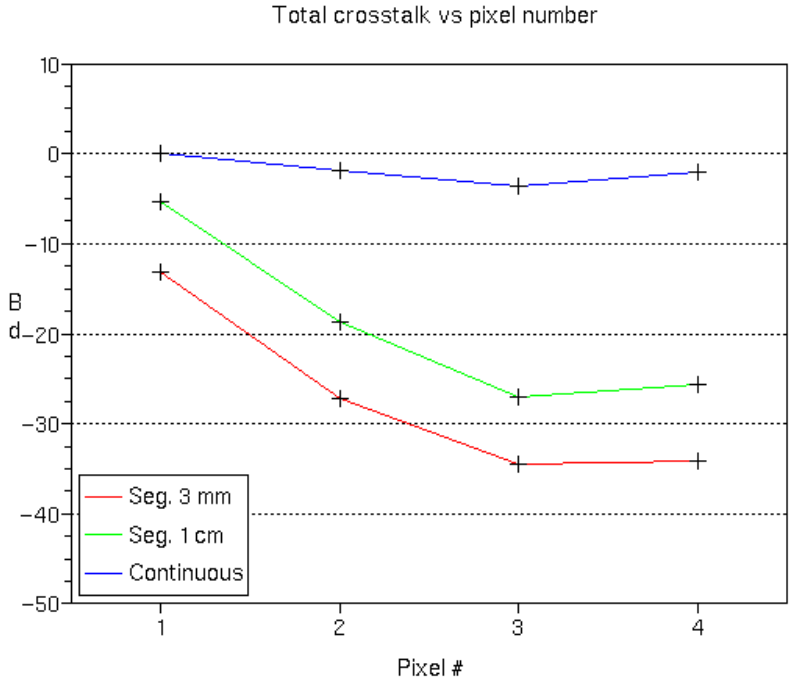
R&D on segmented guard rings



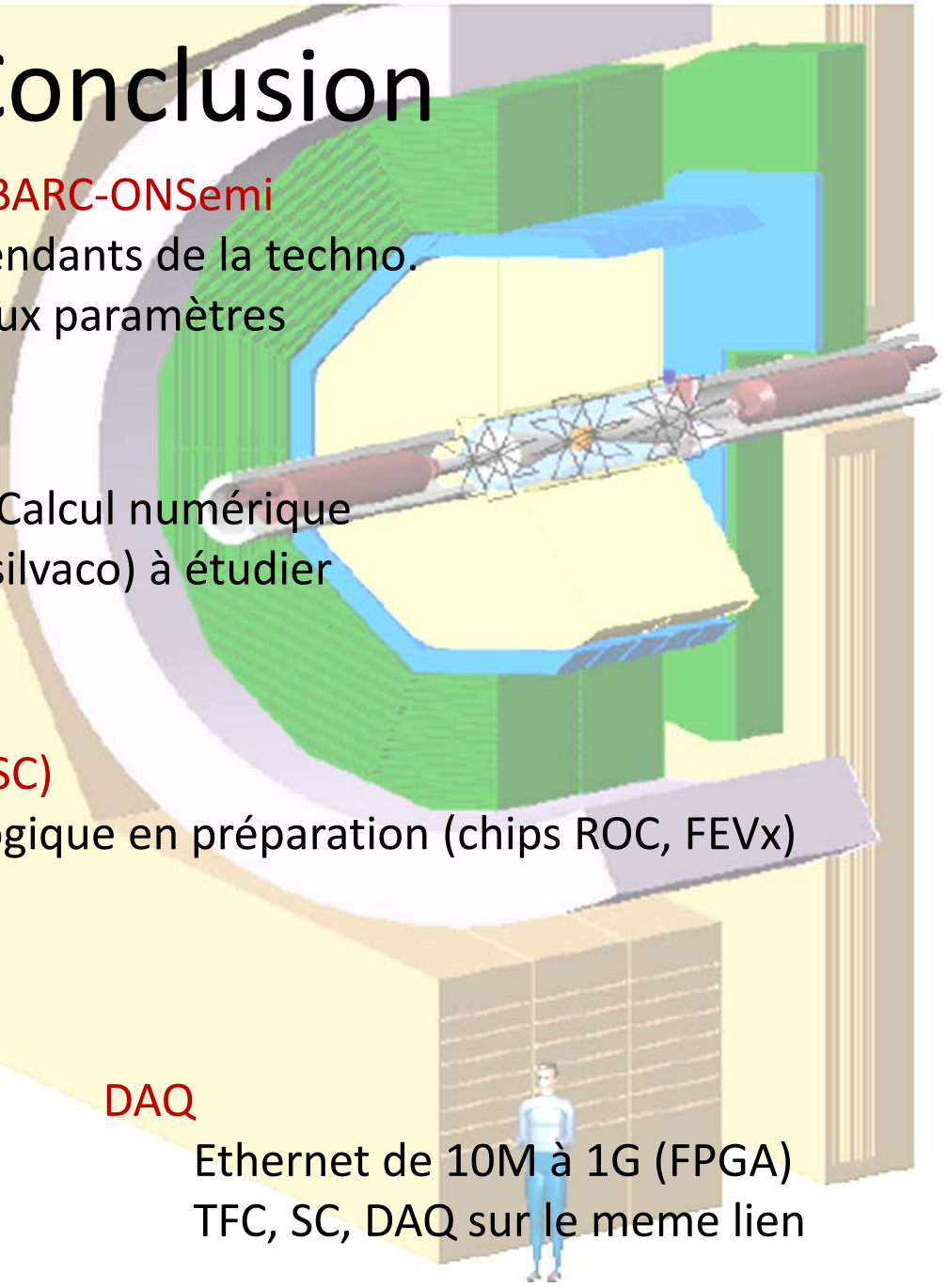
Yield (Breakdown >250V)

- Continuous: 100%
- 1 cm: 85%
- 3 mm: 40%
- Mixed: 70%

Sum of GRs contribution
Xtalk lowered by a factor 50 (with 3 mm segments (measurements made at LPC)



Conclusion



Collaboration LLR-LPC-BARC-ONSemi

Résultats très dépendants de la techno.

Difficulté d'accès aux paramètres

Utilisation d'outils variés

CAO, TCAD, Physique, Calcul numérique

Couplage CAO-TCAD (silvaco) à étudier

Si-W ECAL (LAL, LLR, LPSC)

Prototype technologique en préparation (chips ROC, FEVx)

ILC / CLIC

ALICE et PHENIX

DAQ

Ethernet de 10M à 1G (FPGA)

TFC, SC, DAQ sur le meme lien