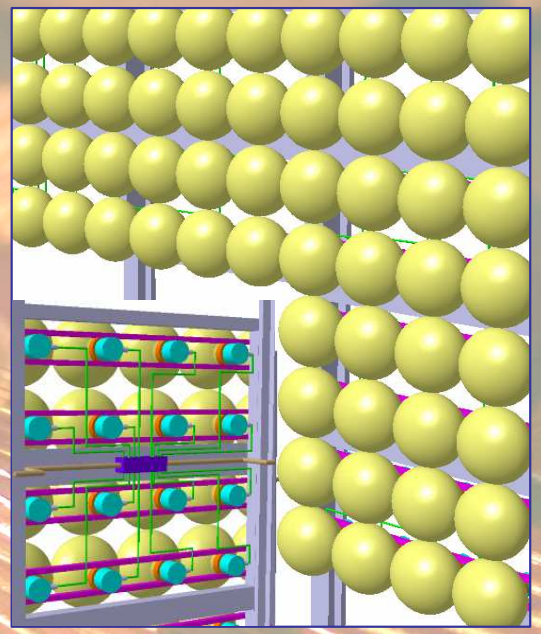
IN2P3 CSNSM

Omega

PARISROC2

Photomultiplier Array Integrated in Sige Read Out Chip



PMm²

DULUCQ Frederic

21/06/2010

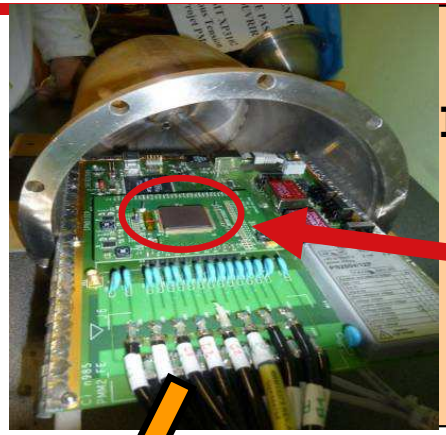
Orsay MicroElectronics Group Associated

Table of contents

- Part 1: PMM2 & PARISROC Overview
- Part 2: Why a second PARISROC
- Part 3: Presentation of PARISROC2
- Part 4: Measurements
- Part 5: Conclusion & future

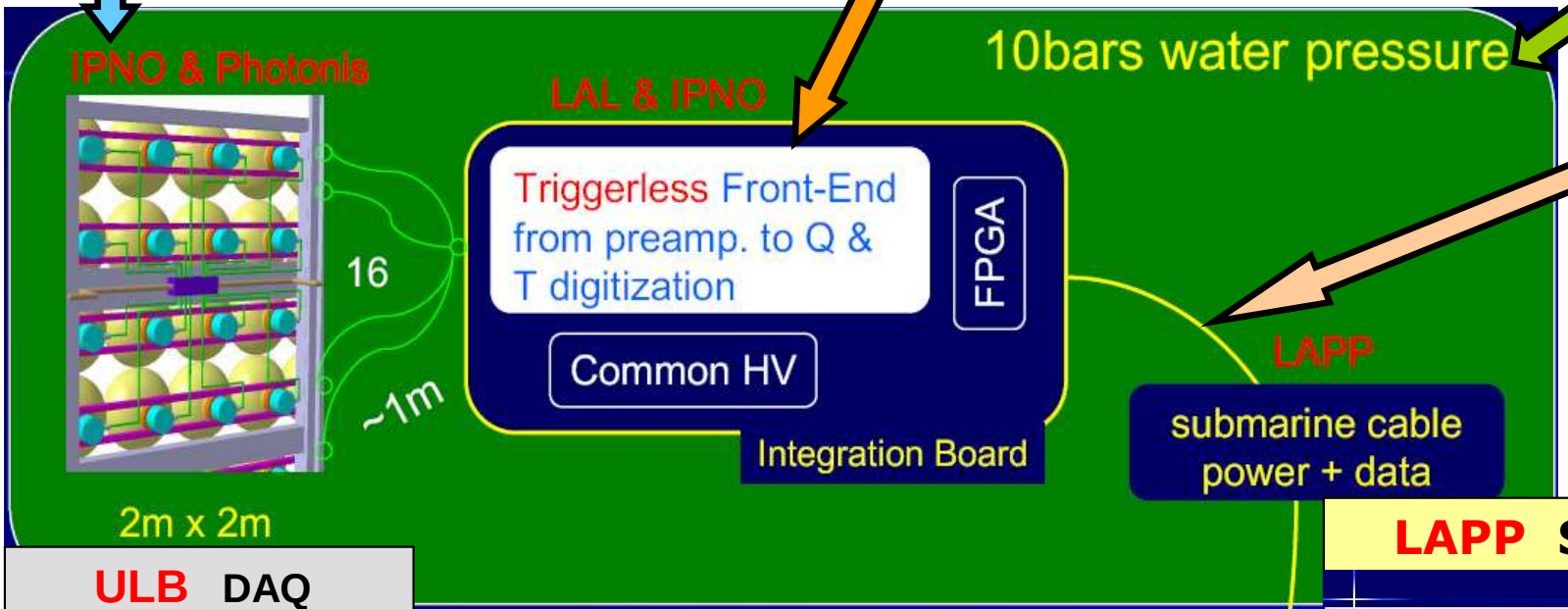
Part1: PMM2 collaboration (ANR)

IPNO
new shape
glass thickness
Photonis
realization



IPNO:
Integration Board
LAL:
PARISROC
Watertight Box

Pressure vessel
(BNL,USA)



LAPP
Hydrocable

ULB DAQ

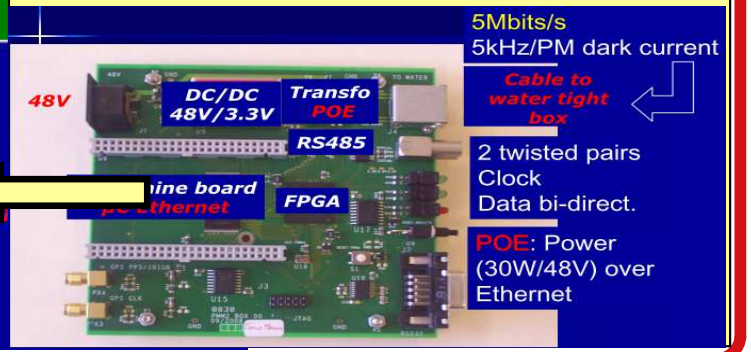
TCP/IP

µControler | FPGA

Power + Decoding Board

ULB

LAPP Submarine Card



Part1: PMM2 & PARISROC 1 overview

- 16 PMTs independent channels

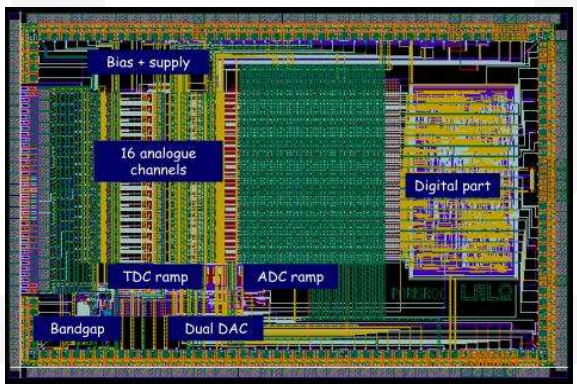
- Analog F.E. + charge and time digitization
- 1/3 p.e. 100% trigger efficiency (50fC @ 10^6)
- Charge dynamic range 0 to 300p.e (50pC @ 10^6)
- < 1 ns time stamping resolution

- Each channel has a variable gain

- To compansate gain vs HV spread for the 16 PMTs

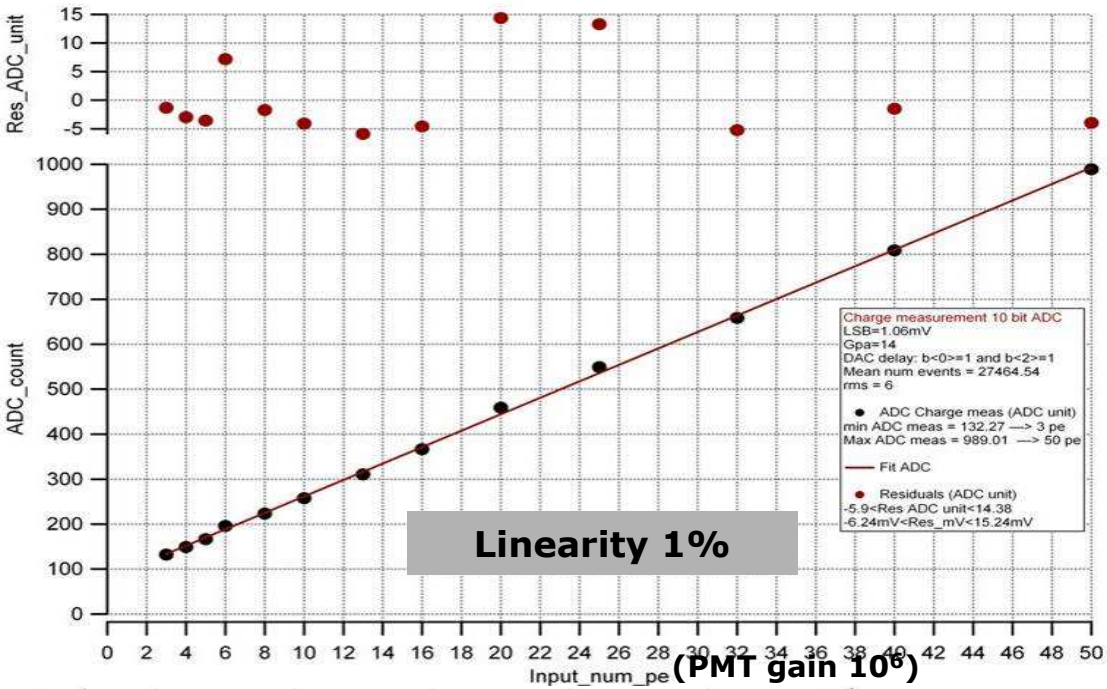
- Triggerless mode & autonomous

- All the PMTs signals above the threshold (1/3 p.e.) generate a trigger and are converted in digital data



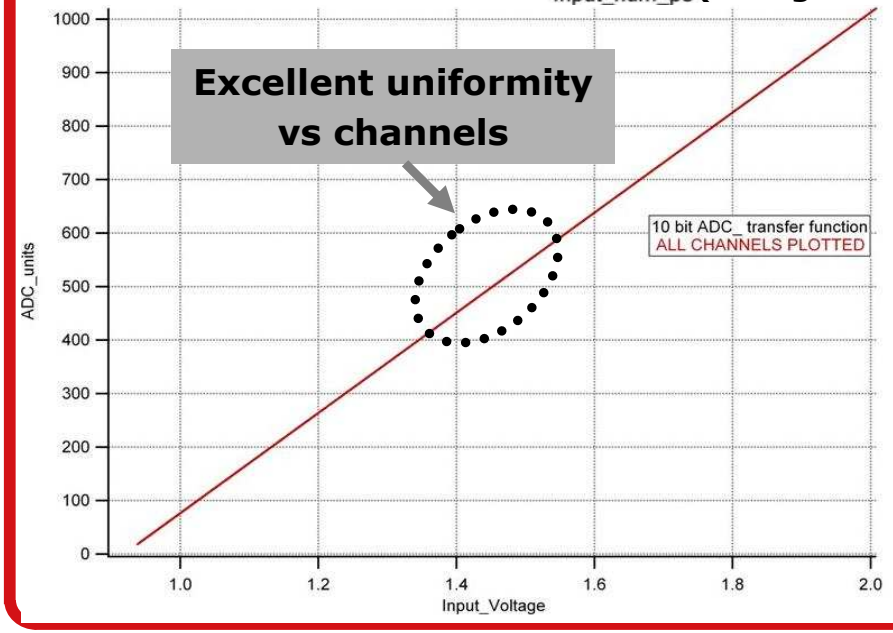
Part2: PARISROC 1 limitations (charge)

Complete chain: Autotrigger+T&H+Internal ADC



Linearity 1%

(PMT gain 10^6)



Excellent uniformity vs channels

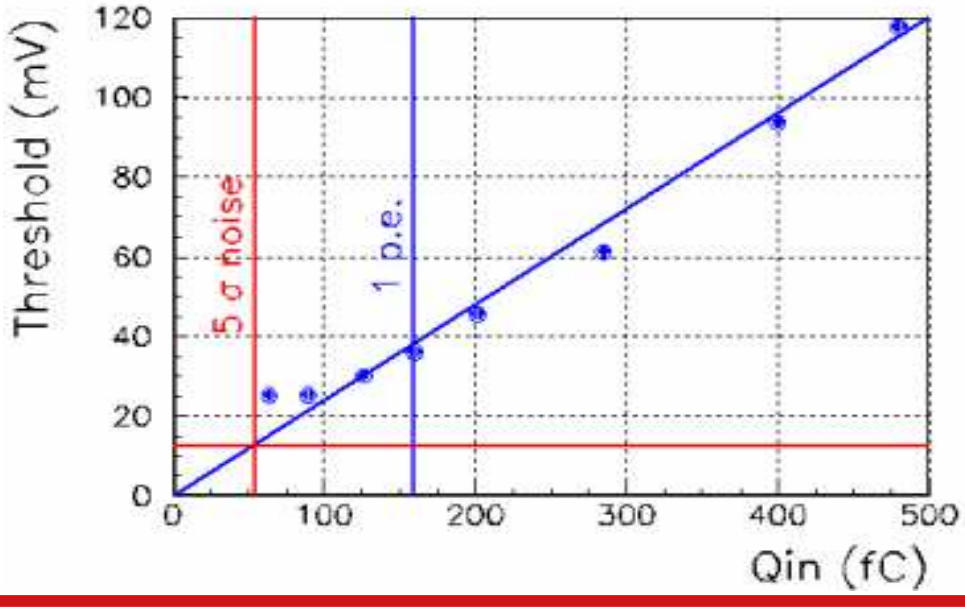
Good overall performance of PARISROC1

- Good analog signals
- Good chip uniformity vs channels
- Good complete chain results

BUT, some extra noise observed

- Low frequency noise
- Clock noise
- Coupling signal

Trigger limited to 10 σ due to discriminator coupling (Noise 13 fC)



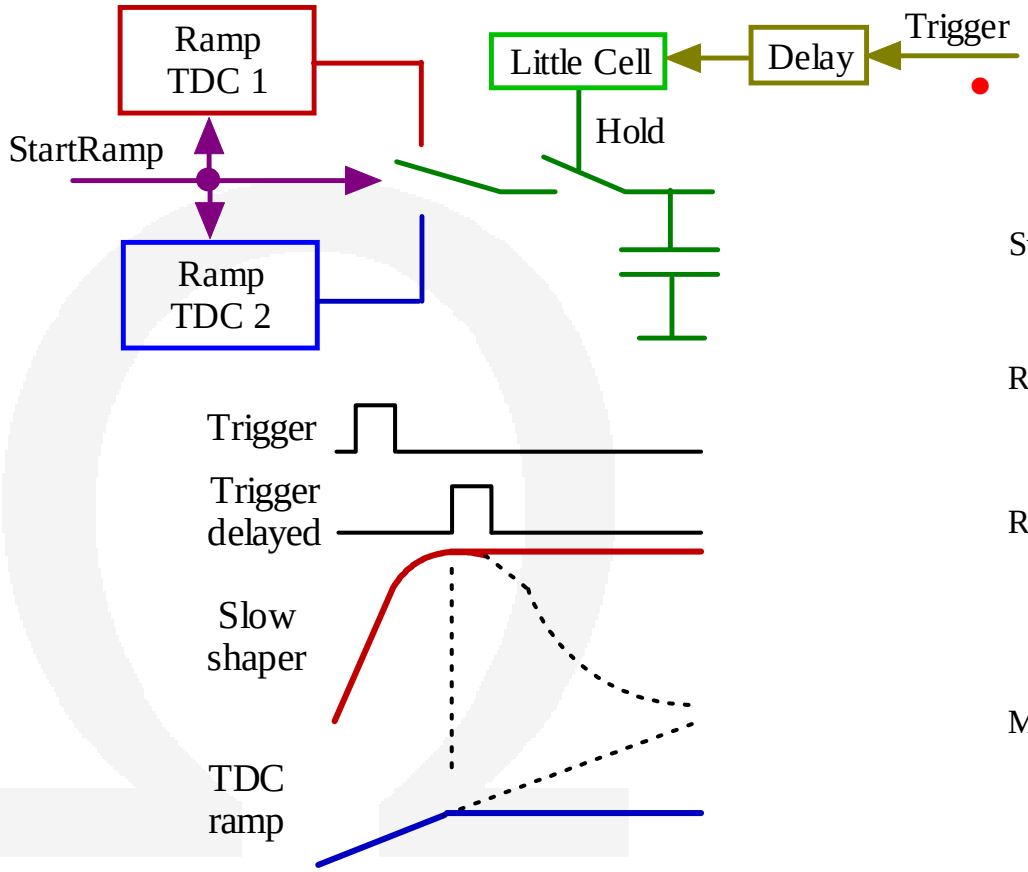
Part2: PARISROC 1 limitations (time)

- Hit rate ➔ Parisroc1 has too high loss rate (up to 16%) for our physics (depends on PMT)

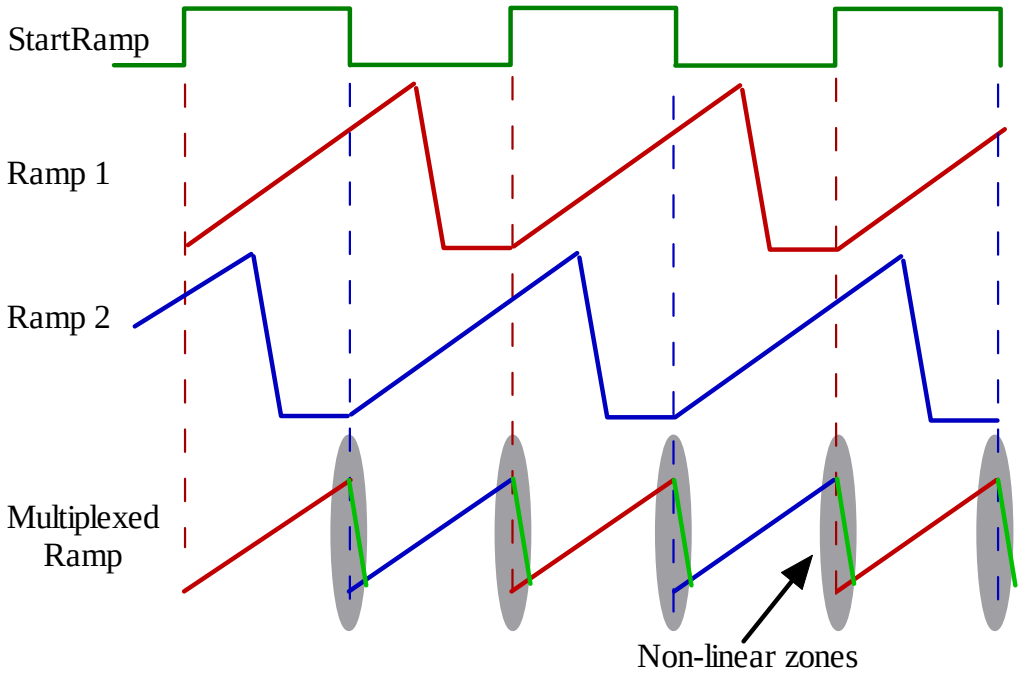
Parisroc1

R_{bkg}	n_{SCA}	n_{bits}	F_{RO}	Taux de pertes (%)
5 kHz	2	12	10 MHz	16 ± 12
0.1 kHz	2	12	10 MHz	0.008 ± 0.6
5 kHz	2	10	10 MHz	6 ± 10

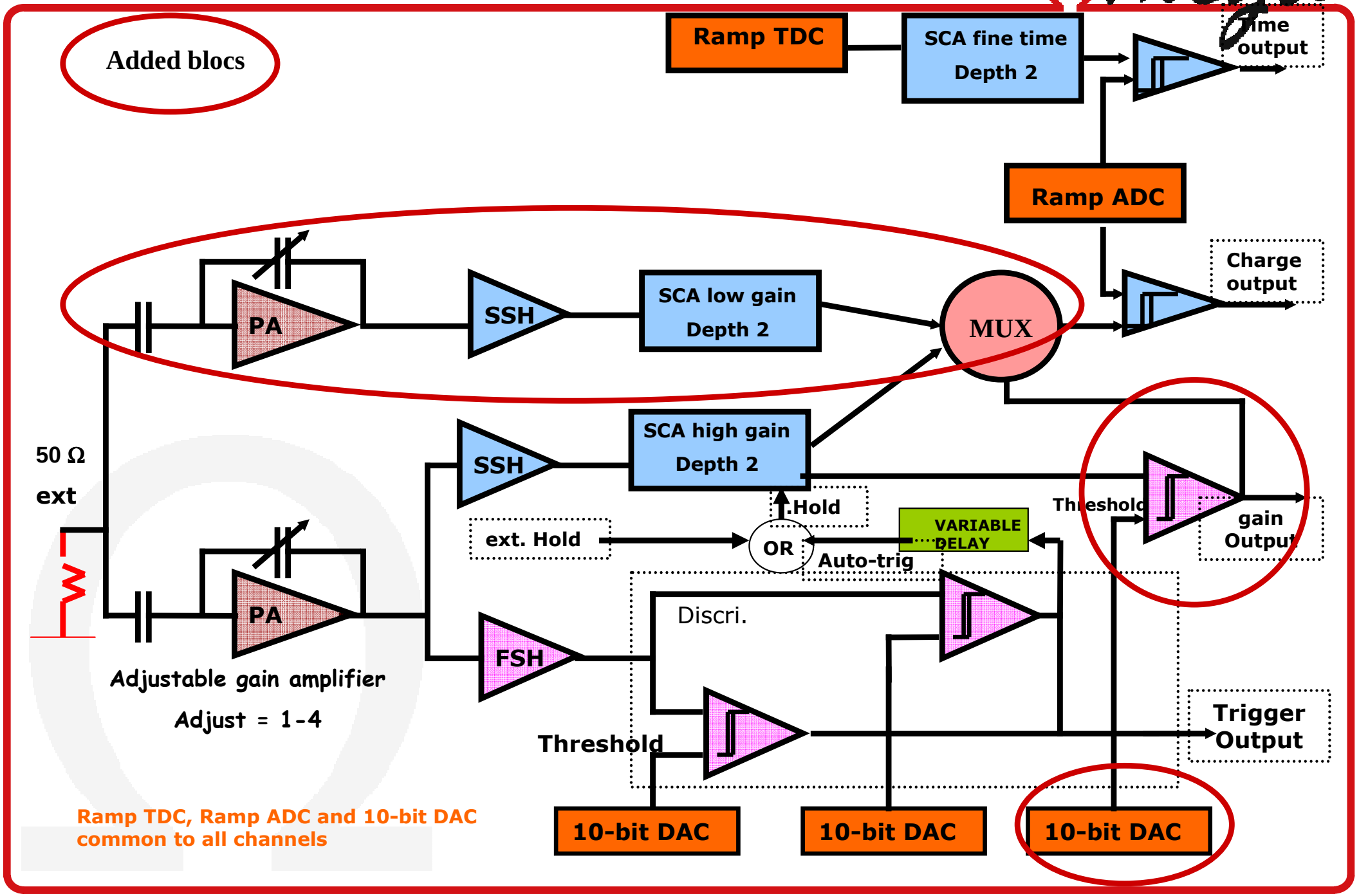
- Time measurement: Delay box jitter (max 300 ps) in time measurement



- Time measurement: 30% blind zone due to ramps multiplexing



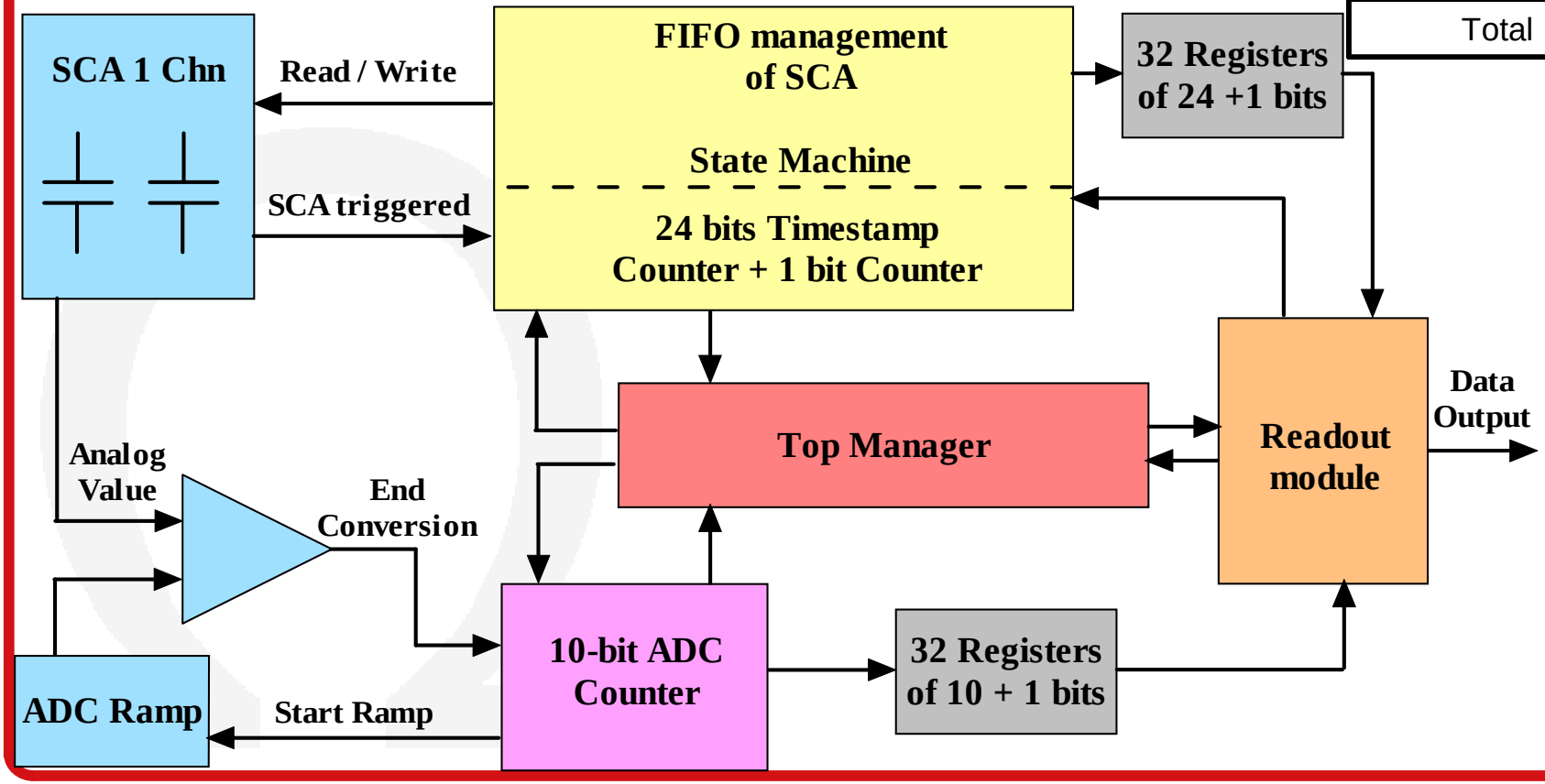
Part3: PARISROC 2 analog



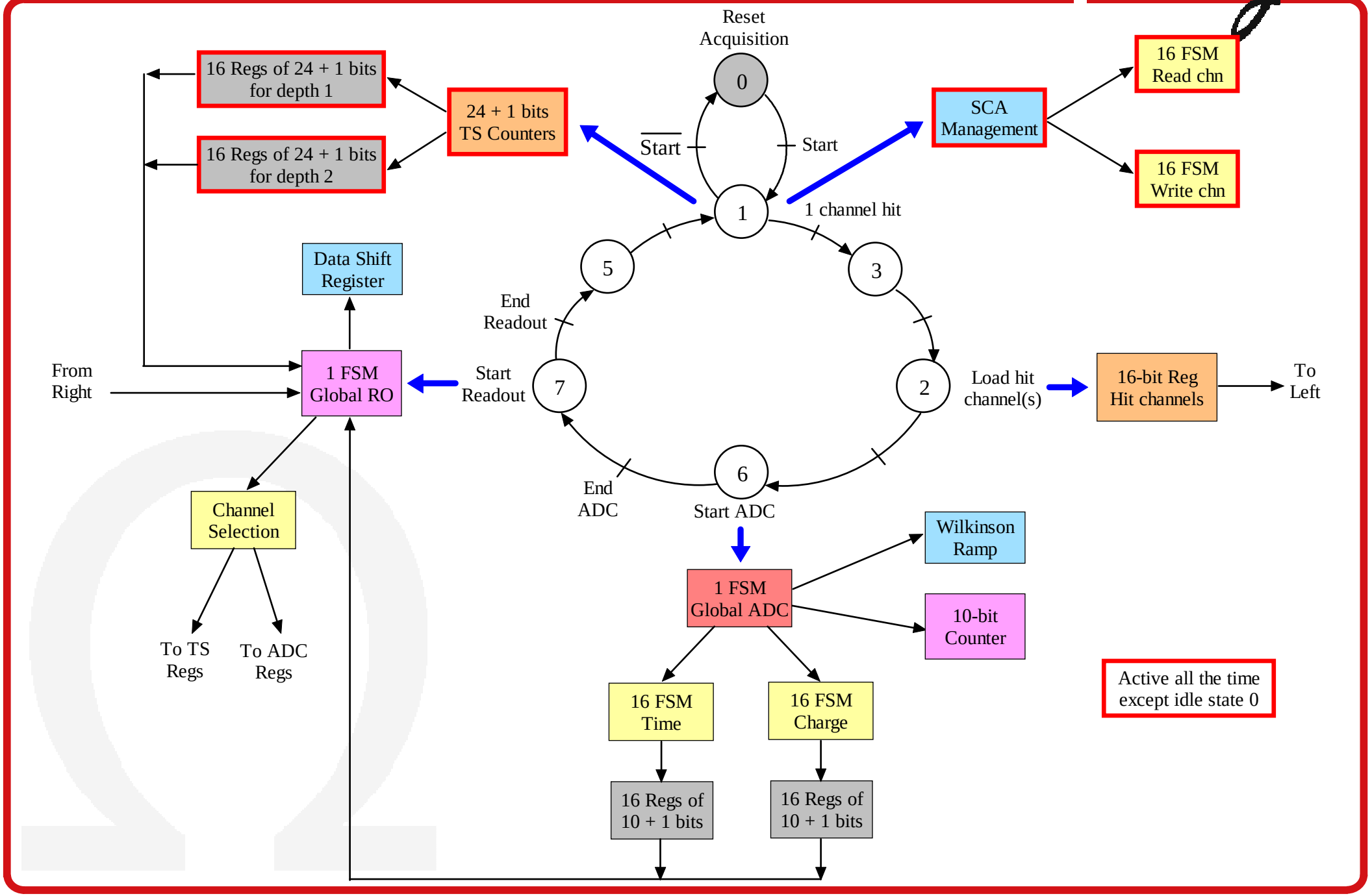
Part3: PARISROC 2 digital (1)

- SCA management of 16 channels independents
- SCA management with depth of 2 for time and charge
- SCA management like FIFO (ping-pong)
- Timestamp 24b +1b counters @ 10 MHz (1.67s)
- 40 MHz clock for ADC + SCA management + readout

	v1	v2
Channel #	4	4
Coarse time	24	24
Extra Coarse time	NA	1
Gain used	NA	1
Fine time (ADC)	12	10
Ramp used	NA	1
Charge (ADC)	12	10
Total	52 bits	51 bits



Part3: PARISROC 2 digital (2)



Part3: Hit rate improvement

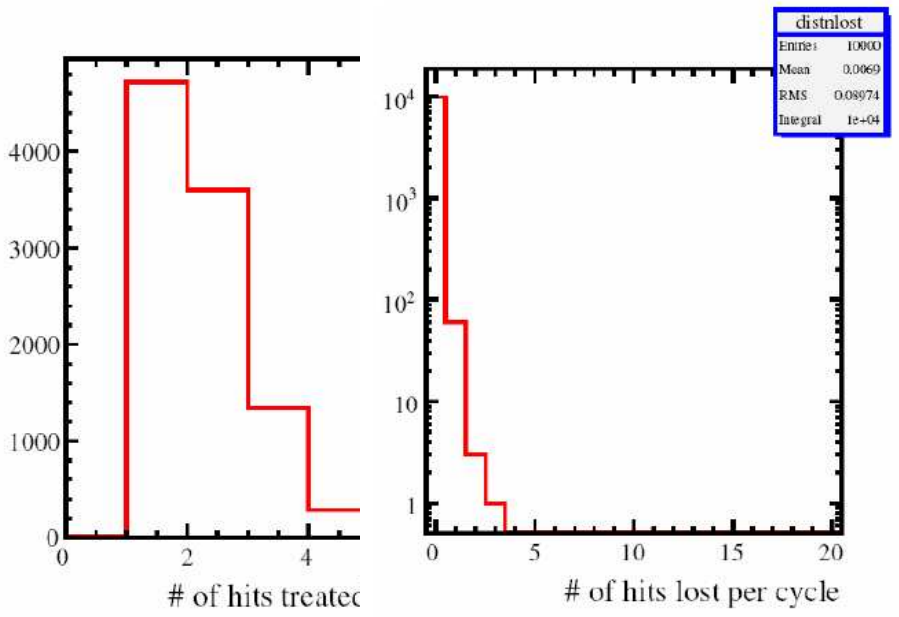
- Parisroc2 must be faster than Parisroc1 (gain of 4 minimum)

	R_{bkg}	n_{SCA}	n_{bits}	F_{RO}	Taux de pertes (%)
Parisroc1	5 kHz	2	12	10 MHz	16 ± 12
	0.1 kHz	2	12	10 MHz	0.008 ± 0.6
	5 kHz	2	10	10 MHz	6 ± 10
Parisroc2	5 kHz	2	8*	40 MHz	0.24 ± 3.1
	5 kHz	4	9*	40 MHz	0.007 ± 0.7

- Conversion 8-9-10 bits by selecting ramp slope
  - 8-9 bits is enough accuracy for time and for charge
  - Internal counter now 10-bit
  - Max conversion time : 25 us @ 10 bits
- Readout @ 40 MHz
  - Max readout time 25 us

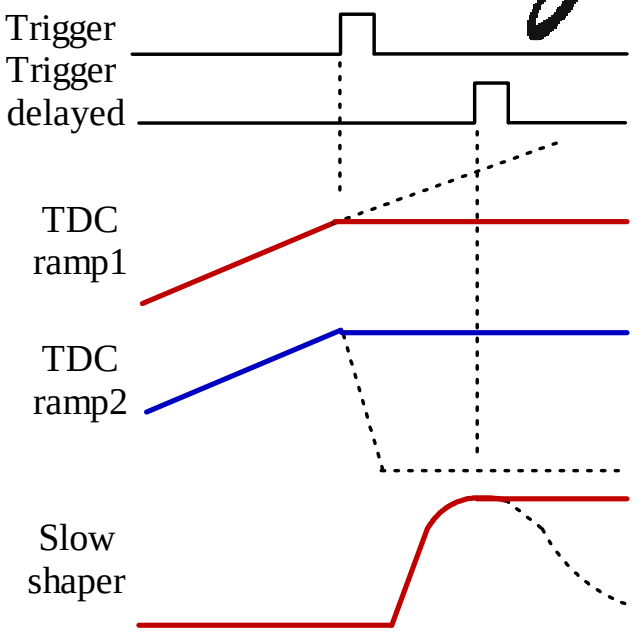
	PARISROC1	PARISROC2
Conversion	103 us	26 us
Readout	101 us	25 us
Total	204 us	51 us

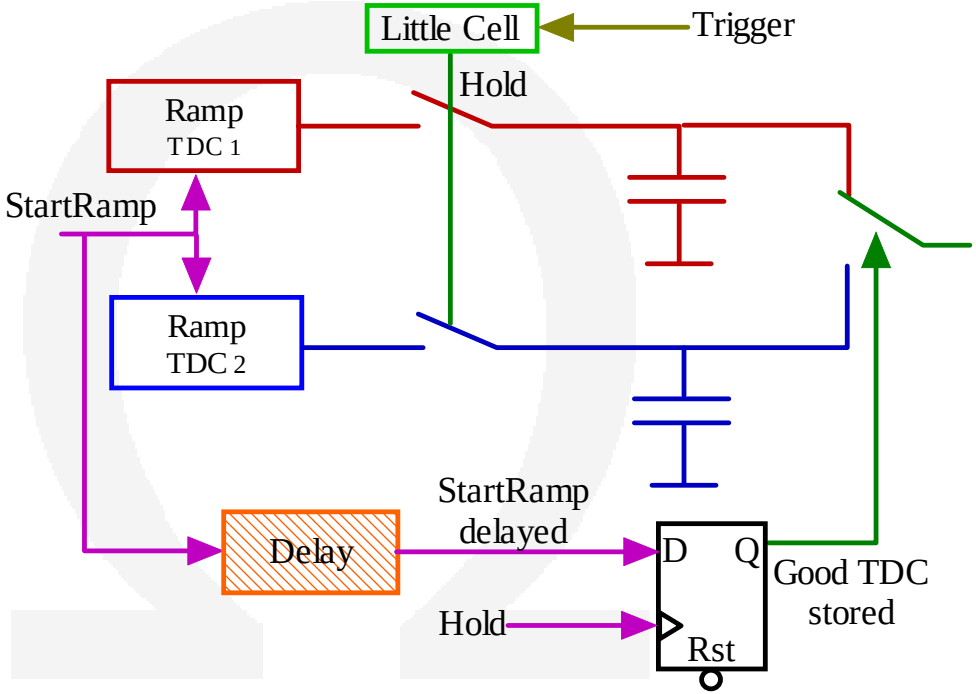
Worst case: 16 chn hit + ADC Ovfl

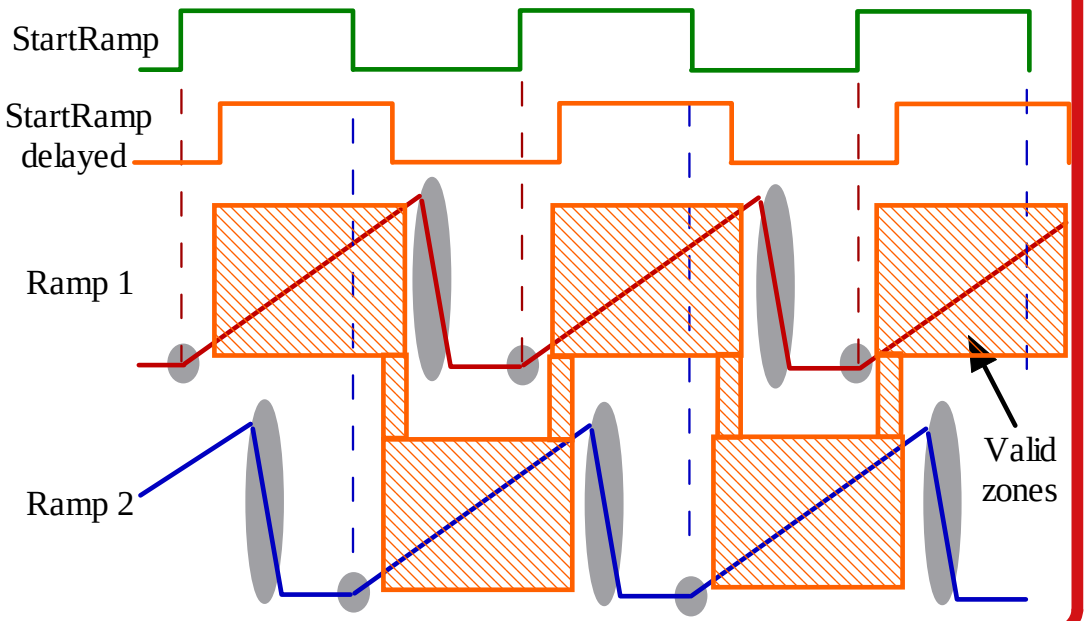


Part3: Fine time improvement

- New fine time (Measurement ➔ Talk S.DROUET)
  - The 2 ramps are stored in a capacitors
  - Overlap around 40ns between ramps
  - Separate hold for charge and time (jitter issue)
  - Need a signal to know which ramp is active and linear ➔ StartRamp delayed by 20ns
  - In overlap zones, coarse time counter has already counted "+1" as delay > clock tree latency + clock skew

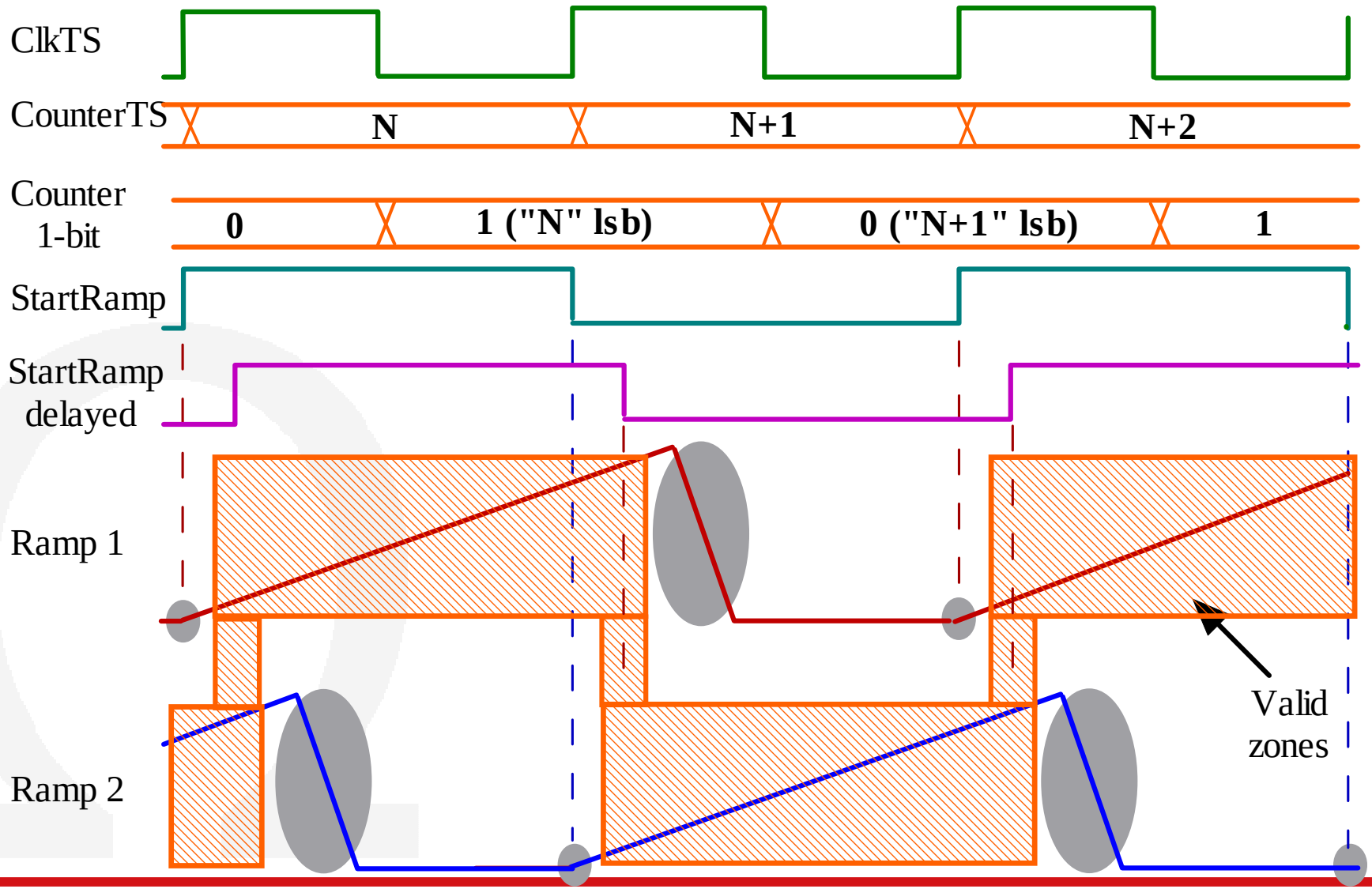






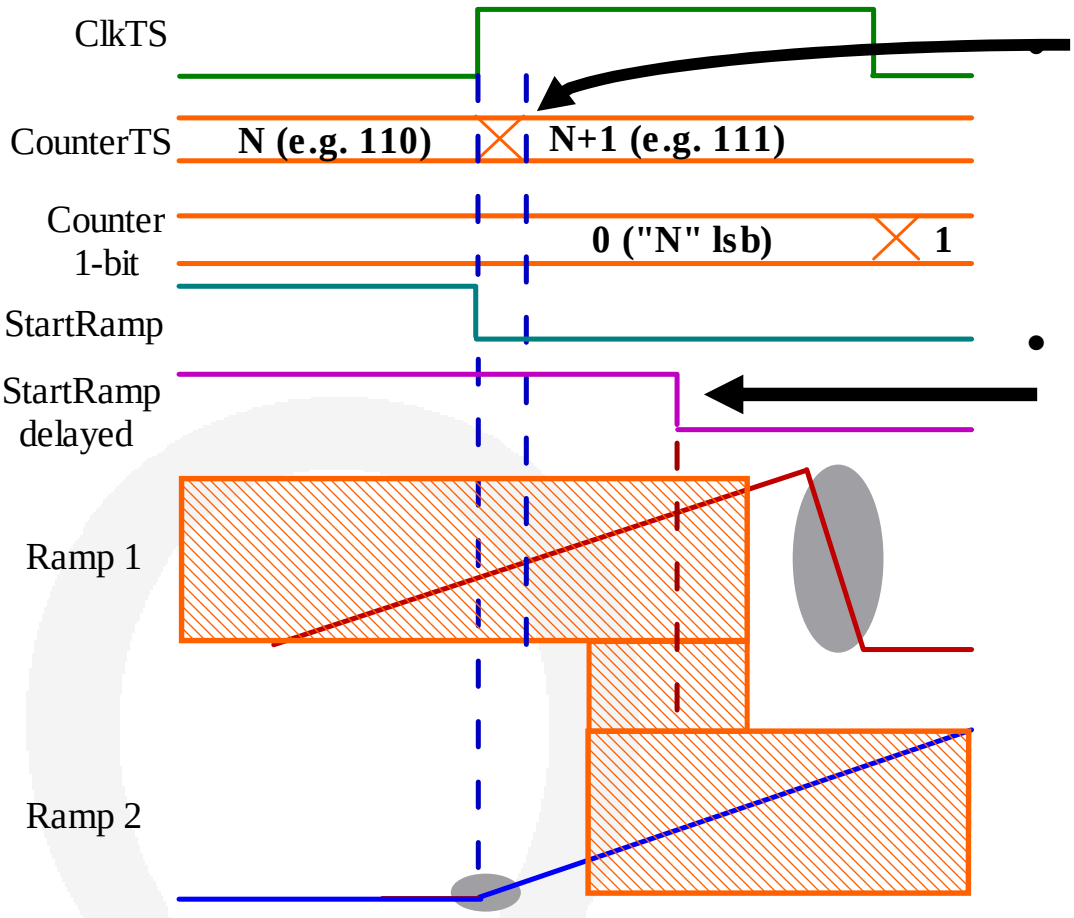
Part3: Coarse time (1)

- In PARISROC1, possible error in TS for triggers synchronous with clock
- In v2, 2 counters are implemented:
  - A 24-bit gray @ rising edge of 10MHz (same as v1)
  - A 1-bit @ falling edge of 10MHz



Part3: Coarse time (2)

- Thanks to overlap, we assume that converted fine time is always good (selection made with 1-bit reg in analog part).



For trigger synchronous with counter ➔
Data stored = (N or N+1), Cpt1Bit and Ttdc

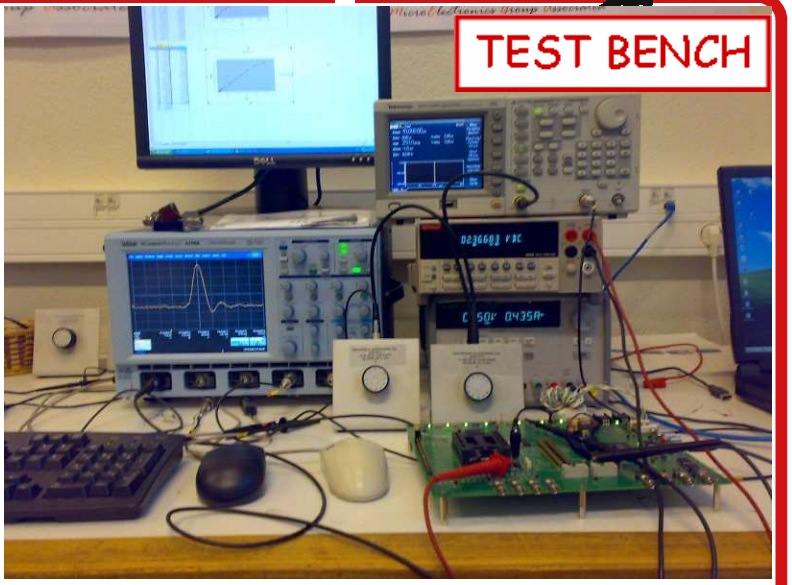
- For trigger synchronous with StartDelayed ➔
  Data stored = N+1, Cpt1Bit and (TtdcRamp1 or TtdcRamp2)

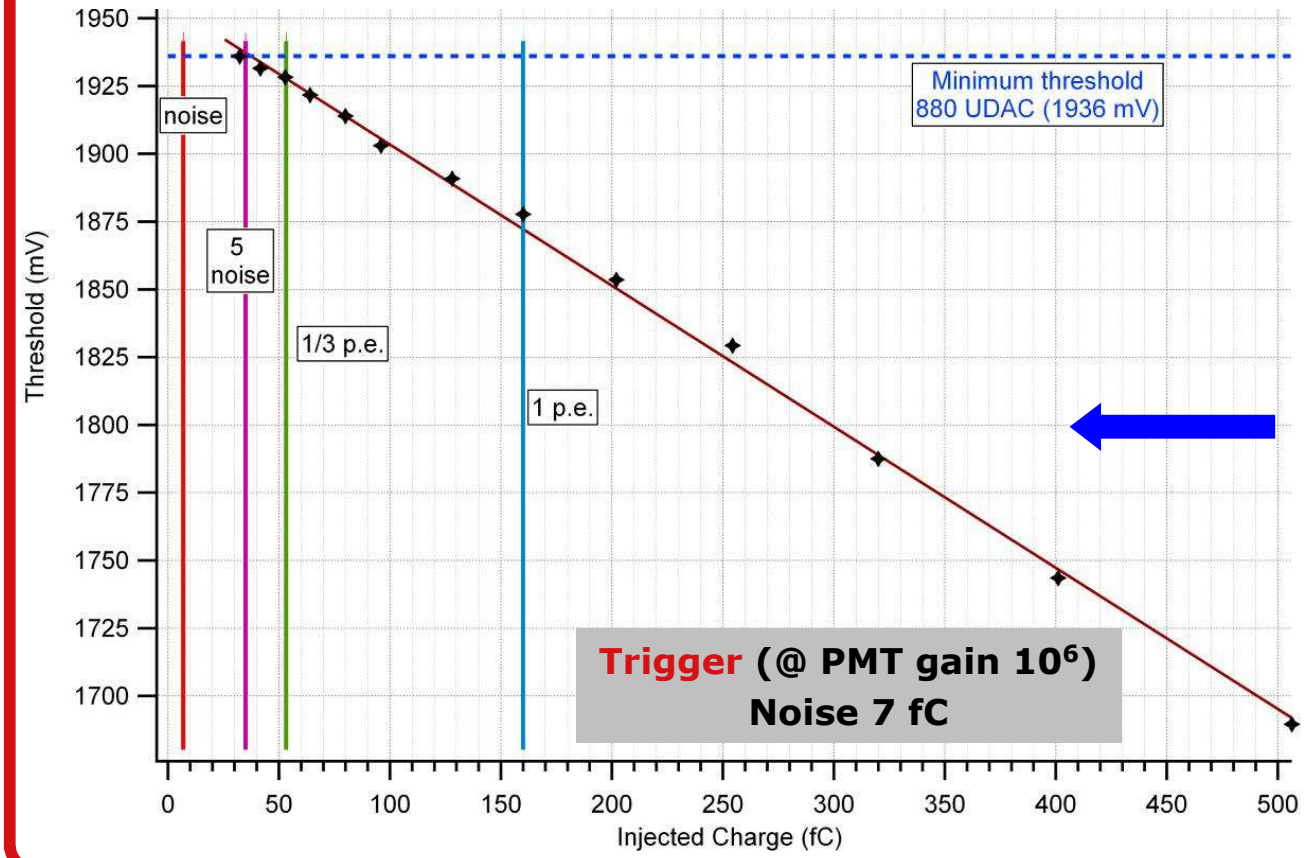
- Recover real time ➔

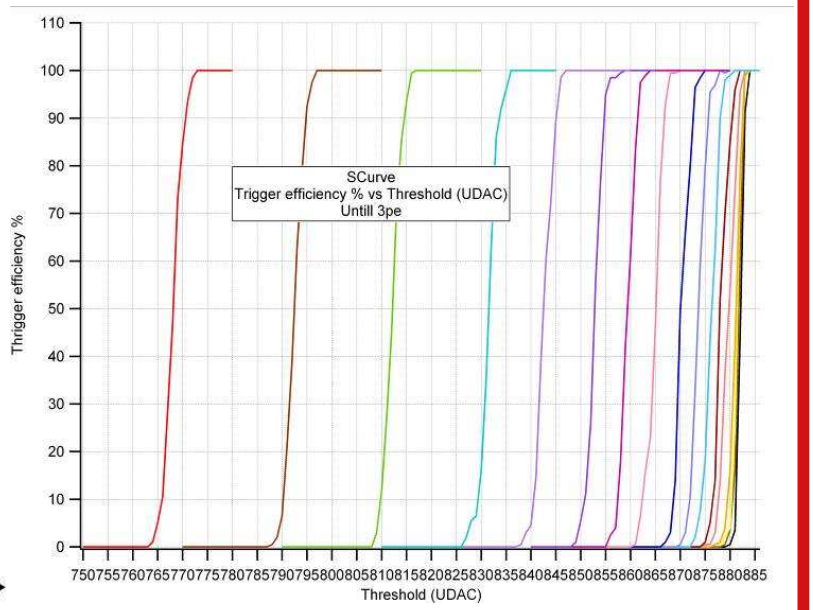
```
If (Ttdc > 90 ns) then
  If LSB(BIN(CptTS)) = (Cpt1Bit) then
        Time = CptTS + Ttdc
  else
        Time = (CptTS-1) +Ttdc
else
  Time = CptTS + Ttdc
```

Part4: First results (charge)

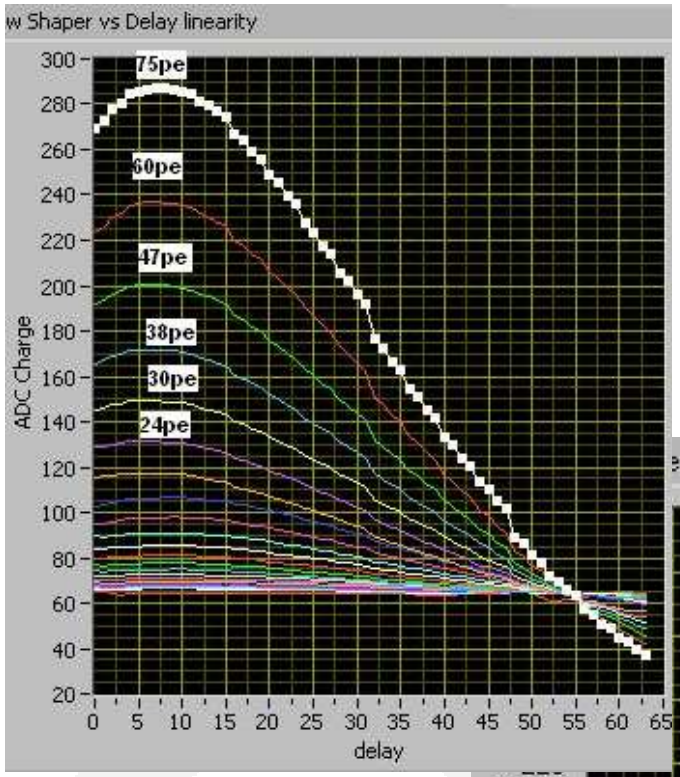
- Improvement in noise low noise; no clock noise
- No coupling signal
- Trigger improvement@ 1/3 of p.e.
  (50fC @ PMT gain 10^6)







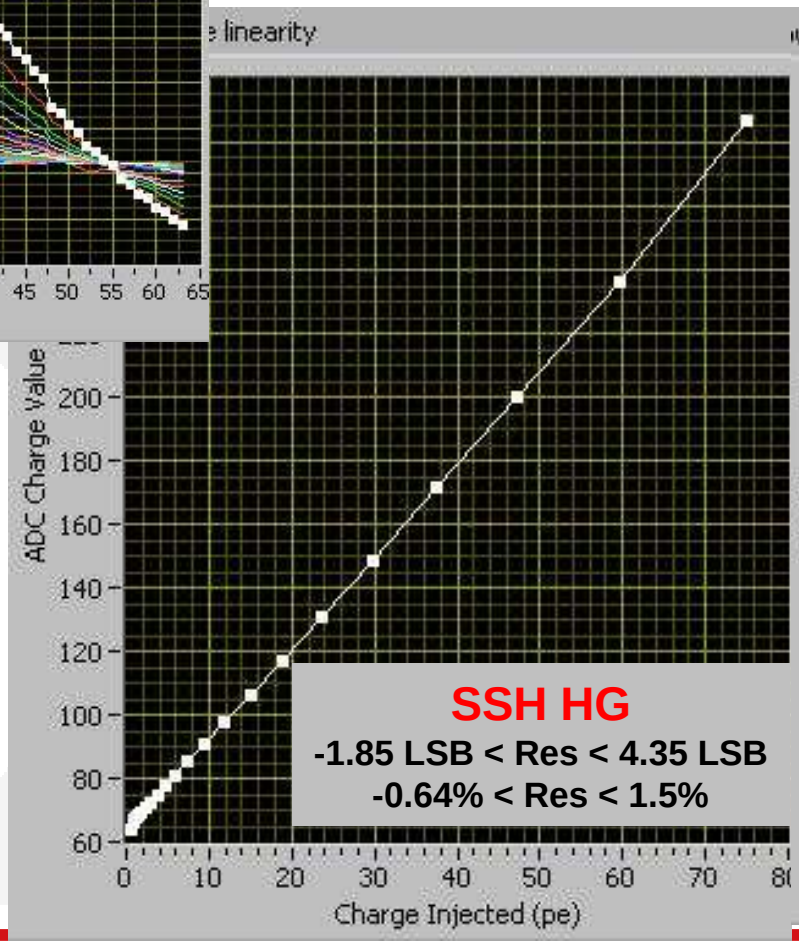
Part4: Charge linearity (full chain)

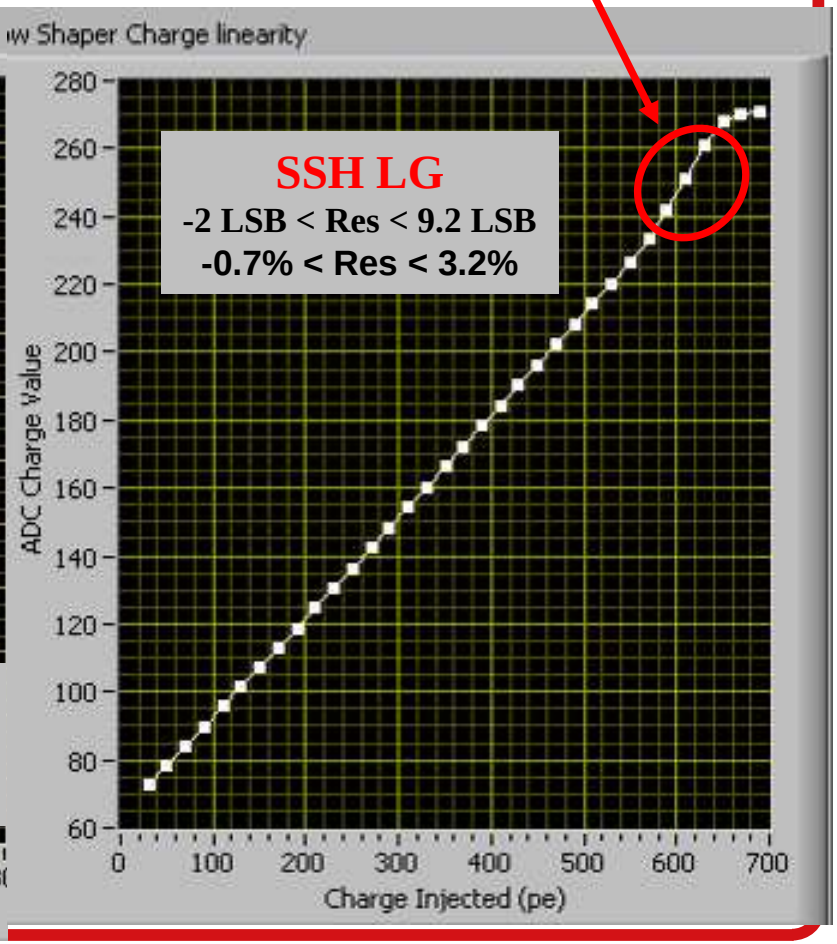


SSH waveform reconstructed with internal delay box

HG chain linearity is correct up to 10 pC (60 pe)
LG chain linearity is correct from 8 pC to 96 pC (600 pe)

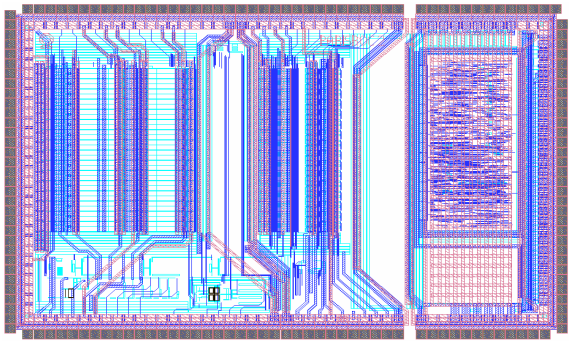
PA HG coupling SSH output for high input





Part5: Conclusion & future

- PARISROC2 up to now:
  - Auto-trigger + chn independent OK
  - No clock noise
  - No Trigger coupling
  - Noise OK to see signal 1/3pe (50fC)
  - Digital part speed up OK
  - New TDC integrated (see S. DROUET Talk)



- PARISROC is evaluated by other experiments:
  - DUSEL (large water cerenkov)
  - LENA (liquid scintillator)
  - IHEP Beijing

- PARISROC for the future:
  - Improve rate capability
  - Need move to pipeline ADC and multiple data lines

	PARISROC	Hit Rate (KHz)
Wilki – Present chips	V1	5.4
	V2	21.4
	2V1 (80 MHz)	42.7
	2V2 (80 MHz + 8 SL)	83.1
10-bit Pipeline 40MSPS	3V1 (40MHz + 8 SL)	216.2
	3V2 (80MHz + 8 SL)	432.4