

# Silicium Tracking (ILC)

## Blocs de test en IBM 130 nm

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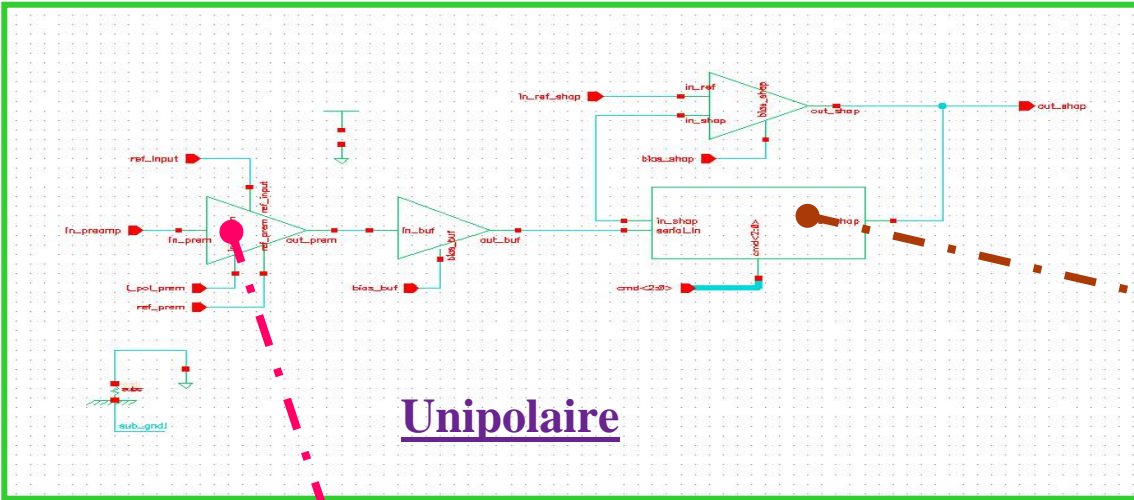
# SITR\_BLOCS



- ❑ Design intermédiaire avant celui d'un circuit multivoies
- ❑ Circuit dédié à la lecture des micro-pistes en silicium ( ILC )
- ❑ CMOS IBM 130 nm ( 1.5 V )
- ❑ 3 amplif-ier-shaper différents ( CR-RC programmable; 3 bit)
- ❑ ADC Wilkinson simple rampe ( 8 bits )
- ❑ Une cellule mémoire avec ses switchs d'écriture et de lecture.
- ❑ Run en cours via le CERN

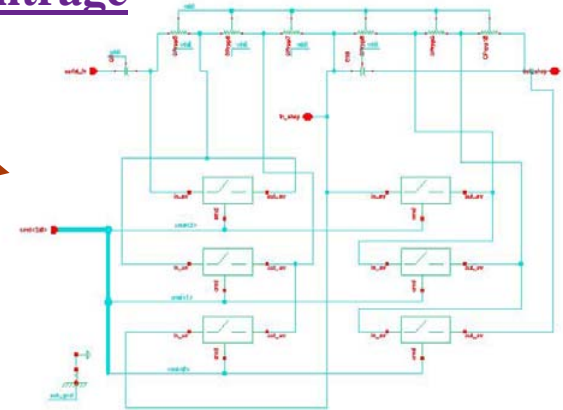


# Amplifier - Shaper V1

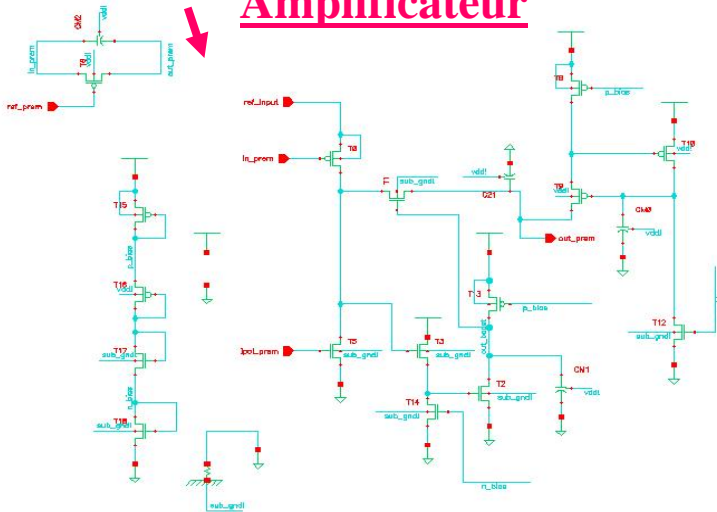


Unipolaire

## Filtrage



## Amplificateur



Gain : 19.4 mV/MIP

Sh\_Time: 600ns – 1us

Bruit @ 1 us : ~ 346 + 19,5 e/pF

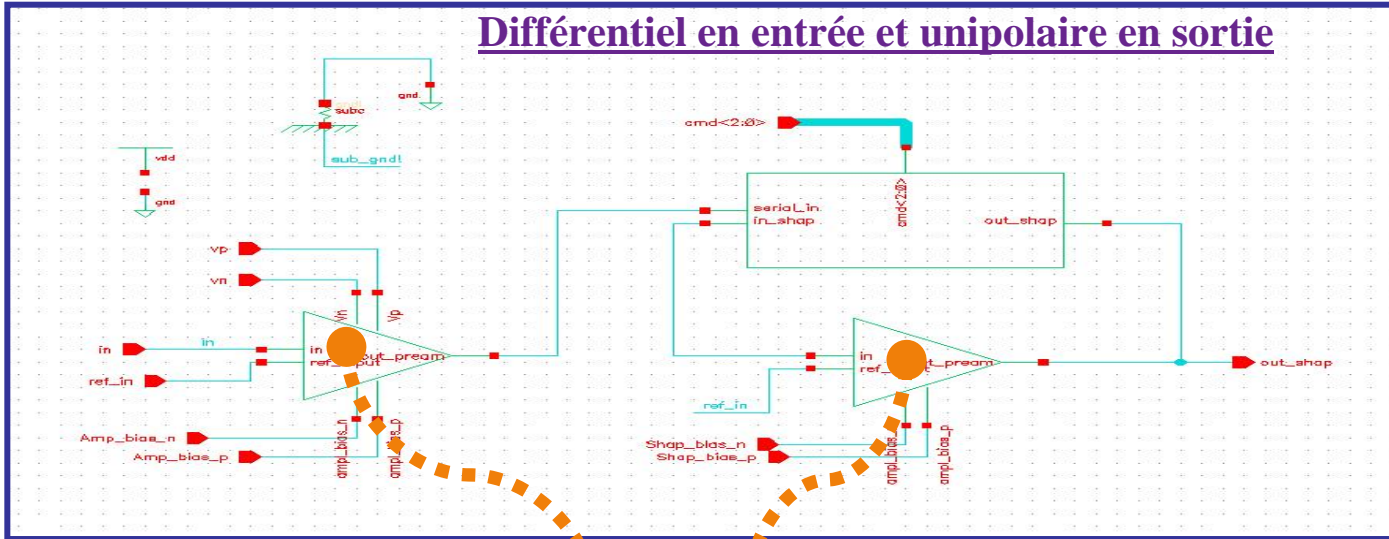
Linéarité < 1% ( 15 MIP )

Consommation : 450 uW

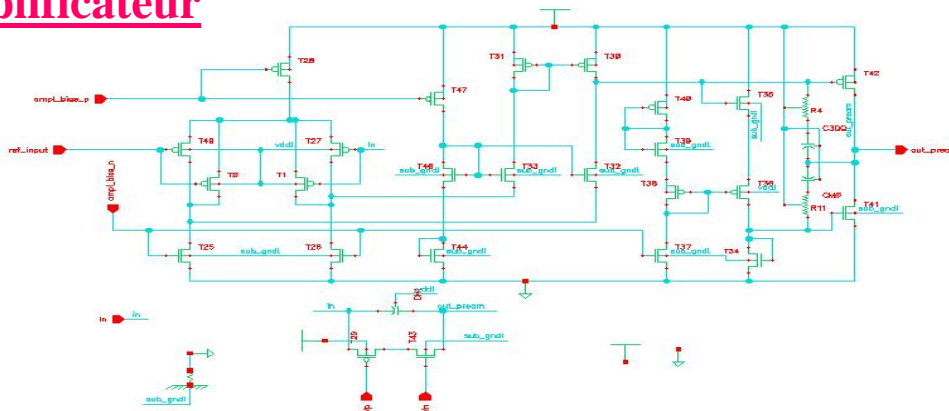
# Amplifier - Shaper V2



## Différentiel en entrée et unipolaire en sortie



## Amplificateur



Gain : 20 mV/MIP

Sh\_Time: 550ns – 1us

Bruit @ 1 us : ~ 189 + 18,9 e/pF

Linéarité < 1% ( 15 MIP )

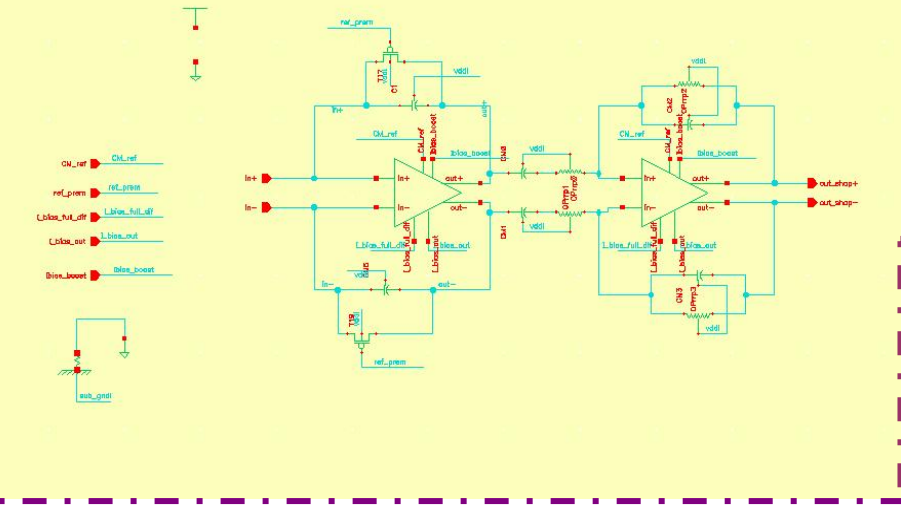
Consommation : 334 uW





# Amplifier - Shaper V3

## Différentiel



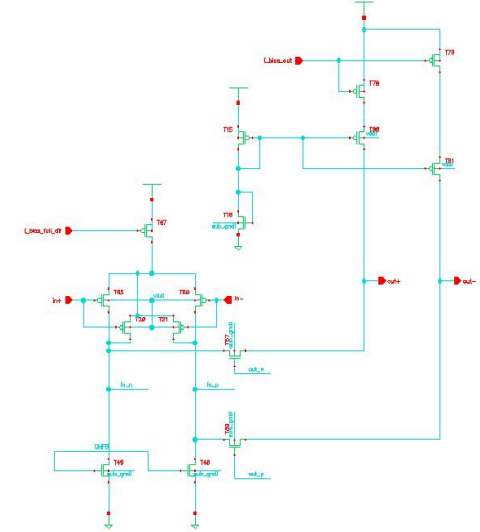
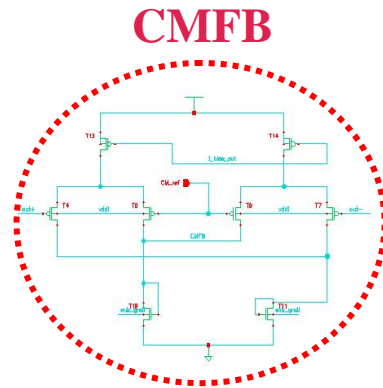
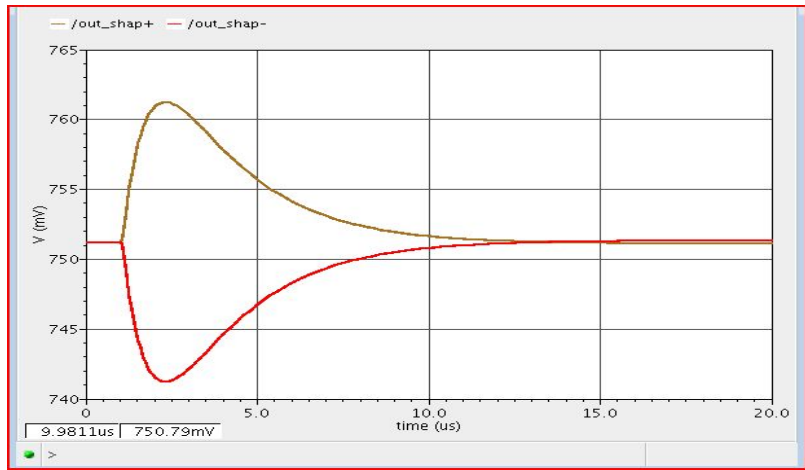
Gain : 20 mV/MIP

Sh\_Time: 700 ns – 1 us

Bruit @ 1 us : ~ 698 + 17.7 e/pF

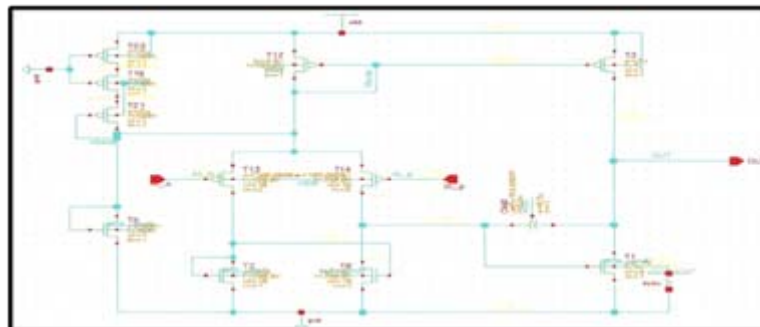
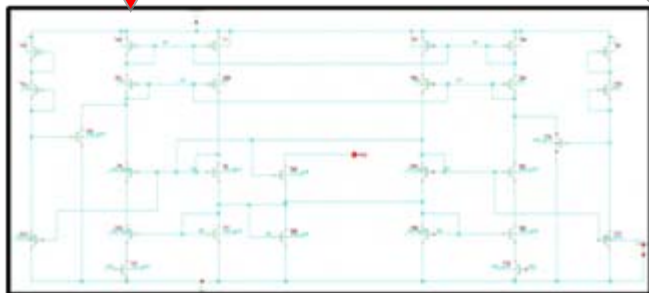
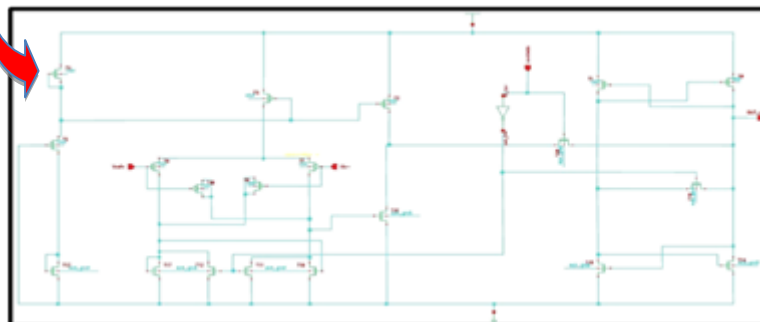
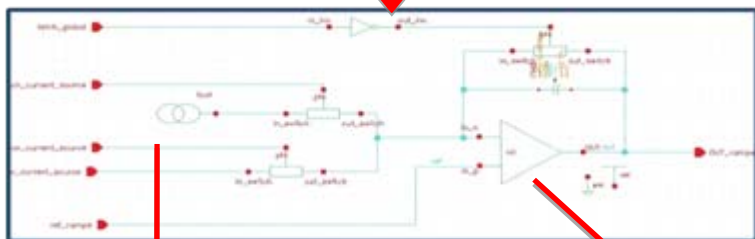
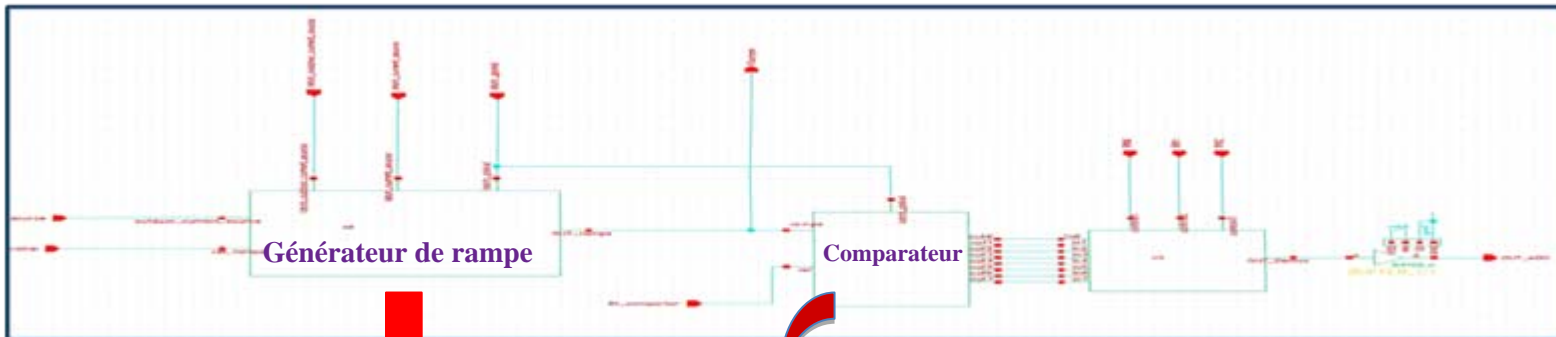
Linéarité < 1% ( 15 MIP)

Consommation : 540 uW



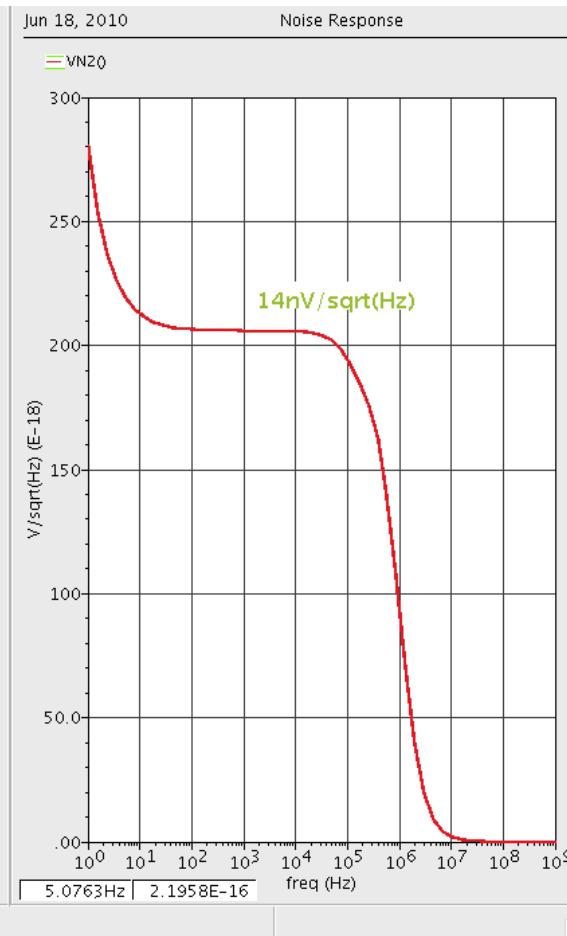
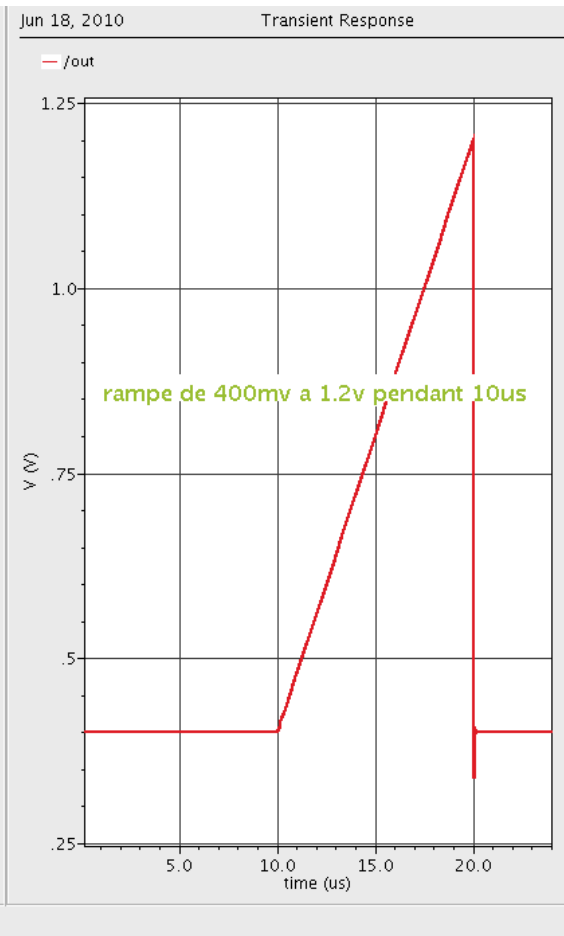
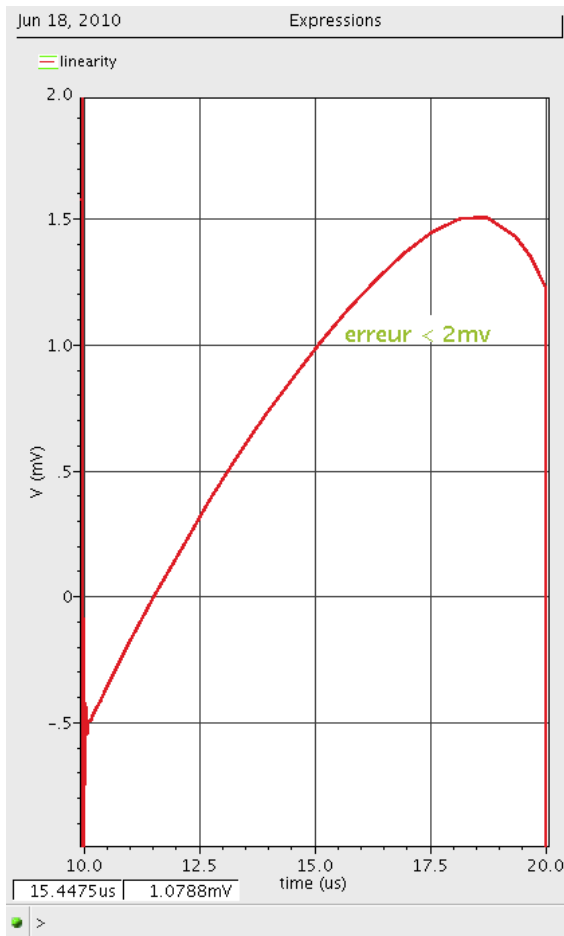
Gain\_boost

# ADC

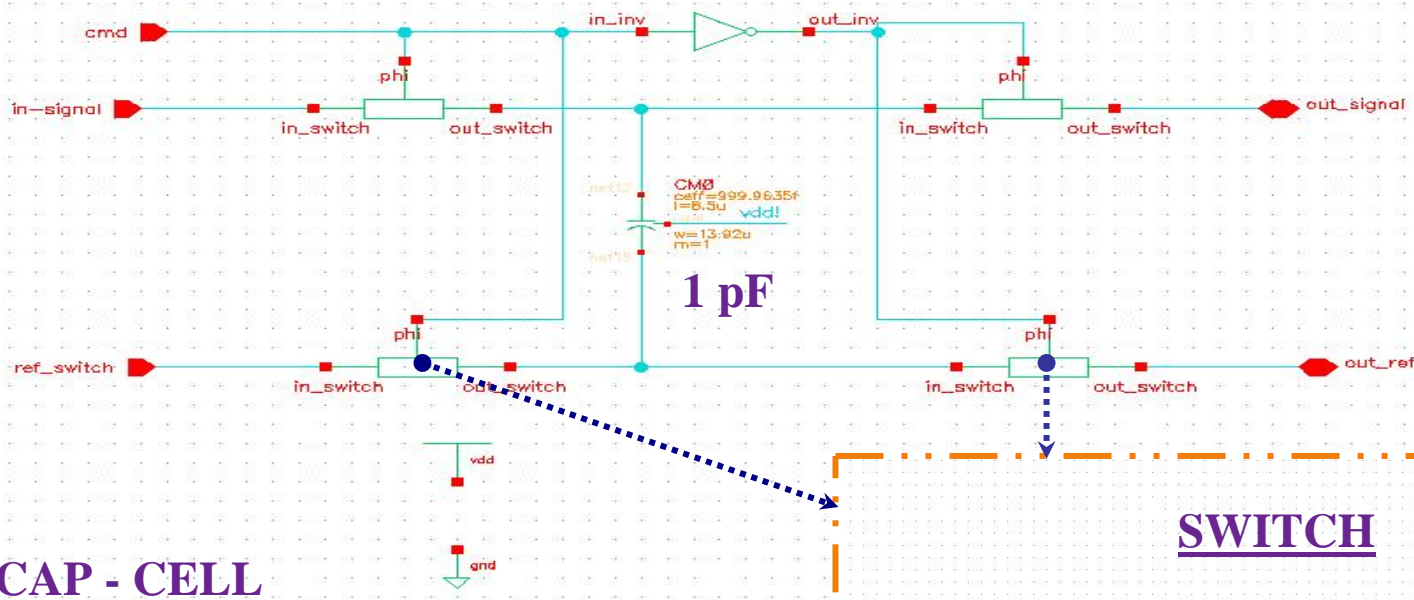




# Simulations - ADC

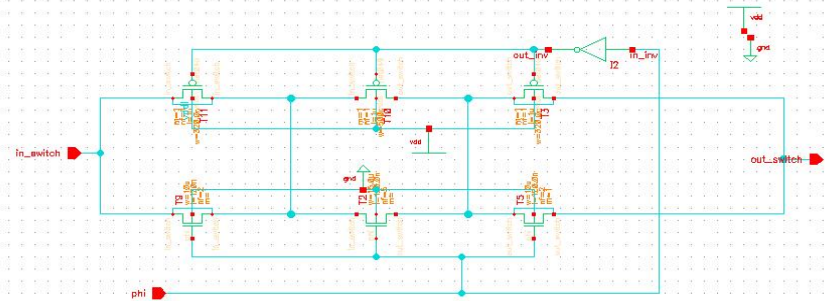


# La cellule mémoire



CAP - CELL

## SWITCH

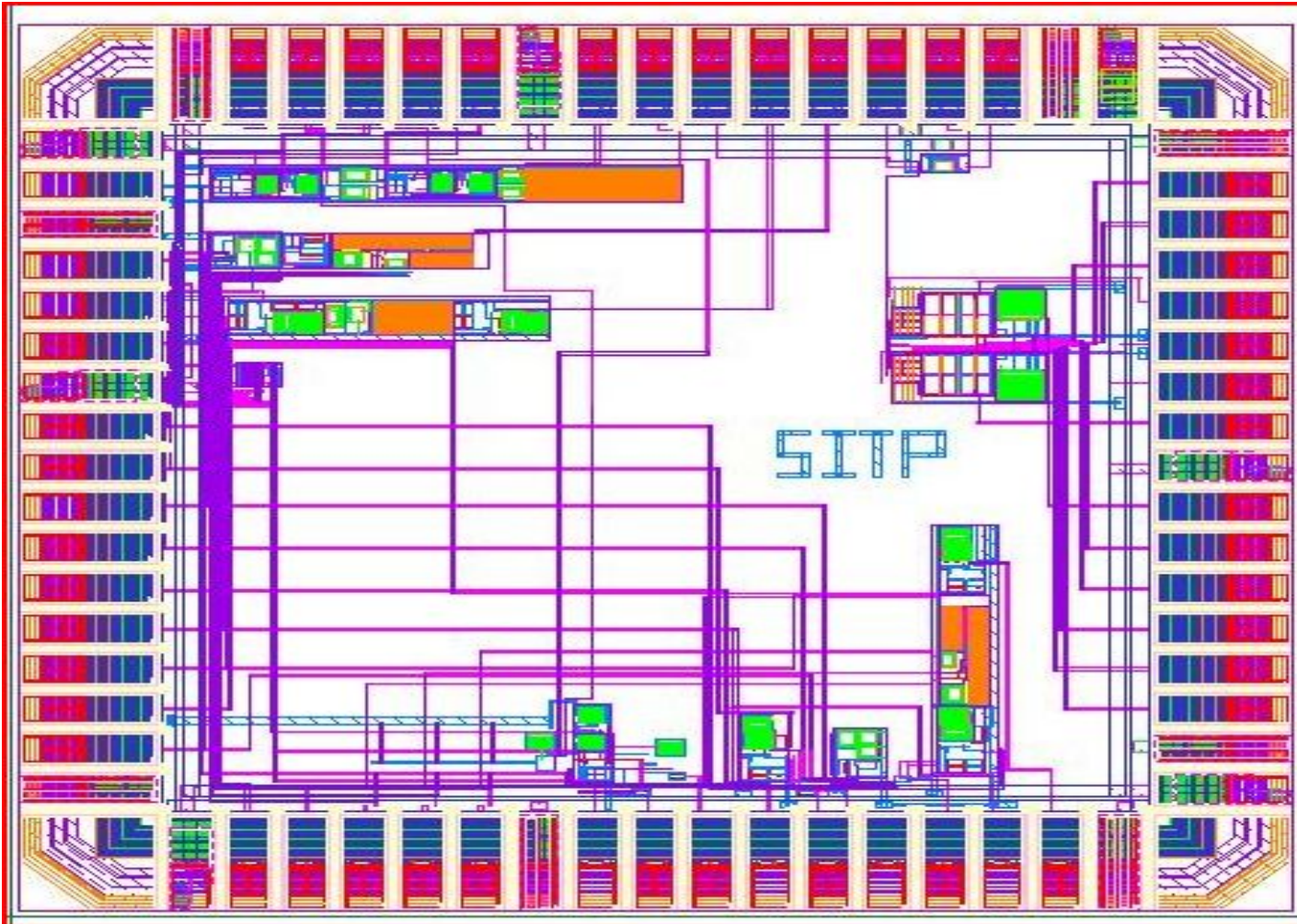




# Layout

2 X 2 mm<sup>2</sup>

68 Pads





**Fin**

**Merci pour votre attention**

**Merci à :**

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