ASIC FEAFS

- A front end chip for SLHC CMS strip module -

Hervé CHANAL

Yannick ZOCCARATO

(CNRS IN2P3 MICHRAU)

Outline

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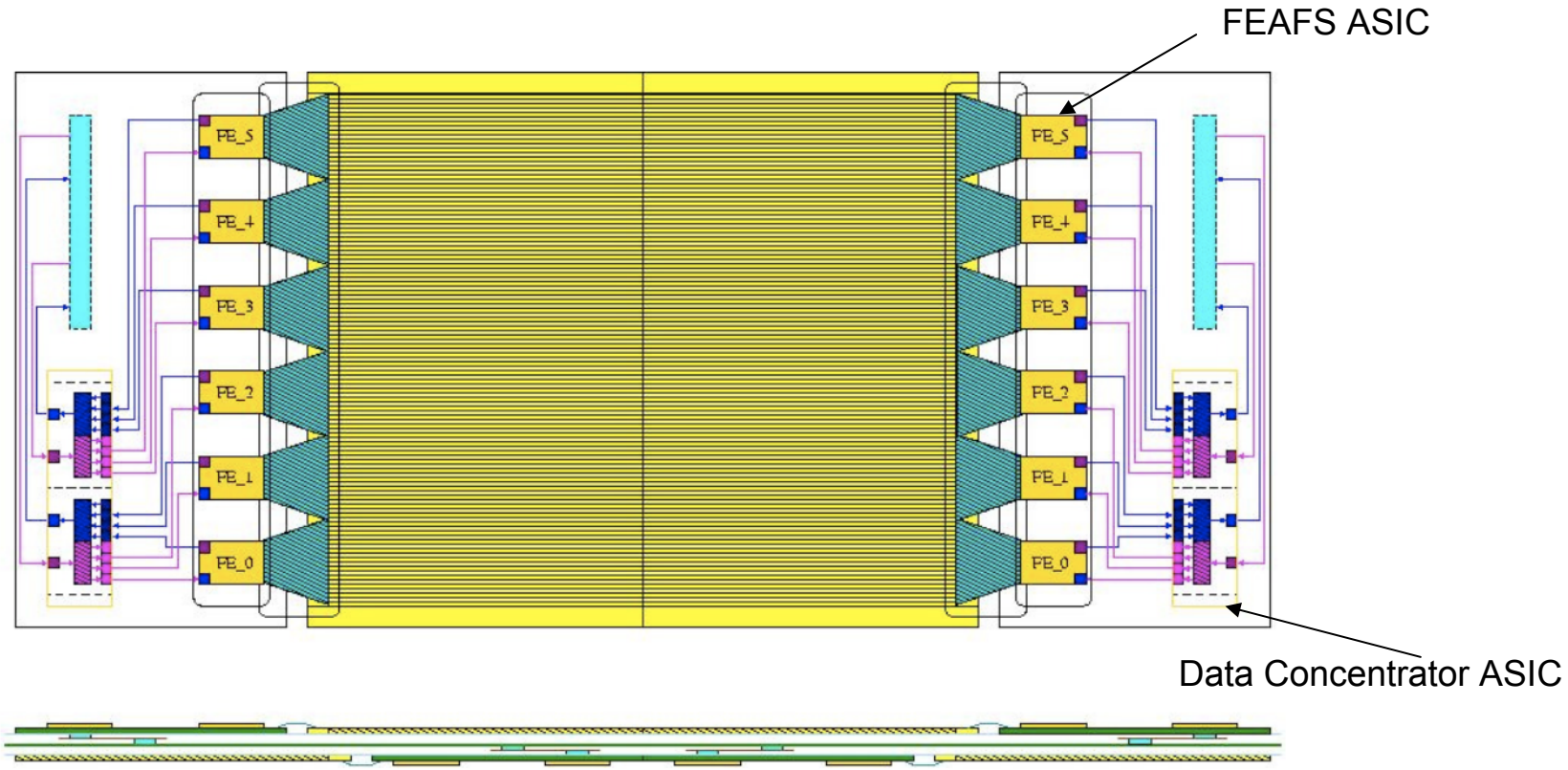
Electronic design for a SLHC CMS strip module :



Design needs for FEAFS

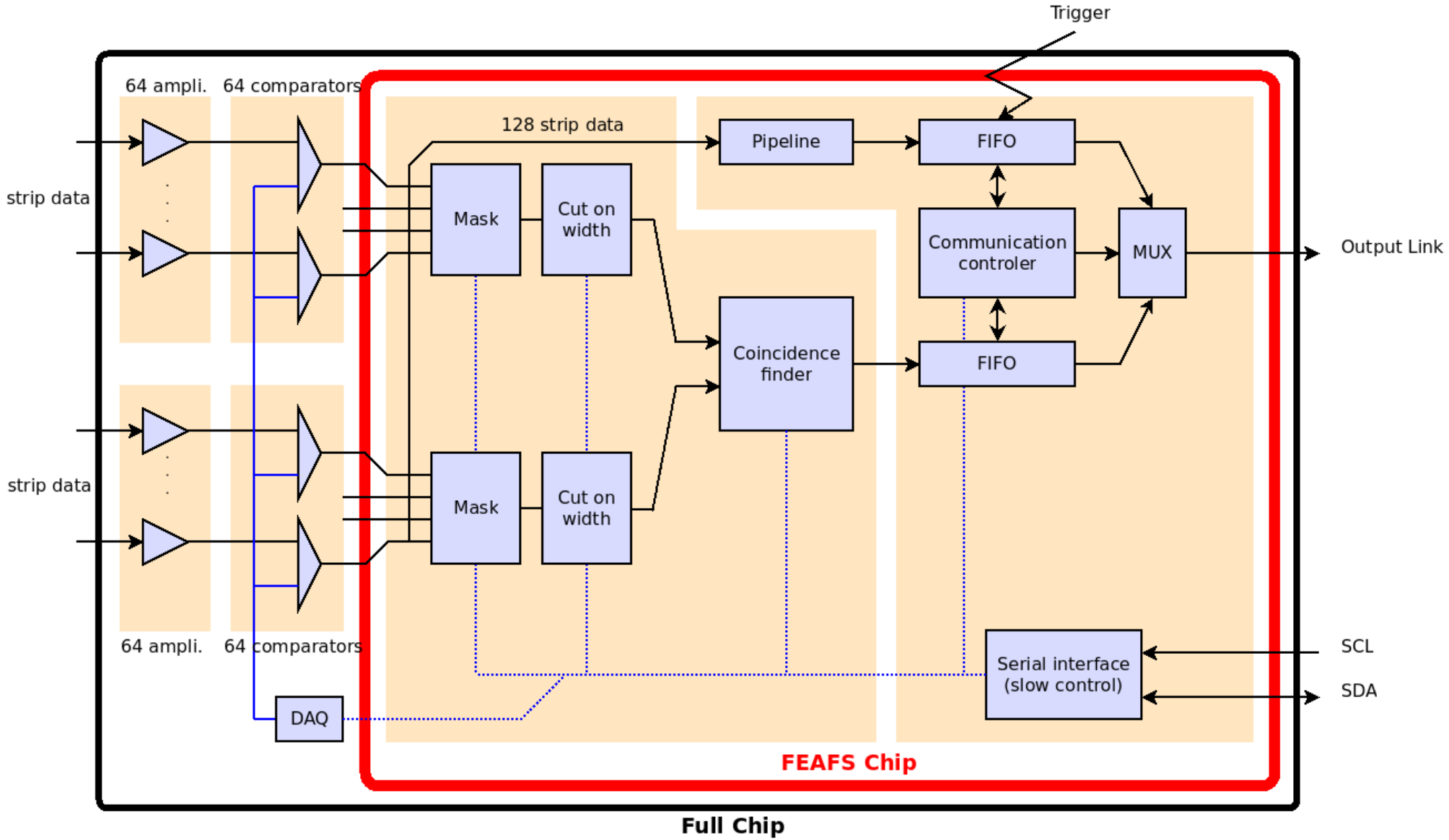
- Find clusters on a set of 128 strips,
- Send two different flows of data to the ASIC concentrator:
  - read out data:
    - average rate : 100 kHz (100kHz * 128b = 12.8 Mbps)
  - cluster data for trigger:
    - average number of clusters (size<3) : 0.25 at 20MHz
    - Foreseen data packet:

      2 bits (No. Clusters) + [5 bits (add) + 2 bits (width) + 3 bits (time stamp)] = 12 bits for 1 cluster

    → average rate: 12b * 0.25 * 20MHz = 60 Mbps

→ Average bandwidth of the link: 60 + 12.8 = 72.8 Mbps.

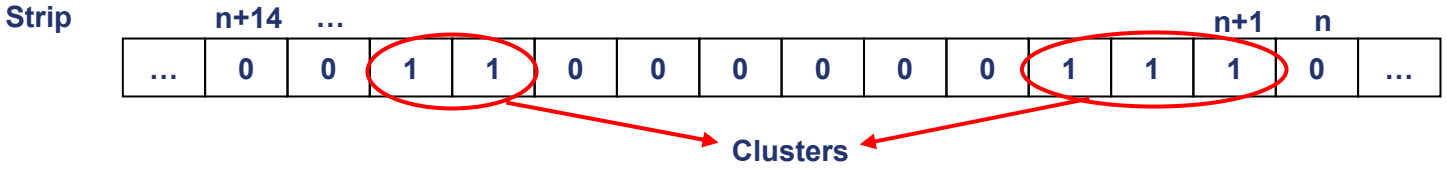
FEAFS architecture



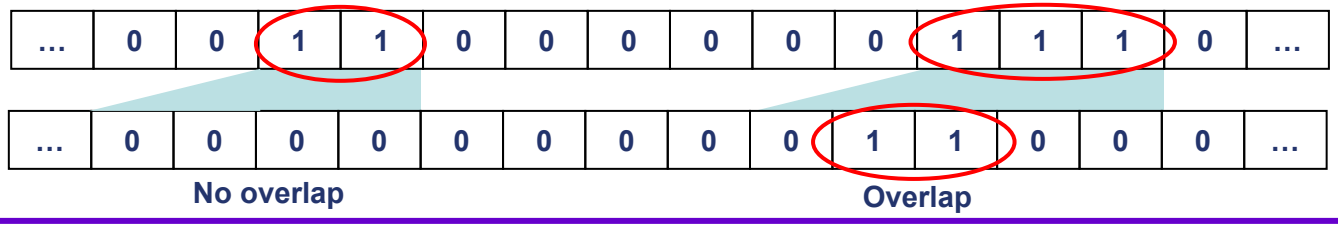
Part I:
Finding the clusters

Cluster Finding : Principle

- Find all the clusters of triggered strip in two set of 64 strips

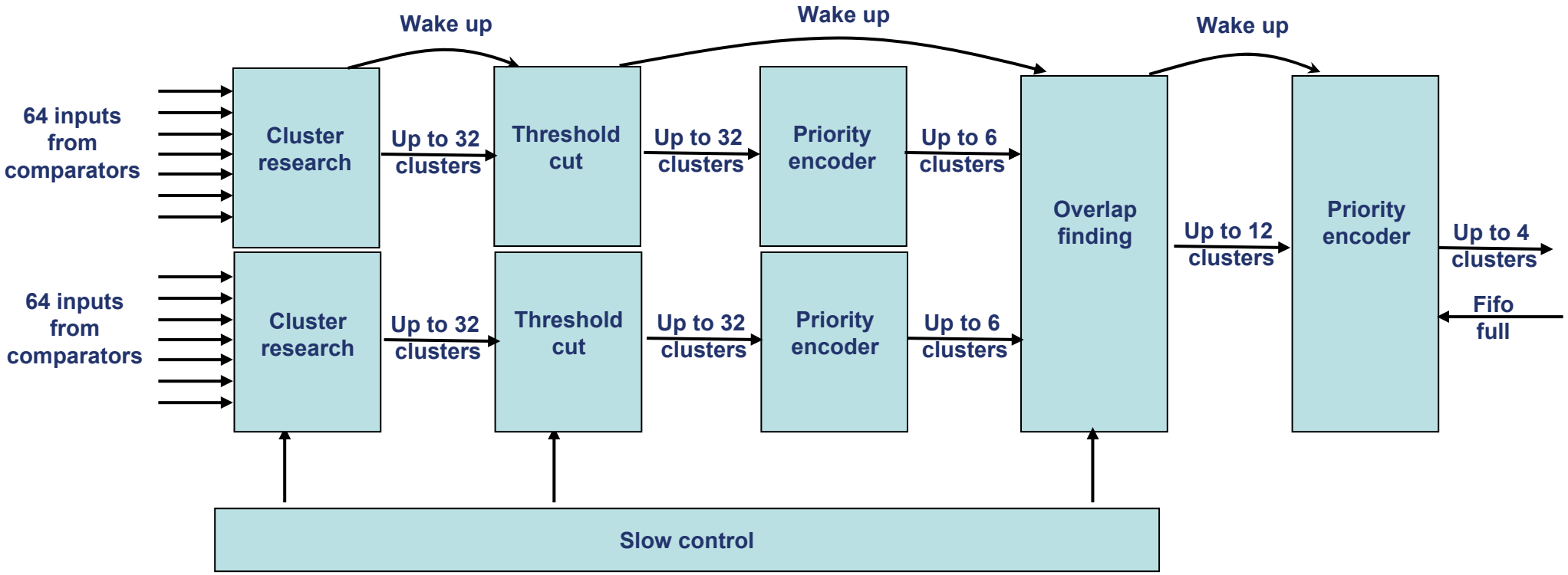


- Compute their address (degraded to 5 bits) and the number of adjacent triggered strips
- Report only these with a size bellow a programmable threshold
- Find clusters overlapping in the two layer in programmable window with an offset



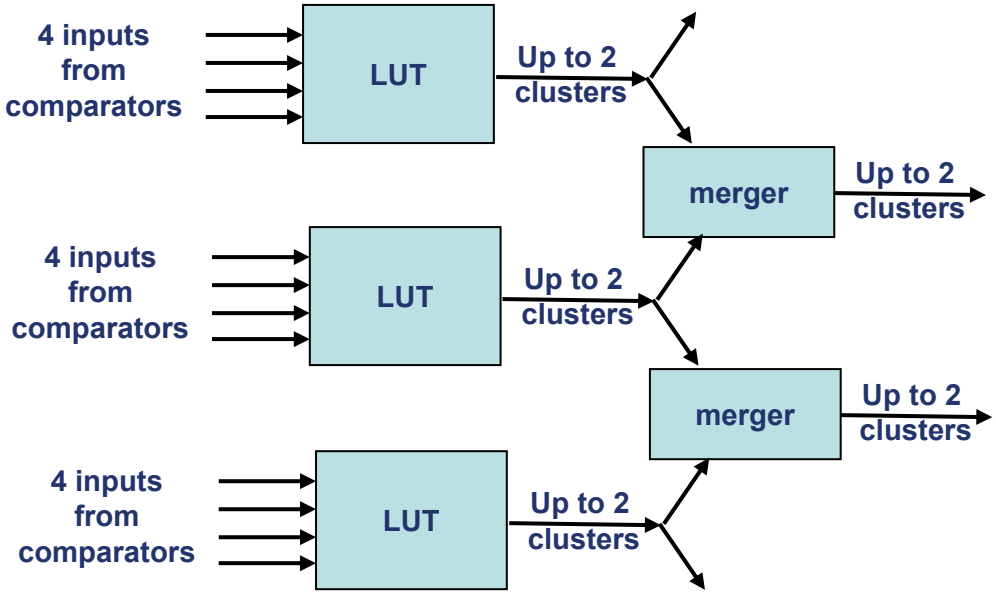
Cluster Finding : Architecture

- Two flows up to the overlap finding
- The bus size is reduced at each step by priority encoders
- Wake up on the internal registers to reduce the consumption



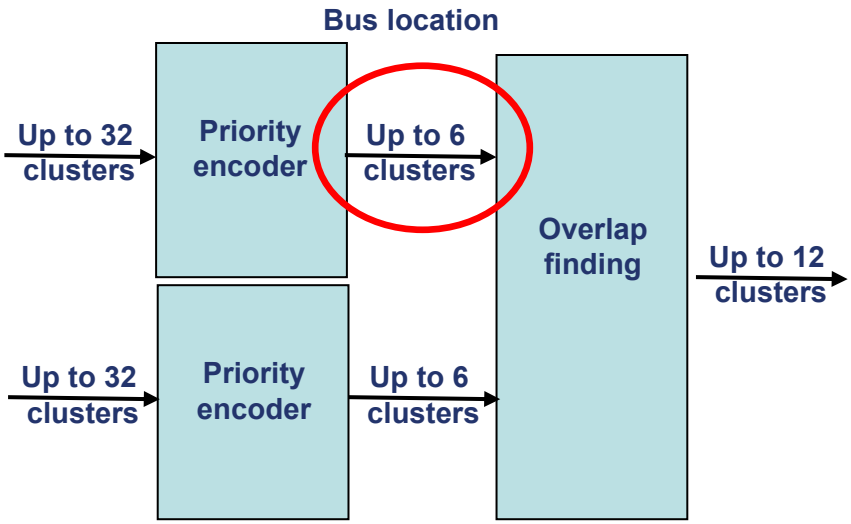
Cluster Finding : Algorithm

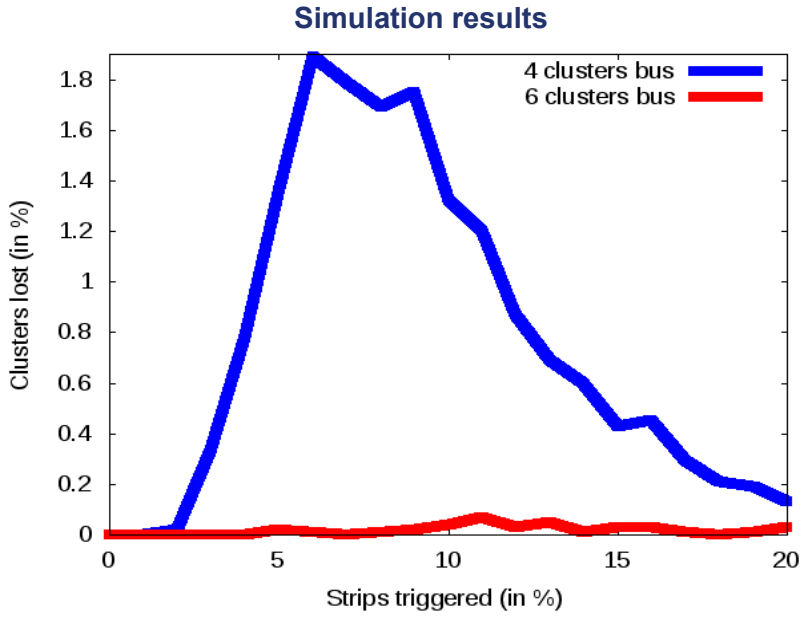
- 2x64 strips ⇒ 2x16 blocks of 4 strips
  - Same granularity as the degraded address (5 bits ⇒ 128 blocks)
  - Need for boundary block to merge clusters
- 32 LUT of 16x16 bits used to find clusters in each block (up to 2 clusters/block)
- Address of a cluster =
  - Address of its block
  - Arbiter when a cluster cross a boundary
- Only 1 clock cycle



Cluster Finding : Bus Size

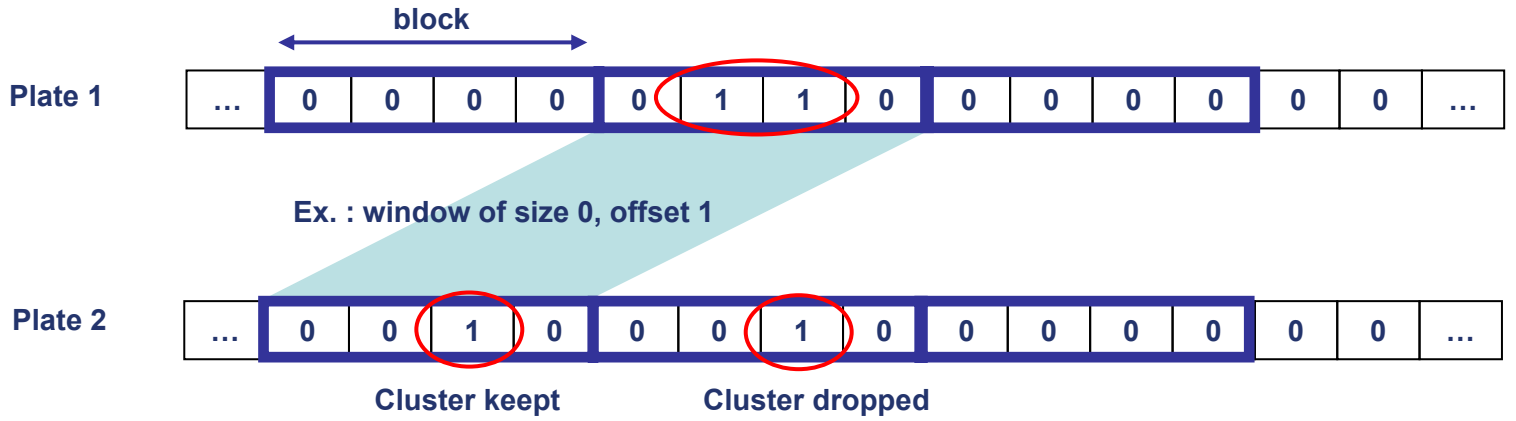
- The first priority encoder can remove clusters which could have been kept in the overlap finding and in the 4 cluster output bus
  - A dedicated test bench with random inputs
  - Simulation of the input load (number strips triggered)
- Simulations shows no loss with 6 clusters/bus with 1% strip occupency





Cluster Finding : Windowing

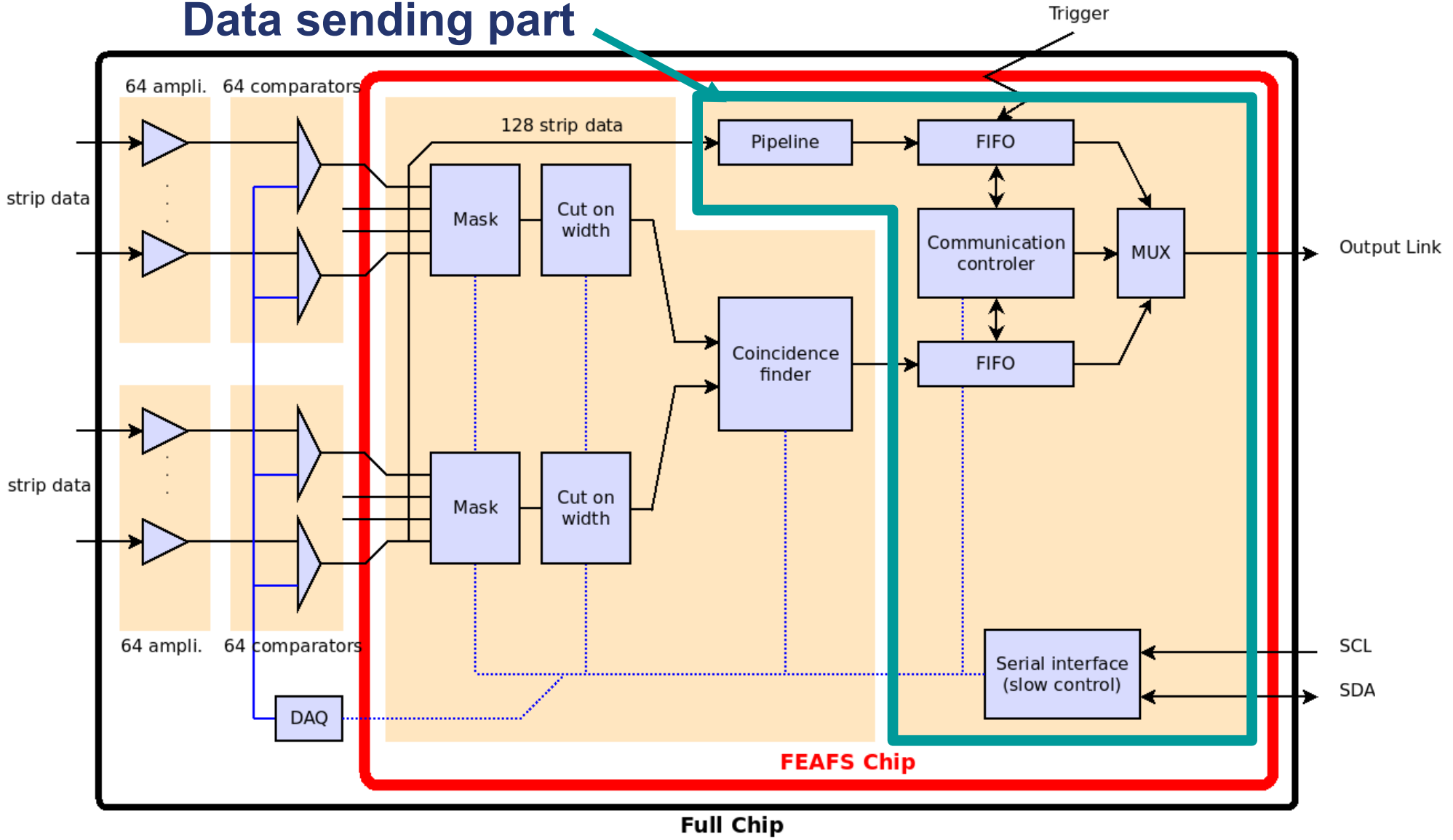
- Comparison of the degraded address (on 4 bits) between the retreived 6 clusters from the two set
- Offset to handle possible position difference between the two layers
- Keep clusters if for a cluster with an address a1 from layer 1, another cluster from layer 2 with an address a2 verify abs(a1+offset-a2)≤threshold.



Part II:
Sending the data

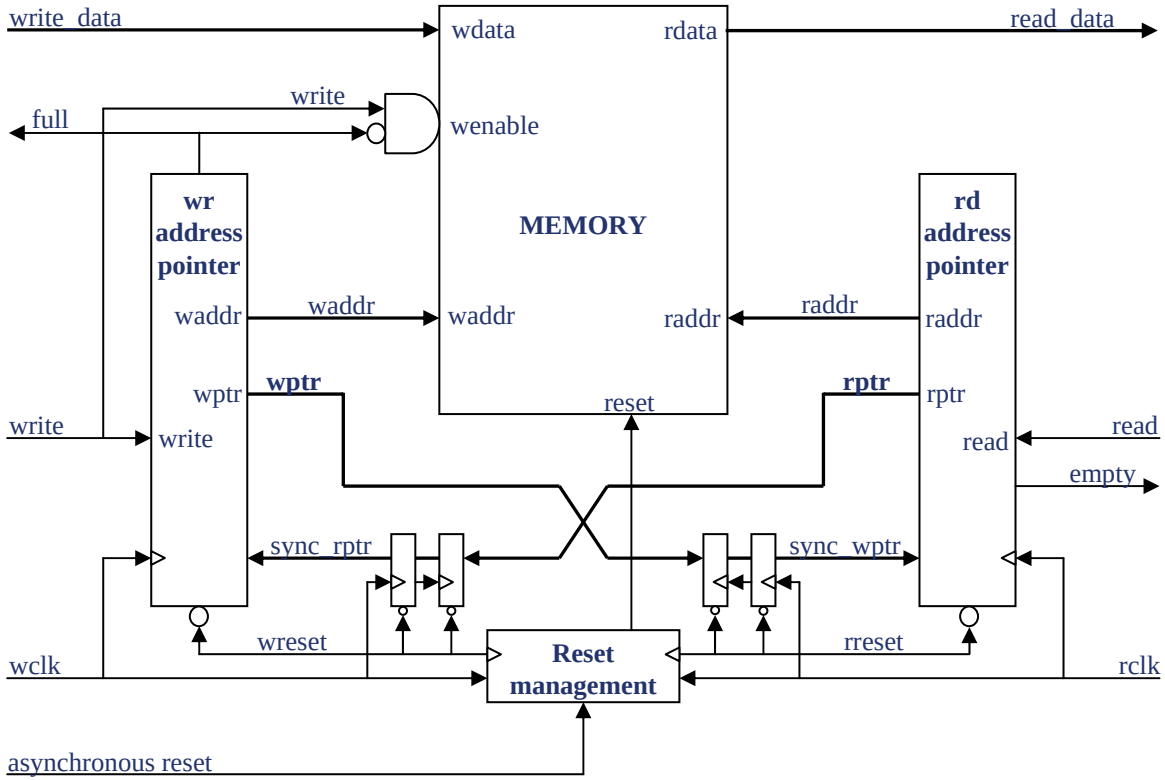
FEAFS architecture

Data sending part



FIFO

- 2 FIFO of 16 words depth for clusters and readout data
- Used to safely pass from LHC clock domain (40MHz) to output link clock domain (up to 100MHz).



Clusters: Output Frame

Chip output: 4 bit bus

Cluster Frame:

From 3 to 8 words of 4 bits, depending on the number of clusters.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id		Nb cl		Cluster 1							Cluster 2							Cluster 3							Cluster 4						
0	1	0	0	Add 1					Size 1																						
0	1	0	1	Add 1					Size 1			Add 2				Size 2															
0	1	1	0	Add 1					Size 1			Add 2				Size 2		Add 3					Size 3								
0	1	1	1	Add 1					Size 1			Add 2				Size 2		Add 3					Size 3		Add 4					Size 4	
Word 1				Word 2				Word 3			Word 4					Word 5		Word 6					Word 7				Word 8				

Readout :Output Frame

The 128 strips are split in 8 words of 20 bits.

4 MSB as Id and word count number.

Trigger frames can be inserted between two readout frame.

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	word			N° Strip															
1	0	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Word 1				Word 2				Word 3				Word 4				Word 5			

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	word			N° Strip															
1	0	0	1	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Word 1				Word 2				Word 3				Word 4				Word 5			

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	word			N° Strip															
1	1	1	1	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128
Word 1				Word 2				Word 3				Word 4				Word 5			

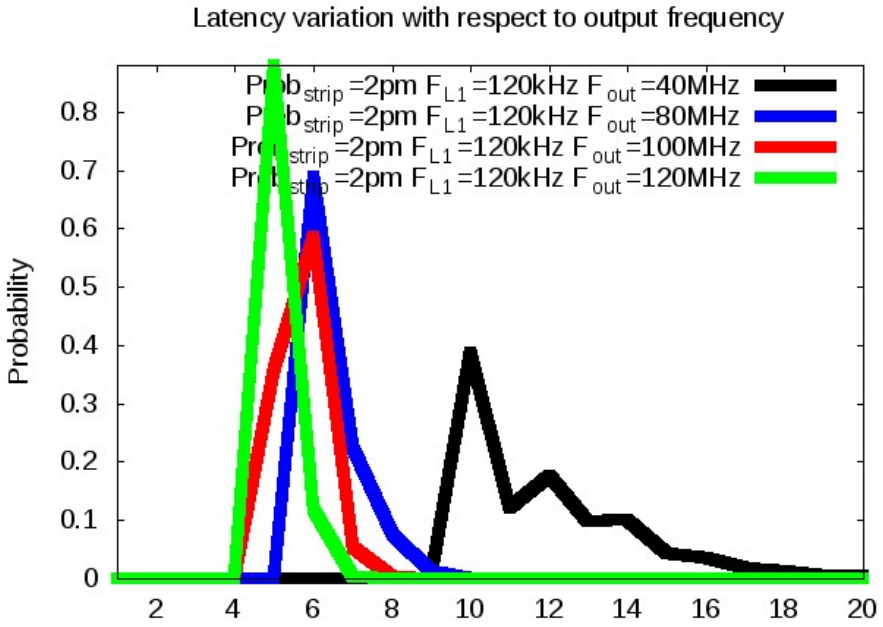
Communication controller

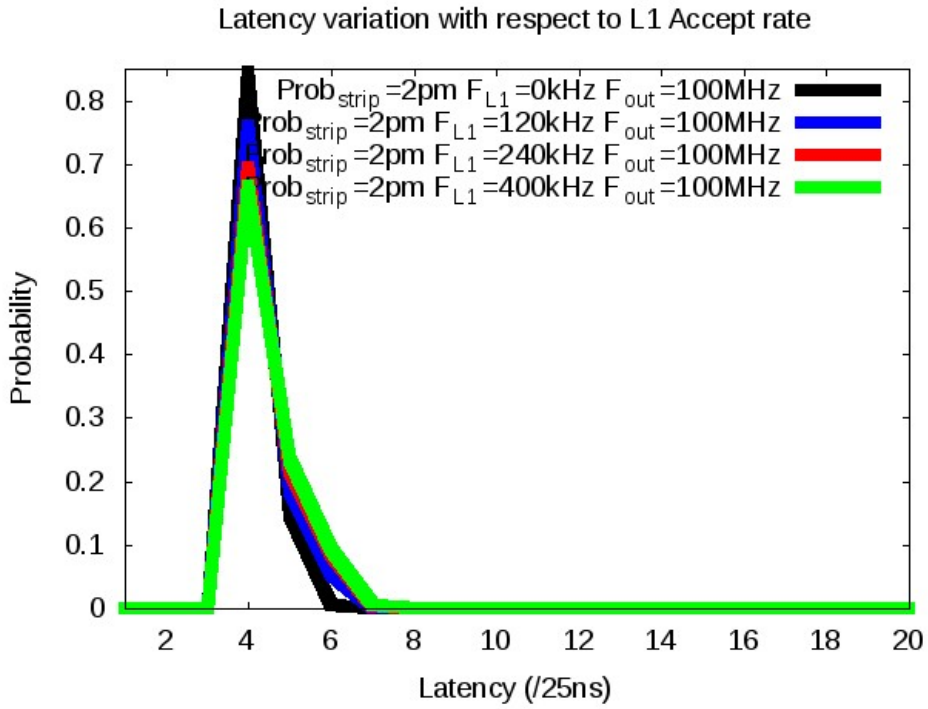
Performs the output bus arbitration with 4 running modes as a function of the FIFO states.

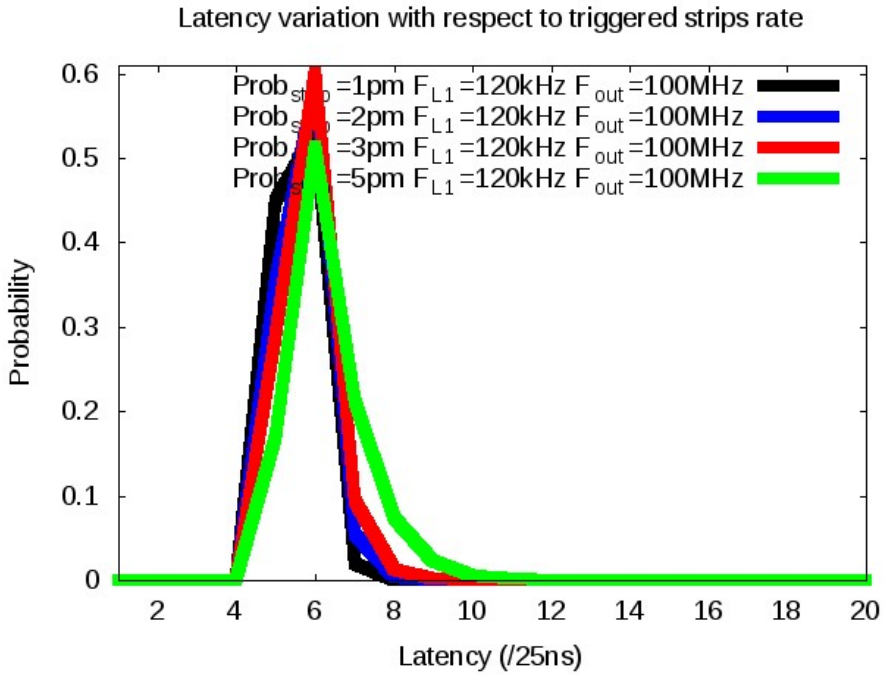
Communication Mode	Priority 1	Priority 2	Special
Normal	Trigger Data	Readout Data	
Derated (Trigger FIFO full)	Trigger Data	Ignored	Signal « trigger off » activated
Busy (Readout FIFO full)	Readout Data	Ignored	Signal « Busy » activated
Survival (Readout and trigger FIFO full)	Trigger Data	Readout Data	Signbal « trigger off » and « busy » activated

Latency

- Study the latency of the full chip with respect to the L1 rate, the triggered strip rate and the output stage







I2C

Monitoring and slow control through an I2C interface :

Slow control for:

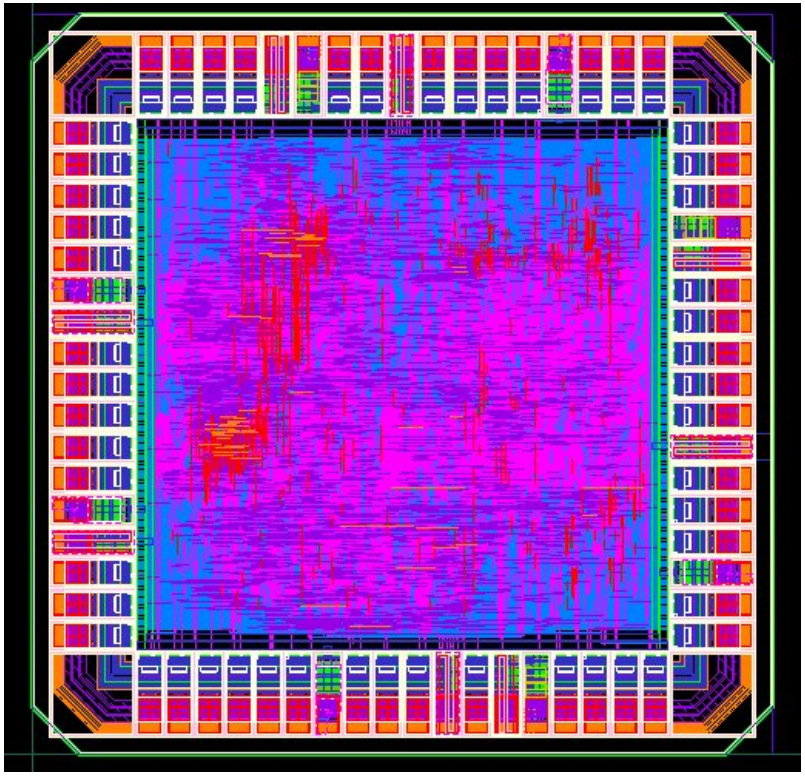
- Gain of preamplifier,
- Discriminator Threshold,
- Strip enable,
- Cluster threshold,
- Coincidence offset,
- Coincidence window,
- Readout and cluster Data for test,
- Configuration register.

Monitoring for :

- Counter of cluster loss,
- Counter of data trigger loss,
- Counter of data trigger loss.

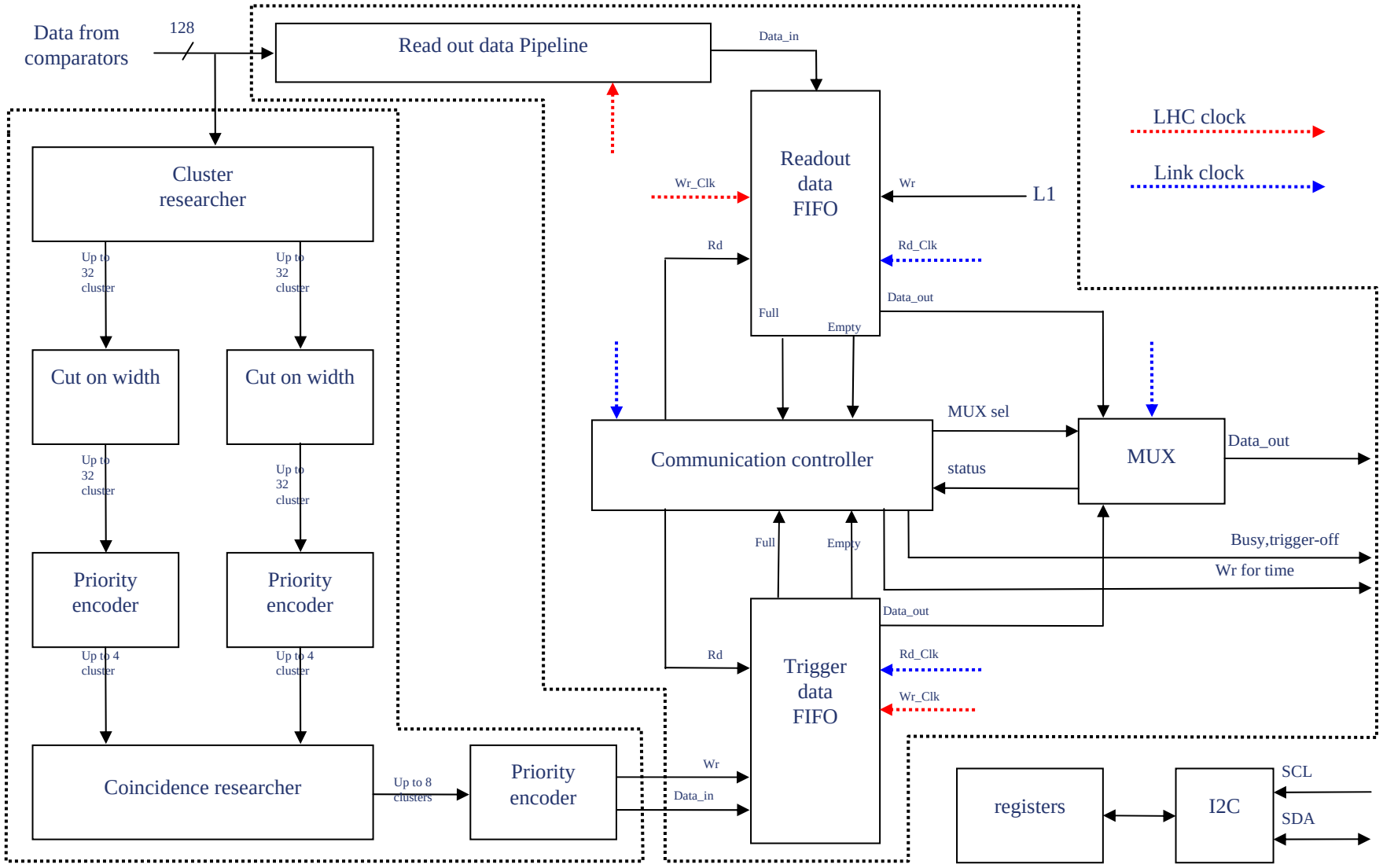
Conclusion

- First prototype develloped in 130nm from IBM with VCAD Standard cells
- Only 32 inputs : internal mutiplexer
- Size: 4mm²
- Sent 31th May to the foundry
- Estimated power (with 20% activity on inputs): 60mW



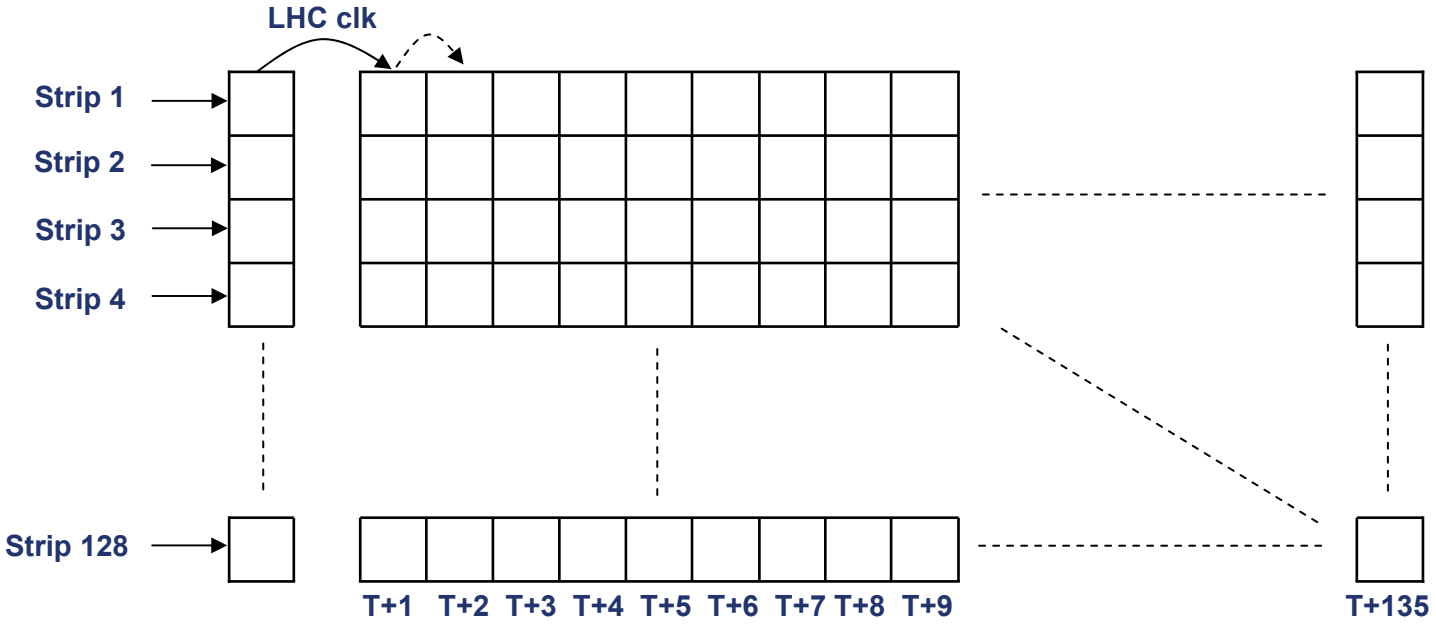
SPARES

SPARE : Numerical part details of FEAFS



Readout data pipeline

Store the readout data while the trigger is being processed.



When the trigger is coming the data is sent in FIFO