Expected feedback from 3D for SLHC

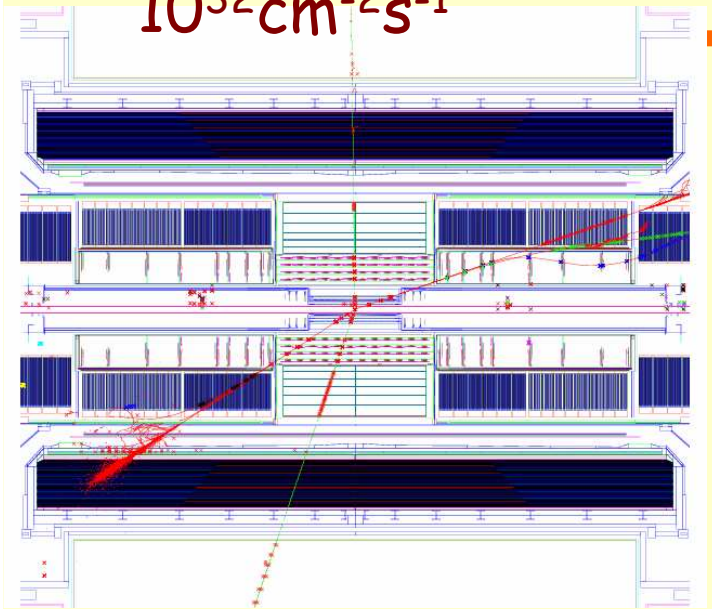
Introduction

- **LHC – 14 TeV pp collider at CERN start summer 2008**
- **Gradual increase of luminosity up to L = 10^{34} cm^{-2} s^{-1} in 2008-2011**
- **SLHC - major increase of luminosity up to L = 10^{35} cm^{-2} s^{-1} in 2016-2017**
- **How can 3D electronics technology help us to challenge the physics at LHC ?**

Expected feedback from 3D for SLHC

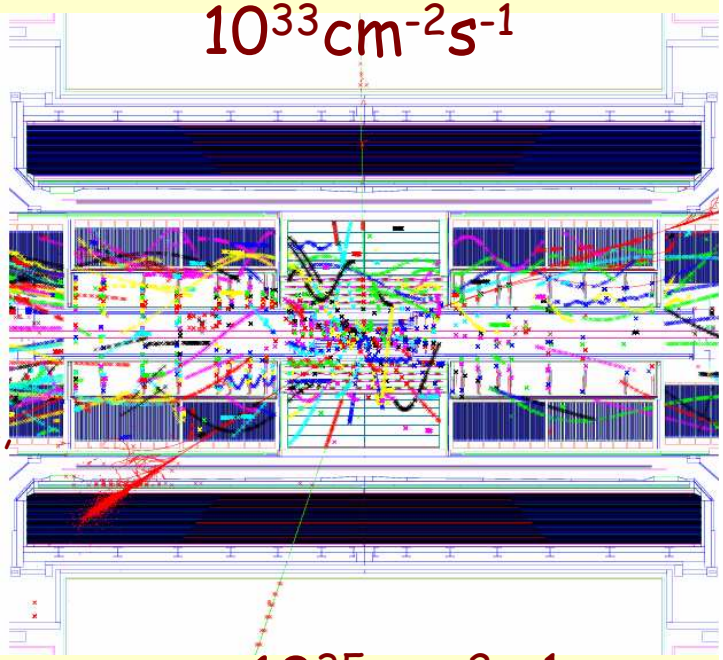
H→ZZ→μμee + minbias evts

$10^{32}cm^{-2}s^{-1}$



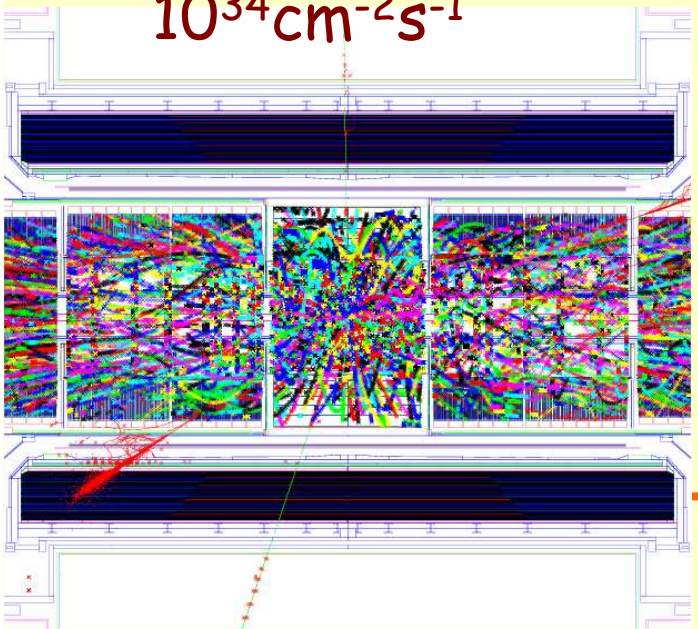
LHC/2008…

$10^{33}cm^{-2}s^{-1}$



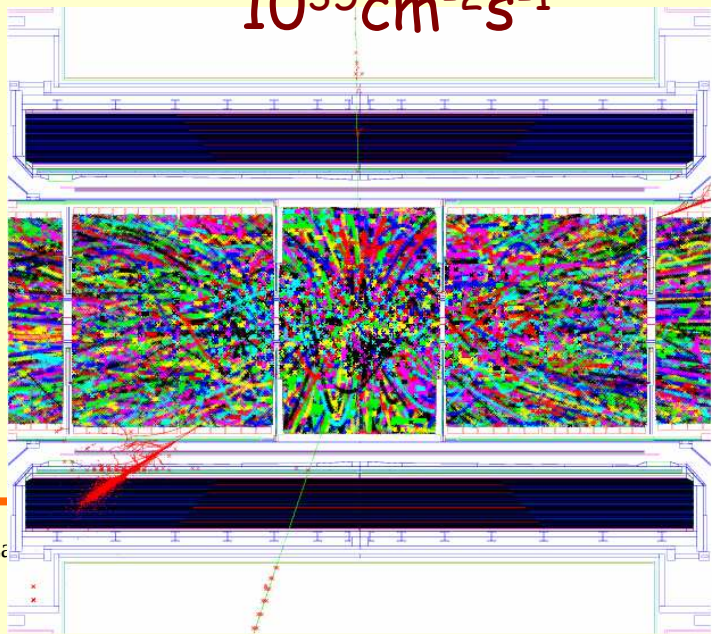
LHC basse luminosité, premières années

$10^{34}cm^{-2}s^{-1}$



LHC haute luminosité

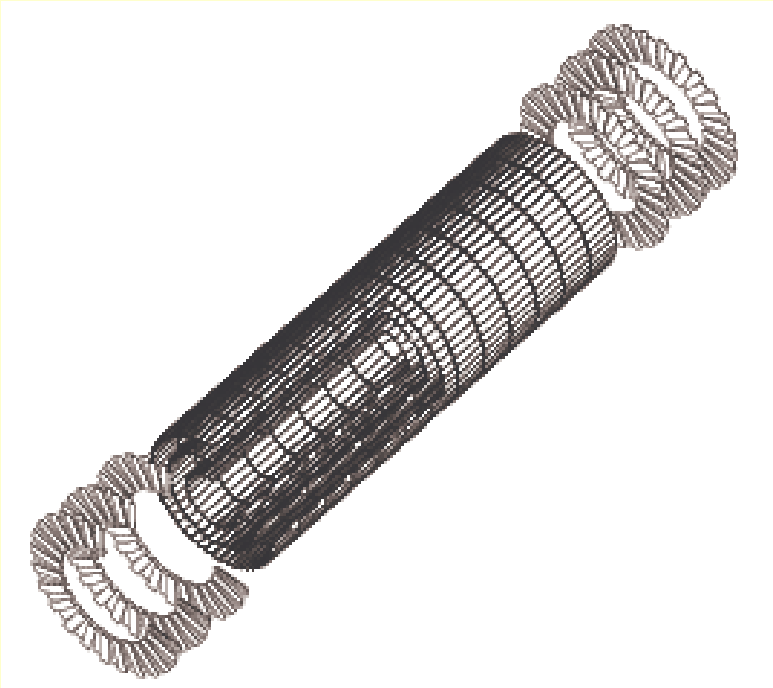
$10^{35}cm^{-2}s^{-1}$

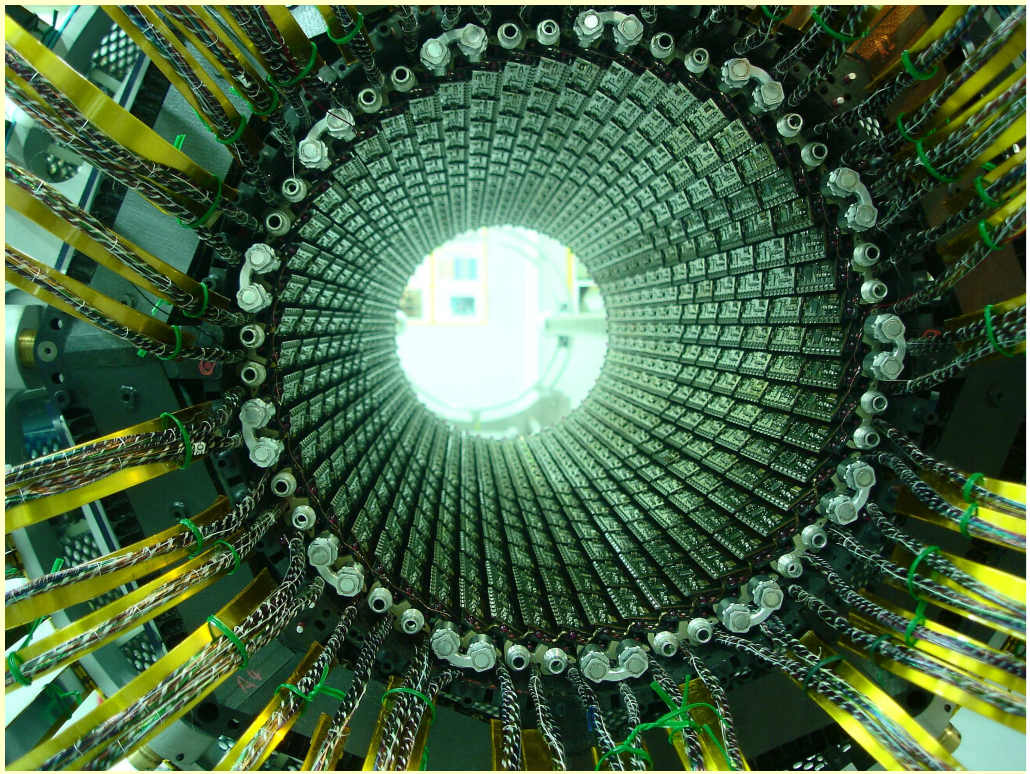


SLHC

Expected feedback from 3D for SLHC

Pixel Vertex Detector





- **ATLAS – 80 millions pixels 50x400 µm**
- **CMS - 66 millions pixels 100x150 µm**

Expected feedback from 3D for SLHC

Pileup

$\langle N_{vrt} \rangle$ - mean number of pileup vertices in ±150μm from primary vertex

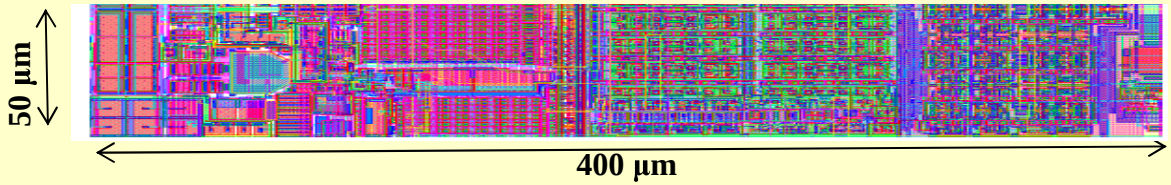
Z_{vertex} resolution for current ID is ≤50μm

	σ_{IR} = 5.6cm N_{int} = 23	σ_{IR} = 2.1cm N_{int} = 88	σ_{IR} = 2.1cm N_{int} = 176	σ_{IR} = 3.5cm N_{int} = 510
$\langle N_{vrt} \rangle$ at Z=0mm	0.05	0.49	0.99	1.71
Z=20mm	0.05	0.31	0.63	1.48

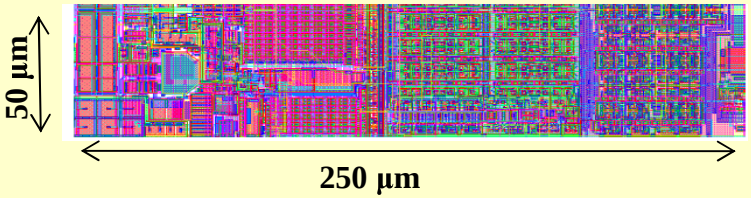
- **LHC L = 10^{34} cm^{-2} s^{-1} pixel occupancy 0.4 10^{-3}**
- **SLHC L = 10^{35} cm^{-2} s^{-1} with 50 ns bunch pixel occupancy 6.0 10^{-3}**
- **Wrong selection of primary vertex, admixture of pileup into jets**
- **Standard pile-up decrease b-tagging performance by ~20%**
- **Decrease of the pixel pitch size from 400 μm to 200 μm compensate b-tagging by ~20%**

Expected feedback from 3D for SLHC

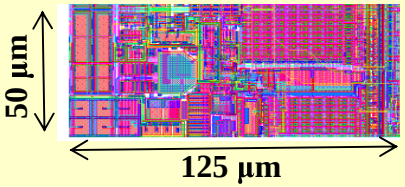
ATLAS Pixel Front End size

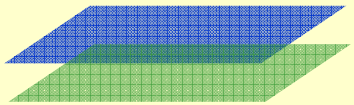


FE-I3 CMOS 250 nm

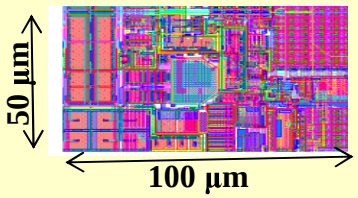


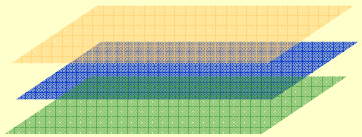
FE-I4 CMOS 130 nm





FE-I4-3D-2 CMOS 130 nm 2 layers

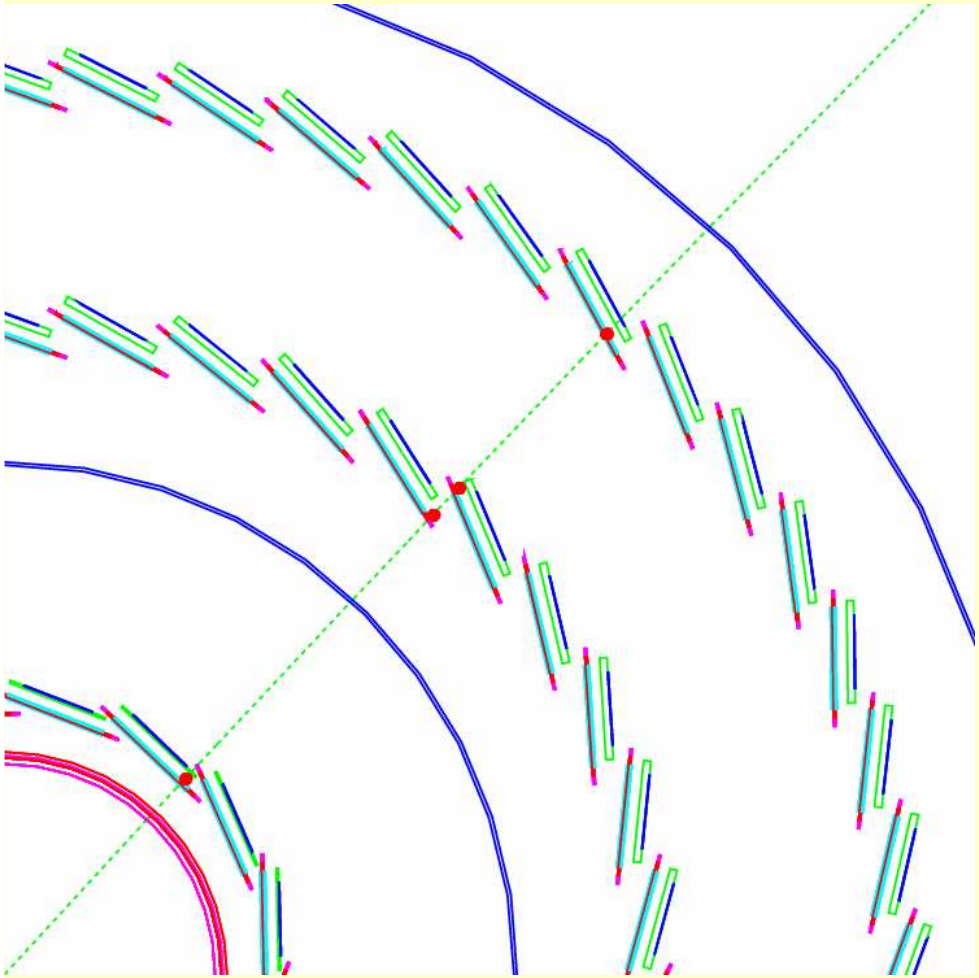




FE-I4-3D-3 CMOS 130 nm 3 layers

Expected feedback from 3D for SLHC

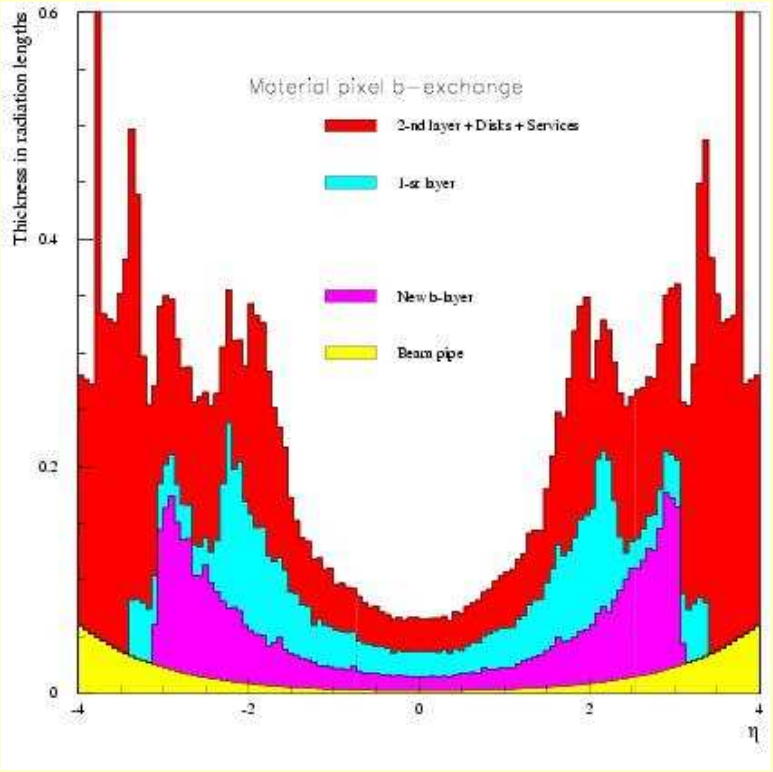
Material budget



R_{b1} = 37.0mm 1.2 % X0

R_1 = 88.5mm 2.3 % X0

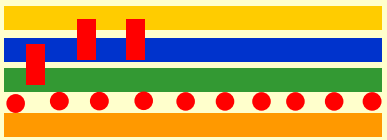
R_2 = 122.5mm

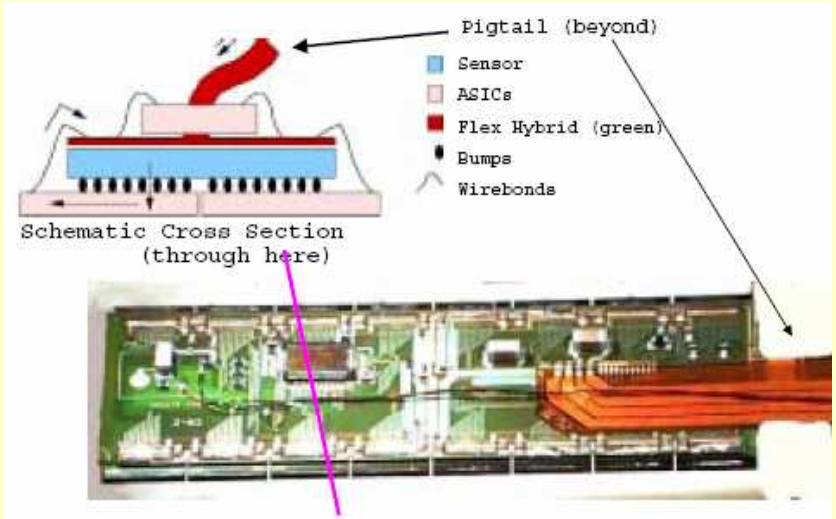


Expected feedback from 3D for SLHC

Importance of low mass

- **Decrease of the material in b-layer by 0.6% X0 improves b-tagging by 20%**
- **Many small gains to be investigated with 3D electronics solutions:**
- **Reduce power consumption->reduce cooling->reduce material**
- **Reduce overlaps: put end of column buffers on 3D tier-3**
- **Replace flex-hybrid and module controller by 3D tier-3**
- **Reduce power cables by DC-DC converters, serial powering. Could 3D help ?**
- **Reduce usage of W and Cu: 1µm W = 4µm Cu/Sn = 26µm Si/Al**

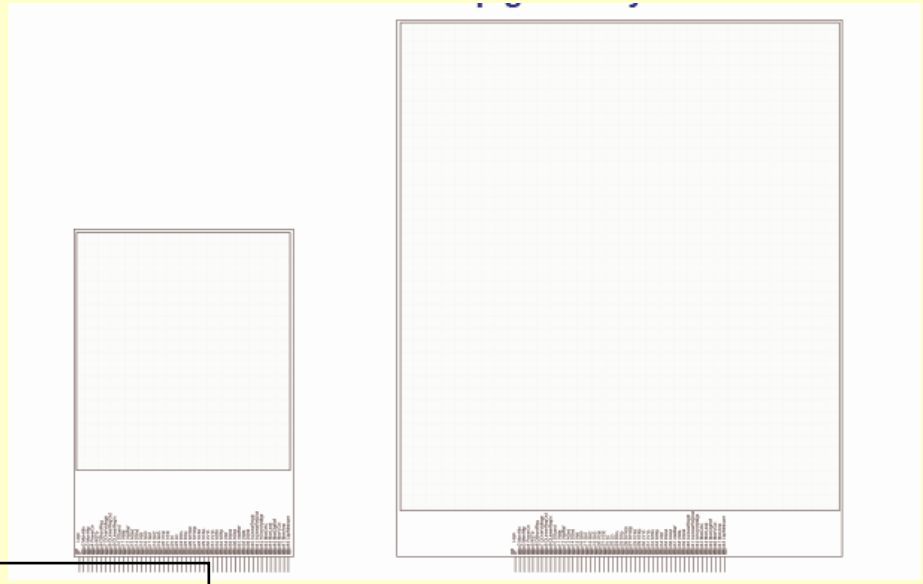




Expected feedback from 3D for SLHC

Efficiency

- **Loss of 3% of b-layer efficiency deteriorate b-tagging by 20%**
- **R&D on yield of 3D interconnections needed**
- **Stability of interconnections with multiple thermal cycling +- 30 degrees ?**
- **Radiation resistance up to 400 Mrad , ageing, corrosions ?**
- **Chip size and yields (wafer to wafer versus dice to wafer)**



FE-I4, 20480 ch. ,
active 16 mm x 17.5 mm

FE-I3, 2880 ch. ,
active 7.2 mm x 8.0 mm

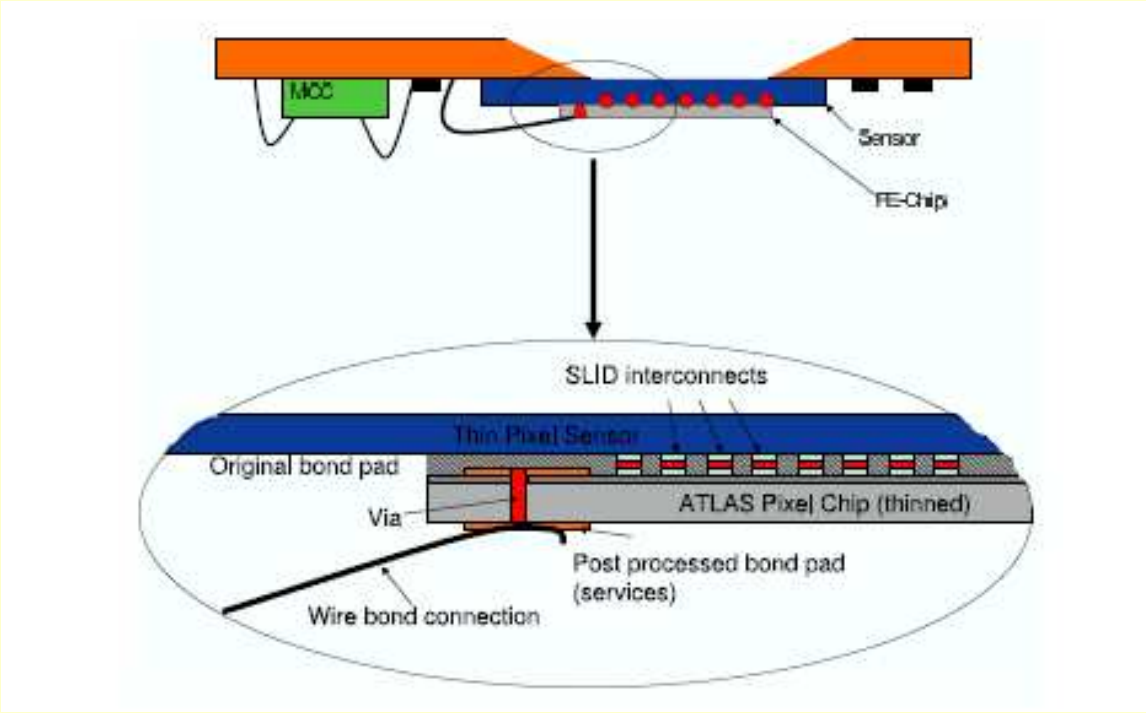
Other 3D feed-backs

- **Reduce significantly the cost by replacing bump-bonding ?**
- **Keep compatibility with different sensor options: planar Si, 3D silicon, diamond ?**
- **Increase SEU tolerance by implementing triple registers in extra space with many Tiers**
- **Potentiality for track trigger option: local clustering, increased latency, fast readout etc**

- **CMS: interest for Fermilab 3D electronics R&D (see talk Ray Yarema)**
- **ATLAS: Bonn-Dortmund-Oslo-Interon-MPI_Munich proposal for RD on 3D integration of sensors and electronics and on thin pixel sensors**
- **ATLAS: interest in Marseille-Orsay-Paris for the R&D on the 3D version of the FE-I4 pixel chip with 130 nm CMOS technology.**

Expected feedback from 3D for SLHC

- **Munich prototype module expected in 2009**
- **Thinned ATLAS FE-I3 chip bonded with SLID to thin 75 µm Si sensor**
- **Via through FE-I3 for wire-bond pad**



Expected feedback from 3D for SLHC

Conclusions

- **3D electronics offers the reduction of the pixel size needed at SLHC**
- **Feedback on the material reduction from 3D electronics should be investigated**
- **RD's for technology choice (SLID, Via (first/last) etc) are needed**
- **Qualifications for efficiency, yields, thermo cycling, radiation are needed**
- **Investigate if 3D interconnections could be less expensive than bump-bonding for interconnections with different kind of sensors**
- **More unexpected benefits of 3D electronics for SLHC are quite probable**

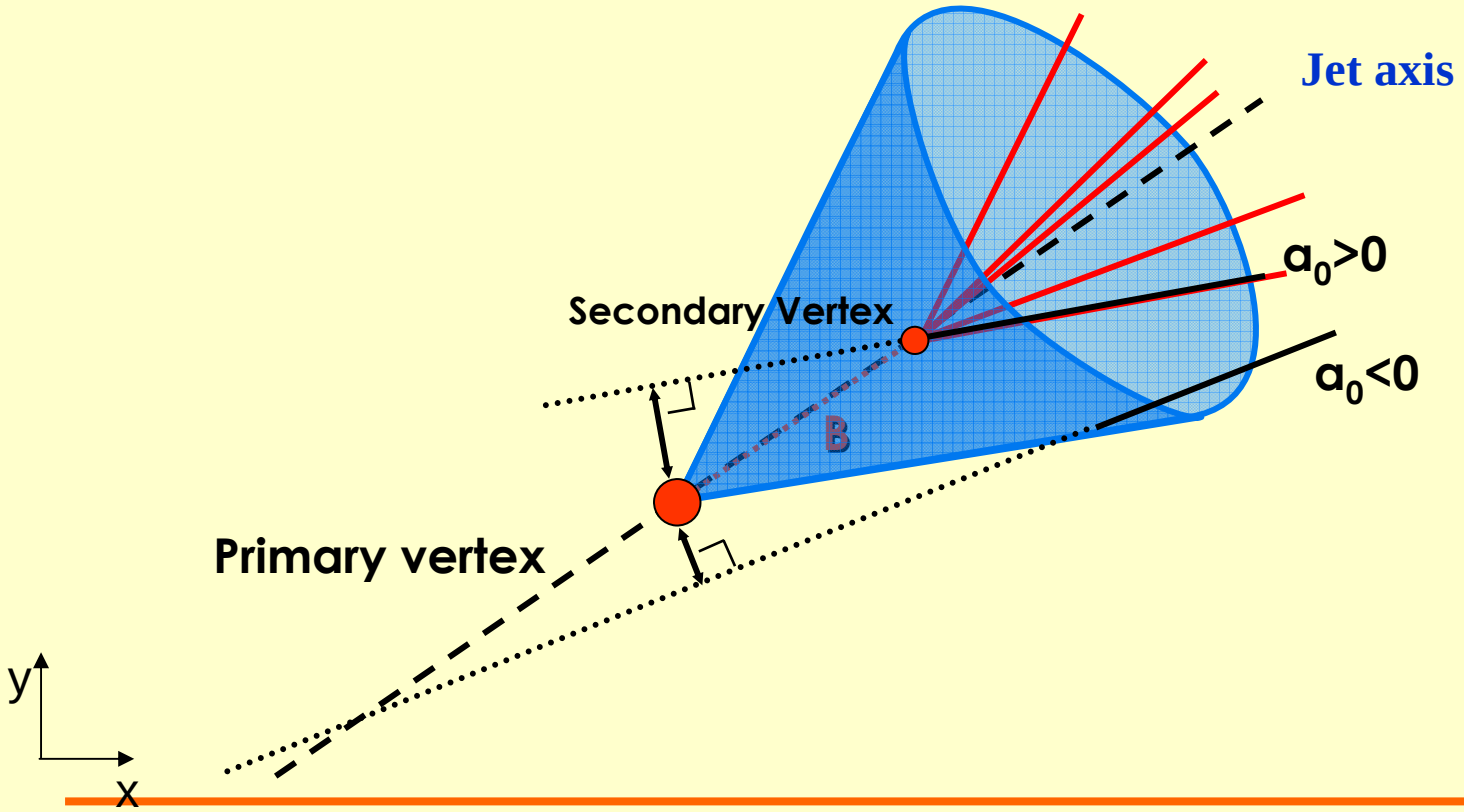
Expected feedback from 3D for SLHC

Spares

Space b-tagging

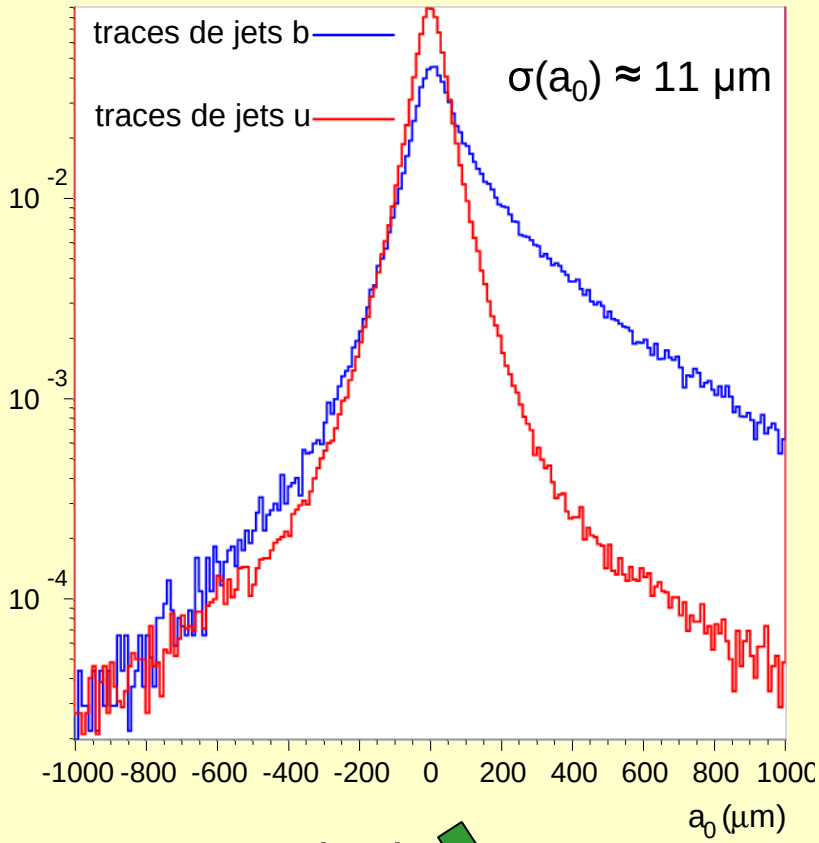
Efficiency of b-jet tagging ε_b

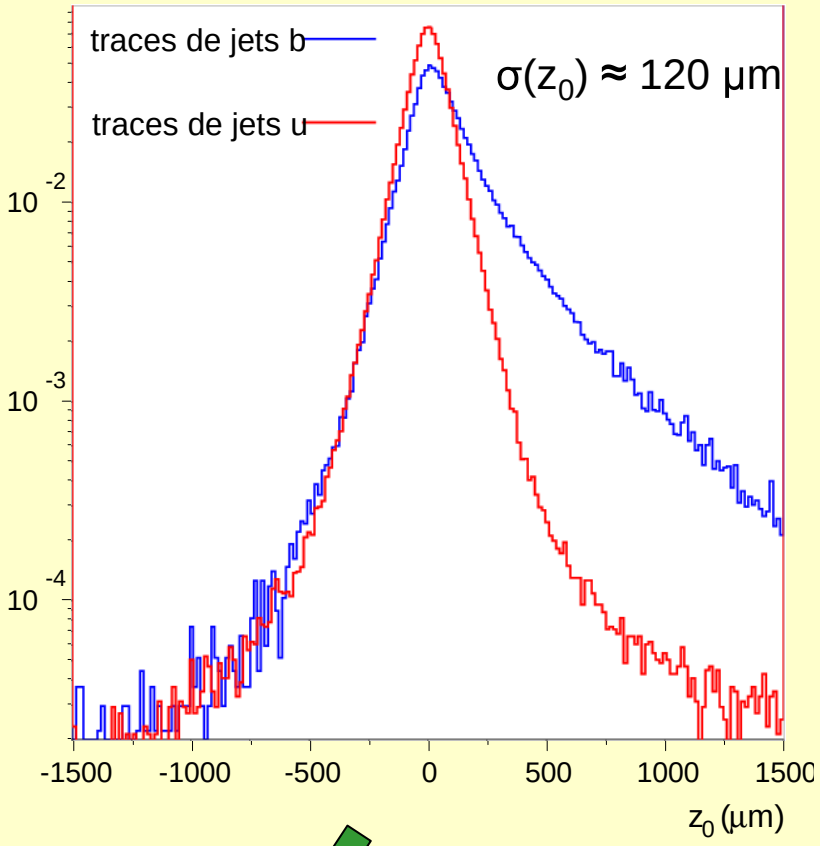
Rejection of light jets (udscg) $R_j = 1./\varepsilon_i$



Expected feedback from 3D for SLHC

Impact parameters





Transverse (2D)

3DMethod

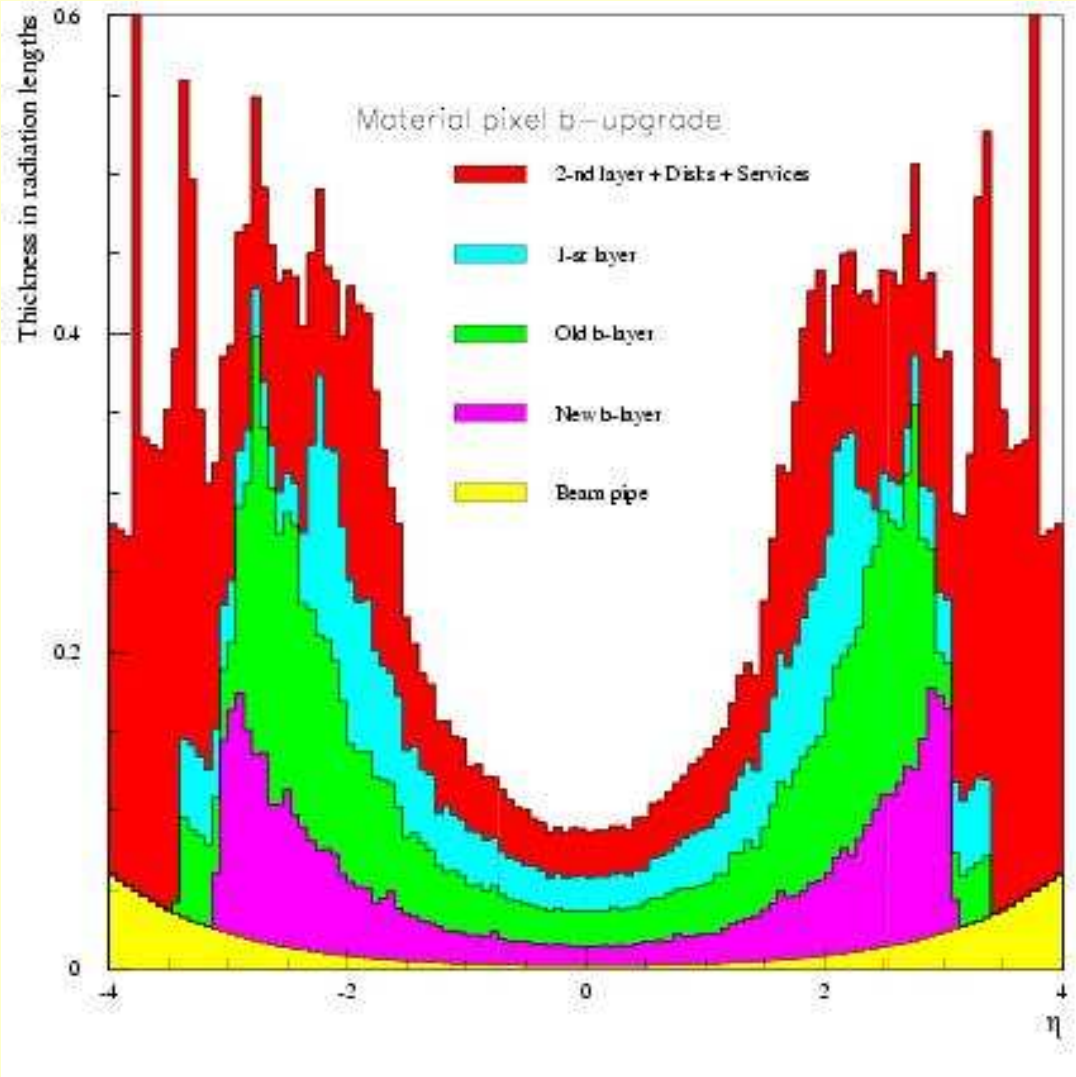
Longitudinal (+1D)

Expected feedback from 3D for SLHC

Layout Material budget

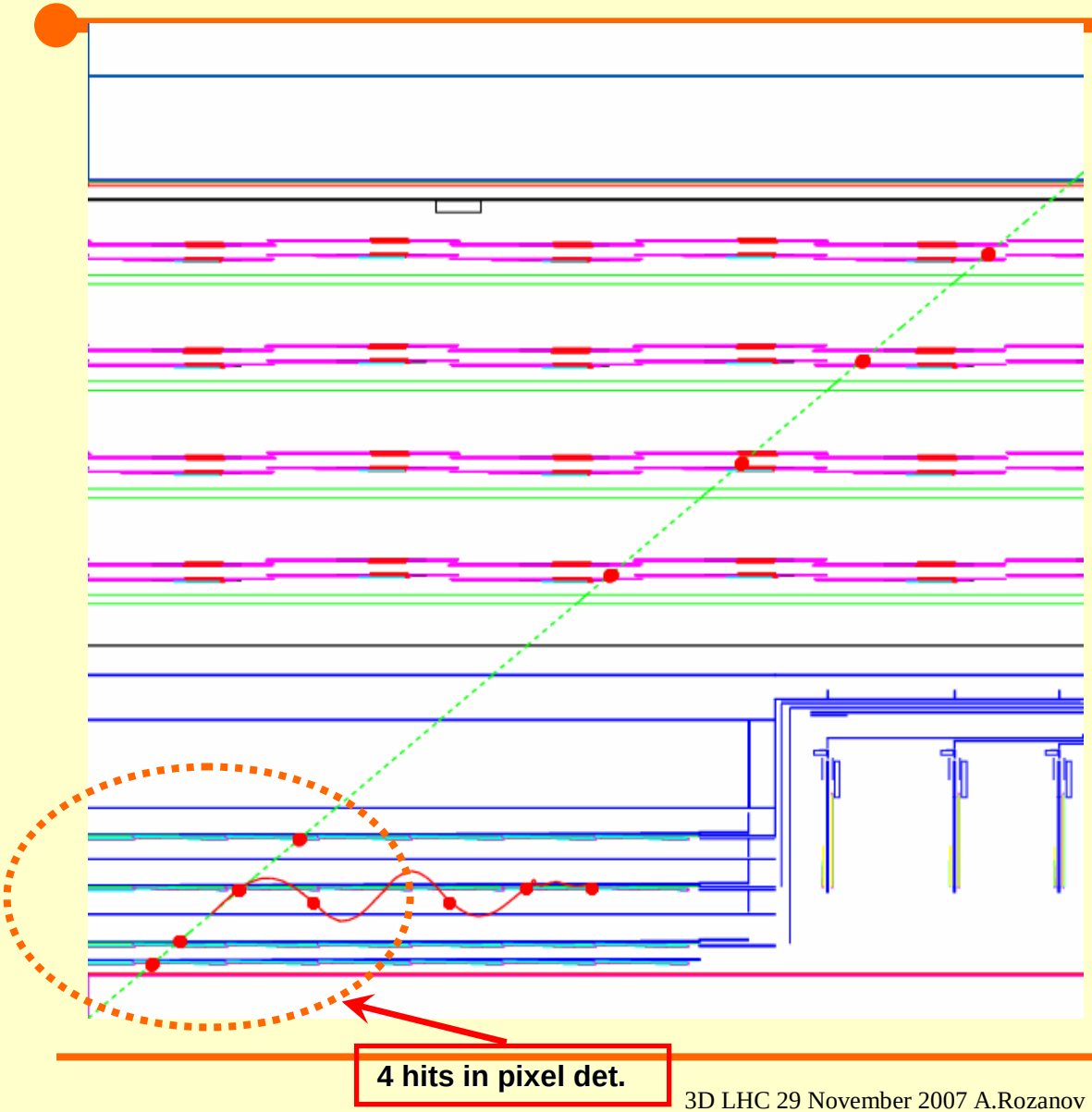
To reduce thickness of new layer:

- **Old b-layer R=5.05 cm 2.2 % X0**
- **New b-layer R=3.7 cm 1.2 % X0**



Expected feedback from 3D for SLHC

Layout



Geant simulation of 3GeV pion in new pixel layout