3D Activities in German (HEP) Labs

(from the MPI point of view..)

Laci Andricek, MPI für Physik, Halbleiterlabor

Interconnection Technology → Interconnecting Technologies

mpi halbleiterlabor

Sensor fabrication

-: high resistivity Silicon
-: double sided processing
-: fully depleted bulk
-: at MPI HLL mainly with integrated first amp. stage (JFET, DEPFET..)
-: "large" feature sizes
...
→ best possible sensor for a specific application

Microelectronics Industry

-: low resistivity Silicon
-: single sided processing
-: most of the bulk insensitive
-: lot of process steps not compatible with sensor fabrication
-: small (really!) feature sizes
-: technology ever changing and improving

→ dedicated readout chip

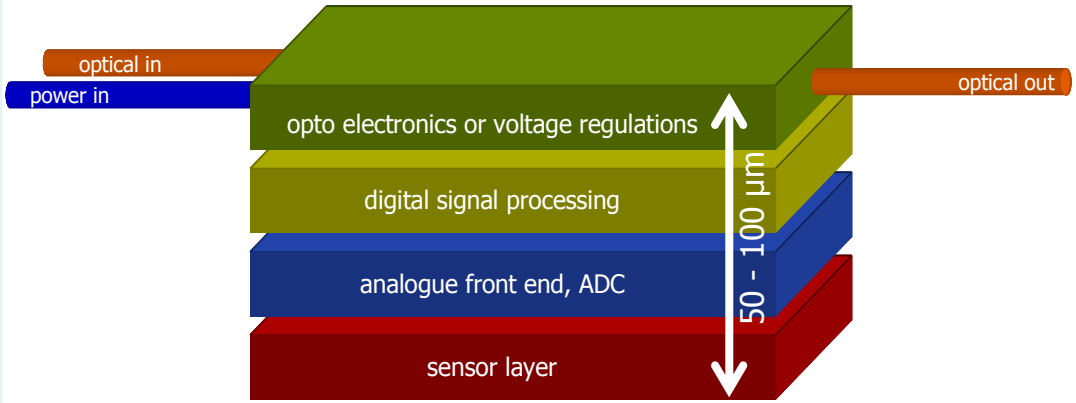
Interconnection

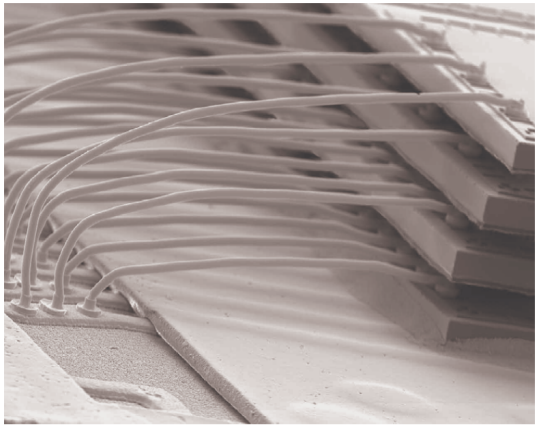
-: wire bonding
-: flip chip / bump bonding
-: 3D integration approach

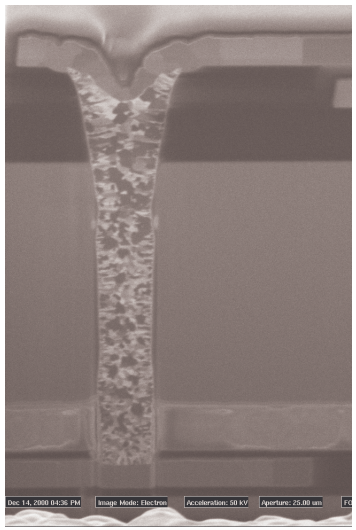
→ Tailored detection system

Sensors made in CMOS Fabs

Vertical System Integration ("3D") - the Vision







-: Different ways to stack Asics: Wafer-to-Wafer, Chip-to-Wafer, via-first, via-last, oxide-oxide bond, Cu-Cu, Eutectic Bonding..

-: Not all of those are fully compatible with sensor technology!

-: Independent control of each of the process steps in the various technologies is needed.

-: The sensor layer should be adapted to the specific application (HEP, X-ray spectroscopy, imaging, single photon counting..)

The Strategy

There is a large momentum in industry to develop vertical integration techniques! We, the detector community, cannot compete with the engineering power of the research departments of big companies like IBM, Intel etc.!

An advantageous strategy could be to develop (adopt) with partners (from industry) a technology, which allows the interconnection of diced 3D chips made in industry or conventional 2D ASICs in a sensor compatible way and to take advantage of the through silicon vias → 4-side buttable devices with signal processing and storage in the pixel.

This technology should keep the way open to stack two or three conventional ASICs on a Sensor wafer without degrading its performance.

Technology: Chip-to-Wafer

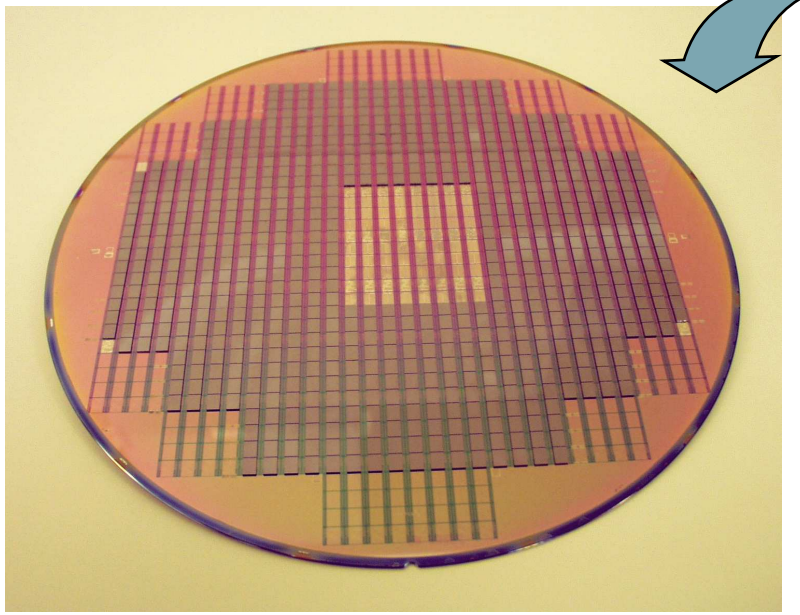
1. ICV/SLID (Inter Chip Via/ Solid-Liquid InterDiffusion), developed by Fraunhofer IZM (Munich) and Infineon
2. University Bonn and Fraunhofer IZM (Berlin) are working on a solder bump technology with Inter Chip Vias

Partner: Fraunhofer IZM, Munich and Berlin

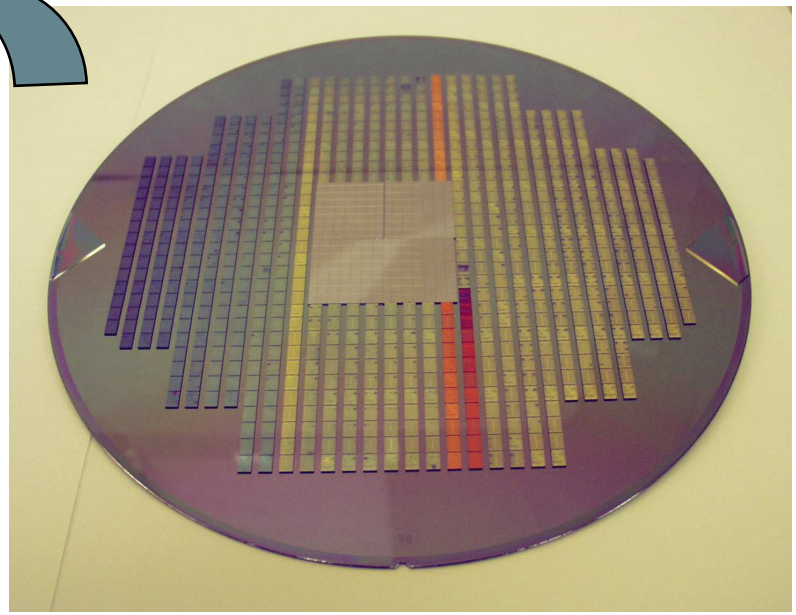
Sensor Layer: simple pad detectors, DEPFETs, SiPMs…

"Chip to Wafer"

target wafer with placed chips
after removal of the handling substrate



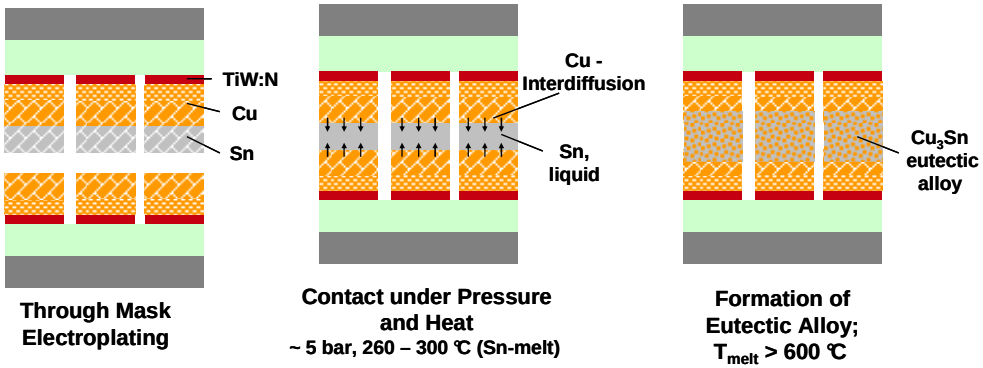
chips on handling substrate

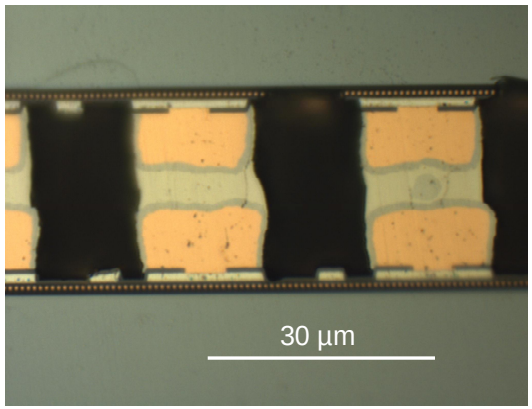


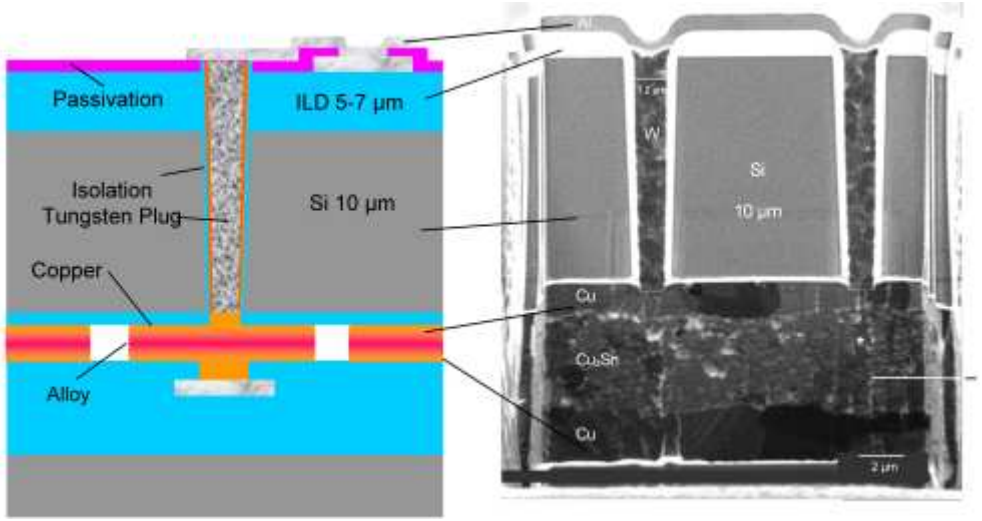
1. tested and diced chips are placed on a handling substrate with alignment marks
2. Handling substrate flipped and aligned to target wafer
3. SLID (temperature and pressure)
4. removal of handling substrate

SLID and ICV

-: Developed at IZM Munich together with Infineon
-: vertical integration is an "add-on process"!! should be compatible with the major technologies







SLID: Solid Liquid Interdiffusion

-: Cu+Sn layers → Cu_3Sn alloy
-: for electical and mechanical connection
-: min. pitch determined by pick and place

ICV: InterChip Via + SLID

-: W or Cu via isolated with SiO_2
-: aspect ratio 8:1 and better with "Bosch process"
-: chip stacking possible

So far so good…

Using this technology we could:

1. build two-layer systems (sensor and r/o chip), interconnected in very fine pitch.
   Due to the inter-chip vias, the (thin!) stack of sensor and electronics would be 4-side buttable.

2. and we would have a tool in our hands to go to "real" 3D integrated systems, if needed for certain applications.

For the time being, the driving projects are :

sLHC: Pixel Detector upgrade → Universities Bonn, Dortmund, Oslo,
Interon, Norway
MPP Munich, HLL

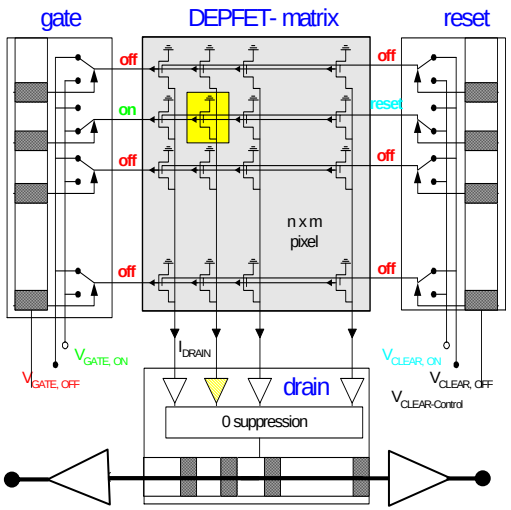
ILC VXD: → Universities Bonn, Karlsruhe, Mannheim
IFIC Valencia, Charles University Prague
MPP Munich, HLL

XFEL: → Universities Bonn, Mannheim, Siegen, Bergamo, Milano
DESY, MPE Munich, MPP Munich, HLL

Projects: DEPFET for ILC and XFEL

see www.depfet.org

DEPFET: Active Pixel Sensor with internal q-I conversion: ~1nA/e-



1. Row wise read-out ("rolling shutter") → Concept for the **ILC VXD**

- select row with external gate, read current, clear DEPFET, read current again → the difference is the signal (row wise CDS)

Advantage

- Low power consumption!
- No advanced interconnection technologies needed

Disadvantage

- limited frame rate

Design goal at the ILC: 50ns row rate (sample-clear-sample)

2. Hybrid-pixel-like approach: one amp. (ADC, RAM..) / pixel

Advantage

- fast! (~ns), frame rate comparable with hybrid pixels

Disadvantage

- challenging interconnection **(→"3D")**
- high power consumption

Option for the focal plane at the **XFEL**

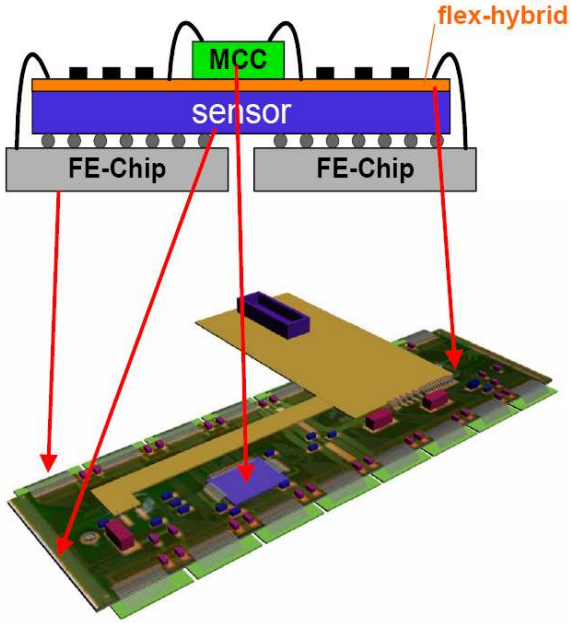
3. Combination of those two

- subdivide large arrays into smaller units
- challenging interconnection **(→"3D")**

→ find optimum for a specific application balancing the pros and cons

under consideration for the **ILC VXD**

Projects: sLHC Pixel upgrade



The present ATLAS Pixel Module

- already an impressive example of vertically integrated systems!!!

a few shortcomings

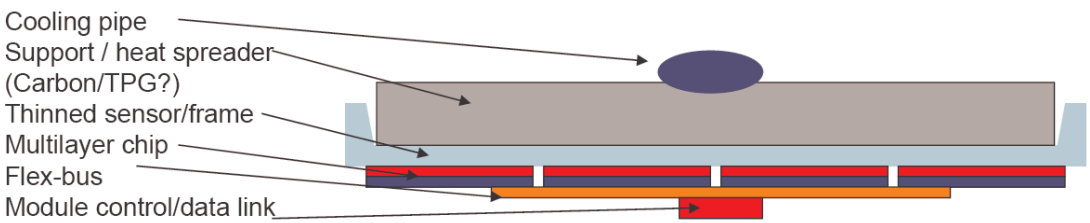
- no ICVs → cantilever → about 30% "dead" area per module
- rad. length 0.48% X_0 (Silicon only)

A new Module concept

- thin n-on-p detectors (50-100 µm)
- SLID/ICV interconnection to a (multilayer) r/o chip

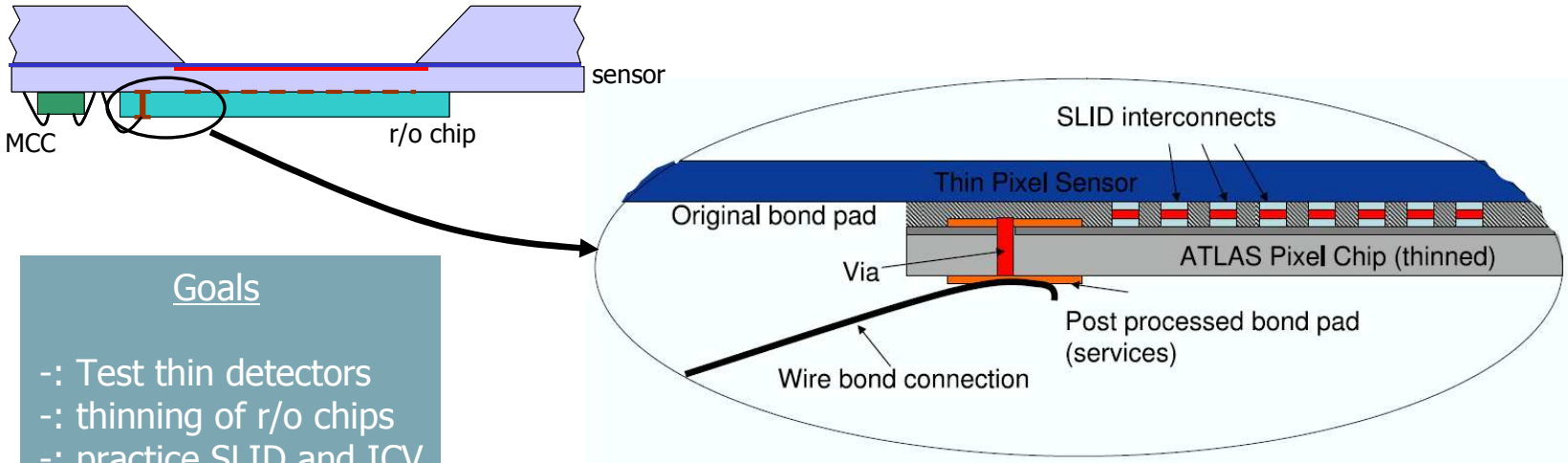
Advantages

- no cantilever → dead region <10%
- Si radiation length 0.12%



sLHC: R&D Program 2007 - 2009 → Demonstrator

Existing ATLAS Pixel chip (FE-I3) face-to-face attached to a thin sensor!



Goals

-: Test thin detectors
-: thinning of r/o chips
-: practice SLID and ICV

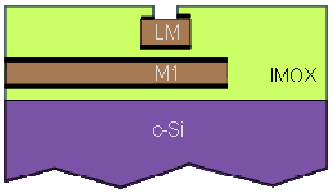
Main Work Packages (with a lot of hidden details!!!):

-: Design and production of thin sensors at MPI HLL → production started
-: Design of a dedicated r/o chip for test sensors - Interon, Uni Oslo → almost finished

-: Post-processing of the sensor wafers (SLID prep.) at IZM
-: Post-processing the FE-I3 wafers and the Interon Chip (SLID prep. and ICV) at IZM

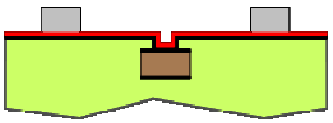
-: Interconnection of sensor and r/o also at IZM

Post-Processing of Sensor and r/o ASIC Wafers(!)



Initial state

Opened passivation
Vias Ø 2 µm, Al or Cu

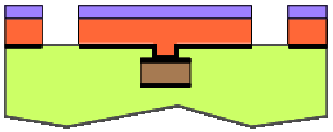


Sputtering

TiW barrier 50nm
Cu seedlayer 100nm

Litho

Insulation trenches



Plating module

Cu 5µm
Top wafer only: Sn 3µm
Resist strip
Wet etch seedlayer & barrier

ASIC Wafer preparation

-: **Preparations** for SLID and via formation (ICV) have to be done **at wafer level**!

-: This is an issue during the R&D phase! (In particular for the ASIC Wafer)

-: We should try to get organized…

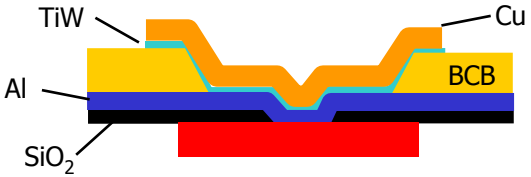
→ multi project runs with ASICs from our community
→ get the whole wafer from the Fab, post-process it
→ distribute the individual chips to the various projects

For sensor wafer:

How does the post-processing change the properties of the sensor??

First tests with IZM

Diodes (our standard test vehicles) have been produced on SOI Wafers:
top layer: 50 µm thick, 150 Ω.cm

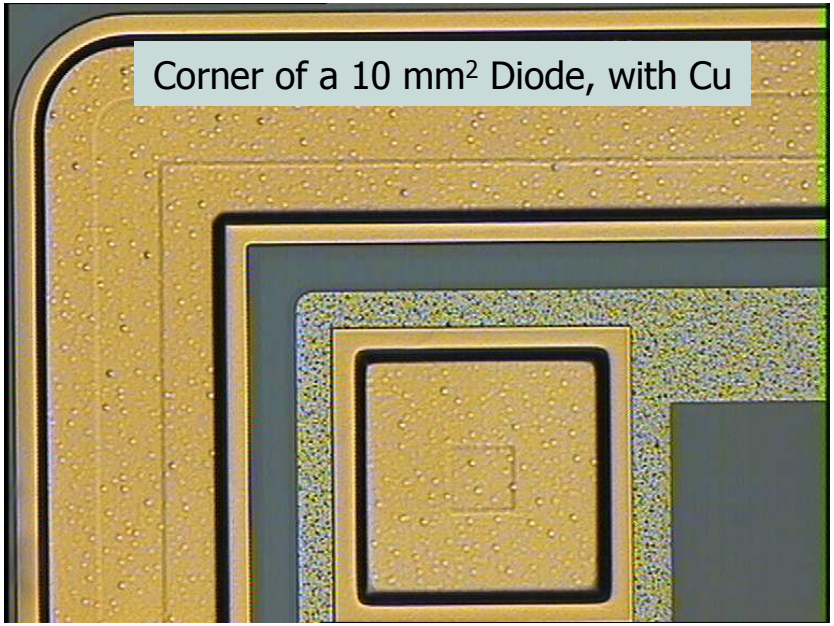


-: BCB layer with openings to define TiW/Cu/Sn System

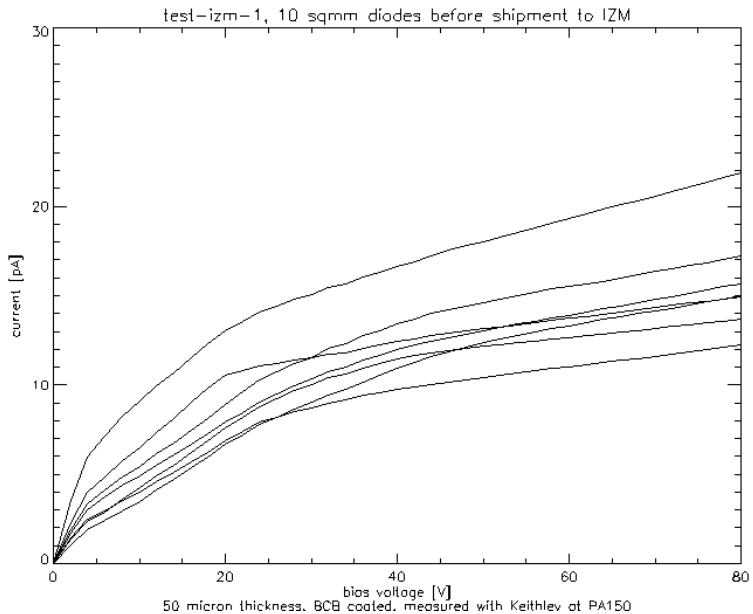
-: Handle wafer acts as back side protection layer during the IZM processing

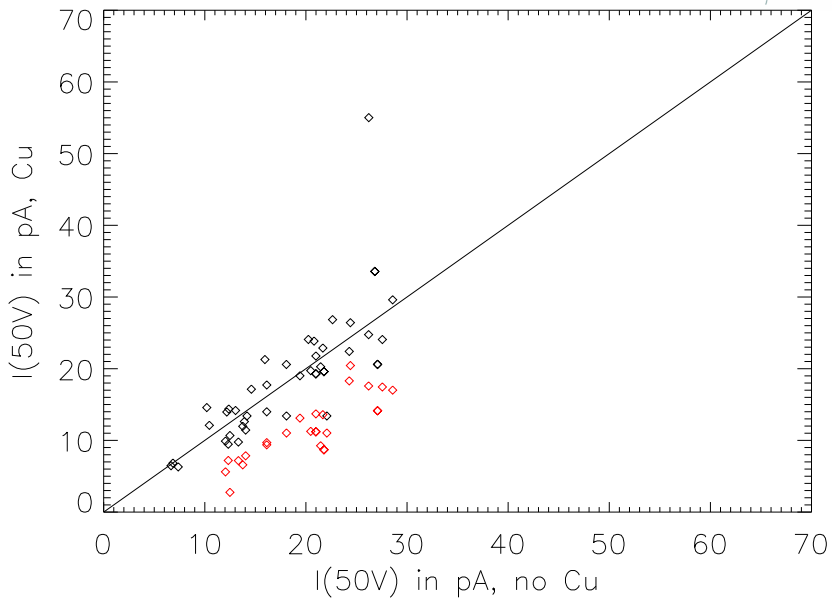
-: Metal system done at IZM:
100 nm TiW, sputtered
200 nm Cu, sputtered
1 µm Cu, through mask electroplated

-: on a 2nd Wafer: TiW + 5 µm Cu + 1 µm Sn



Characteristics





-: IV Curves before Cu metallization
-: measured at HLL, right before shipment to IZM
-: from CV curves → full depletion at 50 V

Correlation of the reverse current at full depletion (50 V) before and after Cu metallization

-: right after Cu-System application (black diamonds)

-: after 320 degC in forming gas - SLID emulation (red diamonds)

→ No significant effect of Cu metallization noticeable!

In Summary

Microelectronics Industry is moving into the 3rd dimension - vertical integration is becoming one of the major topics of semiconductor technology conferences and it is on the door step to be transferred to the production lines.

We have to keep up to date with our interconnection technology to be in the position to take advantage of this development.

The ICV/SLID technique offers the opportunity to connect highly granular pixel detectors with pre-tested and ultra-thin r/o chips and allows the construction of multi-layer detector stacks, if needed.

Even in the case of a "simple" two-layer stack of sensor and r/o, the use of inter-chip vias allows the construction of 4-side buttable devices, reducing the dead region for large area pixel detectors.

Very first tests of the sensor post-processing needed for SLID are promising. A much larger study (including ICV) in the frame work of the sLHC pixel upgrade is about to be launched.

The outcome of this R&D program will certainly have an impact on other projects like the ILC VXD and XFEL.

…. yet another Workshop

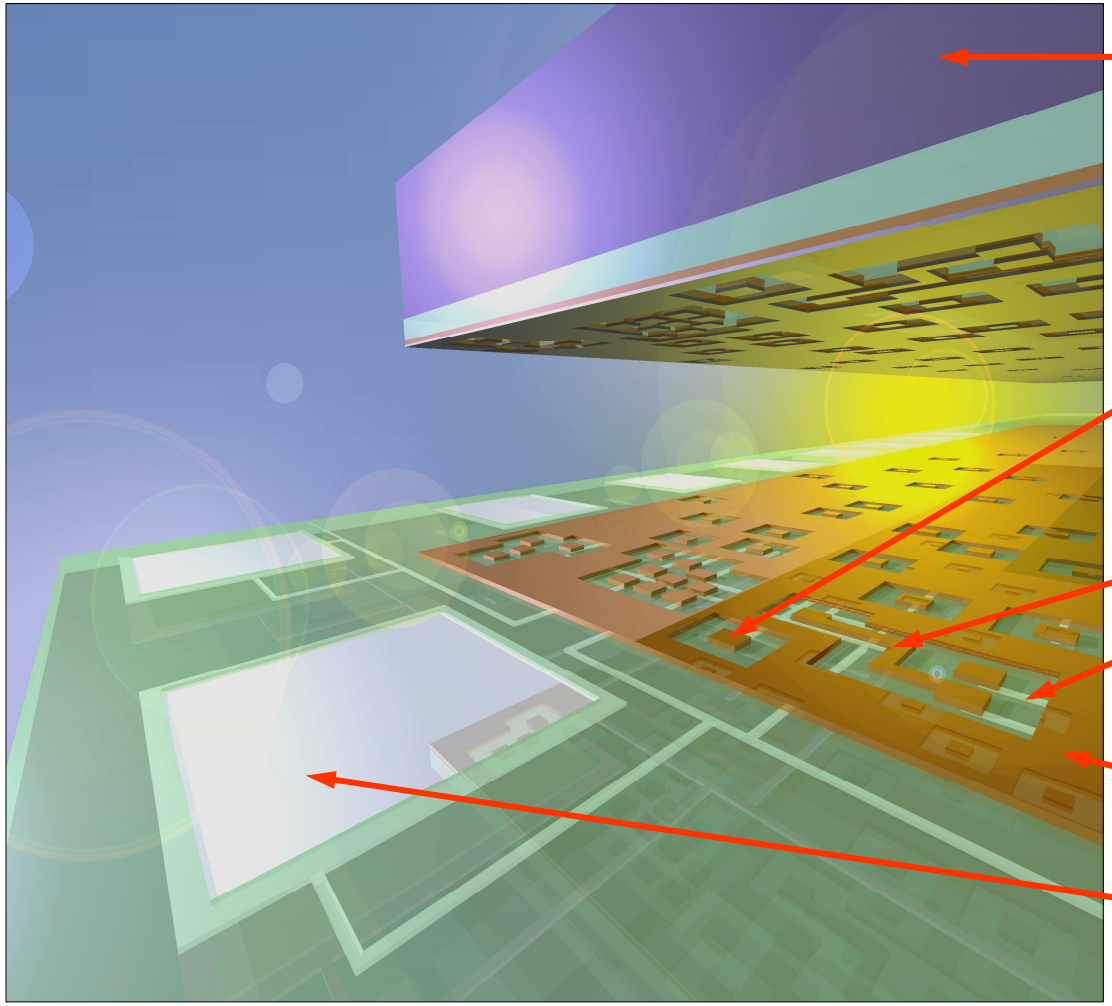
3D Integration Technologies for HEP and X-Ray Imaging

Ringberg Castle, Tegernsee, Germany

April 6, 2008 - April 9, 2008

- Backup slides follow….

Face-to-Face SOLID Process (IFX)



Top chip
Cu and Sn coating

Bottom chip
Cu coating, bond pads

No underfill

Inter chip vias
15 x 15 µm²
5 µm vias to LM

Redistribution

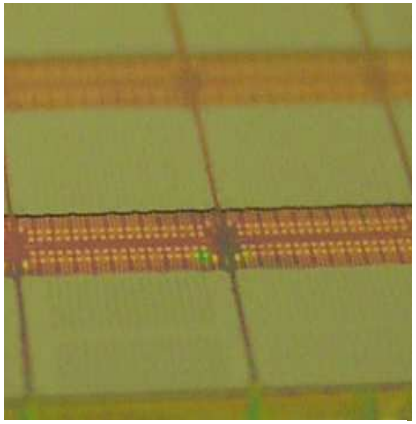
Insulation trenches
15 µm

Passive area
heat spreader

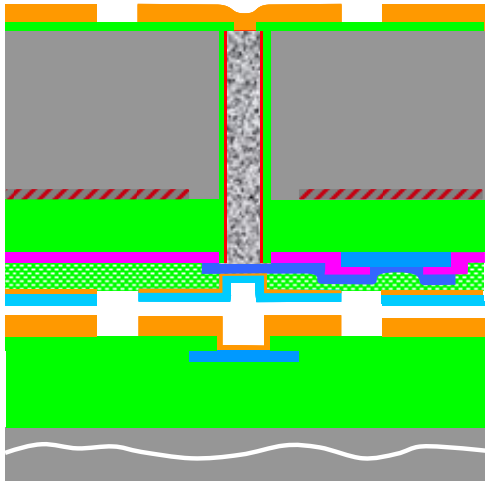
External IOs
standard wire bonds

The 3rd Layer - InterChip Vias (ICV) → IZM, Munich

1. thin the attached chip and make a contact to the buried metal layer

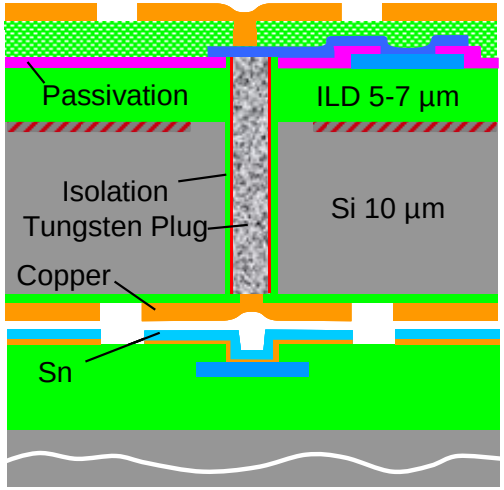


After Thinning on Target Substrate
Chip Thickness 10 µm



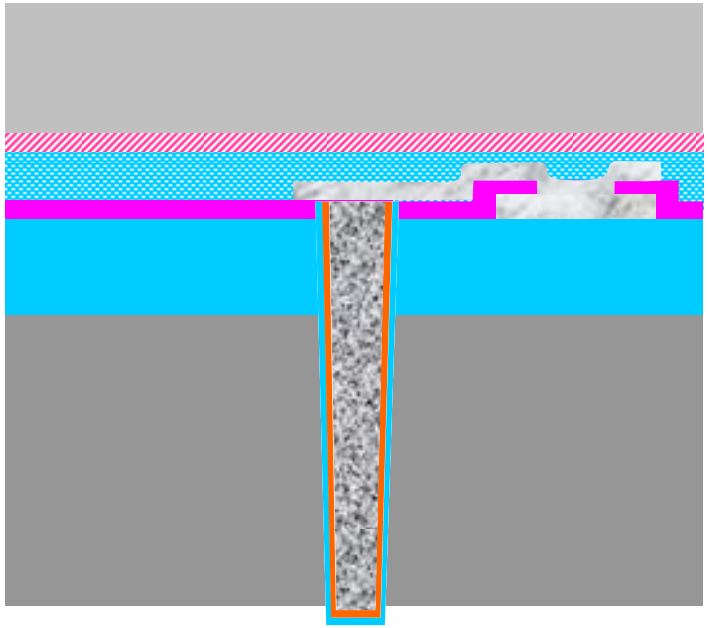
W-Plug / Cu / Sn

2. or….face up attachment of a thin chip to the target wafer →

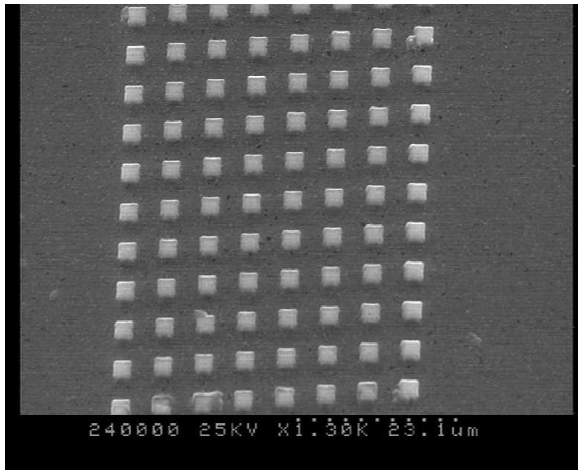


W-Plug / Cu / Sn

The 3rd Layer - InterChip Vias (ICV) → IZM, Munich

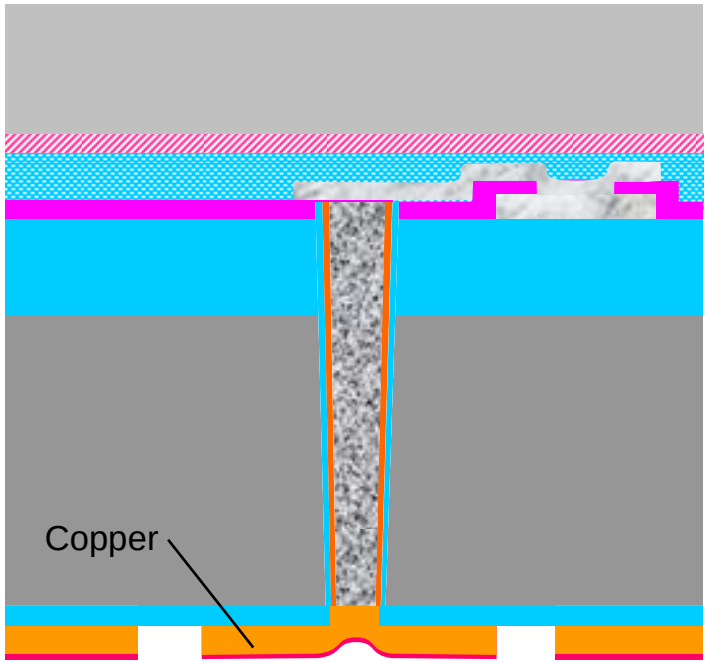


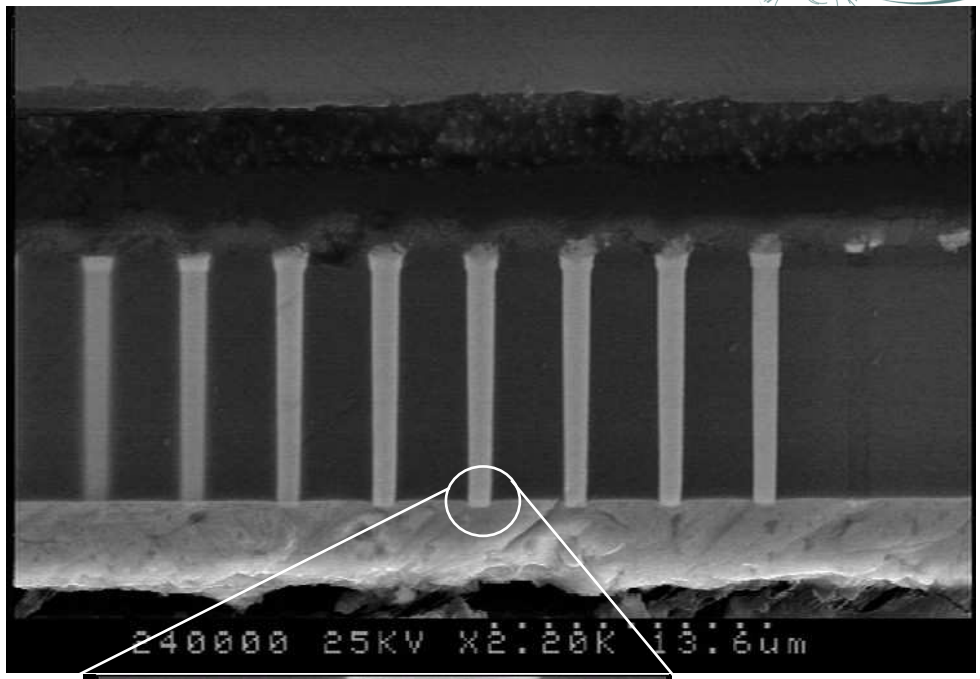
- Fabrication of Tungsten-filled InterChip Vias on Top Substrate
- Via Opening and Metallization
- Bonding to Handling Substrate
- Thinning



IZM, Munich

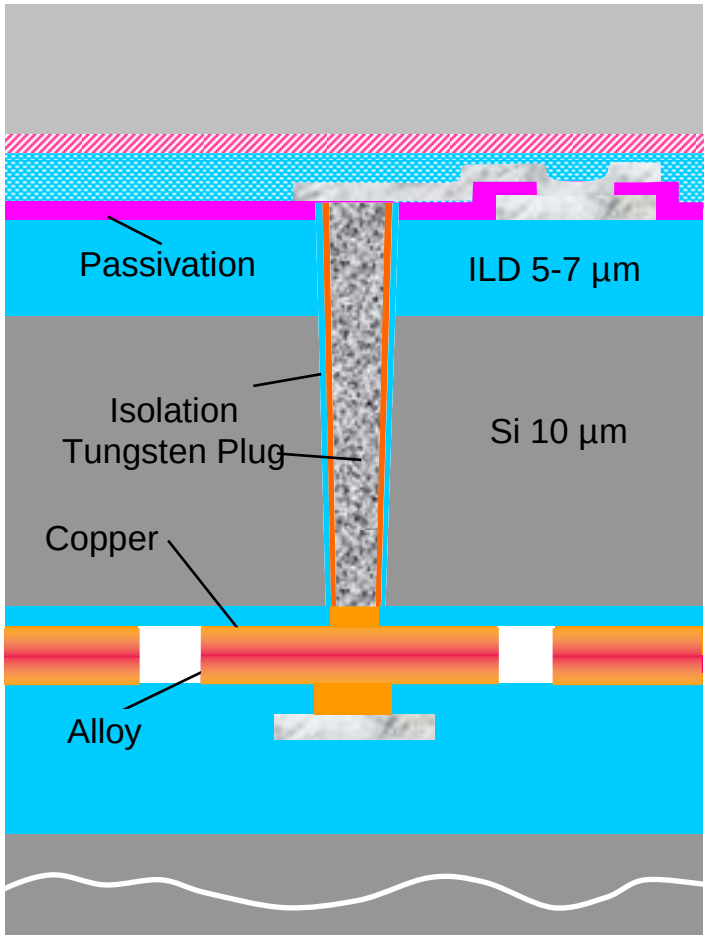
The 3rd Layer - InterChip Vias (ICV) → IZM, Munich





IZM, Munich

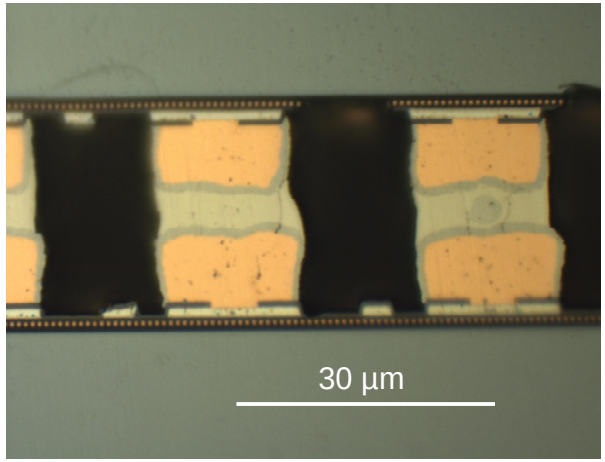
The 3rd Layer - InterChip Vias (ICV) → IZM, Munich

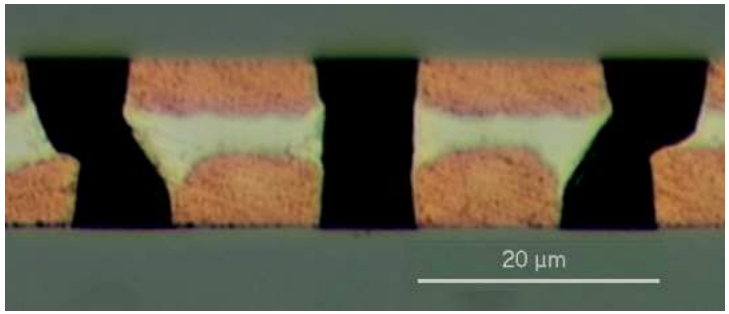


- Fabrication of Tungsten-filled InterChip Vias on Top Substrate
- Via Opening and Metallization
- Thinning
- Opening of Plugs
- Through Mask Electroplating
- Alignment and Soldering

IZM, Munich

Face-to-Face SOLID Process (IFX)





- Standard contacts (defined by bonder alignment): 15 x 15 µm², 5 x 5 µm² vias to last metal
- 10 µm pads with 20 µm pitch demonstrated
- 5 µm crossed lines have successfully been bonded
- No influence of particles seen (class 10000 CR)
- Thickness of the top chips: 80 µm, typically 125 µm
- Shear strength of the bond: >120 N @ 25 mm² chip size
- Measured contact resistance: 5 mΩ for a standard contact
- Worst case simulation of stray capacities: 34 – 40 fF (w/o and w/ underfill)