3D Integrated Technology Perspectives
First Worshop on LHC-ILC prospects

CMP

Infrastructures For Microelectronics & MEMS

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Outline

- Motivation
- IC fab
- Advanced processes
- MEMS fab
- Design kits
- CAD tools
- IP
- Packaging
- Test
- New at CMP in 2007
- Conclusions: trends

Motivation

MPC/MPW Infrastructures for Education, Research and Industry

Why?

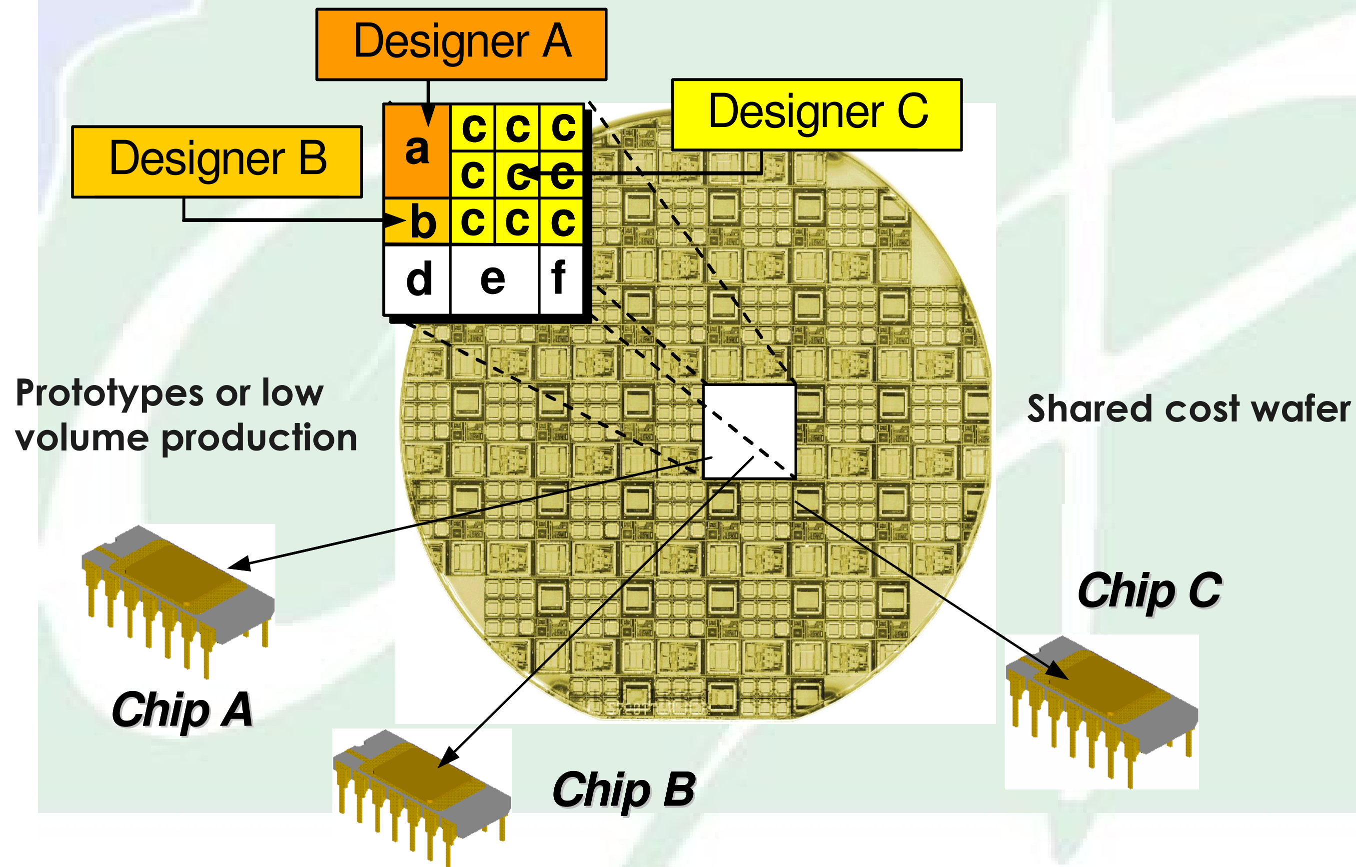
- + to well educate students, who will become good engineers
- + to produce good researchers
- + to provide SMEs with small volume production

How?

- + sharing the wafers, to share the cost
- + sharing various needs

mass production : circuits are cheap because of batches of hundreds of wafers

few circuits : shared wafers
Universities, SMEs, ...
prototyping, low volume



Generalities

- CMP created in 1981
- industrial quality process lines (University process lines cannot offer a stable yield)
- design kits to link CAD and MPW, to facilitate the design.
- Customer base development
  + Universities / Research Labs
  + Industry
  + 1000 Institutions in 70 countries
- Non-profit, non-sponsored

Technical development

1981–1982	:	launching CMP with NMOS
1983–1984	:	development of NMOS, launching CMOS
1984–1986	:	development of CMOS
1987–1989	:	abandon NMOS, increase the frequency of CMOS runs
1990–1994	:	launching Bipolar, BiCMOS, MESFET GaAs, HEMT GaAs, advanced CMOS (.5 μ TLM) and MCMs
1995–1997	:	launching CMOS, BiCMOS and GaAs compatible MEMS, DOEs, deep-submicron CMOS (.25 μ 6LM)
1998	:	launching surface micromachined MEMS, abandon MESFET GaAs
1999	:	launching SiGe, .18 μ CMOS
2001	:	.35 μ HBT SiGe BiCMOS, .12 μ CMOS
2003	:	PolyMUMPS, MetalMUMPS, SOIMUMPS
2004	:	90 nm CMOS, BCD-SOI
2005	:	ASIMPS, SUMMIT/SANDIA
2006	:	65 nm CMOS, 0.6 μ CMOS Bulk Micromachining

Summary of services : one stop shop

ICs :	austriamicrosystems	0.35 µ CMOS 0.35 µ SiGe 0.35 µ CMOS-Opto 0.35 µ CMOS HV 0.35 µ CMOS EEPROM
	STMicroelectronics	65nm CMOS 7LM 90nm CMOS 7LM 0.12 µ CMOS 6LM 0.35 µ SiGe BiCMOS 0.25 µ SiGe:C BiCMOS
	OMMIC / PML	0.2 µ HEMT GaAs HEMT
	CSMC	0.6 µ CMOS 2LM/2LP/HRES
MEMS :	CMP/austriamicrosystems CMP/CSMC	0.8 µ BiCMOS bulk micromachining 0.6 µ CMOS bulk micromachining
	MEMSCAP	PolyMUMPS MetalMUMPS SOI-MUMPS

CAD Tools : Tanner, ARM , Mentor Graphics, SoftMEMS
IP exploitation : ARM cores on STMicroelectronics processes (0.12 µ and 65nm)
Design kits : more than 35 different kits

Packaging : Ceramic, plastic, custom …

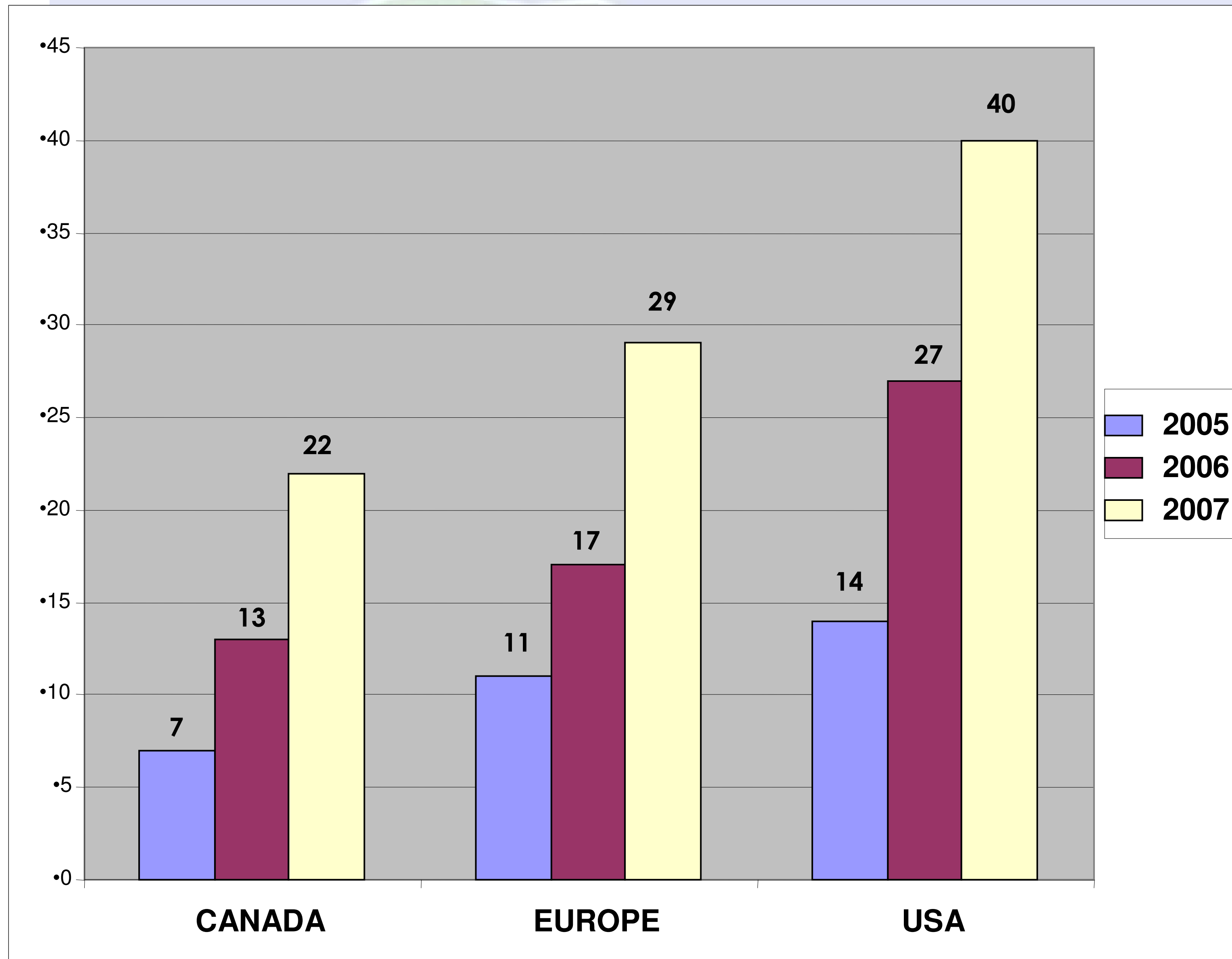
Advanced processes at CMP

CMOS

120 nm	2001	:	210 ICs to date
90 nm	2004	:	160 ICs to date
65 nm	2006	:	32 ICs to date

(45 nm 2007 to selected Institutions)

Number of circuits in 90nm CMOS (3 regions)

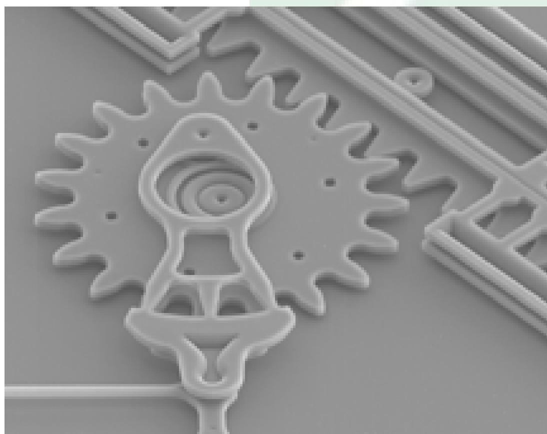


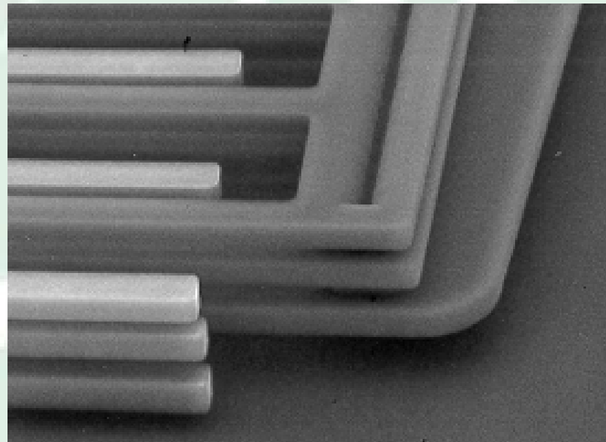
MEMS

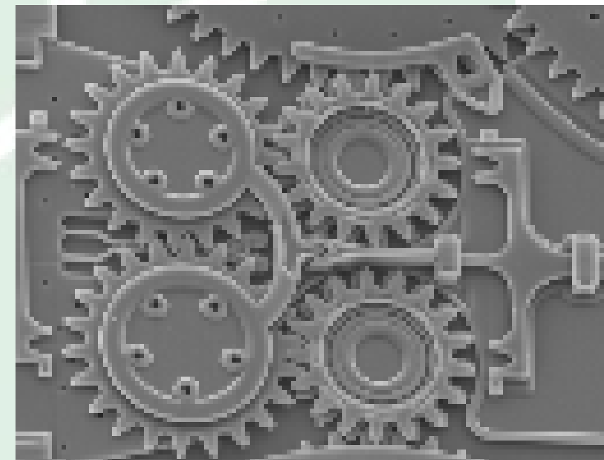
MUMPS from MEMSCAP

SUMMIT from SANDIA

CMU post-process on .35 SiGe BiCMOS ST







Very sophisticated mechanical structures with Sandia MEMS Process

Design kits for ICs

Foundry / Process	CAD tool	Version
austriamic. CMOS 0.6 CUP	Cadence 4.4.6 (QSR2 minimum)	3.40
austriamic. CMOS 0.6 CUP	Synopsys	
austriamic. CMOS 0.6 CUP	Mentor Graphics rel. C2	3.20
austriamic. CMOS 0.6 CUP	Tanner/L-Edit rel. 6, 7, 8	3
austriamic. CMOS 0.6 CUP	Exemplar-Leonardo	
austriamic. CMOS 0.35 C35B4C3	Cadence 4.4.6.100.87 and 5.0.32	3.51
austriamic. CMOS 0.35 C35B4C3	Mentor Graphics	3.51
austriamic. SiGe BiCMOS 0.35 S35D4	Cadence 4.4.6.100.87 and 5.0.32	3.51
austriamic. SiGe BiCMOS 0.35 S35D4	Mentor Graphics	3.51
ST 0.18 CMOS HCMOS8D	Cadence 4.4.3	6.1.3
ST 0.12 CMOS HCMOS9	Cadence 4.4.6	
ST 90nm CMOS CMOS090	Cadence	
ST 0.35 SiGe BiCMOS BiCMOS6G	Cadence 4.4.6	
OMMIC GaAs ED02AH	ADS2003A exclusively	2.7
OMMIC GaAs ED02AH	AWR (Microwave Office Simulator) v5.53	1.1
OMMIC GaAs ED02AH	PSpice models	04-2000
OMMIC GaAs ED02AH	CADENCE	

CAD Tools from CMP

Tanner Res.	L-Edit T-Spice	.35 CMOS
Mentor Graphics	Leonardo ModelSim	.35 CMOS
SoftMEMS	MEMS PRO MEMS Xplorer	Poly, SOI, Metal MUMPS
ARM tools	ADS ESL tools	.12 CMOS

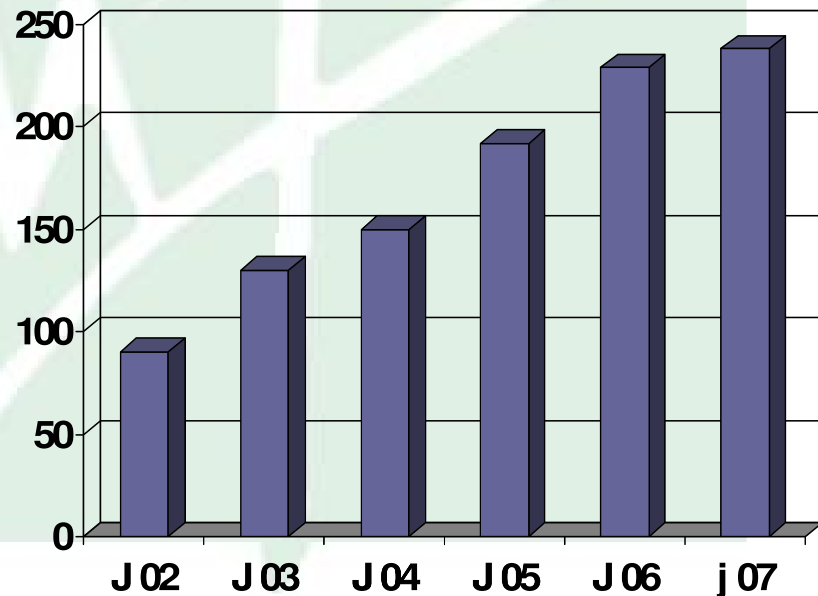
ARM

- ARM suite of tools for programming ARM cores ($500)
- Educational kit ($999)
- All other ARM tools

- routes to fab for ARM cores

Centres

Licences



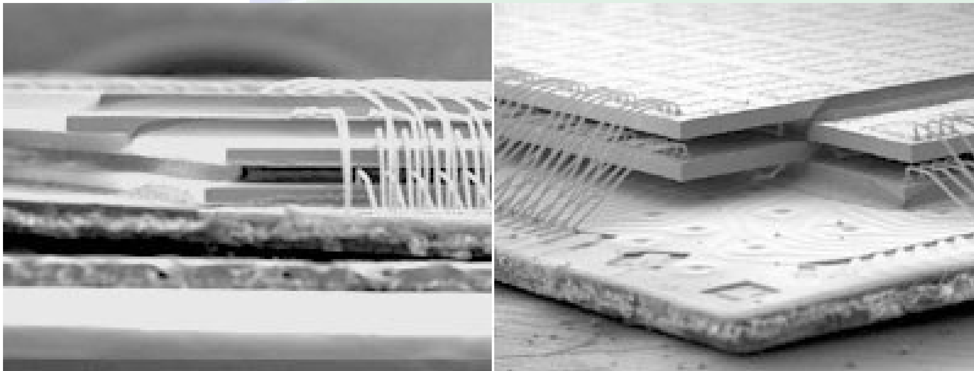
Packaging

— Ceramic / Plastic

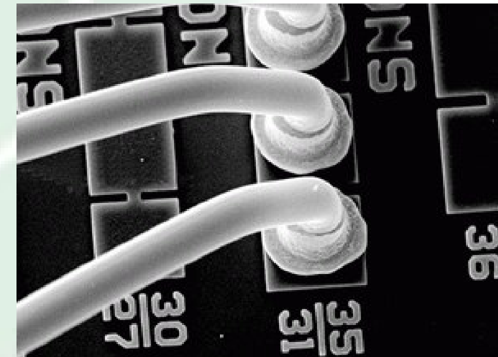
— Prototyping / Low volume

— Wide Range of Packages

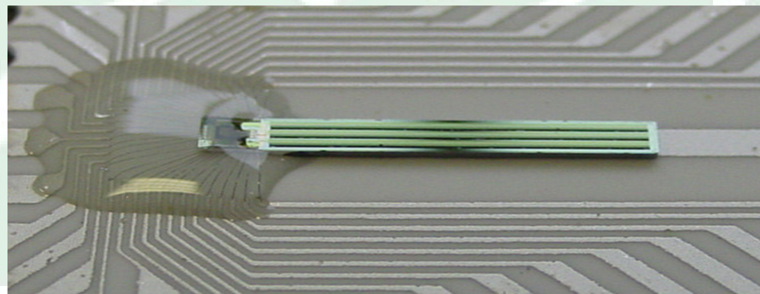
— Lead-free & Green programs



Stacked dies / Multi-Stacked dies



Ultra fine pitch bonding



Custom Packaging for MEMS

Packaging

<u>Several assembly houses</u>

— **HCM**	***Ceramic,…***
— **SYSTREL**	***Ceramic,…***
— **i2a, CEI**	***Plastic,…***
— **Gamberini**	***Specific requirements (MEMS,…)***

Test

On request,
from the user specifications

- *Percentage analog/digital*
- *number pads*
- *clock frequency*
- *number of test vectors*
- *etc.*

- **SERMA Technologies, France**
- **LCIE, France**
- **BULL, France**
- **CSEE, Switzerland**
- **austriamicrosystems, Austria**
- **NNTTF, Australia**

New at CMP in 2007

- CMOS 65 nm ST (Q4 2006)
- SANDIA (DK from SoftMEMS ready)
- ASIMPS (First run started in May 2007)
- All ARM ST cores available in 65nm CMOS
- Low cost 0.6um CMOS and bulk micromachining
- SOI ?

3D Integration Technologies

- **Could be offered by CMP :**
  - **Organizing MPW runs like for the 2D processes**
  - **Using the experience on logistics and support**
  - **Using the expertise on handling complex processes**
  - **Promoting to the customer base and sharing the cost**

Conclusion : trends

- going global
- technologies targeted: electronics, photonics, mechanics, fluidics, ...
- advanced processes (because of CAD, for education), very advanced to keep leadership
- quality of service : CMP certified ISO 9002/1994 moving to ISO 9001/2000