3D technologies at CERN: stacking and tracking for future physics

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CERN Genève

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29 November 2007

ACTIVITY in Si TECHNOLOGY at CERN

MOST RESOURCES GO INTO LHC MACHINE TERMINATION

PH MICROELECTRONICS GROUP ME (Marchioro) :

FOLLOW-UP of CHIP DESIGNS ATLAS, CMS, ALICE, TOTEM, ...

MPW + RUNS + SUPPORT CMOS 0.25 um

NOW / SOON ALSO 0.13 um and 90 nm

RADHARD CHIPS STUDIES total dose, SEU MODELS, .. (Faccio)

NEW EXPERIMENTS : NA62

EXTERNALLY FUNDED DEVELOPMENT:

AMORPHOUS Si (Jarron cs) MEDIPIX (Campbell cs)

PH SUPPORT GROUP TA1(Joram) :

EP Si FACILITY : LHC CONSTRUCTION (Moll)

RADHARD Si DETECTORS COORD RD50 }

IRRADIATION FACILITIES PS p,n (Glaser)

FUTURE Si ACTIVITY SLHC / ILC / CLIC

EVALUATE + INTRODUCE NEW CMOS TECHNOLOGY

CMOS 0.25 um SUCCESFUL, SPECIAL RADHARD LIBRARY

EVALUATION of 0.13 um and 90 nm from FEW FOUNDRIES

RADHARD STUDIES , MODELS, LIBRARY

SOME FOUNDRIES PROMISE 3D BACK END TECHNOLOGY

through-wafer vias

pads with under-bump-metal

thinning down to 20 (?) um

SPECIFIC PROJECTS :

CHIP DESIGN

e.g. DC/DC POWER SUPPLIES, OPTICS DRIVERS,

GASEOUS DETECTORS with DIRECT CHIP READOUT:
TIMEPIX EUDET (NIKHEF-SACLAY-FREIBURG-)

OTHER ? e.g.FP7 ?

NEW COLLABORATIONS ??

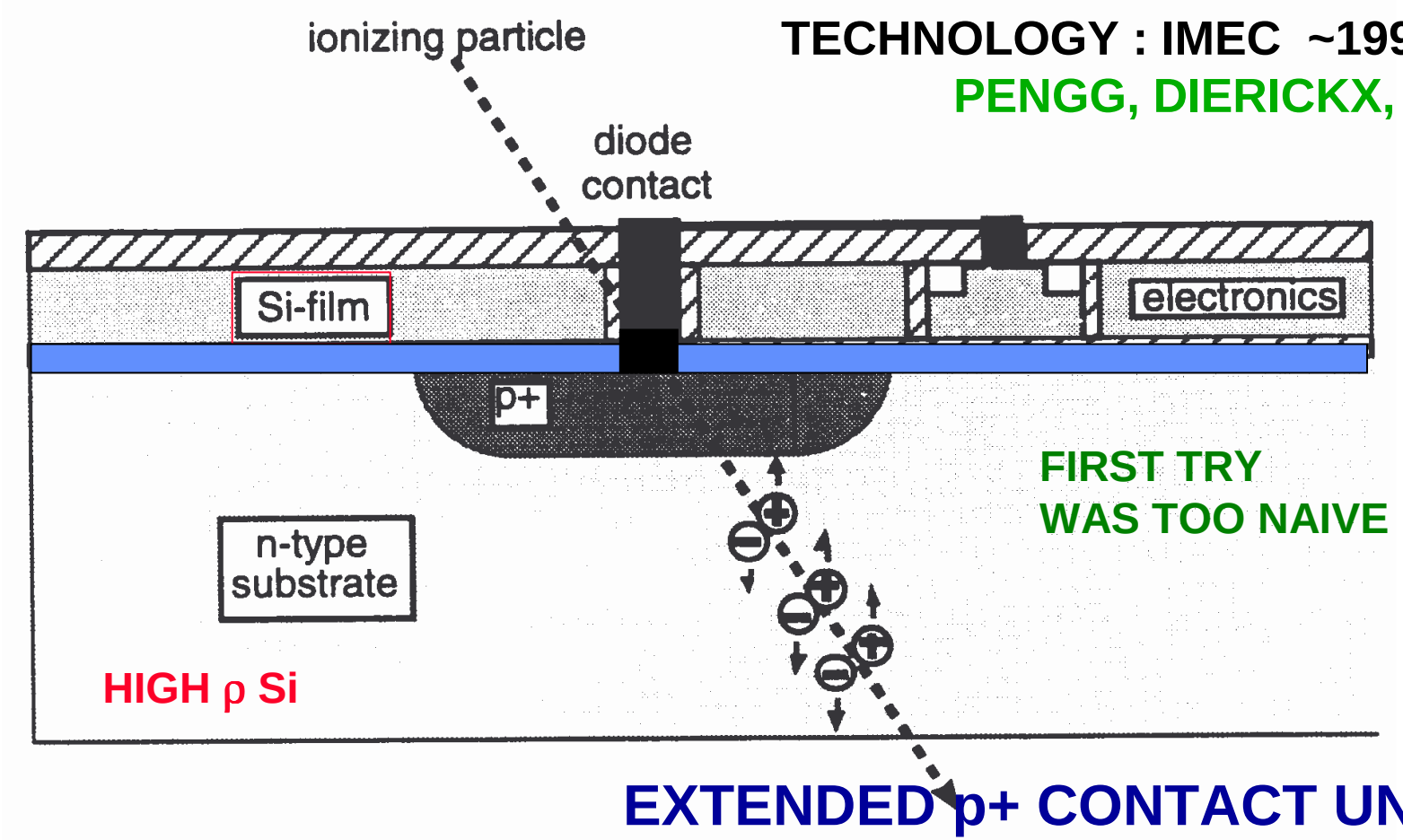
'RECENT' Si ACTIVITY at CERN

Erik HEIJNE CERN PH Department

Paris 29 November 2007

SOI on HR Si in RD19

SOI PIXEL DETECTORS



TECHNOLOGY : IMEC ~1992

PENGG, DIERICKX, BOSISIO, HEIJNE

BOX

FIRST TRY
WAS TOO NAIVE FOR MHz SPEED

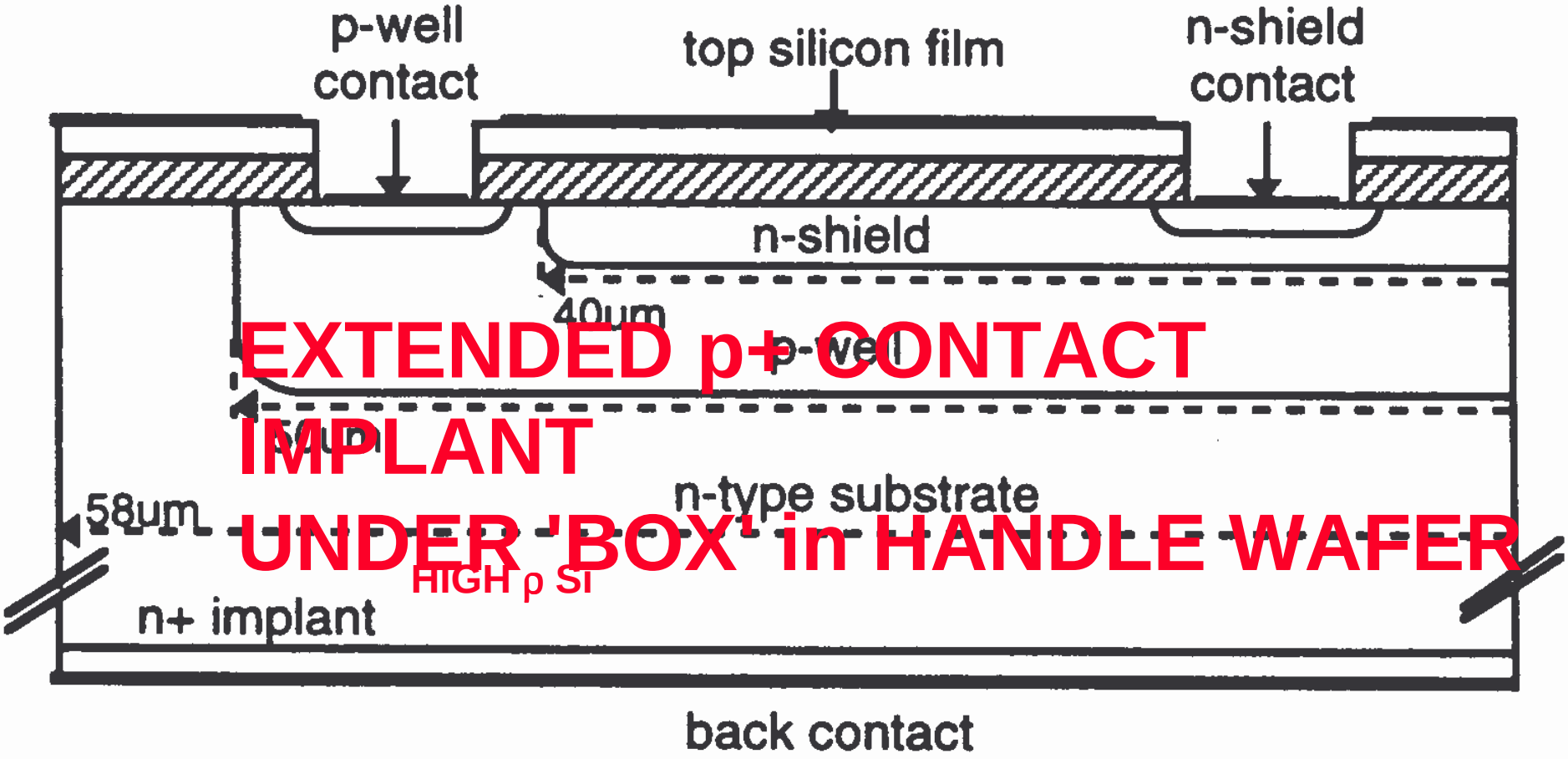
EXTENDED p+ CONTACT UNDER 'BOX'
in HANDLE WAFER

SOI PIXEL DETECTORS

MORE SOPHISTICATED DESIGN **CAREFU□L DESIGN for THERMAL BUDGET**

INCLUDES DEEP p-WELL 'COLLECTOR'

and THIN n+ SHIELDING **PENGG, DIERICKX, BOSISIO, HEIJN**



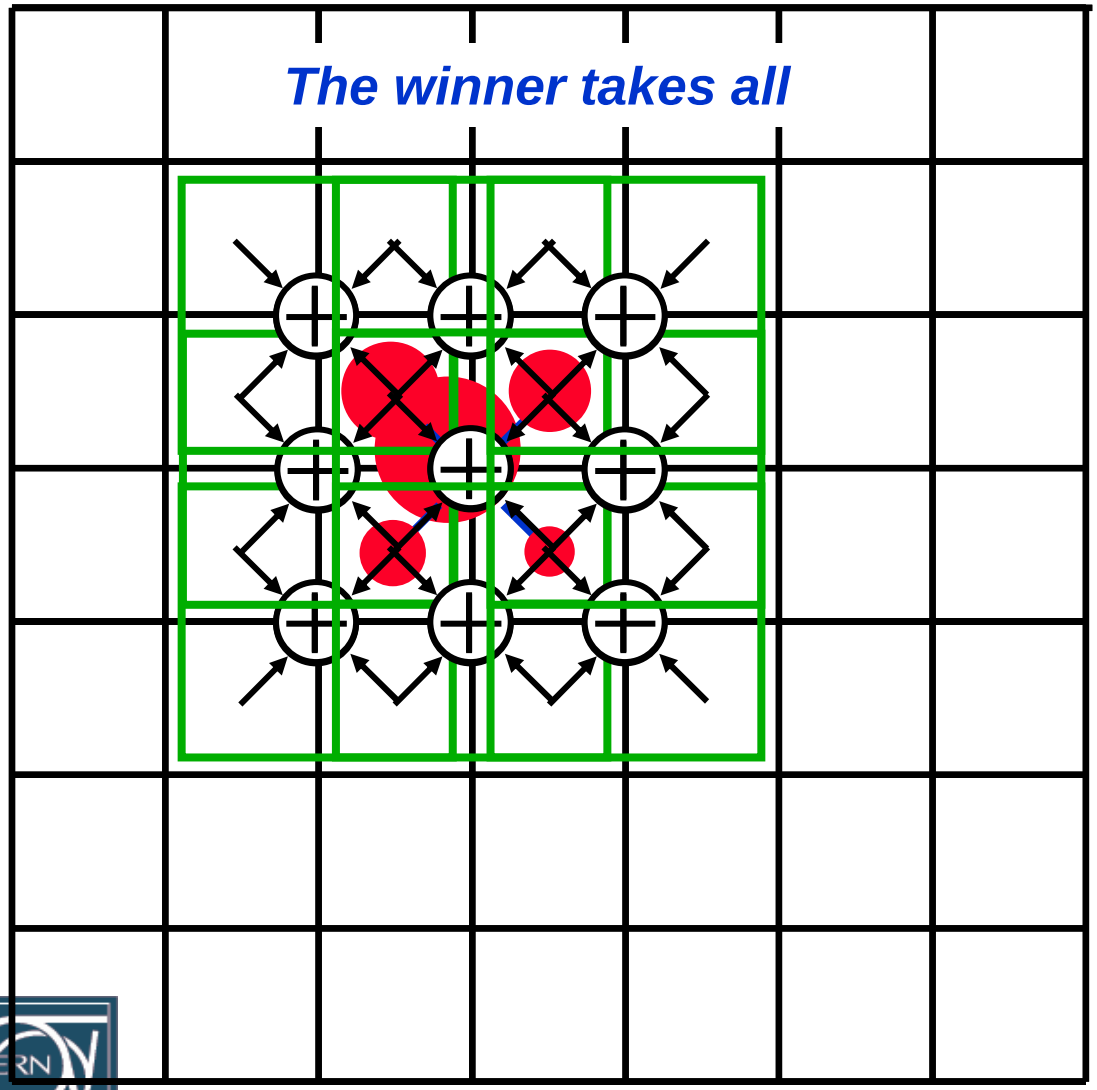
EXTENDED p+ CONTACT IMPLANT UNDER 'BOX' in HANDLE WAFER

HIGH ρ Si

COMPLEX SIGNAL PROCESSING

INCREASED FUNCTIONALITY
INTER-PIXEL COMMUNICATION
MEDIPIX3

Medipix3 – charge summing concept



- ***The incoming quantum is assigned as a single hit***

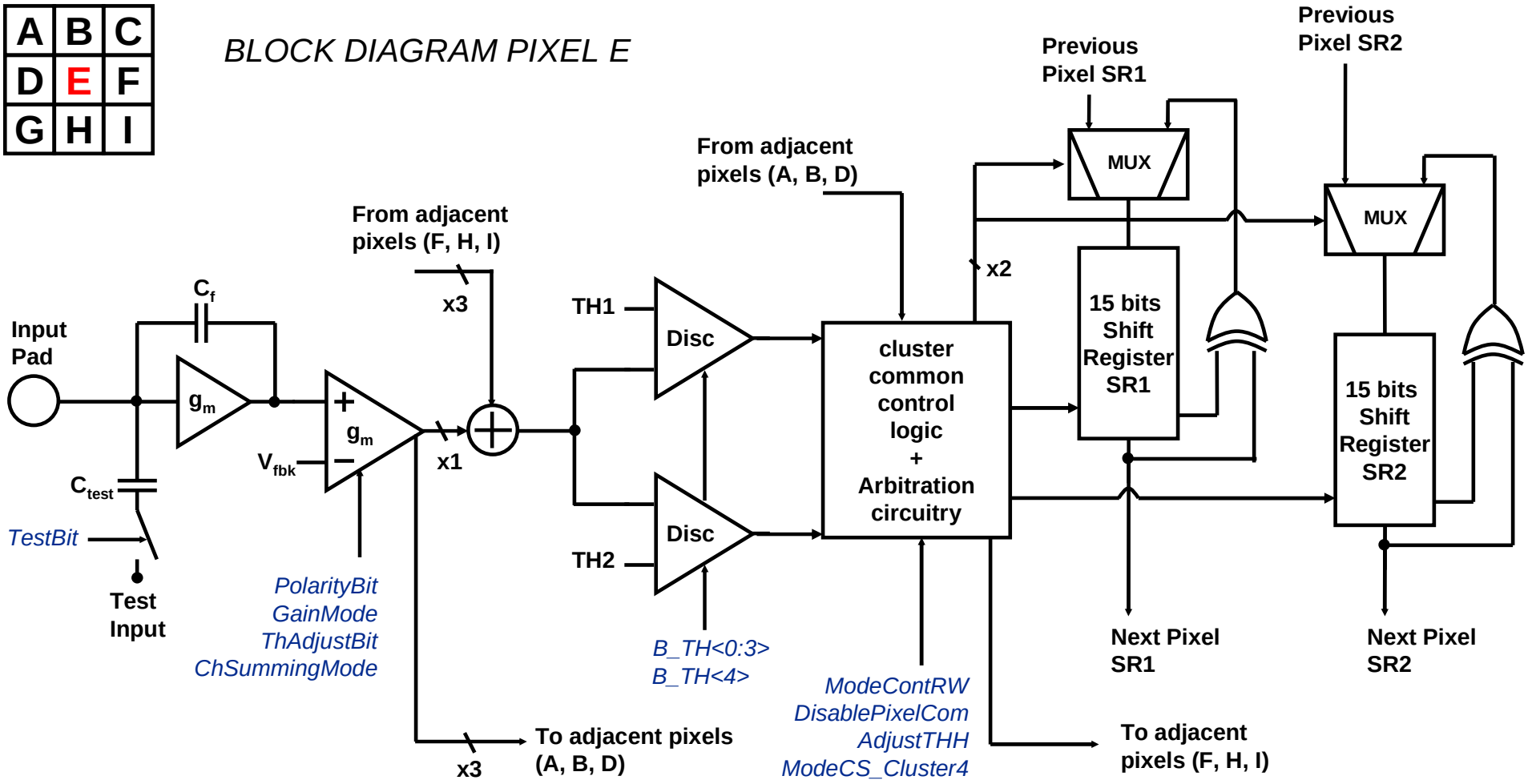
- ***Charge processed is summed in every 4 pixel cluster on an event-by-event basis***

Rafael BALLABRIGA
Michael CAMPBELL
Xavier LLOPART
Winnie WONG

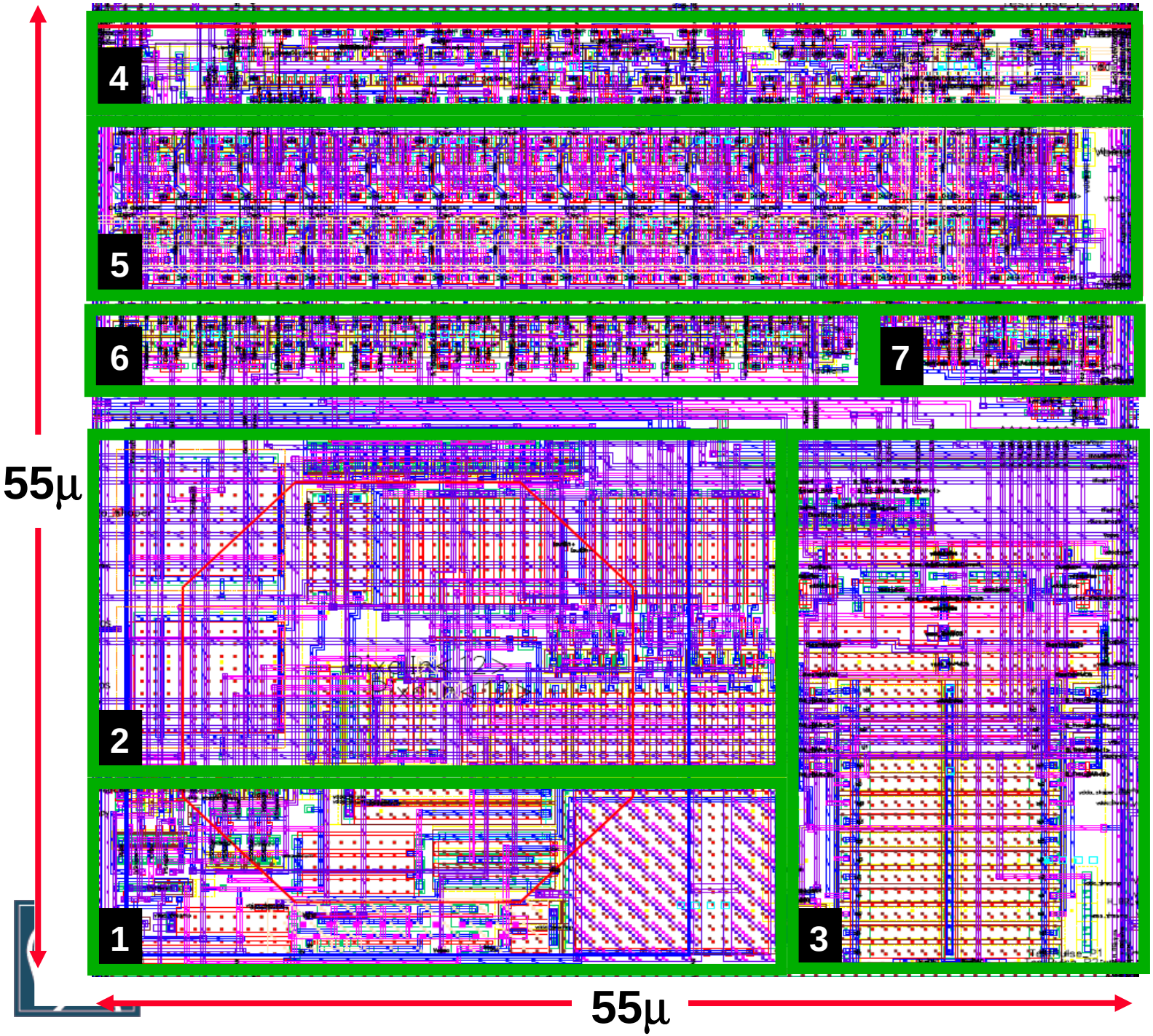
Medipix3 prototype – pixel block diagram

A	B	C
D	E	F
G	H	I

BLOCK DIAGRAM PIXEL E



ANALOG *DIGITAL*



DIGITAL CIRCUITRY

4. Control logic (124)
5. 2x15bit counters / shift registers (480)
6. Configuration latches (152)
7. Arbitration circuits (100)

Total digital 856

ANALOG CIRCUITRY

1. Preamplifier (24)
2. Shaper (134)
3. Discriminators and Threshold Adjustment Circuits (72)

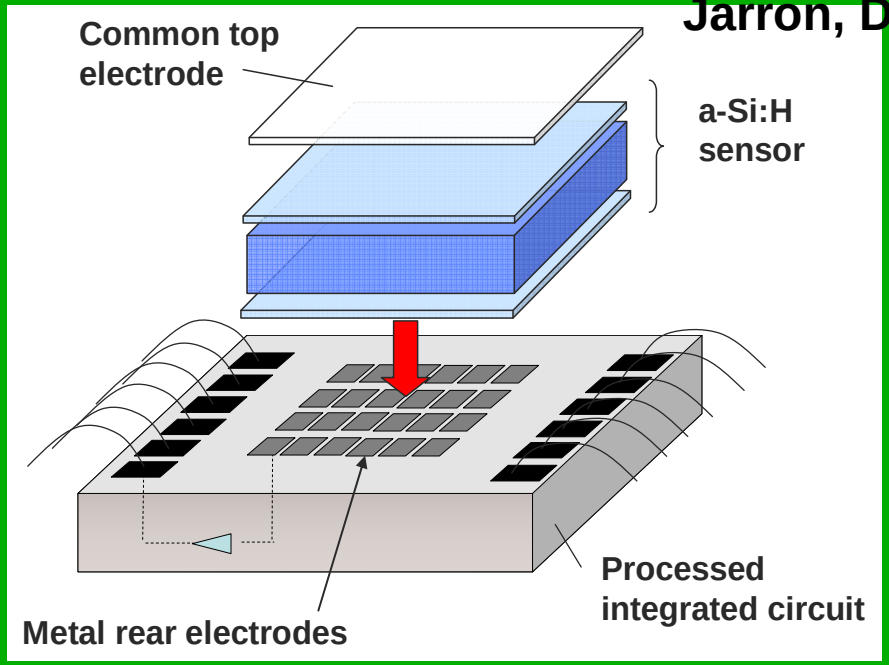
Total analog 230

Rafael BALLABRIGA

STACKING of HYBRID SENSORS + CHIPS

Si, α-Si, MCP, GAS,...

α-Si THIN FILM on ASIC (TFA)



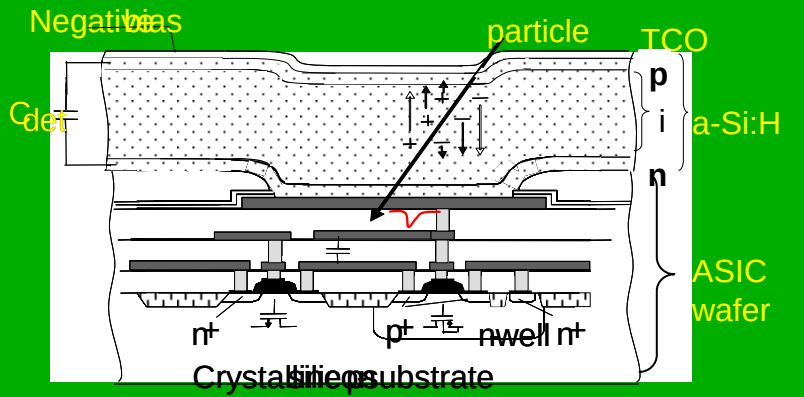
Jarron, Despeisse,..

Institute of Micro-Technology in Neuchatel

Deposition of hydrogenated amorphous silicon on ASIC

Very High Frequency Plasma Enhanced Chemical Vapor Deposition (VHF - PECVD)

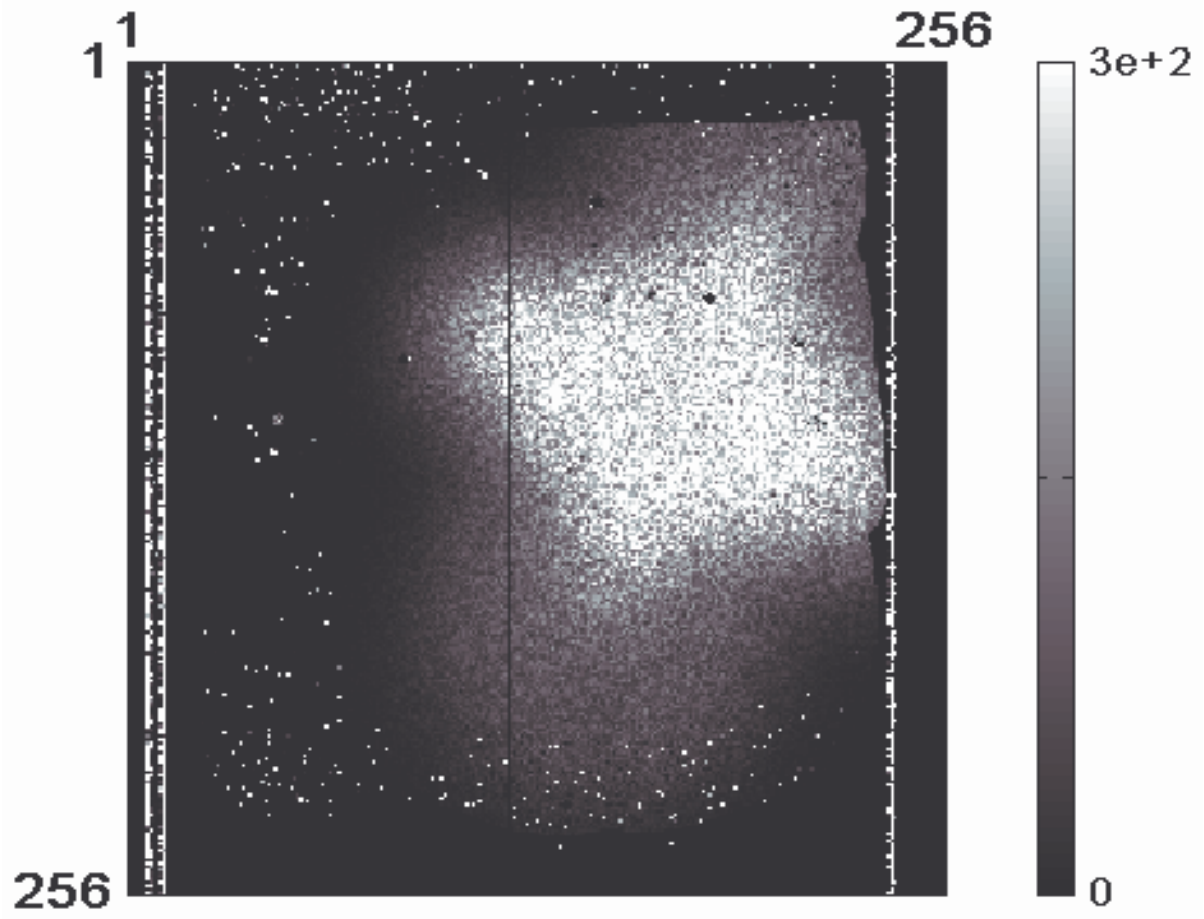
Micromorph module production at UNAXIS



large-volume, low-cost manufacturing of thin-film silicon PV modules

KAI simultaneous coating of 20 glass plates of 1.4 m² each

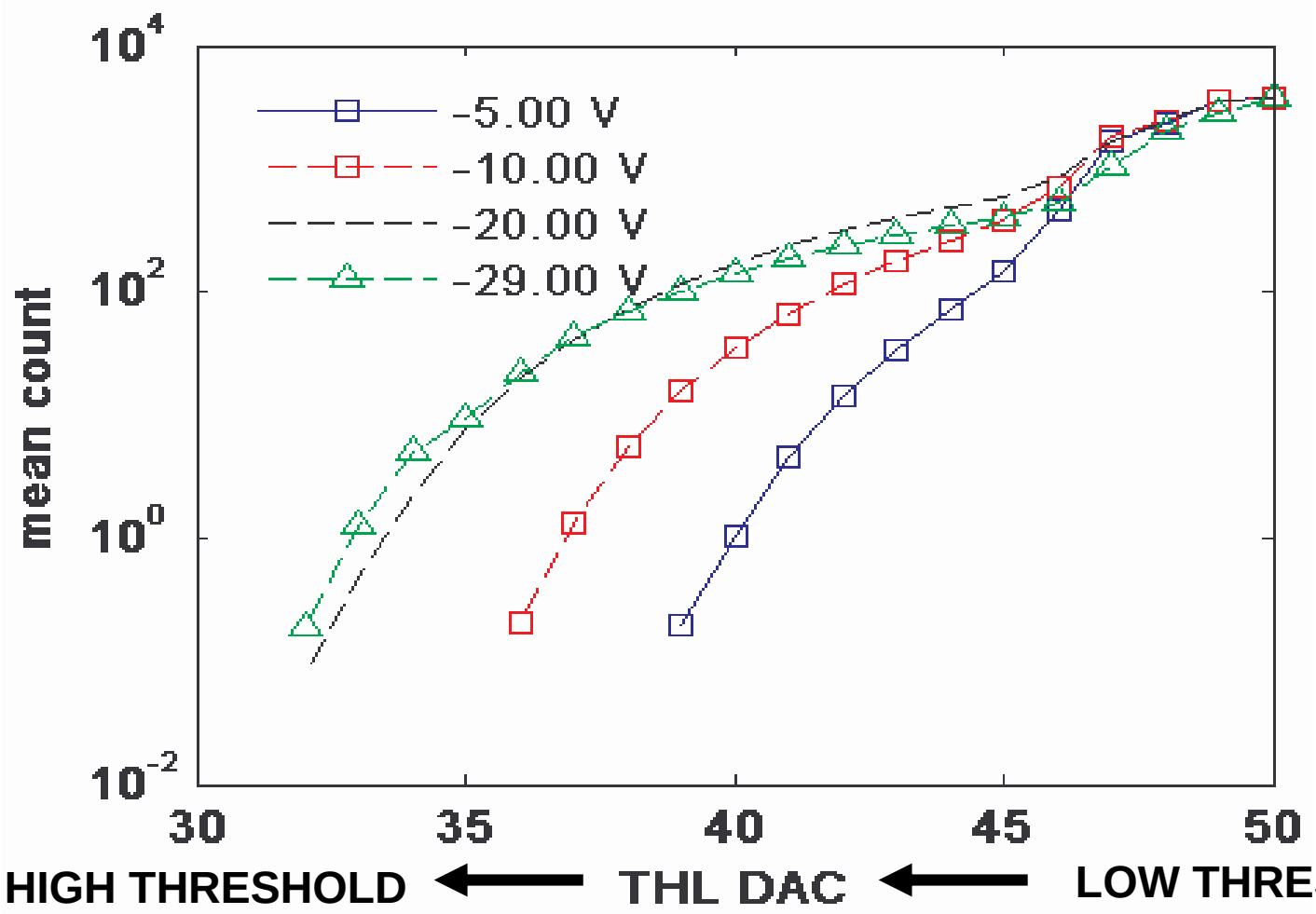
Medipix2 with amorphous Si



Pierre JARRON
Lukas TLUSTOS
Danielle MORAES
Matthieu DESPEISSE

Image with 20 keV electrons (Class D chip)
No bump bonding, 'evaporated' α Si
Si layer thickness ~ 5 μm

Threshold scan 20 keV electrons in a - Si

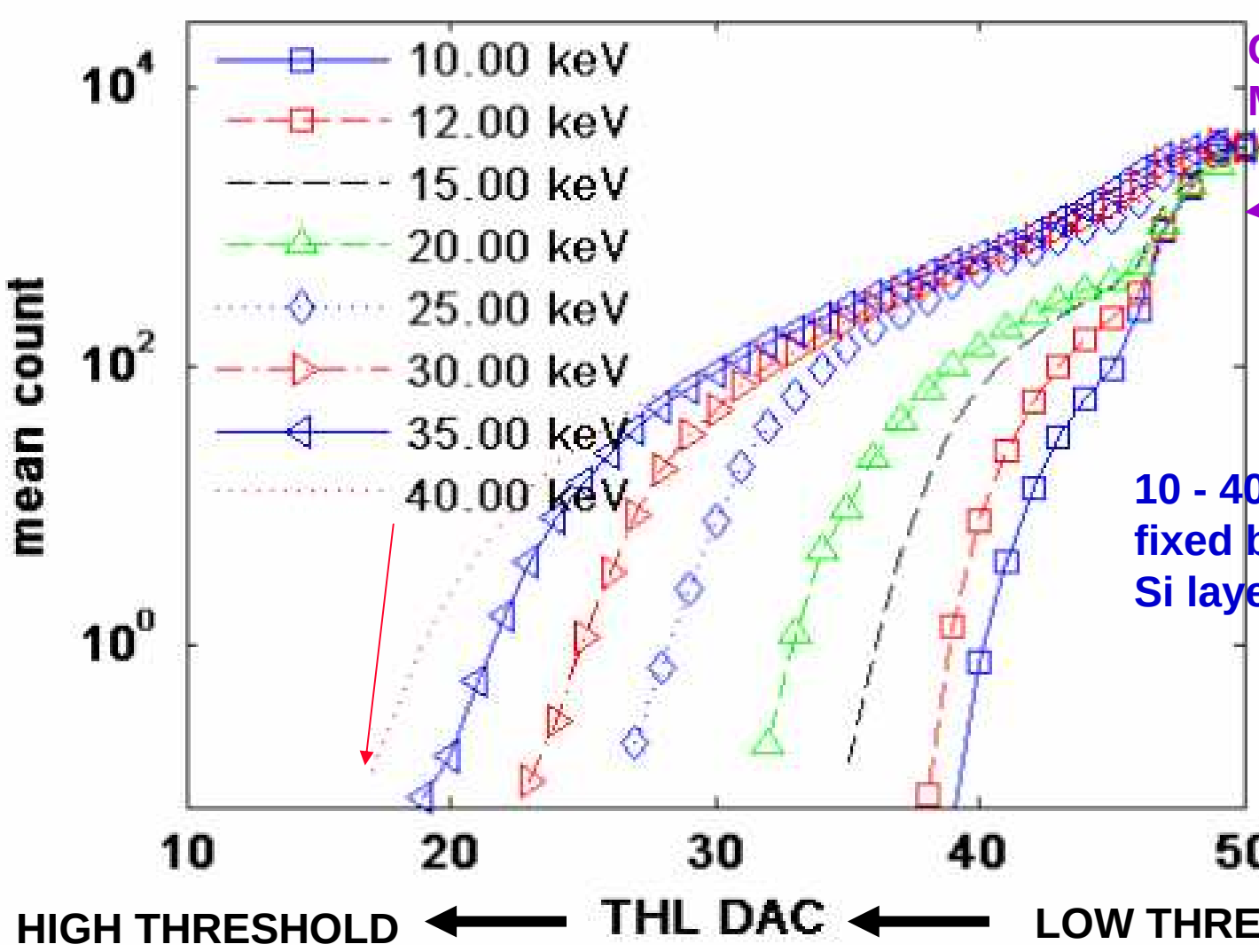


SINGLE ELECTRONS ARE COUNTED in EACH PIXEL

SIGNAL SATURATES ~ 29 V BIAS

Pierre JARRON
Lukas TLUSTOS
Danielle MORAES
Matthieu DESPEISSE

ELECTRON SIGNAL a- Si vs keV ENERGY

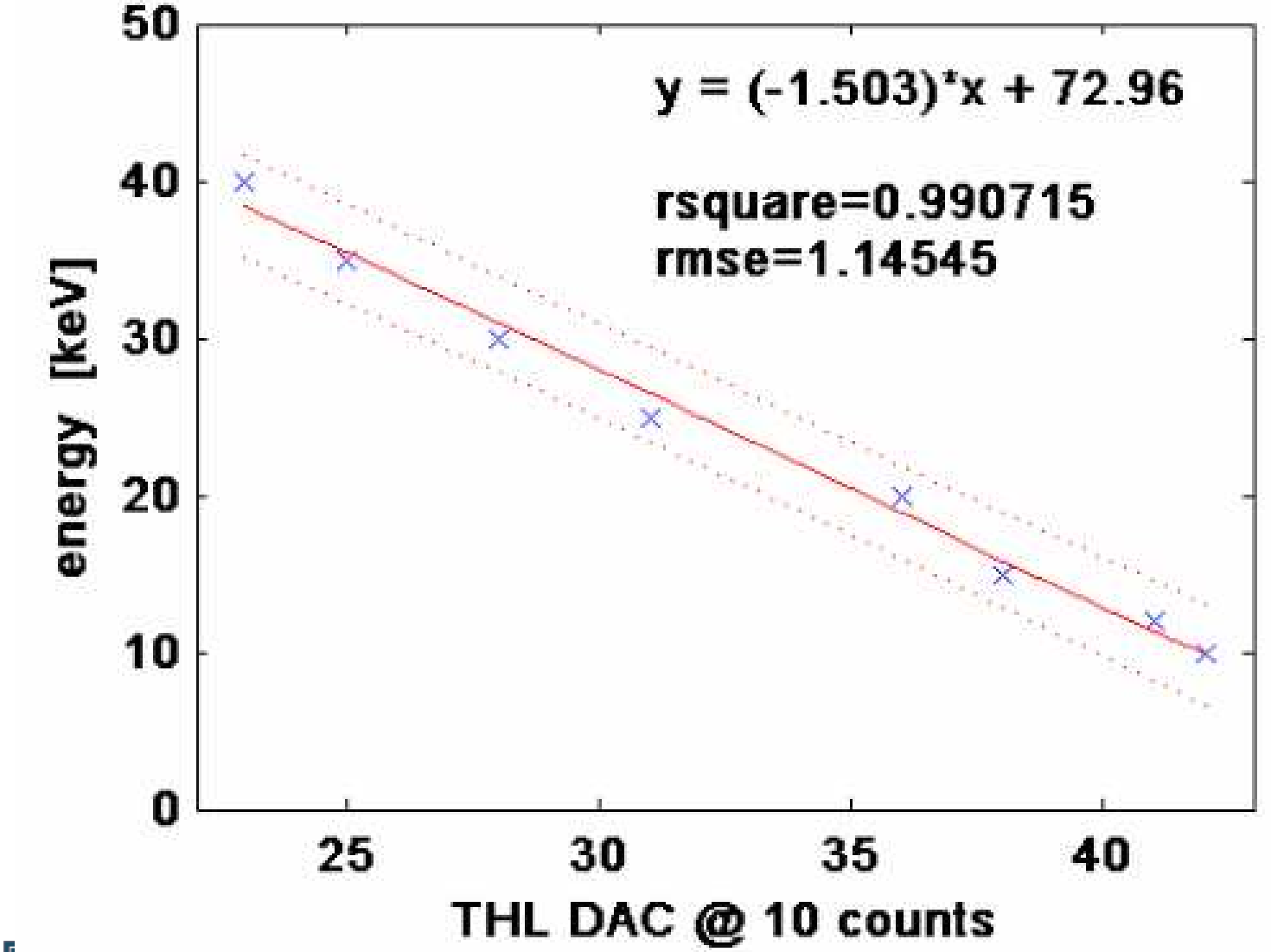


CHARGE SHARING
MULTIPLE COUNTS

10 - 40 keV electrons
fixed beam rate setting
Si layer thickness ~ 5 μm

Lukas TLUSTOS
Danielle MORAES

ENERGY vs THRESHOLD a - Si



MCP

VISIBLE PHOTONS

Visible Photon Imaging

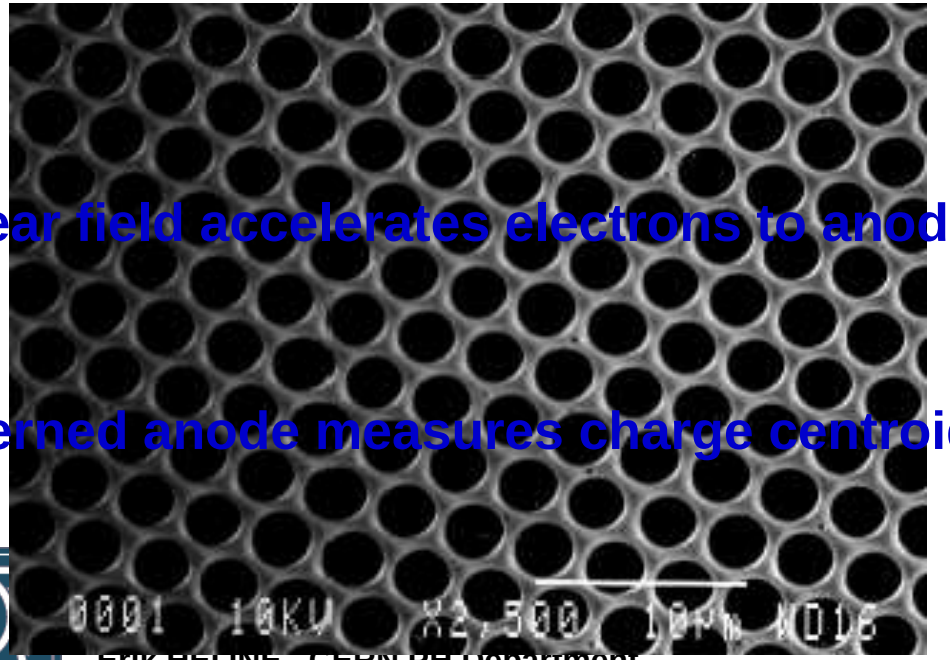
John VALLERGA LBL
+ MEDIPIX COLLABORATION

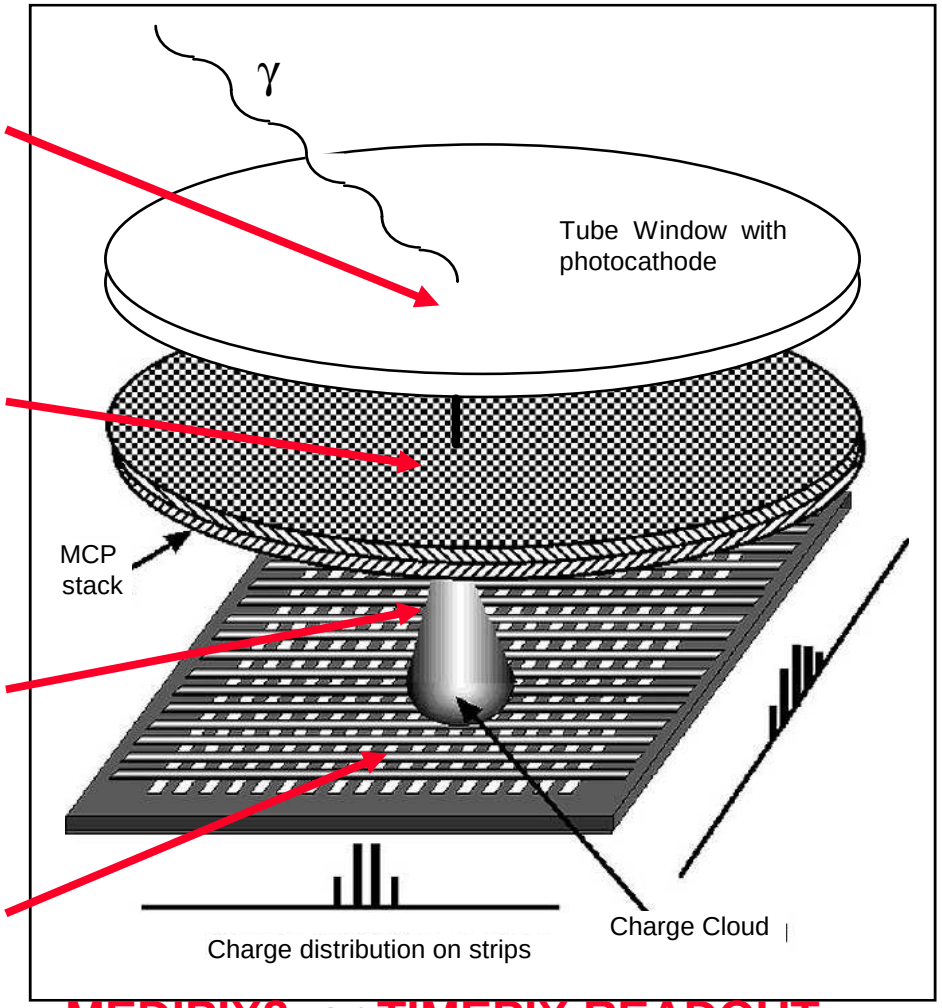
Photocathode converts photon to electron

MCP(s) amplify electron by 10^4 to 10^8

Rear field accelerates electrons to anode

Patterned anode measures charge centroid





MEDIPIX2 or TIMEPIX READOUT
NOW kHz FRAMES DAQ from ESRF

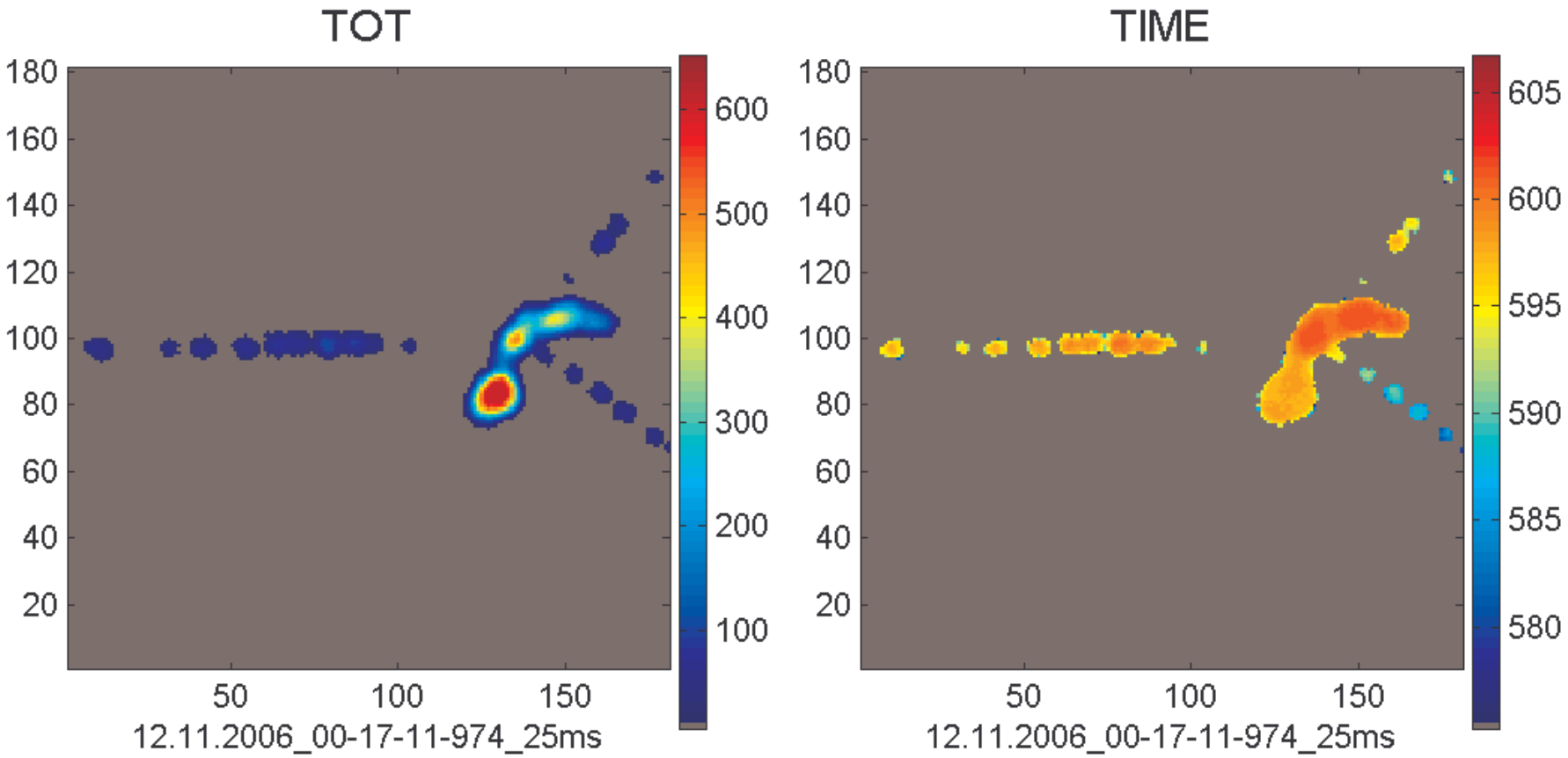
GAS MULTIPLICATION ABOVE PIXEL CHIP

TIMEPIX

Timepix with 3-GEM detector

MPXR CHIP MODIFICATION Xavier LLOPART (CERN), idea J. VISSCHERS (NIKHEF)

DESY testbeam in November 2006
(A.Bamberger, U. Renz, M.Titov)



Timepix with Micromegas

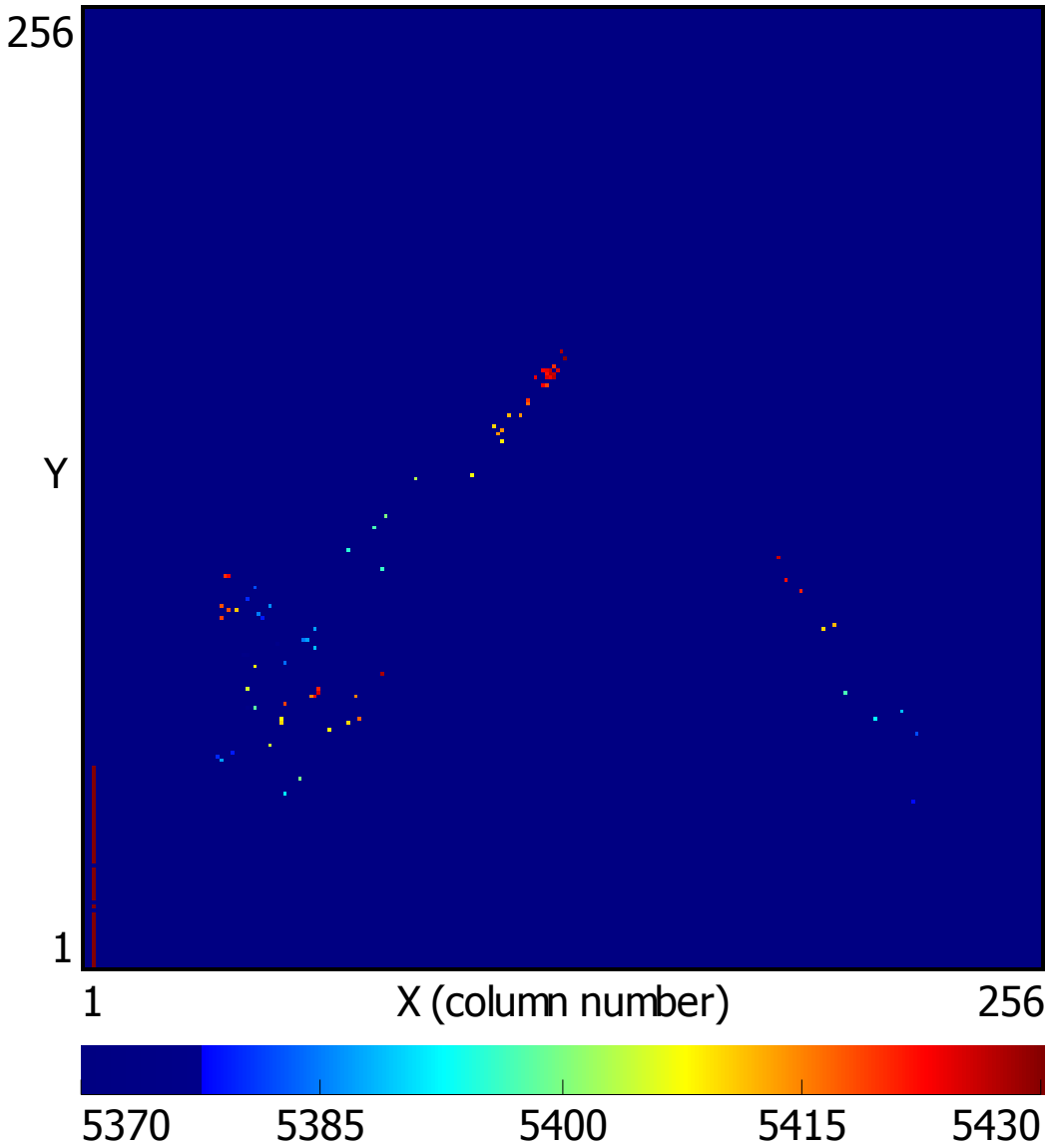
January 2007

Nikhef + Saclay

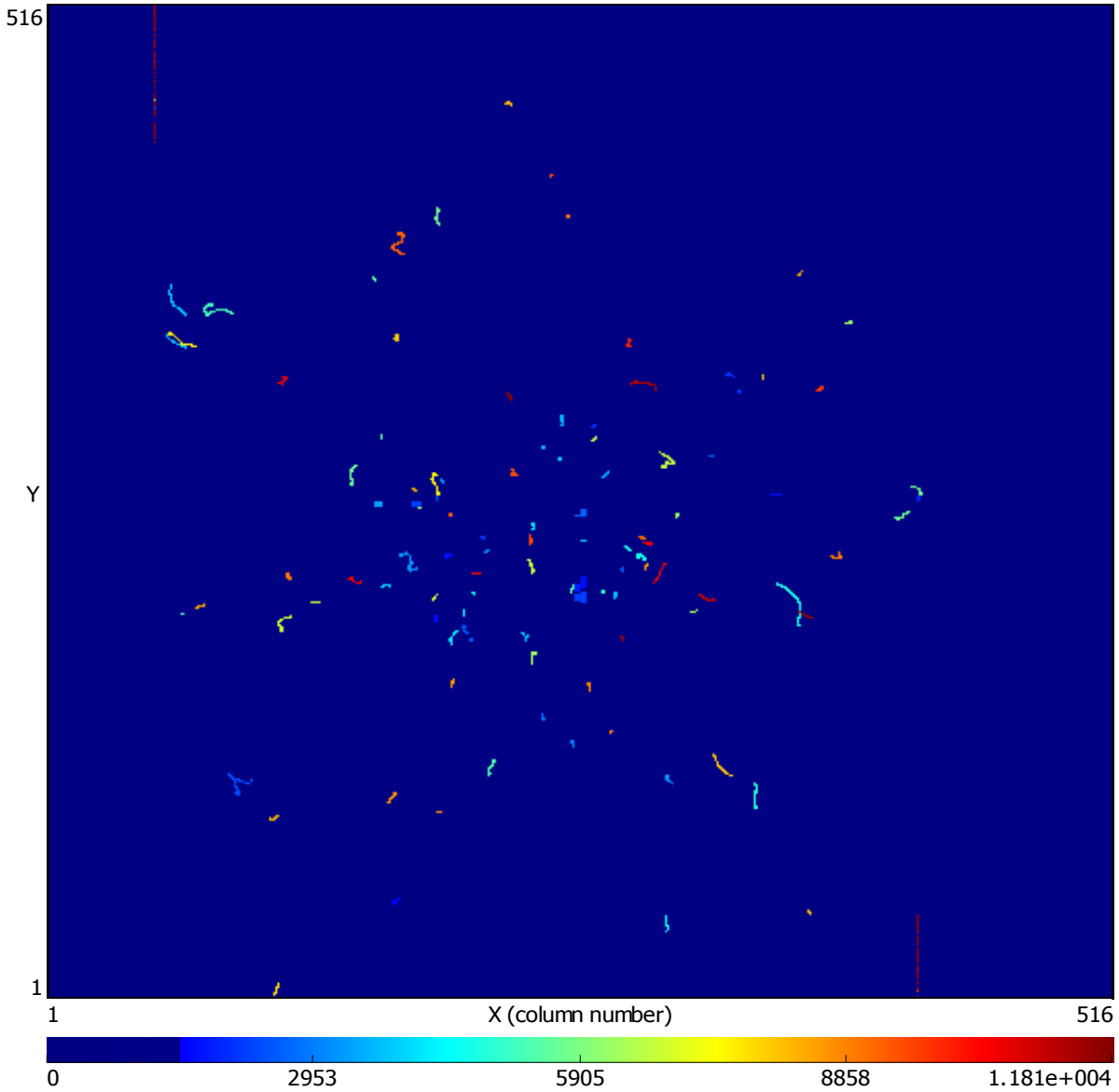
Jan Timmermans

Harry van de Graaf

TIME of ARRIVAL on CHIP of ELECTRON in GAS



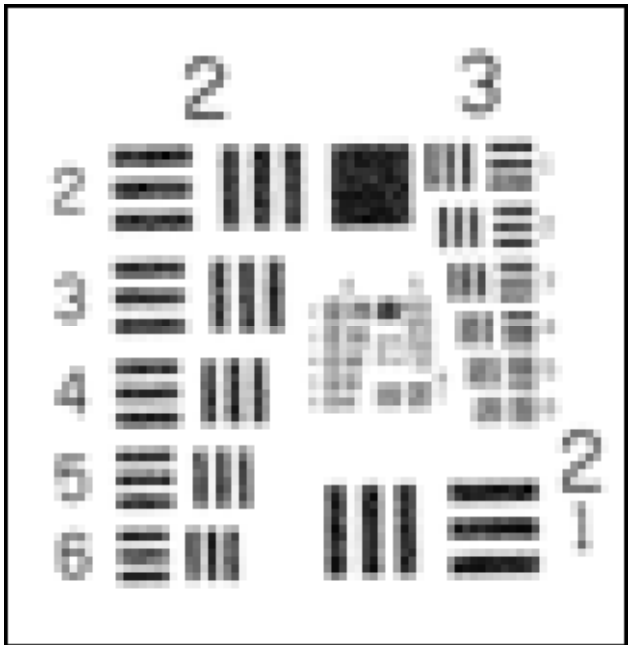
TIMEPIX QUAD Si Arrival Time electrons ^{90}Sr



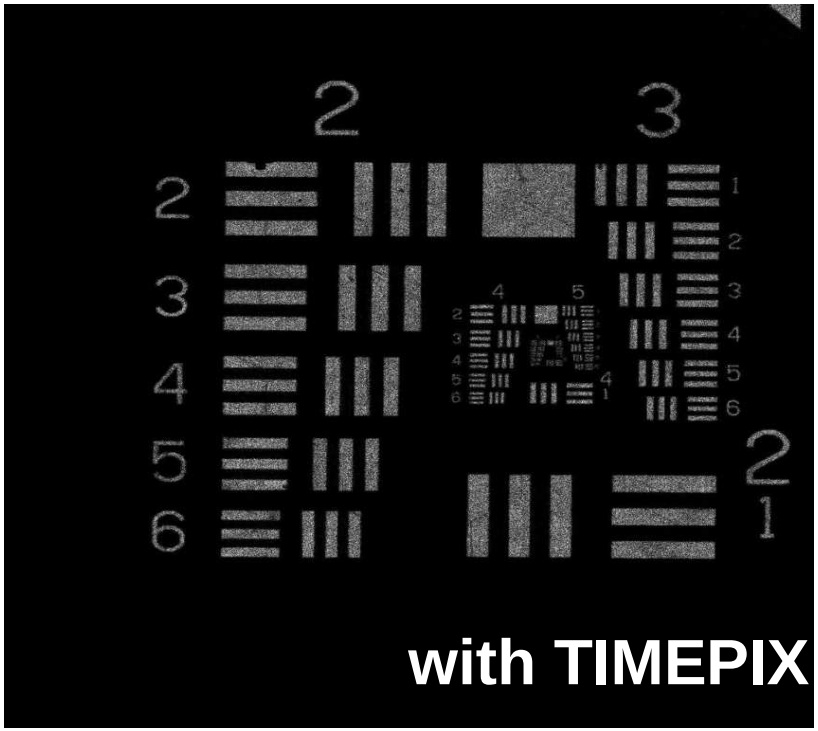
Visible imaging - Sub-Pixel Resolution

John VALLERGA LBL
+ MEDIPIX COLLABORATION

sub-pixel resolution with analog cluster centroiding algorithm



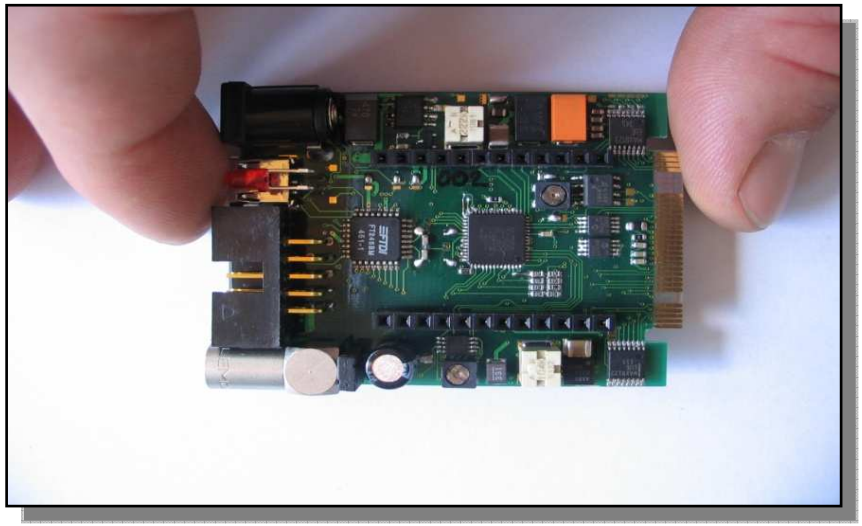
Theoretical pixel resolution 9 lp/mm (55 μm).

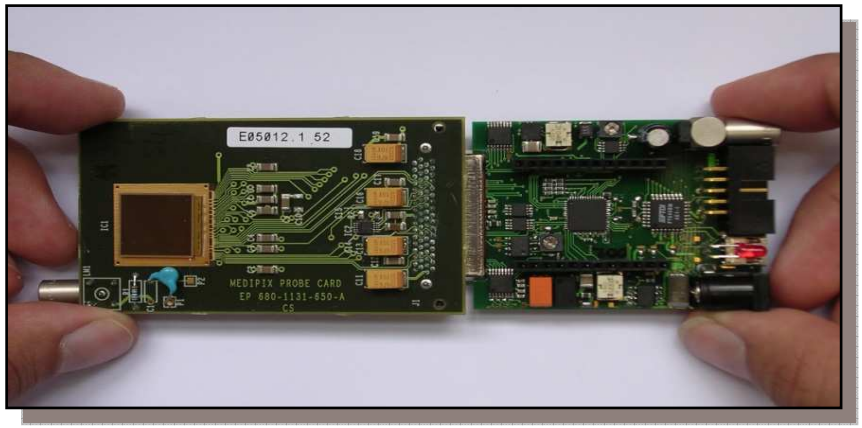


AirForce 5-6 pattern resolved corresponding to 57 lp/mm (8.8 μm).

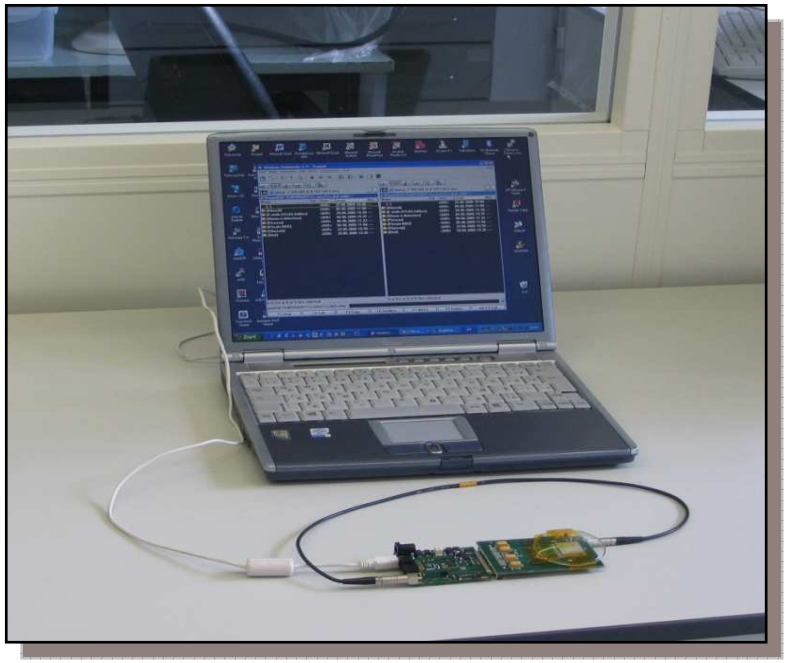
MINIATURIZATION
PACKAGING
STACKING
SYSTEM

USB based Medipix2 Readout System





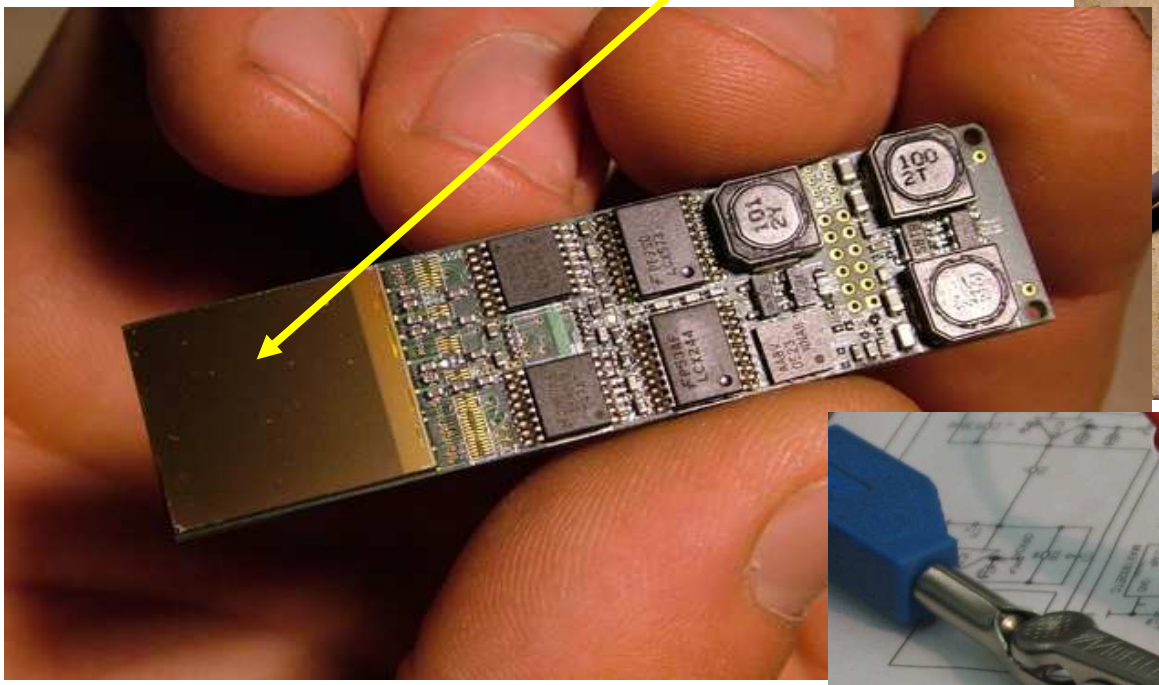
USB1 compatible
Includes Pixelman readout software
Developed by S. Pospisil et al. CTU, Prague

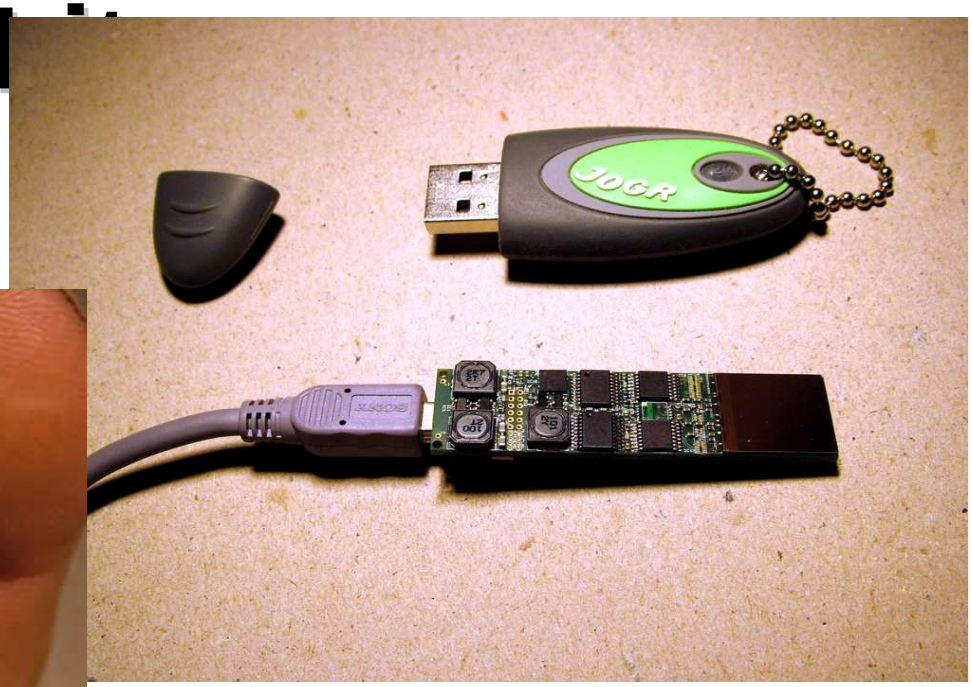


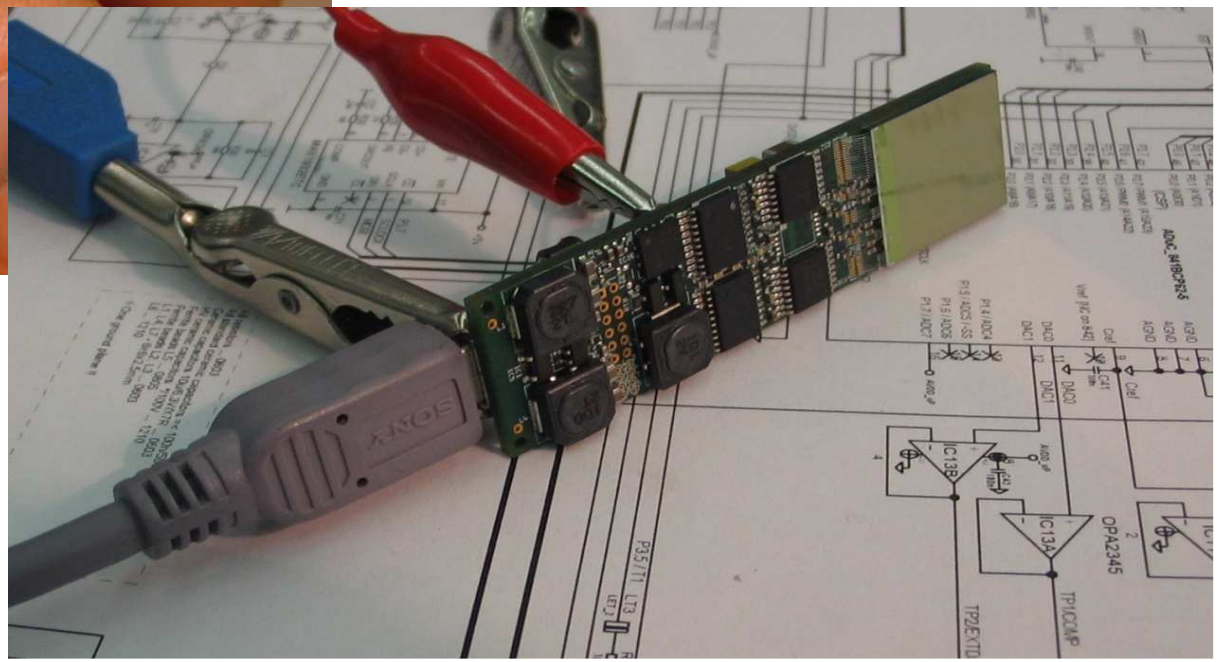
MEDIPIX USB

with hybrid, bonded bare chip

APPLY MINIATURIZATION in PHYSICS !!!!!







CTU Prag

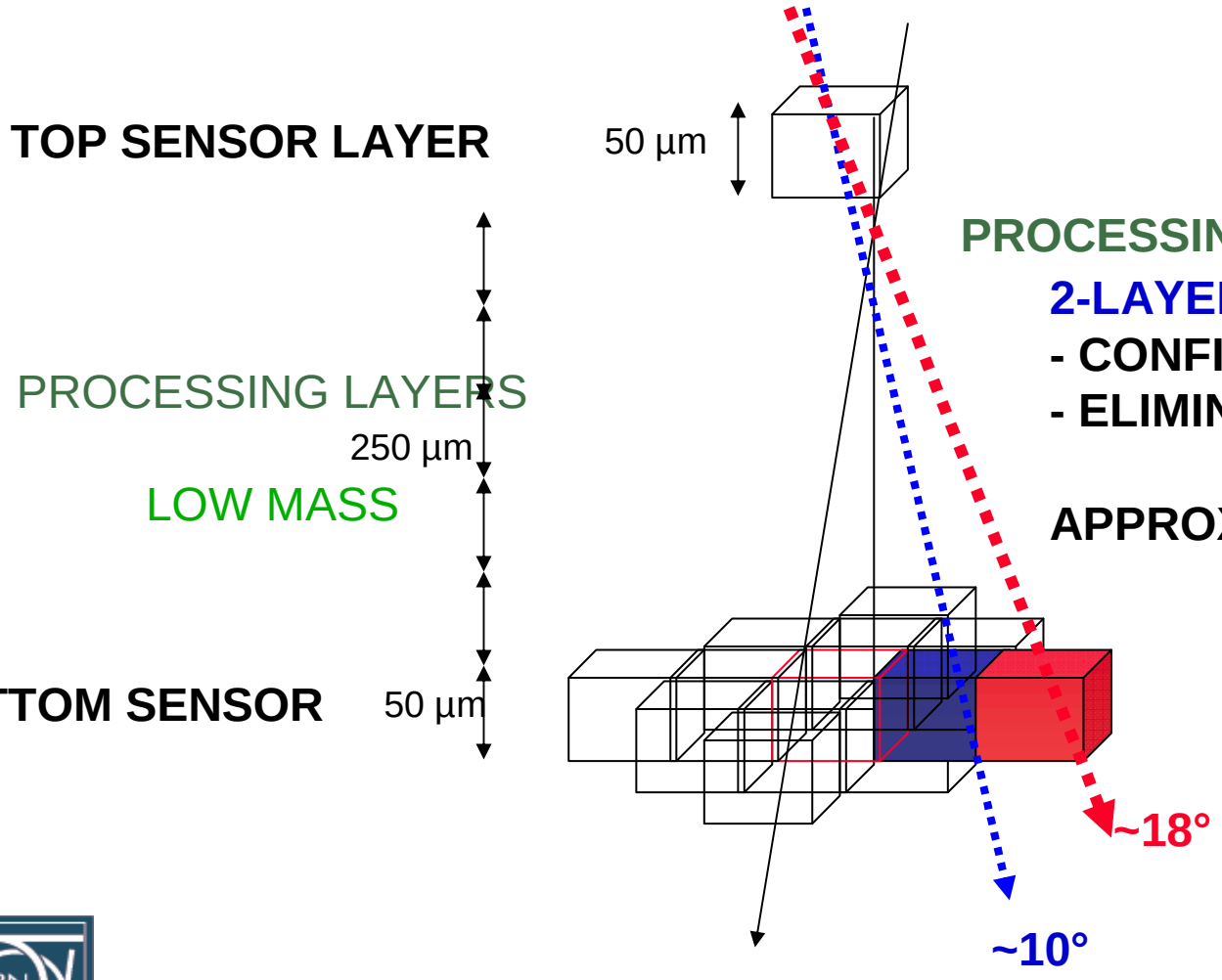
Erik HEIJNE CERN PH Department

STACKING
THIN CELLS

50 um CUBES

SMALLER PIXELS

50 x 50 x 50 µm → SIGNALS ~ 3500 e^-



PROCESSING BETWEEN SENSORS

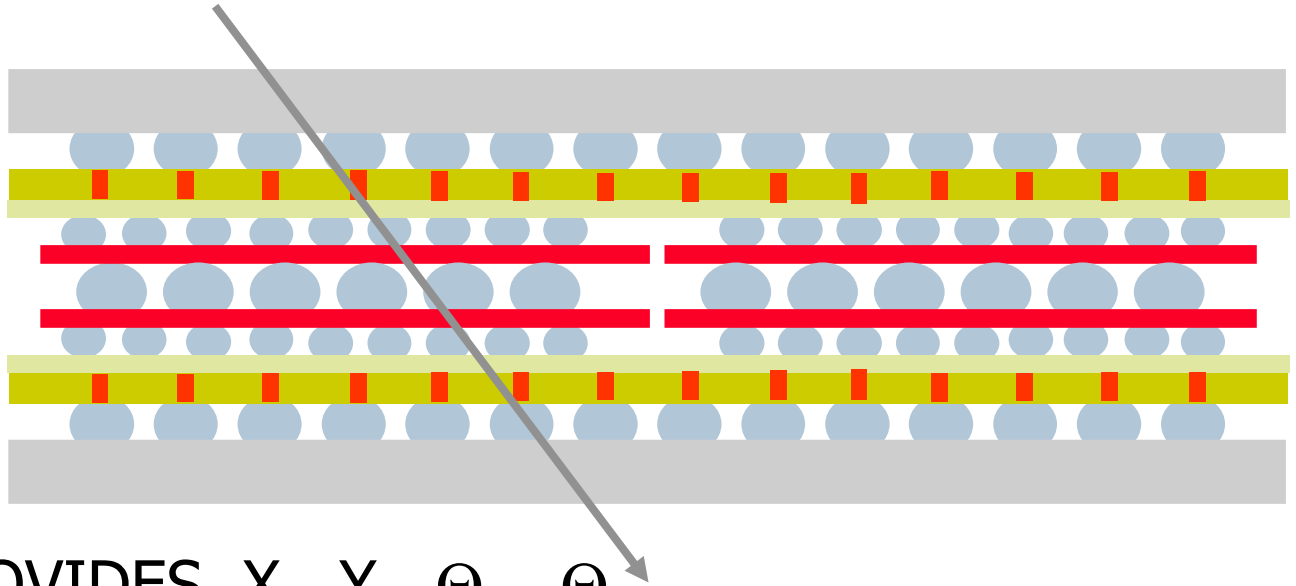
2-LAYER COINCIDENCE :

- **CONFIRMS TRACK STUB**
- **ELIMINATES PHOTON HIT, NOISE**

APPROXIMATE VECTOR

TRACK VECTOR DETECTOR

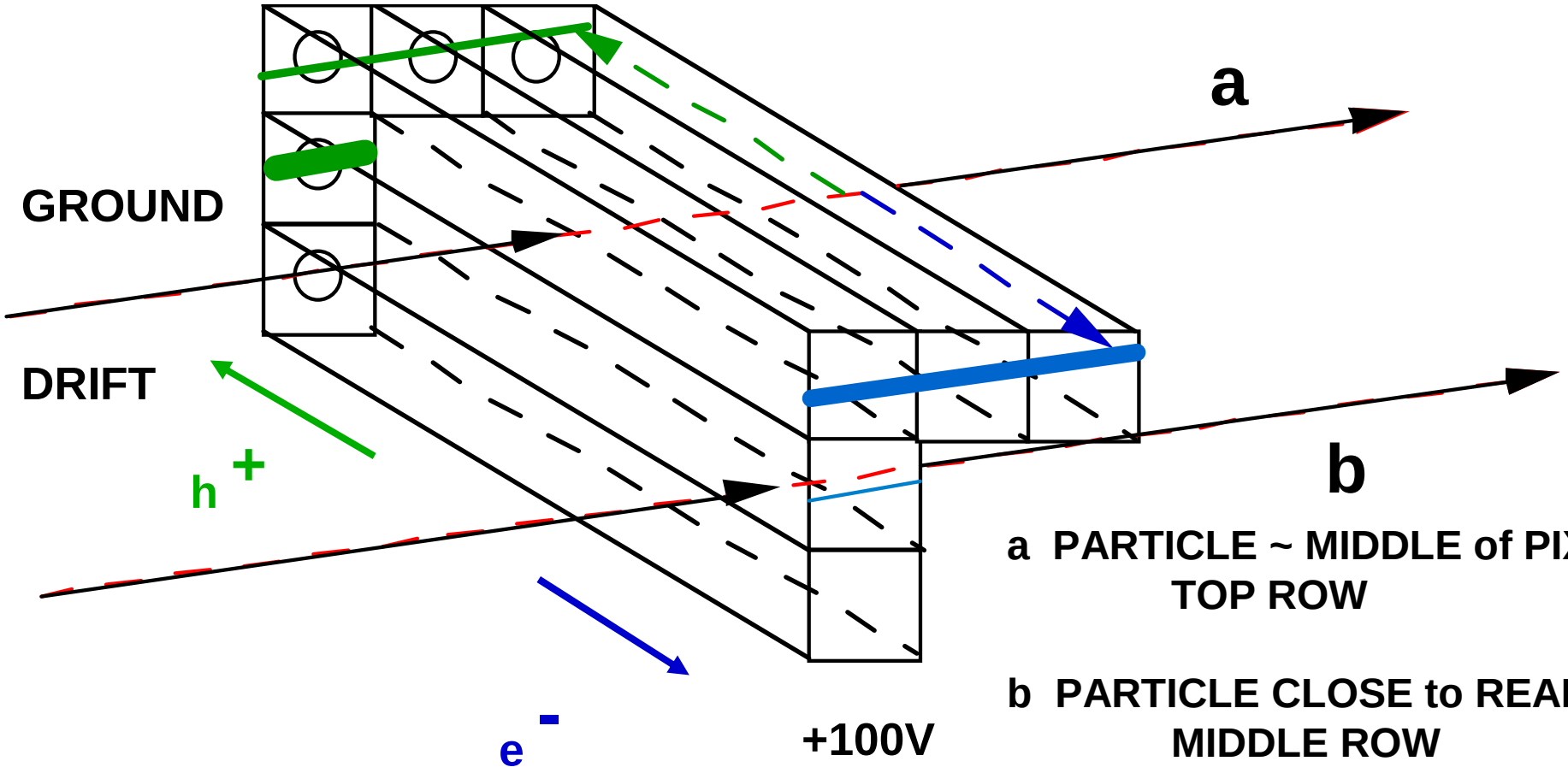
3D MULTILAYER ASSEMBLY



PROVIDES X , Y , Θ_X , Θ_Y

intersecting position + angular direction

CHARGE COLLECTION & LATERAL DIFFUSION



a PARTICLE ~ MIDDLE of PIXELS TOP ROW

b PARTICLE CLOSE to REAR MIDDLE ROW

TRY with Si MEDIPIX

DIFFUSION width shown EXAGGERATED

TIMEPIX as SILICON 'EMULSION'

256 'STACKED' Si CELLS

H6 PION BEAM 2007

INCIDENT from RIGHT

BEAM 

QuickTime™ and a
TIFF (Uncompressed) decompressor
are needed to see this picture.

Erik HEIJNE
Dominic GREIFFENBERG
John IDARRAGA - ANALYSIS

MEASUREMENTS with MIPs in Si TIMEPIX (2007)

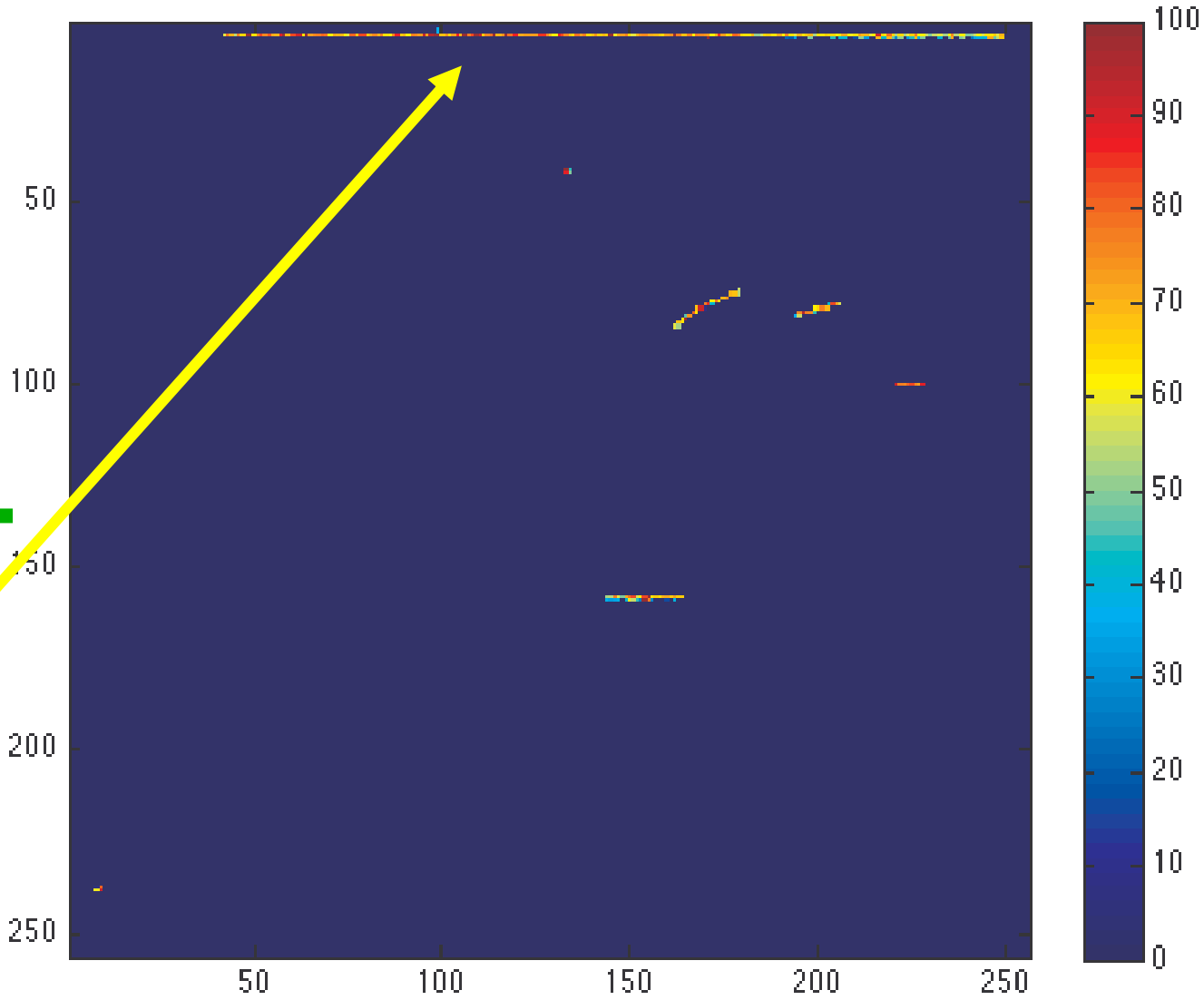
MUONS
H6 in EHN1

June 2007

INCIDENT from RIGHT

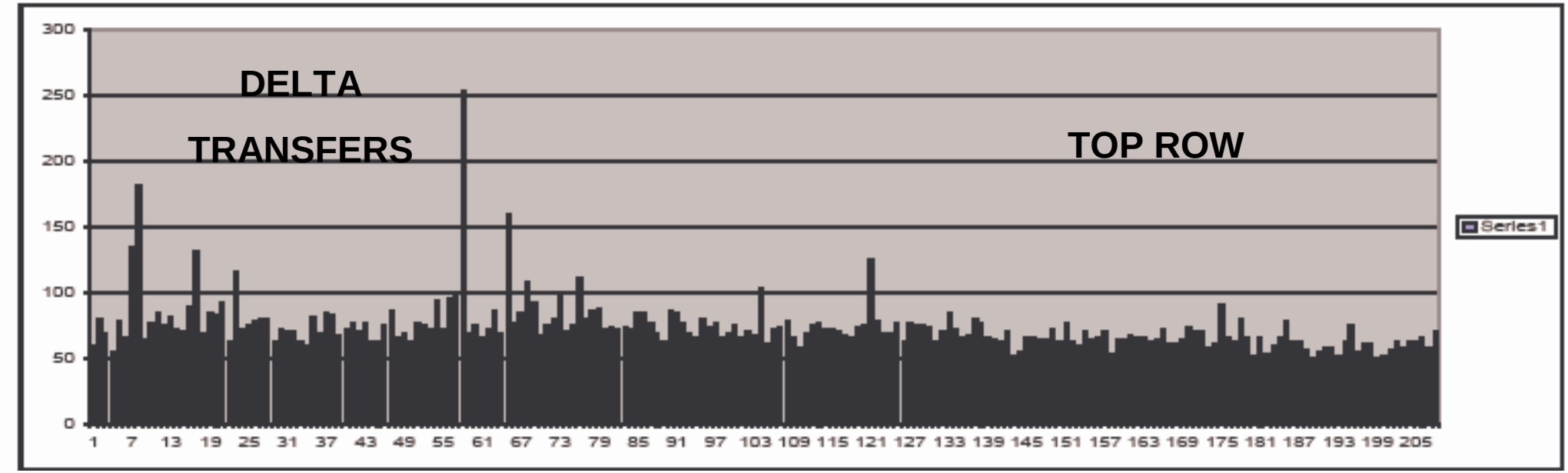
BEAM

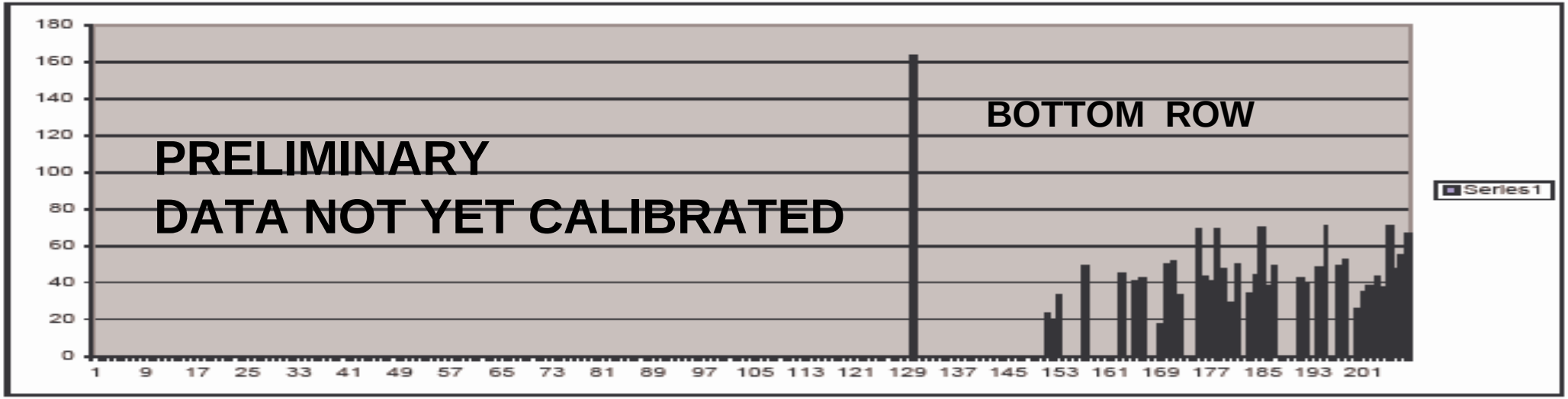
ANALYZED TRAIL



JOHN IDARRAGA
DOMINIC GREIFFENBERG
ERIK HEIJNE

TRAIL ANALYSIS FRAME 29853





MAJOR OPPORTUNITIES

THIN SILICON for CMOS and for SENSORS

LOW NOISE NEEDED < 80 e^- rms

THIN SENSORS MORE RADHARD ?

3D SPACE POINTS 50 or 40 um cubes ?

TRIGGER FUNCTIONS with STACKED LAYERS

ENHANCED FUNCTIONALITY on SMALL AREA

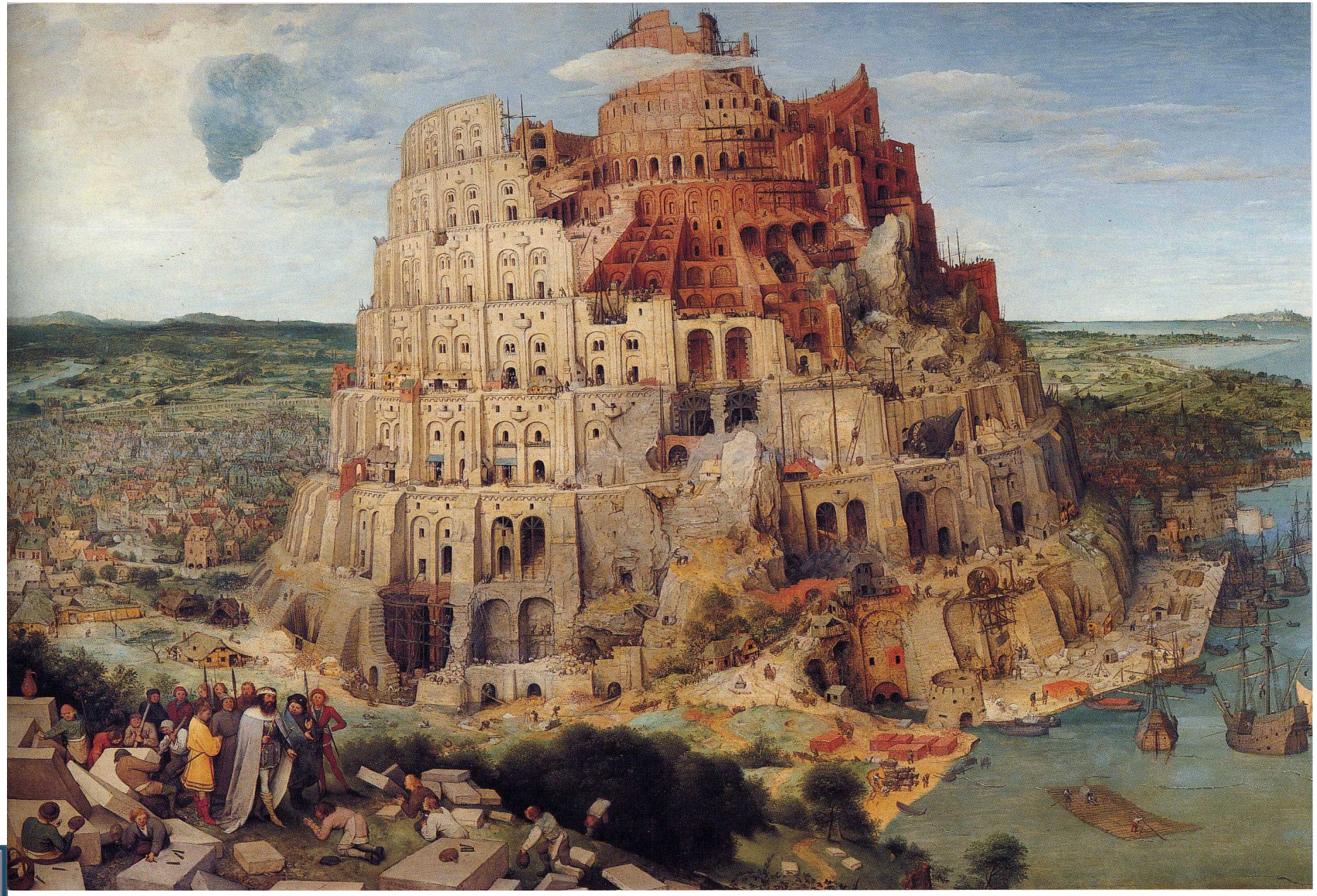
TRACK VECTORS + SELECTIVITY on STIFF TRACKS

WHICH NEW PHYSICS CAN BE DONE WITH THIS ?

INTRODUCTION of Si MICROSTRIP TECHNOLOGY
ALLOWED STUDY of CHARM and BEAUTY

THE END

AMBITIOUS MULTI-LAYER STRUCTURE

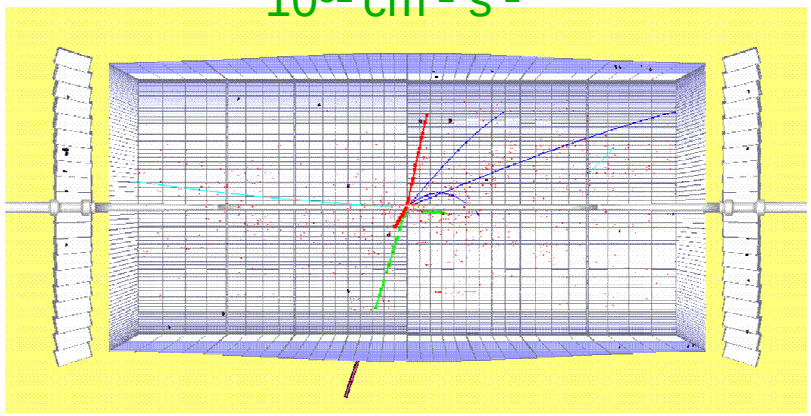



CERN

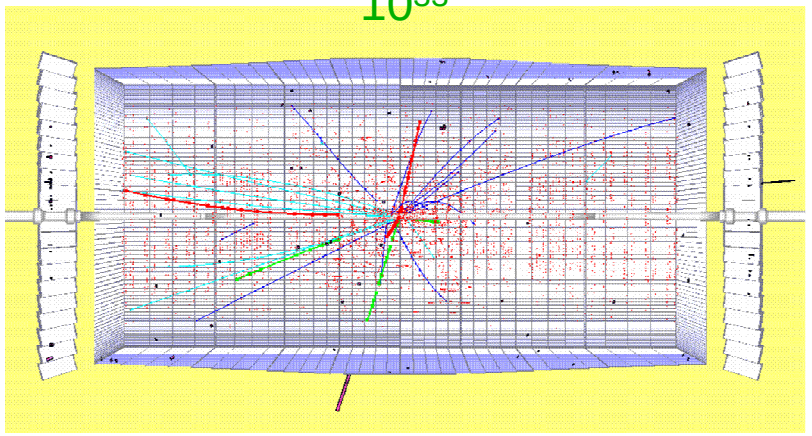
ADDITIONAL SLIDES

CMS from LHC to SLHC

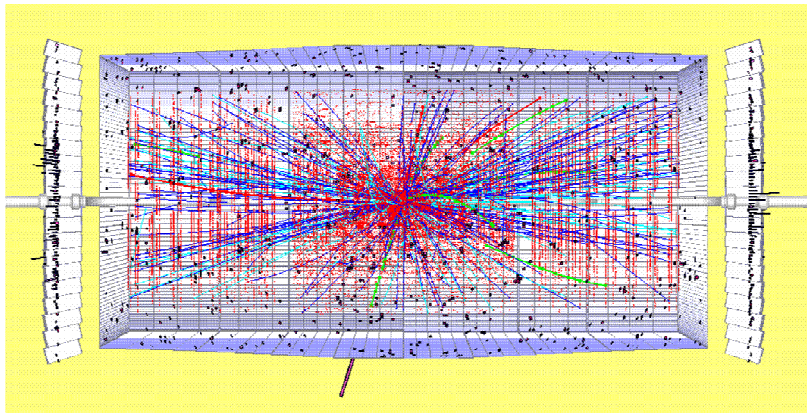
10^{32} cm^{-2} s^{-1}



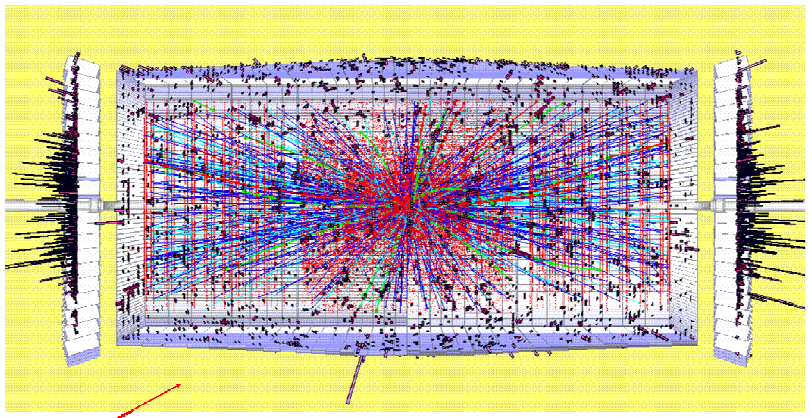
10^{33}



10^{34}



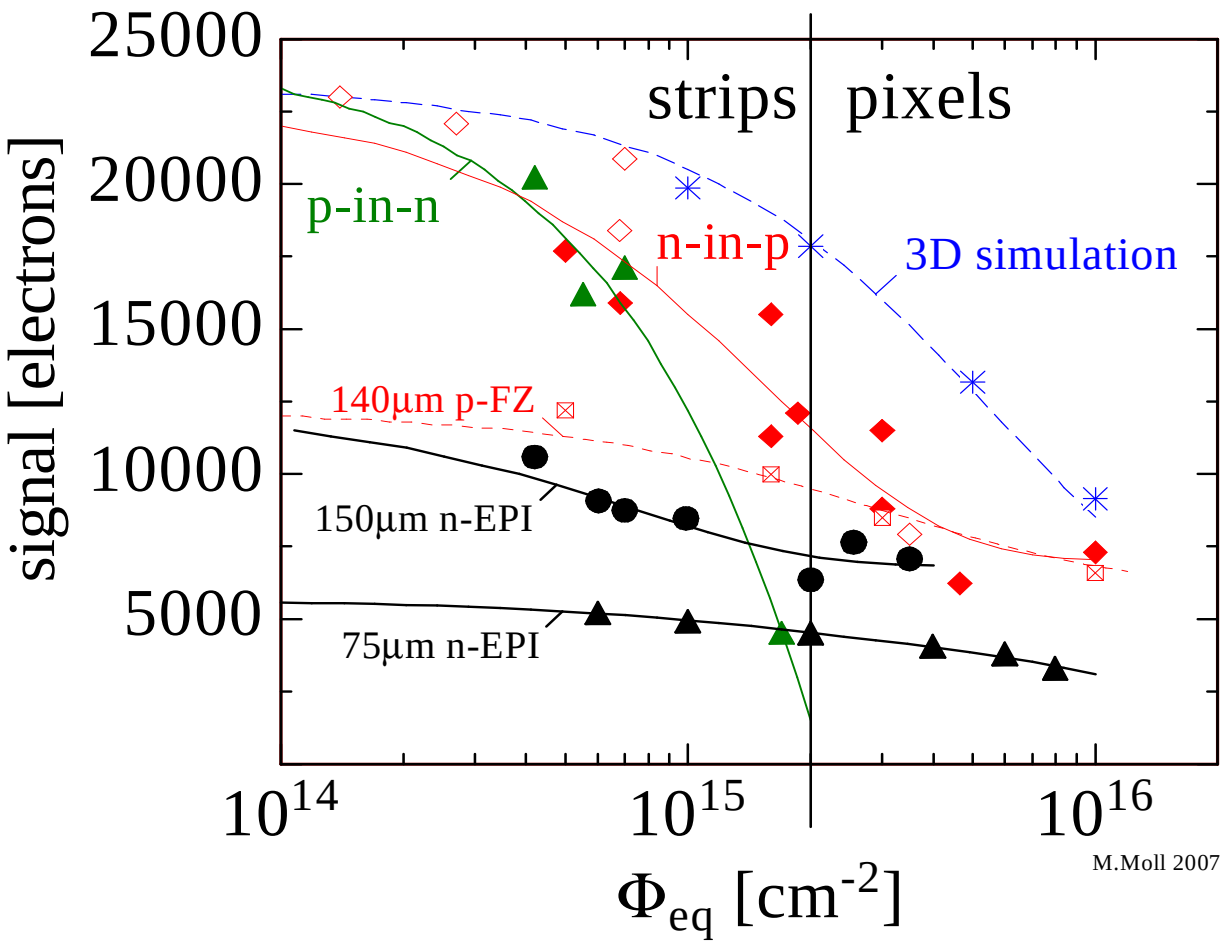
10^{35}



The tracker is the key detector which will require upgrading for SLHC

I. Osborne

COMPARISON VARIOUS Si SENSORS



✳ Double-sided 3D, 250 µm, simulation! [1]
◆ n-in-p (FZ), 280 µm [2,3]
◇ n-in-p (MCZ), 300µm [4,5]
▲ p-in-n (MCZ), 300µm [6]
⊠ n-in-p (FZ), 140 µm, 500V [7]
● p-in-n (EPI), 150 µm [8,9]
▲ p-in-n (EPI), 75µm [10]

[1] 3D, double sided, 250µm columns, 300µm substrate [Pennicard 2007]
[2] p-FZ, 280µm, (-30°C, 25ns), strip [Casse 2007]
[3] p-FZ, 280µm, (-30°C, 25ns), strip [Casse 2004]
[4] p-MCZ, 300µm, (-30°C, µs), pad [Bruzzi 2006]
[5] p-MCZ, 300µm, (<0°C, µs), strip [Bernadini 2007]
[6] n-MCZ, 300µm, (-30°C, 25ns), strip [Messineo 2007]
[7] p-FZ, 140µm, (-30°C, 25ns), strip [Casse 2007]
[8] n-EPI, 150µm, (-30°C, 25ns), strip [Messineo 2007]
[9] n-epi Si, 150µm, (-30°C, 25ns), pad [Kramberger 2006]
[10] n-epi Si, 75µm, (-30°C, 25ns), pad [Kramberger 2006]

See also: [M. Bruzzi et al. NIM A 579 (2007) 754-761]
[H.Sadrozinski, IEEE NSS 2007, RD50 talk]

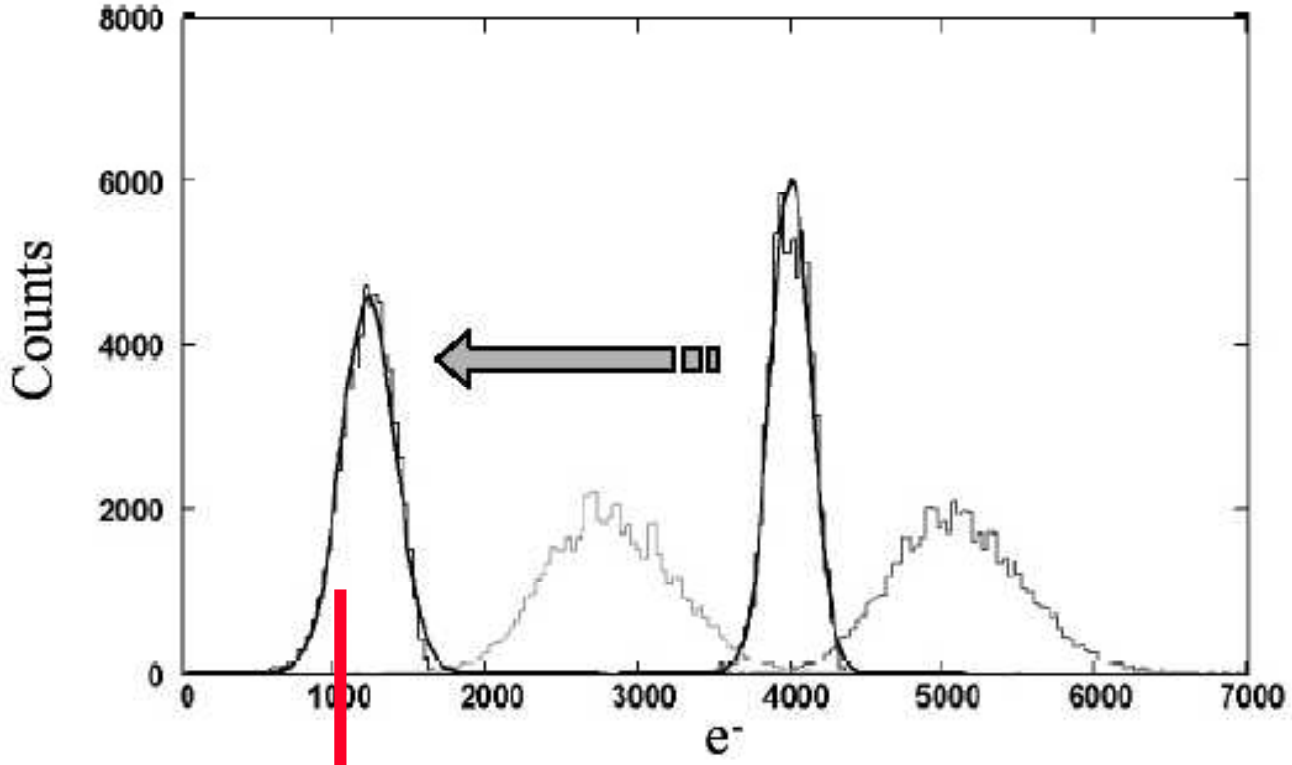
RD50 M. Moll

~ 10^{15} n_{eq}/cm^2 all planar sensors loose sensitivity: trapping

No obvious material for innermost pixel layers : OPTIONS ?

COLUMN '3-D' sensors ? THIN sensors ? replace inner layers ?

LOW SIGNALS CAN BE EMPLOYED



MEDIPIX2
SMALL PIXEL CELL
55µm x 55µm

LOW NOISE
LOW THRESHOLD
BINARY DETECTION

THIN DETECTOR
LOW RESISTIVITY :
AT ROOM TEMP
LESS DAMAGE

TRIMMED THRESHOLD can be MOVED to ~LOWEST VALUE

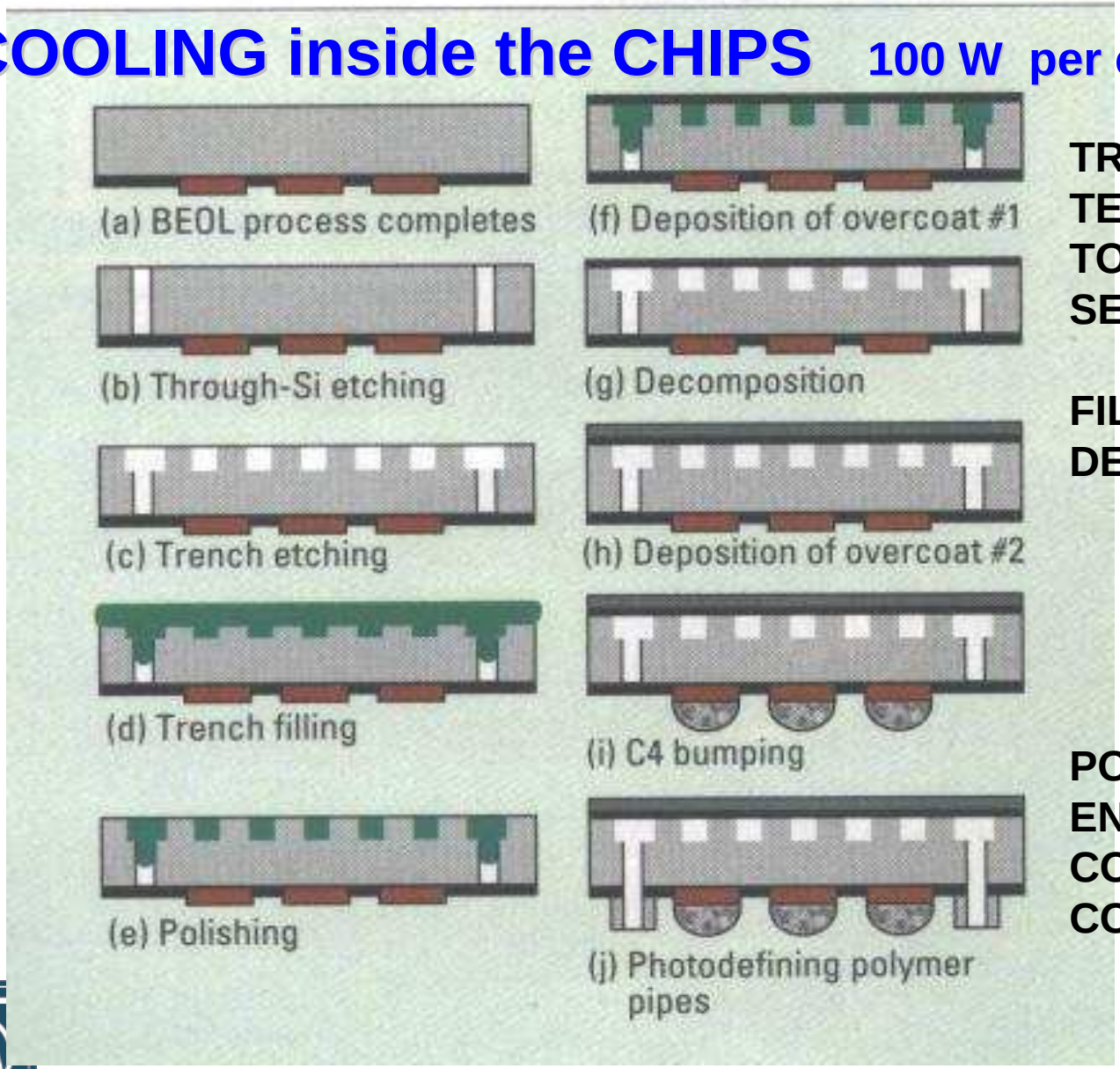
1100 e^- or 4 keV in Si

GENERATED by M.I.P. in ~25 µm Si

COOLING

SYSTEM INTEGRATION : COOLING

COOLING inside the CHIPS 100 W per cm2 possible



TRENCHES are FILLED TEMPORARILY TO ALLOW FLAT SEALING LAYERS

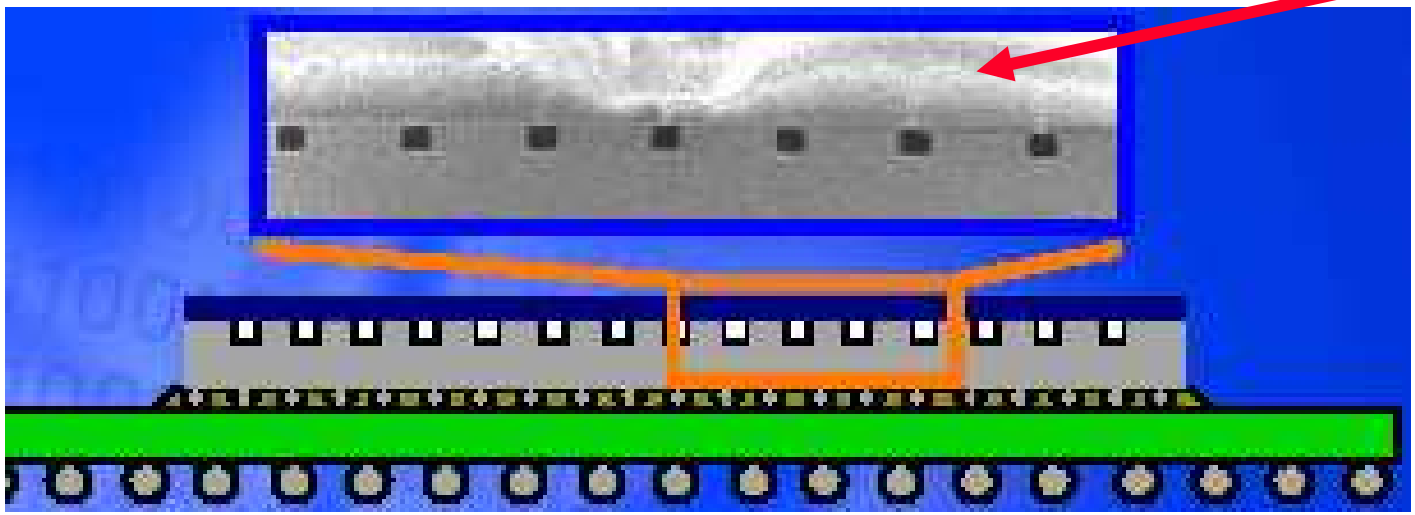
FILLING IS DECOMPOSED by HEAT

POLYMER PIPES for ENTRY/EXIT of COOLING FLUID CONNECT TO SUBSTRATE

INTEGRATED CHIP COOLING

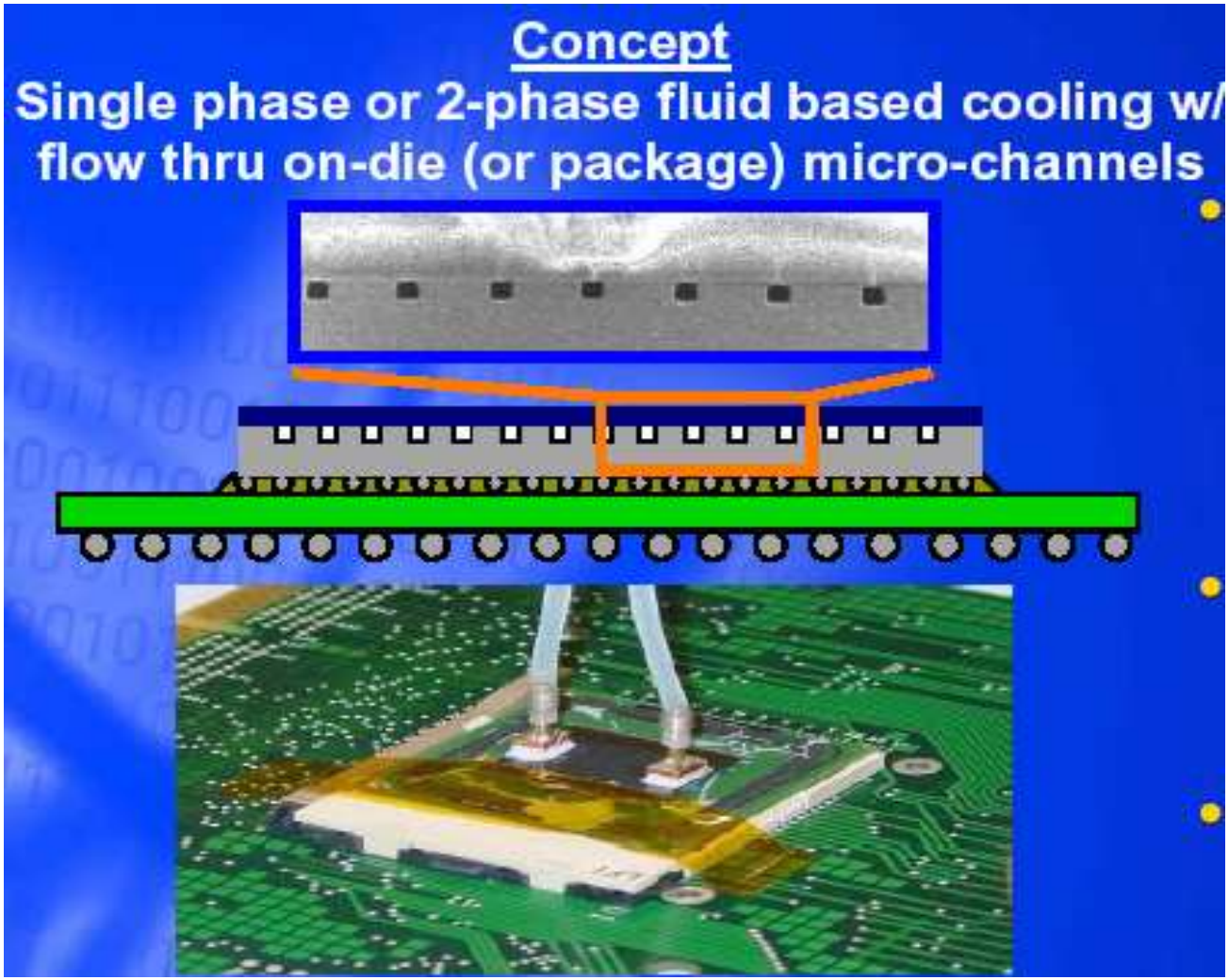
BRING COOLING CLOSE to HEAT SOURCE

'NORMAL' CMOS WAFER



INTEGRATED CHIP COOLING

WAFERS are FUSED after ETCHING CHANNEL



STACKING

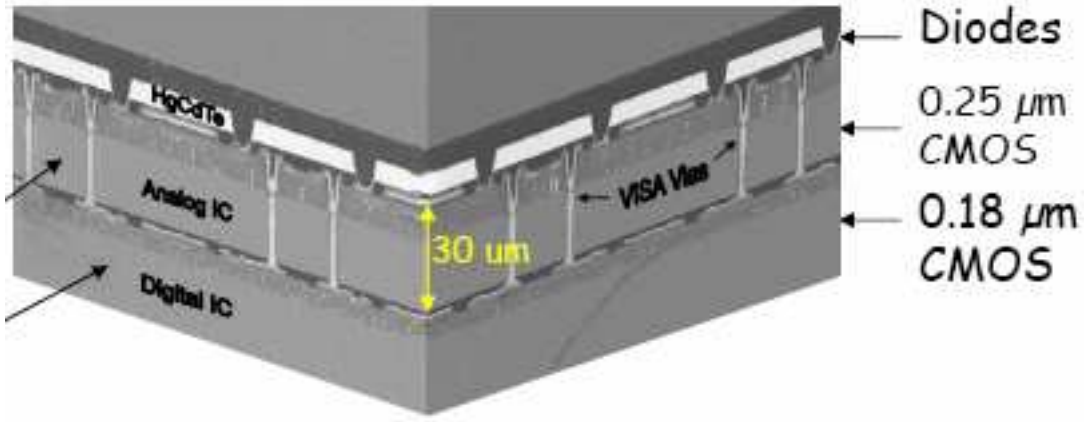
INTERCONNECTS

WIREBONDING STILL WIDELY APPLIED

MULTILAYER now OFTEN USED for SENSORS (IR)

BUMP BONDING for

- HIGH RELIABILITY
- HIGH DENSITY
- THIN PACKAGE



FUTURE 'BUMP-LESS BUILDUP' maybe THINNER

NEW DETECTORS ?

SILICON submicron CMOS ALLOWS PIXEL FUNCTIONS

SELECTIVITY CAN BE BUILT-IN

VERY LOW NOISE with SMALL PIXELS ~40 e^- rms

3D FUNCTIONS with HYBRID PACKAGING

TRACK VECTORS + SELECTIVITY

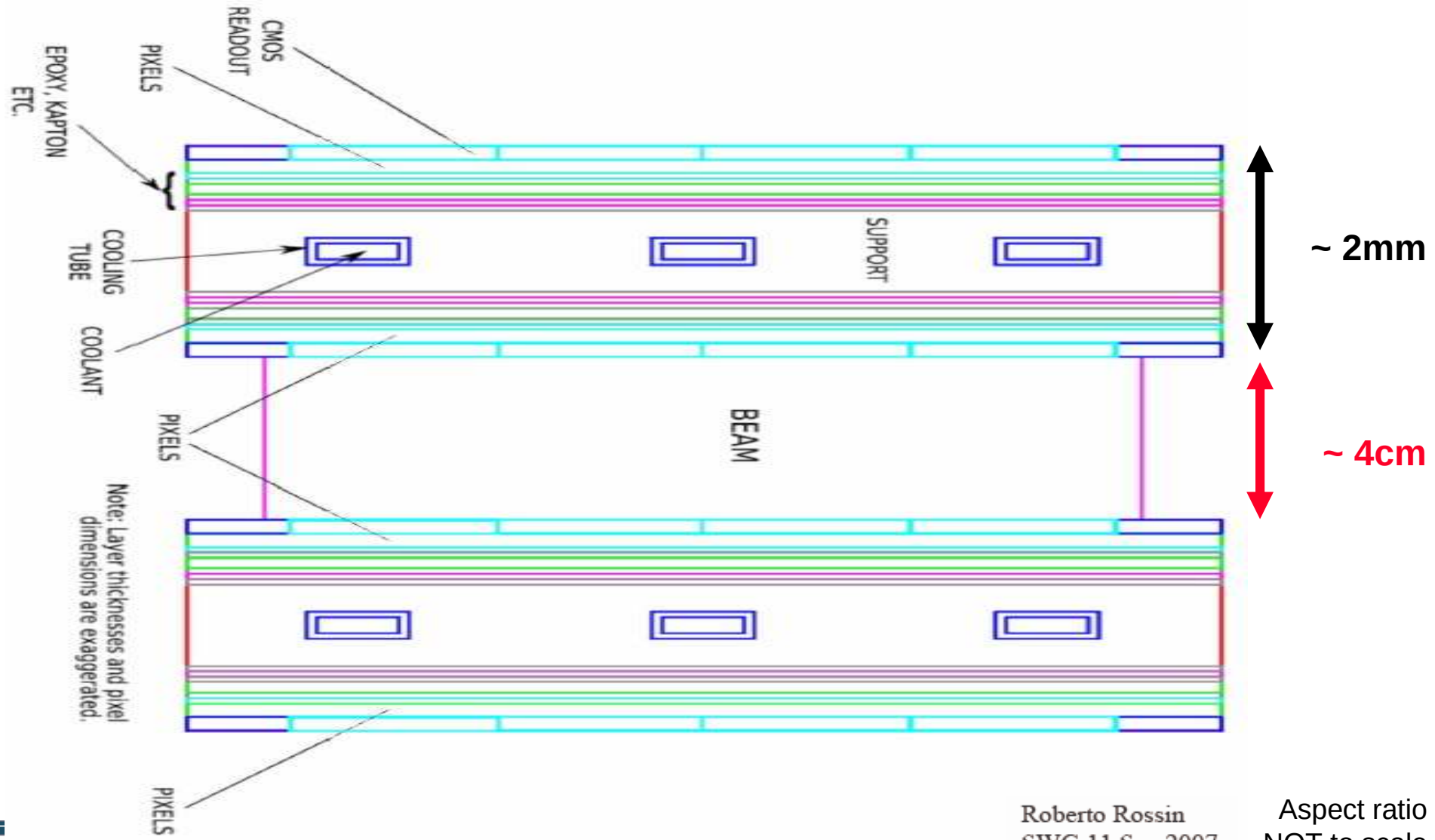
THIN DEVICES ARE RADHARD

IDEAS for VECTOR DETECTOR in CMS

Erik HEIJNE CERN PH Department

Paris 29 November 2007

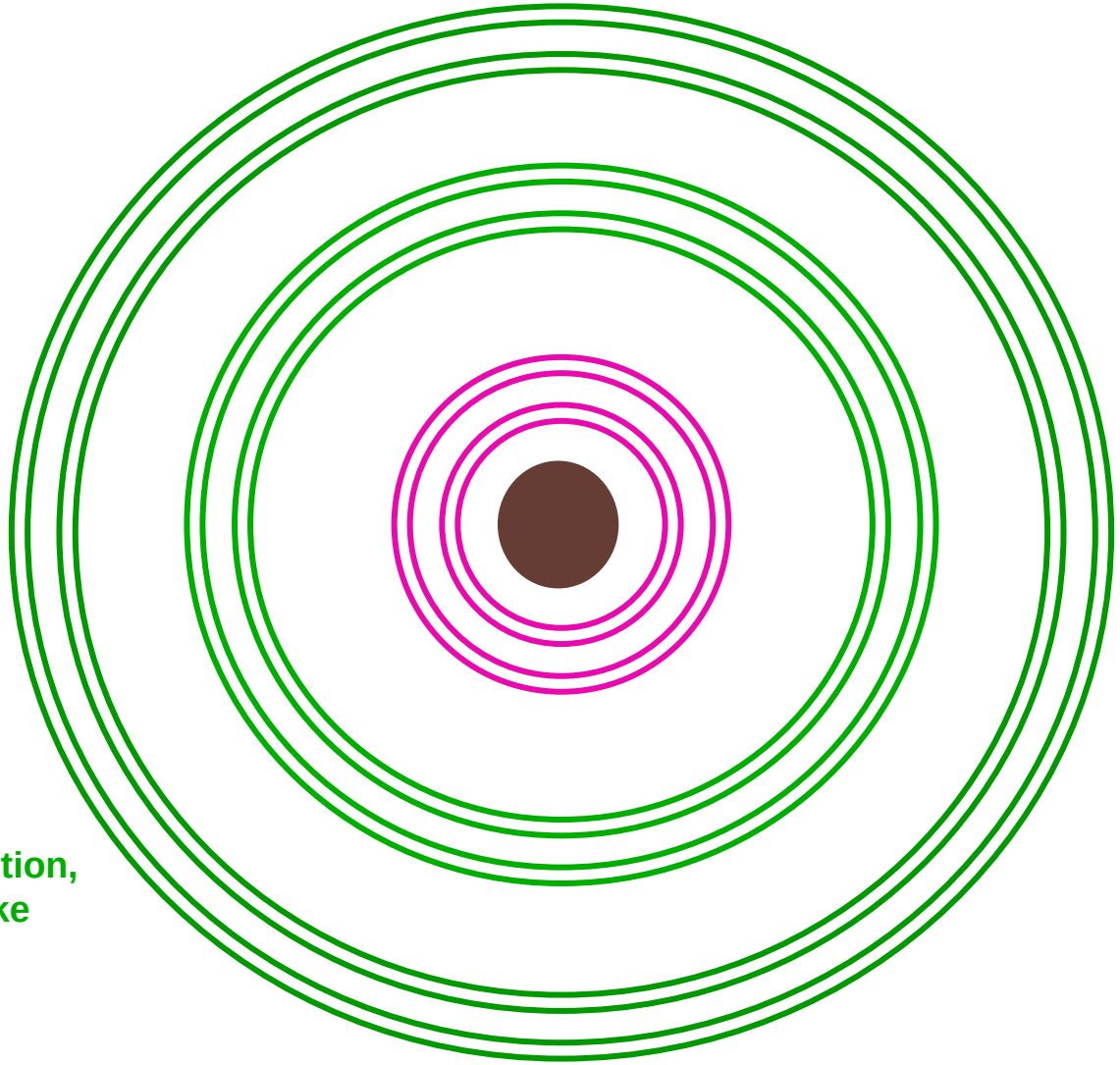
CMS SLHC TENTATIVE TRACKER 'Straw Man' LAYOUT



CMS TENTATIVE TRACKER DESIGN SLHC

CMS STUDIES are ONGOING

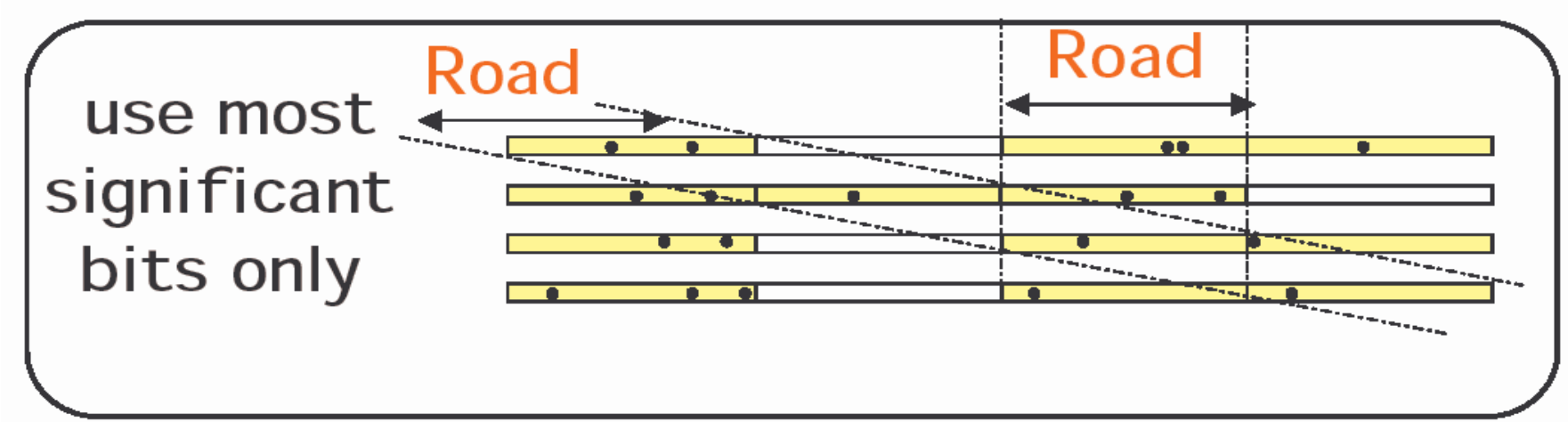
- Hit Pair Pt Resolution
- Track Stub Pt Resolution
- Fake Rate & Efficiency if require
  - Single Hit Efficiency: 95%~99.5%
  - 4/4 hits in sensor pair
  - 1/3 vs 2/3 Track Stubs
- Min radius at which scheme works effectively
- All the above varying the design parameters over the plausible range
  - Eg. Effect of cell geometry on resolution, occupancy and resulting effect on fake rate & efficiency



SOFTWARE or also HARDWARE ?

FAST-TRACK COLLABORATION

USE MICROPROCESSORS for FAST TRIGGER



MULTI-LAYER-DETECTOR with LOCAL PROCESSING :

SPACE-POINT + VECTOR

VERTEX SELECTION, BACKGROUND SUPPRESSION, ..

STACKING