Wafer Level and

3D System Integration

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Outline

- Introduction
- Experience in Packaging of Pixel Detectors
- Future Options and Requirements:
  - Thin Silicon
  - Thin Chip Integration
  - 3D Integration

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Forschungsschwerpunkt
Technologien der Mikroperipherik

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seph von Fraunhofer (1787 - 1826)

Researcher

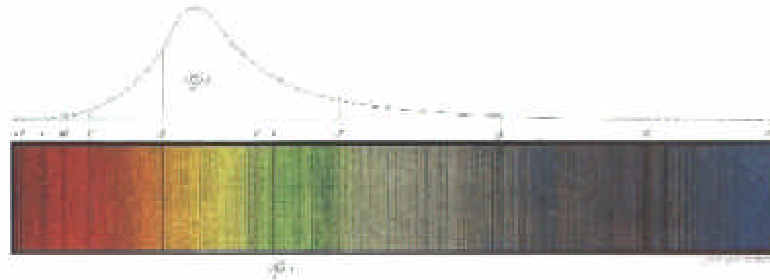
discovery of "Fraunhofer Lines"
in the sun´s spectrum

Inventor

new methods of lens processing

Entrepreneur

head of royal glass factory



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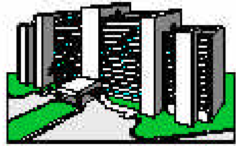
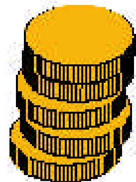
Fraunhofer in profile

59
institutes



12500
employees
(full-time
equivalence

1000 million Euro
bugdet



Materials and components

Production technology

Information and communication

Microelectronics and microsystems

Sensor systems, testing technologies

Process engineering

Energy, contruction, environment, health

Technical and economic studies

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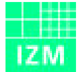

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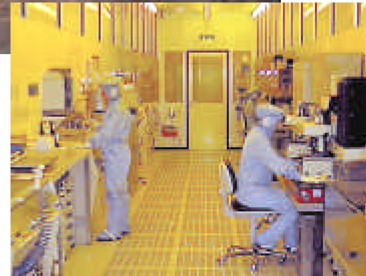

250 Scientists and Engineers (+100 Students)/ Cleanroom 800 m^2

Applied Research and Development of Advanced Packaging Solutions for Microelectroni

Branch Labs and Centers in Chemnitz, Teltow, Paderborn, Oberpfaffenhofen and Munich

Worldwide Technology Transfer and Consulting Services

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ATLAS Detektor Large Hadron Collider (CERN)

Length: 50 m

Diameter: 25 m

Weight: 7000 t

ATLAS and ATLAS Inner Detector

ID length: 7 m
ID diameter: 2m

Barrel SCT
Forward SCT
TRT
Pixel Detectors

H.-G. Moser, Max-Planck-Institut für Physik, Munich

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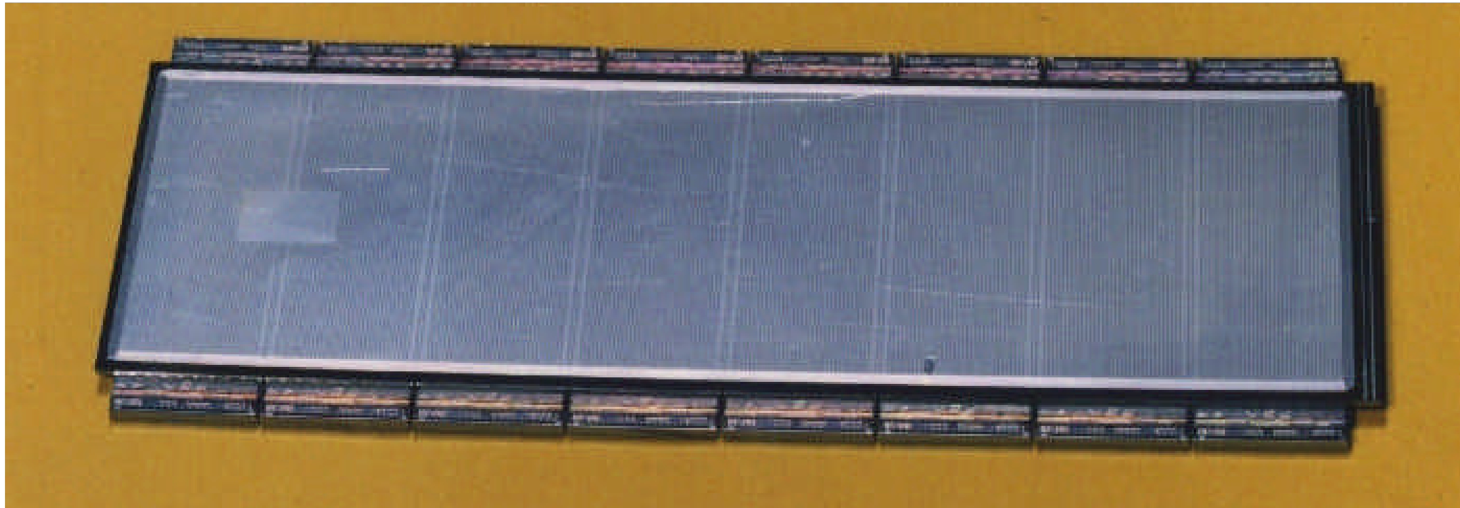
ATLAS Pixel Detector Module



- Thin-Film-Multichipmodul
- Size 22 x 64 mm²
- Silicon Sensor
- 16 Readout ICs (KGD)
- 46 080 IO-Bumps pitch 50 µm, electroplated SnPb

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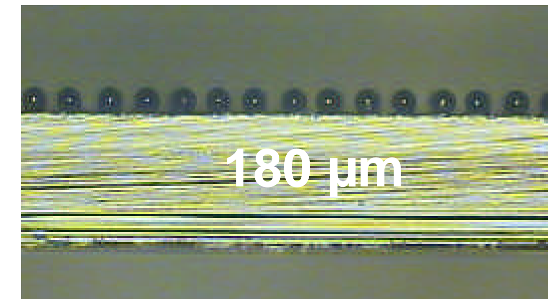
High Density ECD Bumping & Flip Chip
IBM 0.25 µm rad tolerant design

4“

2800 Bumps / chip
size / pitch :
30 µm / 50 µm

8“

Thinning of bumped wafers:



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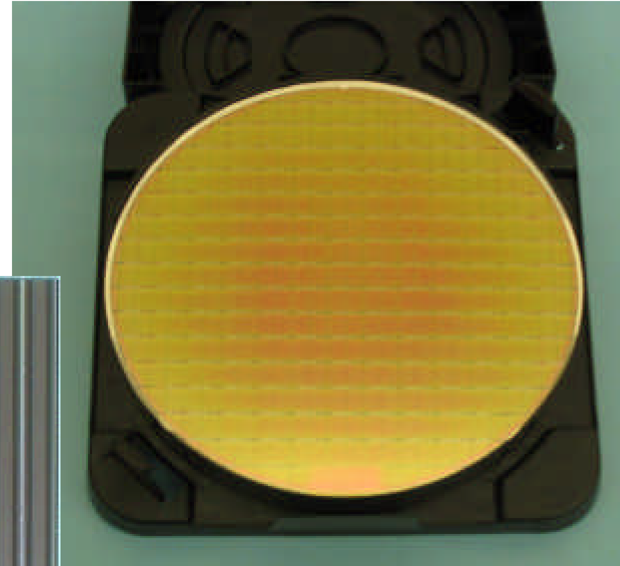
ATLAS FE-I3 CMOS IC

98 Readout Chipwafer

200 mm Si-Wafer, CMOS 0.25µ Technology

288 tested Chips per Wafer

Chip Size: 7,4 x 11 mm²



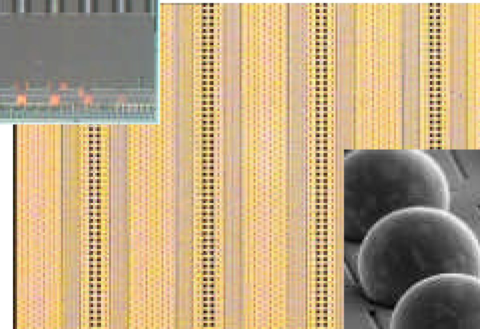
Electroplated I/O Bumps:

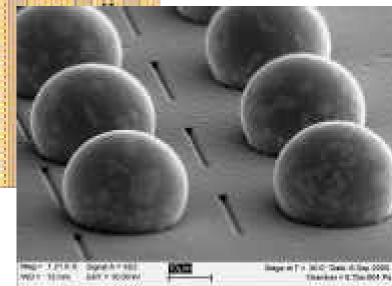
- 841 000 Bumps per Wafer, Ø 25µm

Plating Base: Ti:W/Cu

UBM: Cu

Solder: Sn60Pb40





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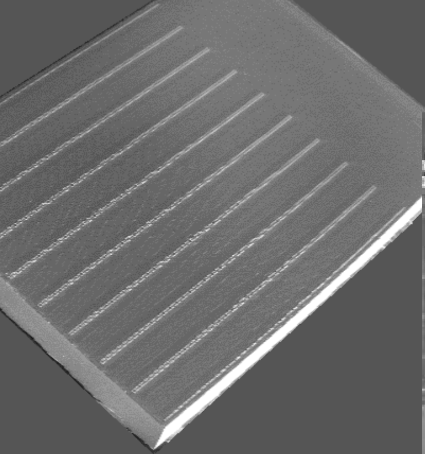
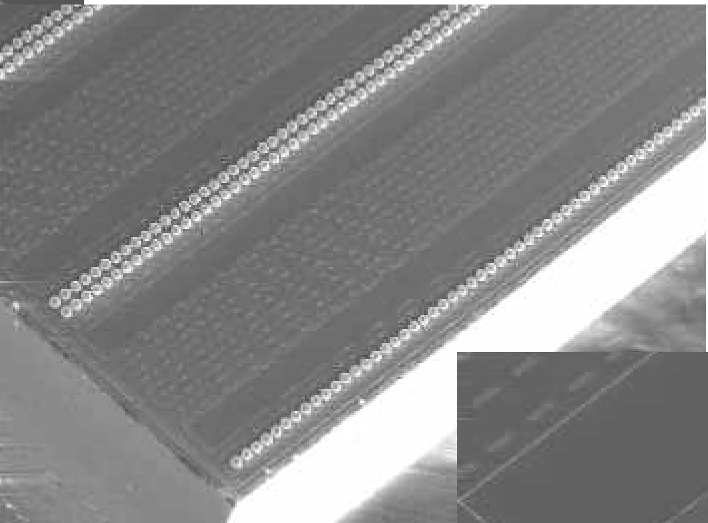
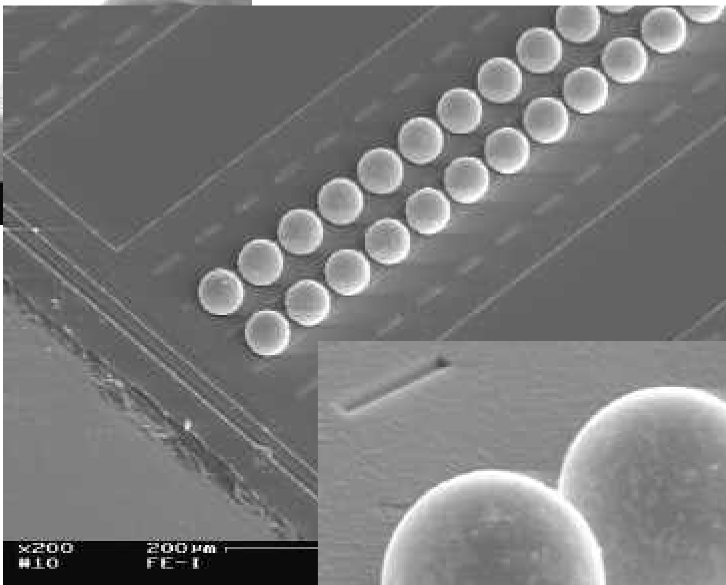
Bumped FE-I Chi

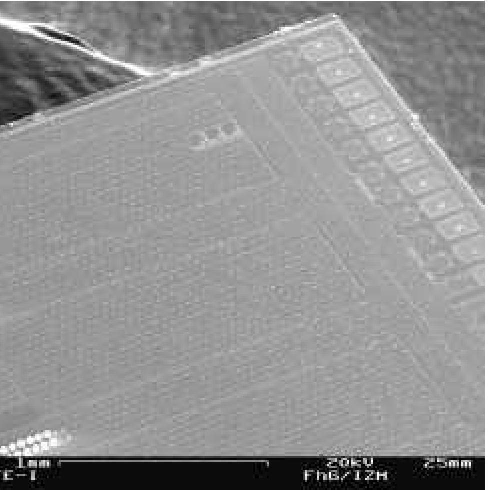
IBM 0.25 µm rad tolerant design

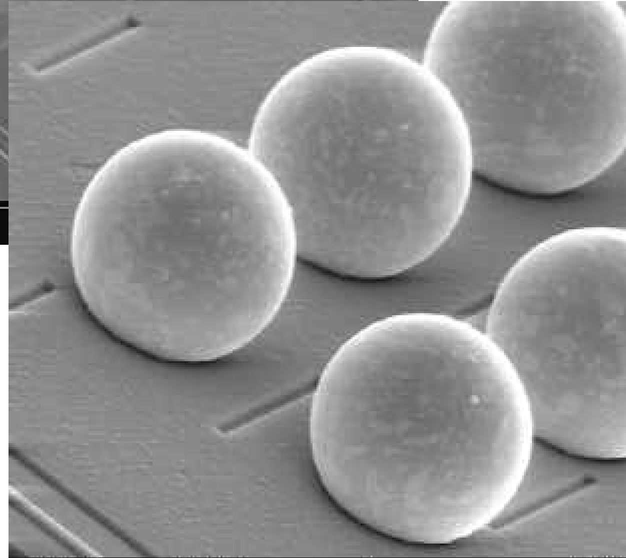


with 9 column pairs









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IC Technology Roadmap: Chip Interconnect Pitch

Chip Interconnect Pitch [µm]

ATLAS

Year

area array

peripheral

Source: ITRS

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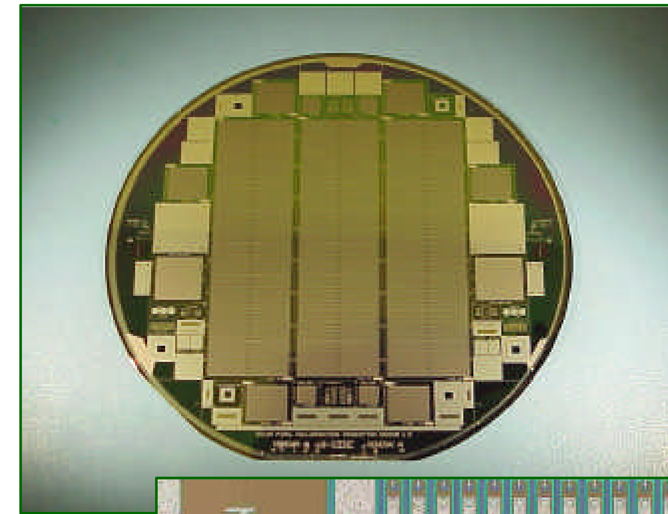
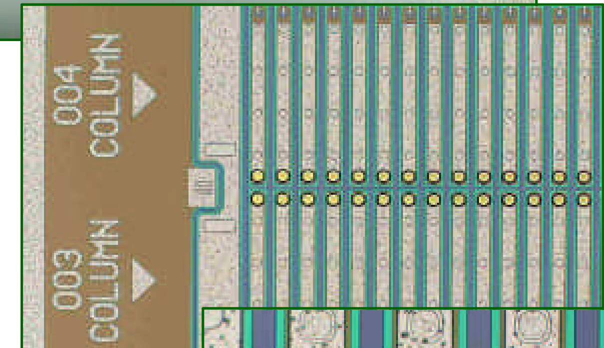
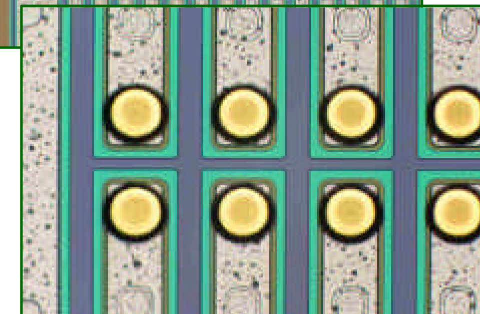
ATLAS Si-Sensor Substrate Wafer

520 Processed Sensor Wafer:

- 100 mm Silicon Wafer
- Double side processed
- Thickness 250 µm
- 3 sensor tiles with
  46080 pixel cells
  50 x 400(600) μm^2







Electroplated Sensor Pixel Contacts :

- Pixelmetallization Al
- Plating Base   Ti:W/Cu
- Pad   5 µm Cu + 1µm Ni + Au

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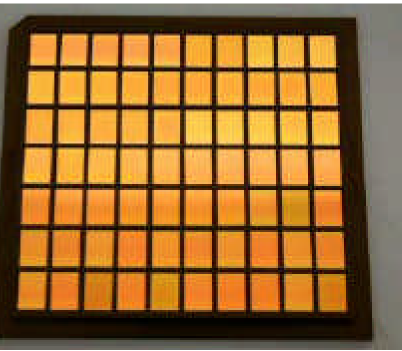
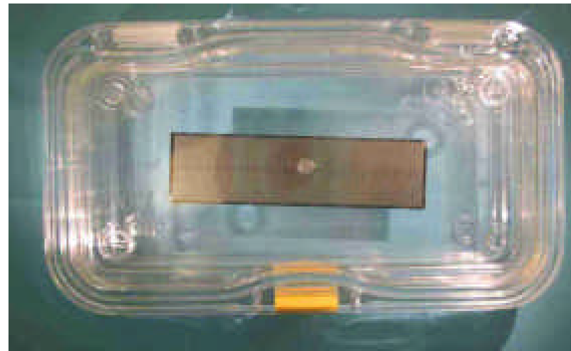
Bare Module Flip Chip Assembly





- **readout chips, sensor tiles:**
  test, inspection, classification

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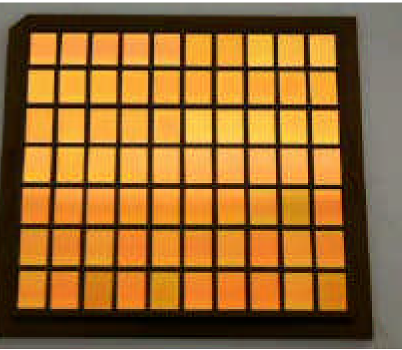

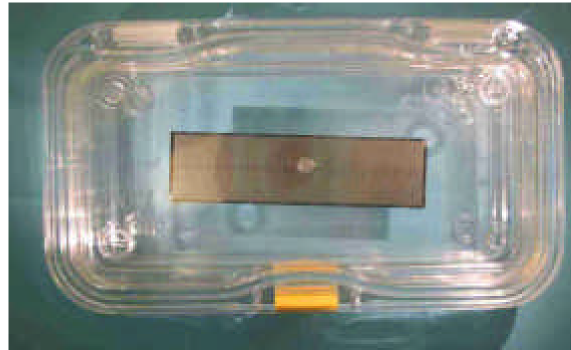

- **readout chips, sensor tiles:**
  test, inspection, classification
- **flux deposition**

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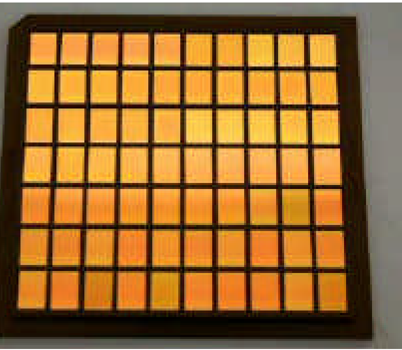

- **readout chips, sensor tiles:**
  test, inspection, classification
- **flux deposition**
- **pick and place:**
  FC150 of SüssMicrotech,
  Pick & Place Accuracy = 3µm

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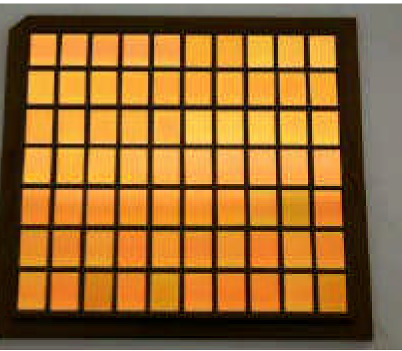

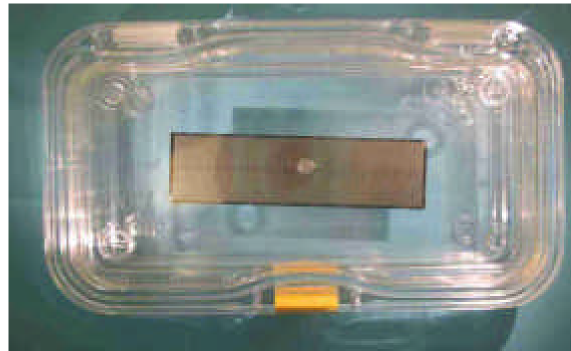

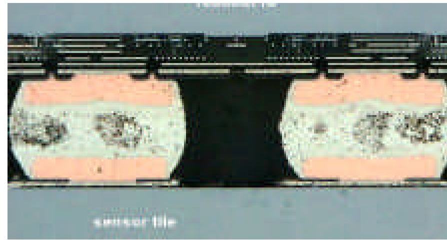

- **readout chips, sensor tiles:**
  test, inspection, classification
- **flux deposition**
- **pick and place:**
  FC150 of SüssMicrotech,
  Pick & Place Accuracy = 3µm
- **reflow:**
  at 250°C, reductive atmosphere

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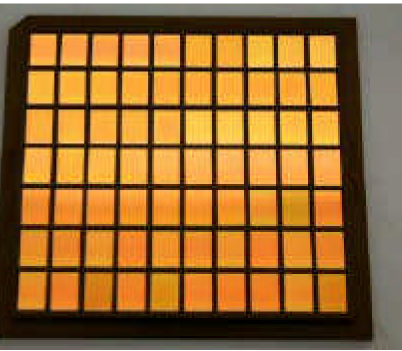

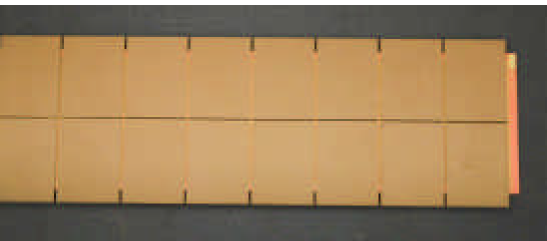

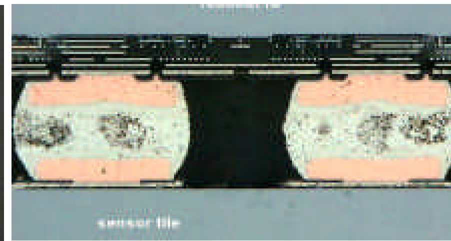

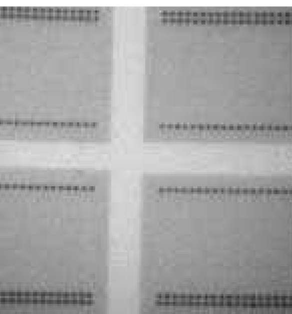

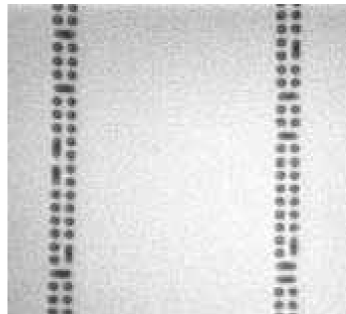

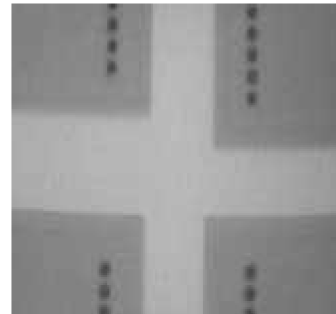

- **readout chips, sensor tiles:**
  test, inspection, classification
- **flux deposition**
- **pick and place:**
  FC150 of SüssMicrotech,
  Pick & Place Accuracy = 3µm
- **reflow:**
  at 250°C, reductive atmosphere
- **inspection and measurements:**
  x-ray inspection, electric module test

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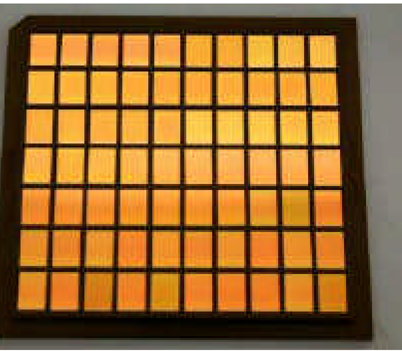

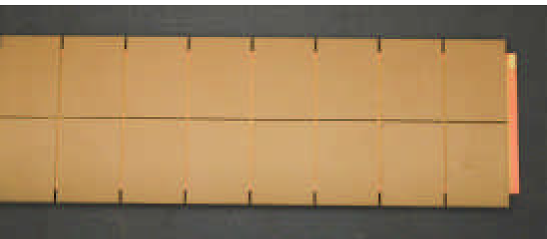

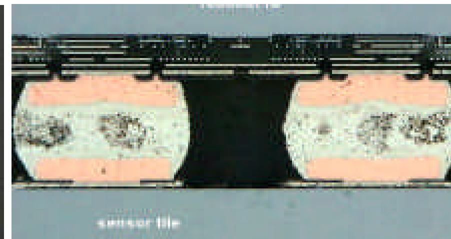

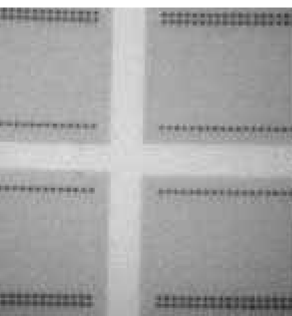

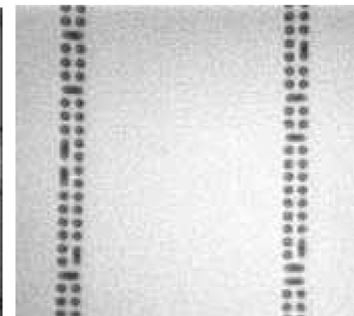

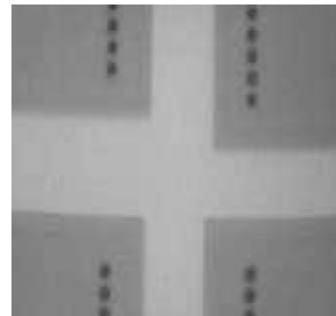

- **readout chips, sensor tiles:**
  test, inspection, classification
- **flux deposition**
- **pick and place:**
  FC150 of SüssMicrotech,
  Pick & Place Accuracy = 3µm
- **reflow:**
  at 250°C, reductive atmosphere
- **inspection and measurements:**
  x-ray inspection, electric module test
- **rework:**
  single die exchange of misplaced die, t
  many bridged bumps, die that failed
  electrical test

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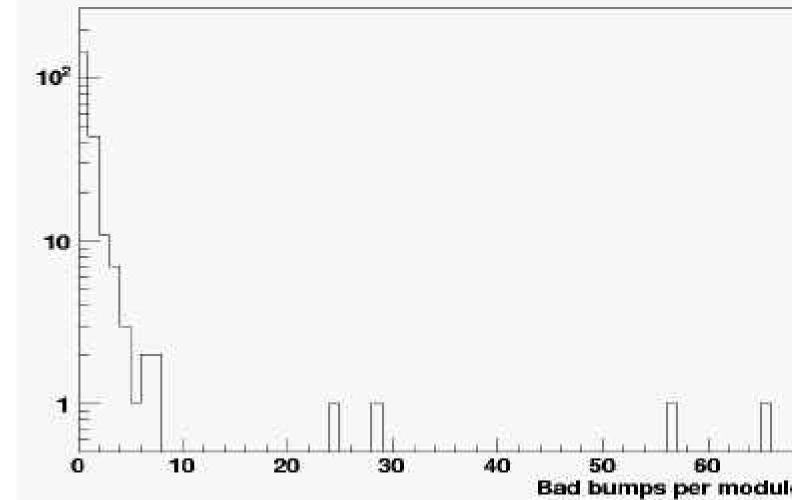
Assembly of ATLAS Pixel Detector Modules

- 16 ROC Flip-Chip Bonded to the Sensor
- 46 080 electroplated SnPb IO-Bumps, Ø 25 µm, pitch 50 µm

- Assembly of 1139 ATLAS Modules
- Assembled Chips: ~ 19000 chips
- Module Yield incl. rework: 97 %
- Chip Rework Rate: 0.7 %



98% der Module mit <10 Bumpdefekten

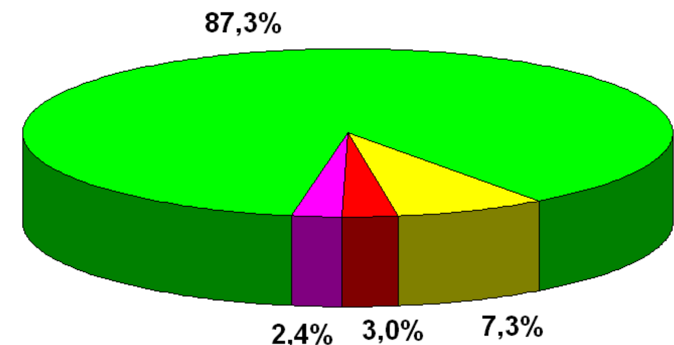
Chip Yield after Bumping:

20.720 processed Readout Chips

Class 1: perfect chips

Class 2: accepted defects
(< 4 defective bumps, small particle, ...)

Calss 3: rejected chips
(> 4 defective bumps, scratches, residues, plating defects,...)



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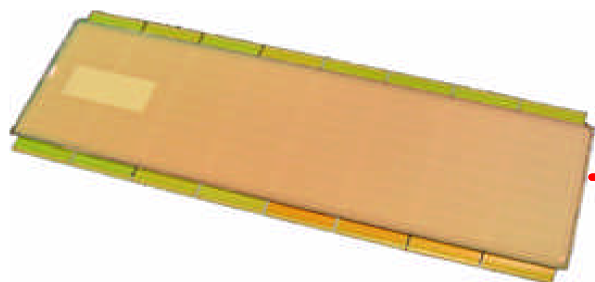
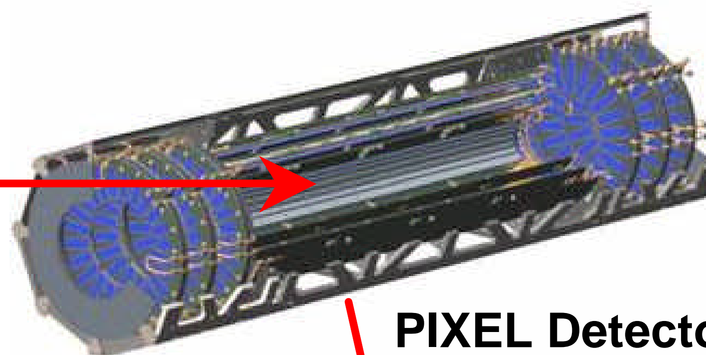
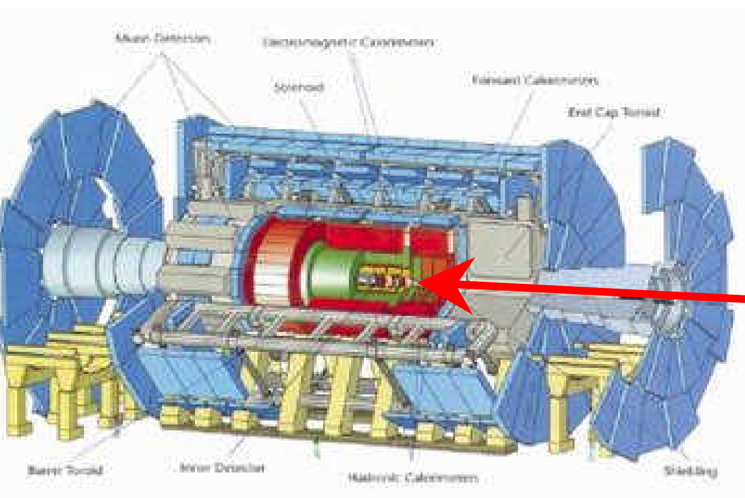
ATLAS Pixel Detector at LHC at CERN



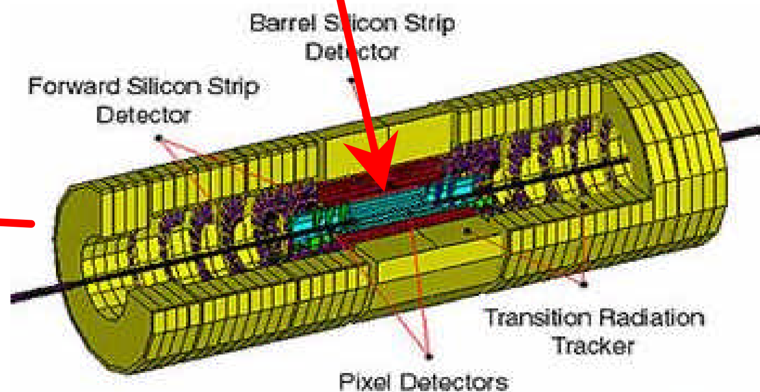
Bare Module 22 x 64 mm²



PIXEL Detector Ø 0.9



ATLAS Detector Ø 25m



Inner Detector Ø 2m

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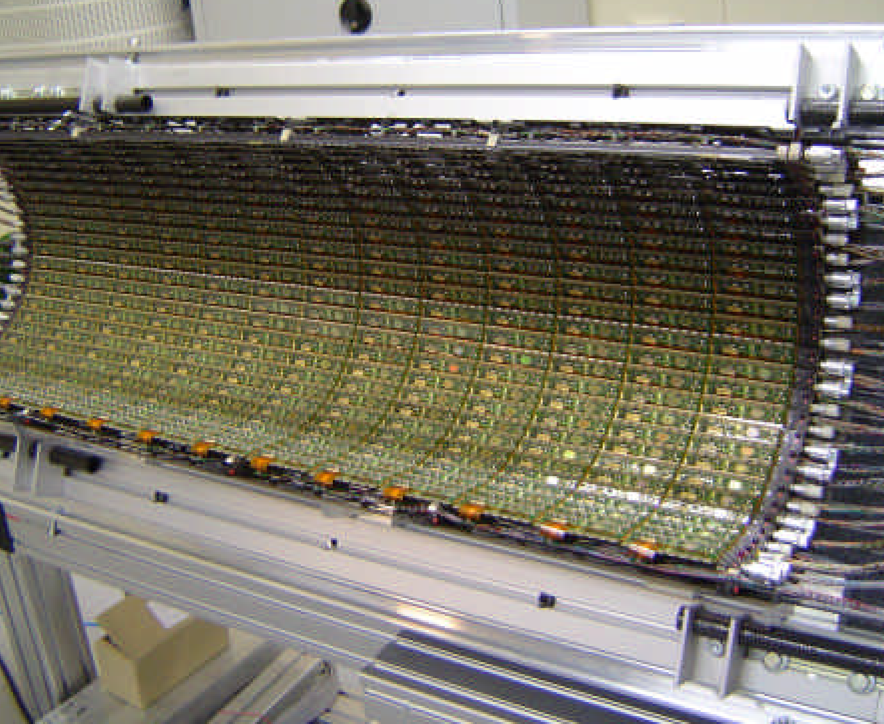
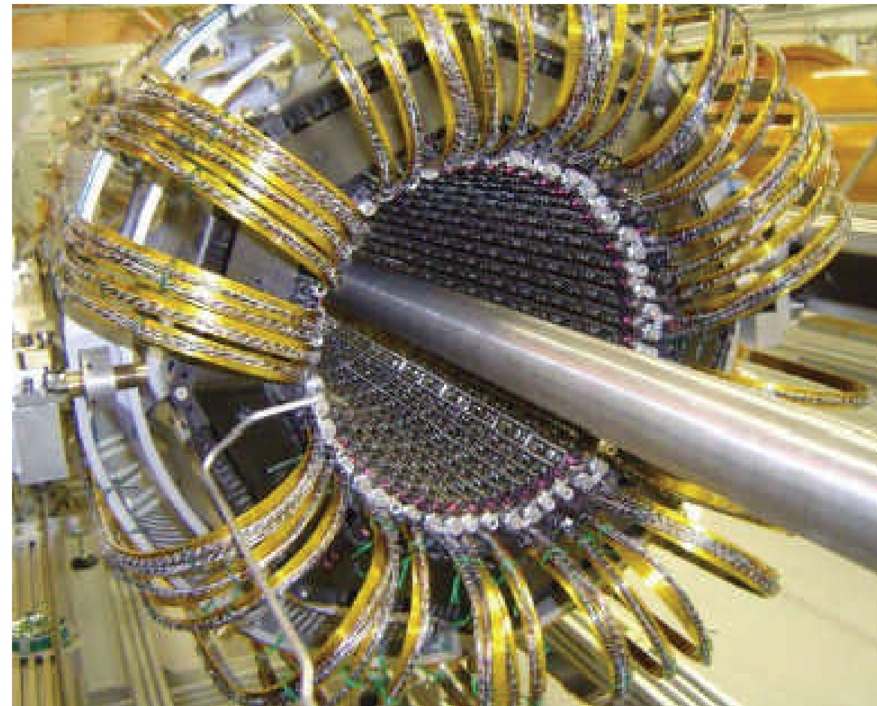


ATLAS Pixel Detector at LHC at CERN



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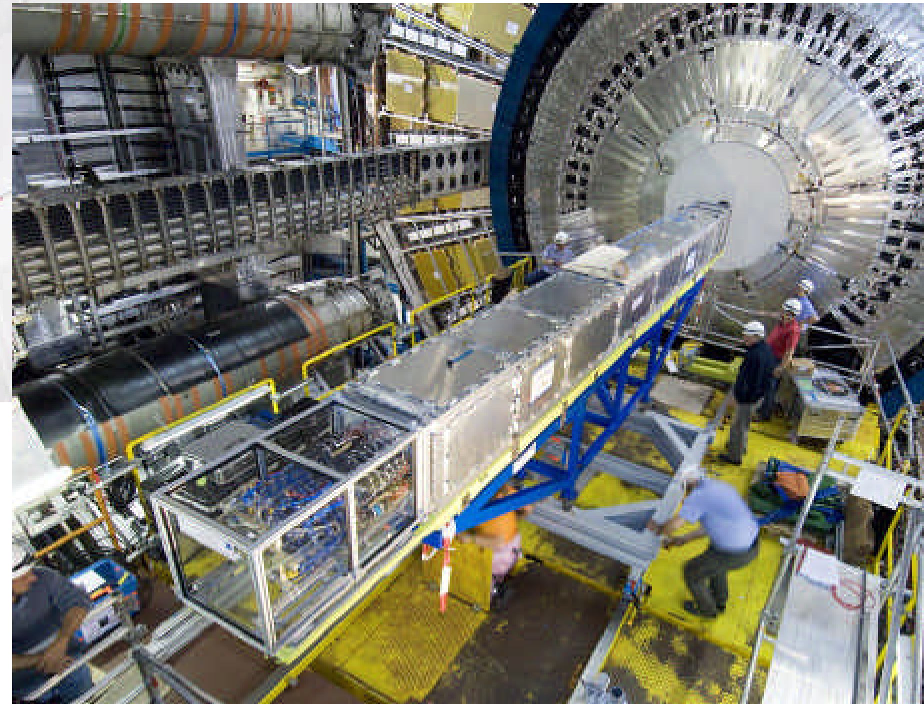

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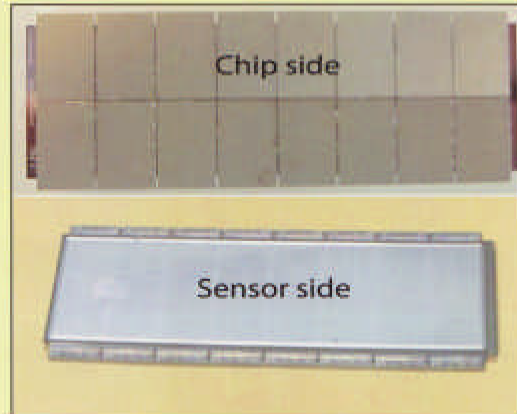
ATLAS Supplier Award

In recognition of excellent supplier performance

ATLAS Supplier Award for IZM

Supply of Modules for the ATLAS Pixel Detector



ATLAS Pixel Module

The Fraunhofer-Institut für Zuverlässigkeit und Mikrointegration (IZM) of Berlin, Germany has supplied about 1300 modules for the ATLAS Pixel Detector. It is the first time that hybrid pixel modules have been produced in such a large number.

The modules, made of 16 front-end chips and one sensor tile, have 46080 channels each and constitute the building block of the ATLAS Pixel Detector. IZM produced the modules starting from wafers of rad-hard electronics and of sensors both supplied by other vendors. Bumps have been deposited on these wafers, the electronics chips and the sensor tiles have been singled out and then flip-chipped to obtain the module. The hybridization technique necessary to build the ATLAS Pixel Detector modules is at the edge of what industry can propose today in terms of contact density.

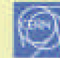
IZM optimized their proprietary bumping and flipping technique based on electroplating deposition of Pb/Sn and a self-alignment reflow cycle. This allowed to match the stringent specifications required by ATLAS (e.g. less than $3 \cdot 10^{-3}$ of non-working channels in each module). IZM worked closely with Bonn University both for the development of the technique and during the production phase. The quality of the modules was very good, exceeding significantly the contractual yield of 90%; the delivery was on schedule and within budget.

The ATLAS Collaboration greatly appreciates the efficient and pleasant cooperation and the excellent performance of IZM-Berlin, which contributed significantly to the success of ATLAS.

Geneva, June 2007

IZM bumps deposited at 50 µm pitch

Dr. Peter Jenni
ATLAS Spokesperson



Dr. Maximilian Metzger
CERN Secretary-General

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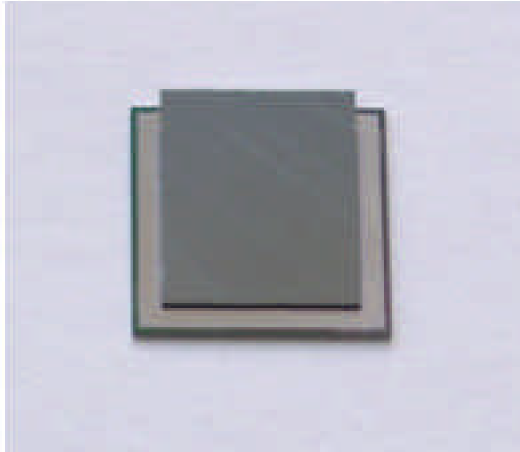
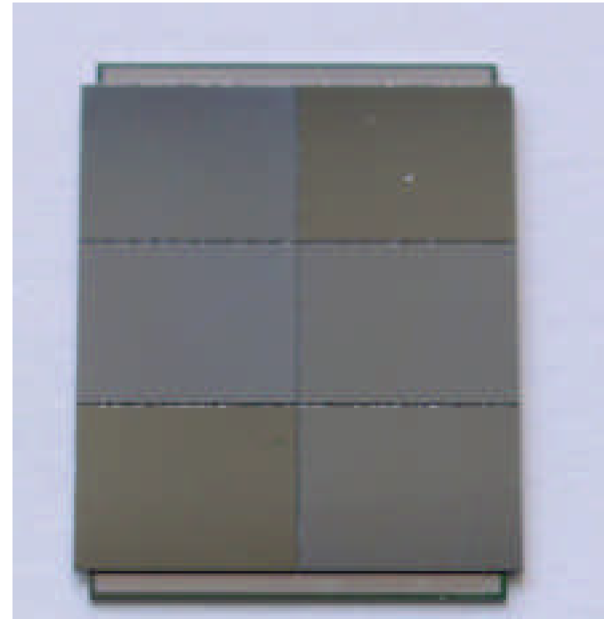
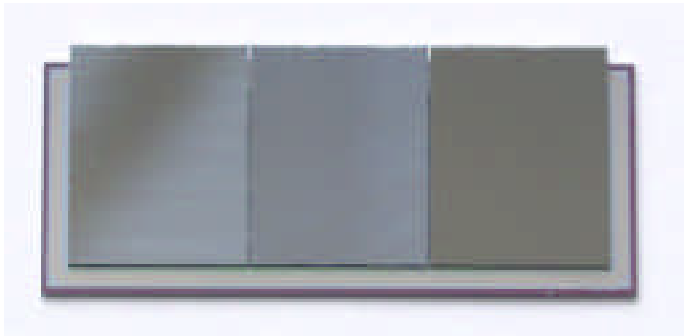
Detector Placquettes for CMS

1 x 1





2 x 3



1 x 3

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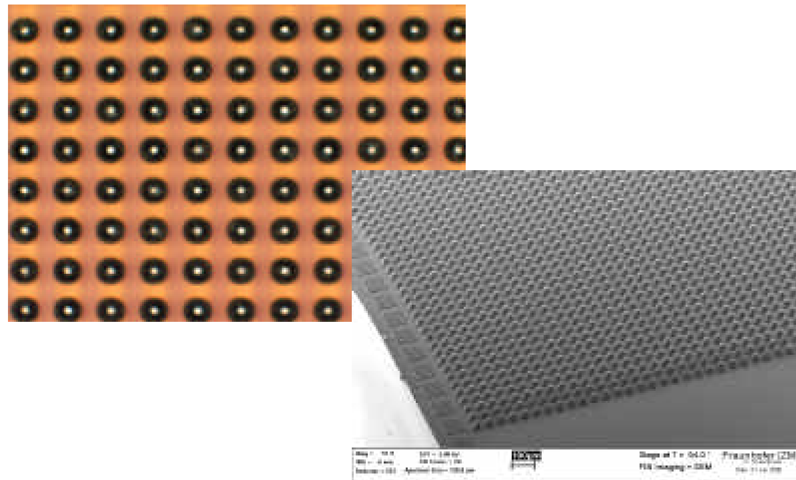
GaAs X-ray Pixel Detector

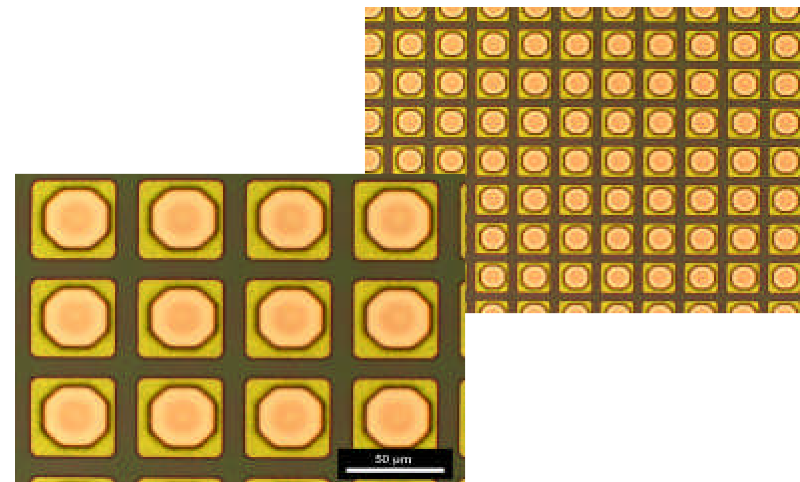
Frontend Readout Chip

- MEDIPIX 256x256 IOs
- Pixel cell size 55 x 55 µm²
- Chip size 14 x 14 mm²
- SnAg Bumps Ø25 µm, more than 6 000 000 bumps/wafer



GaAs Sensor Chip

- GaAs Detector 256x256 pixels
- Pixel size 55 x 55 µm²
- Chip size 16 x 16 mm²
- Electroplated Cu-Pad, height 5 µm



project partners: MPD, Fine Tech, FhG-IZFP, FhG-IZM
funded by: EFRE and the Free State of Saxony

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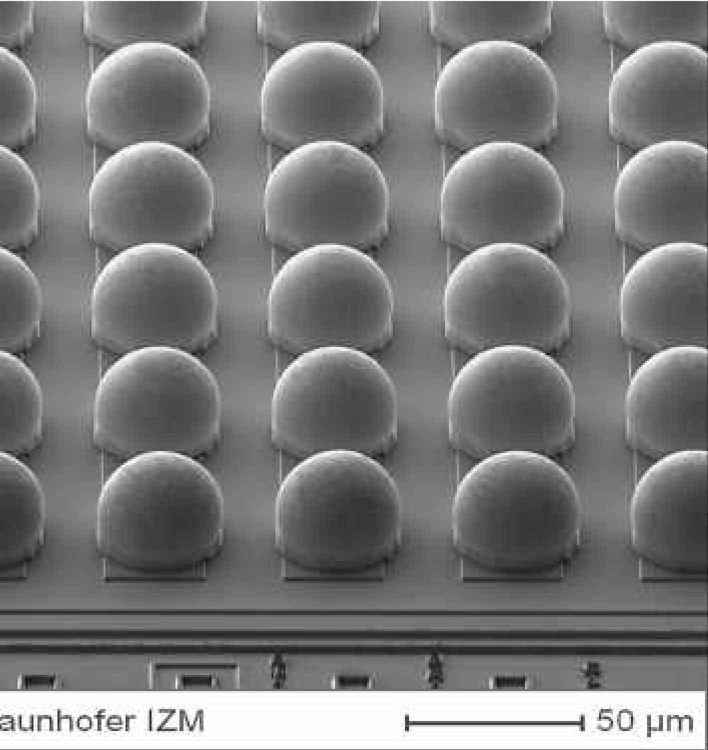

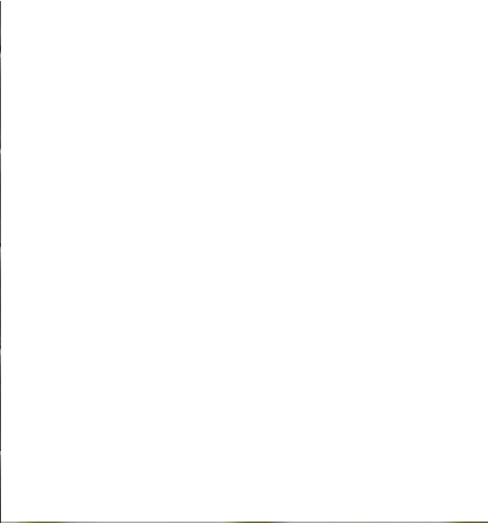

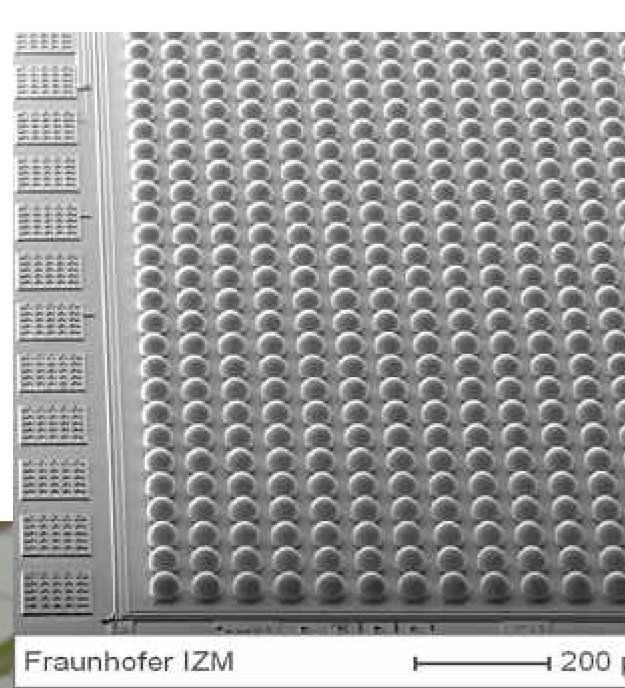

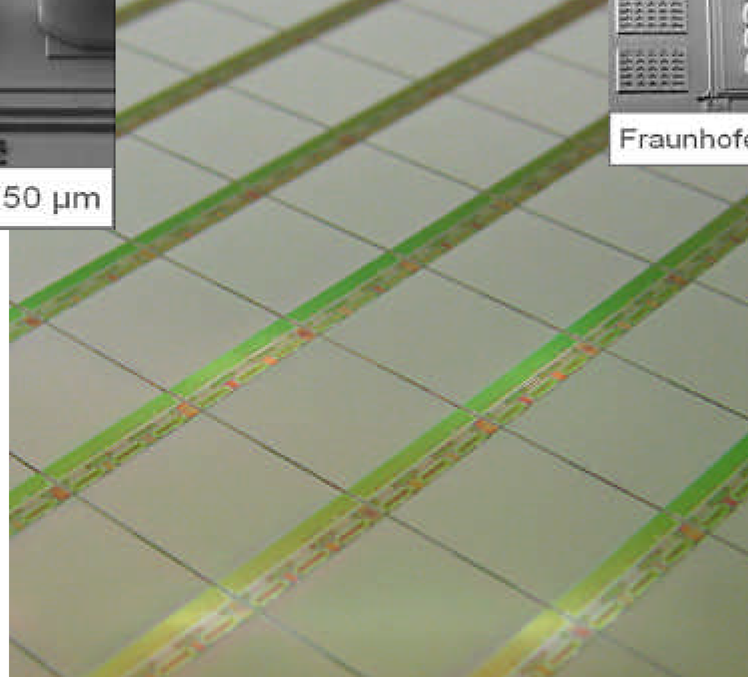

ad Free Bumping
SnAg

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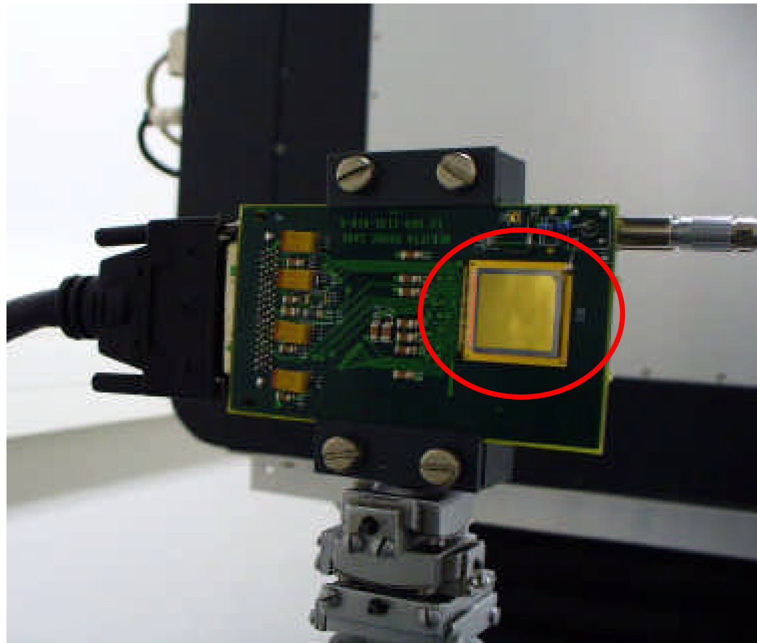
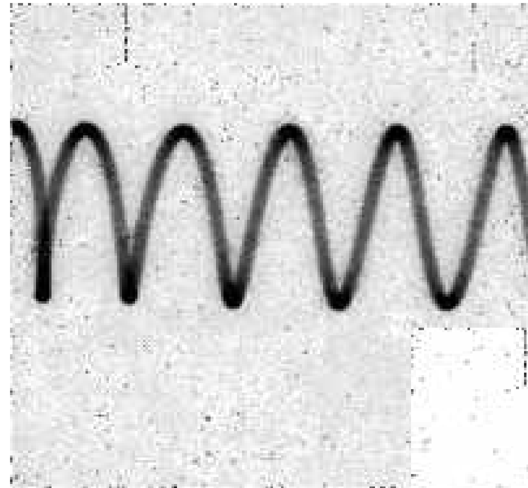
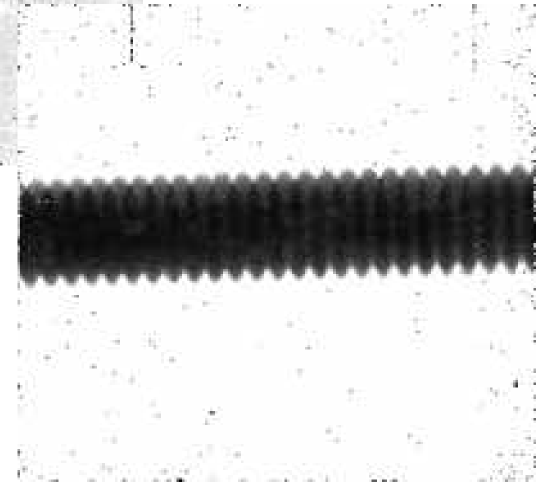
GaAs Hybrid Pixeldetector: X-Ray Test







Pixeldetector assembled on MEDIPIX board and tested at FhG-IZFP

x-ray images of a spring and a screw using the 202x202 pixel detector prototyp (photography by FhG-IZFP)

project partners: MPD, Fine Tech, FhG-IZFP, FhG-IZM
funded by: EFRE and the Free State of Saxony

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7 Chip-Module CPPM

Medipix Applications

Diamant Sensor Applications

Ultrasonic Sensor Applications

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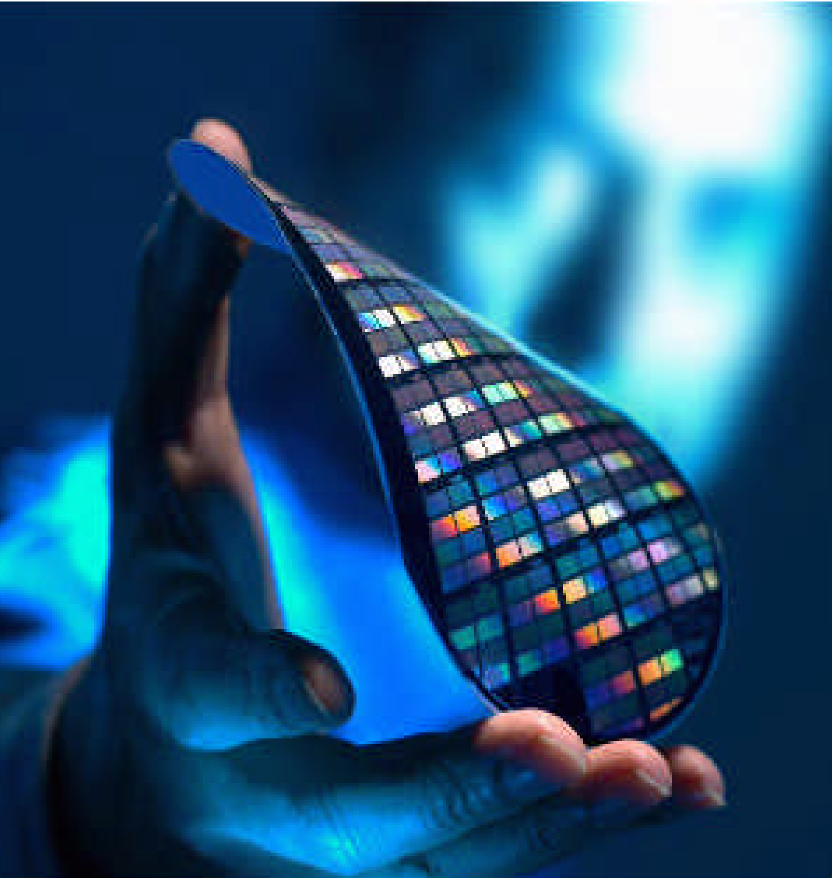
Future Requirements: Thin Silicon



Silicon becommes flexible when thickness is reduced down to less than 30µm

- bending radius 1mm / 1µm thick-ness
- fully flexible and ultra thin systen available
- best opportunities to proceed wit FC and CSP technologies
- basis for 3D chip integration

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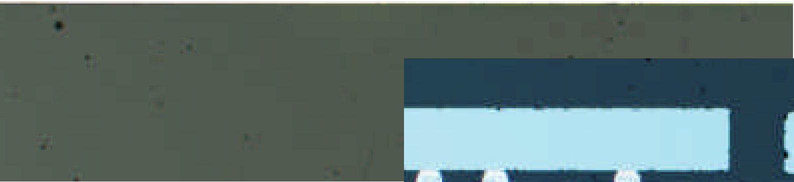
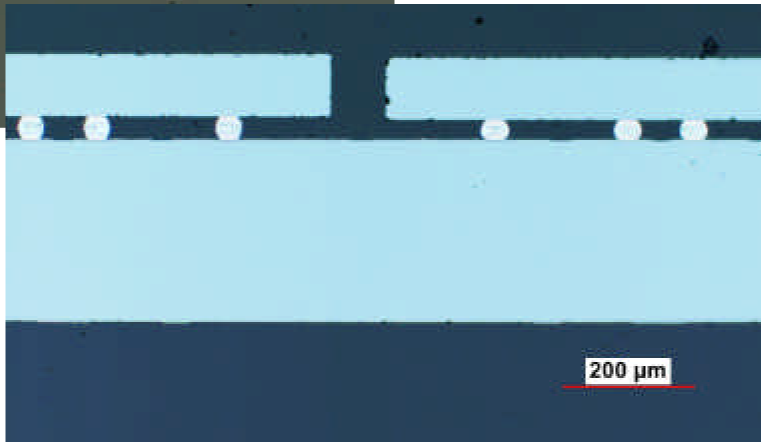
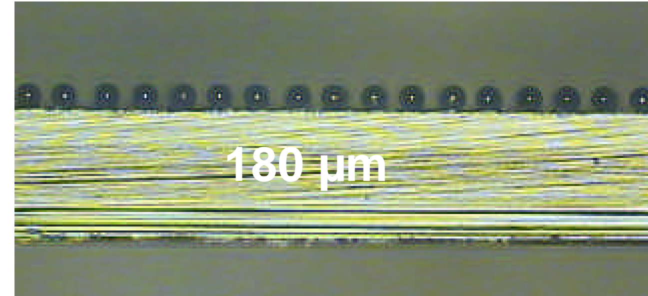
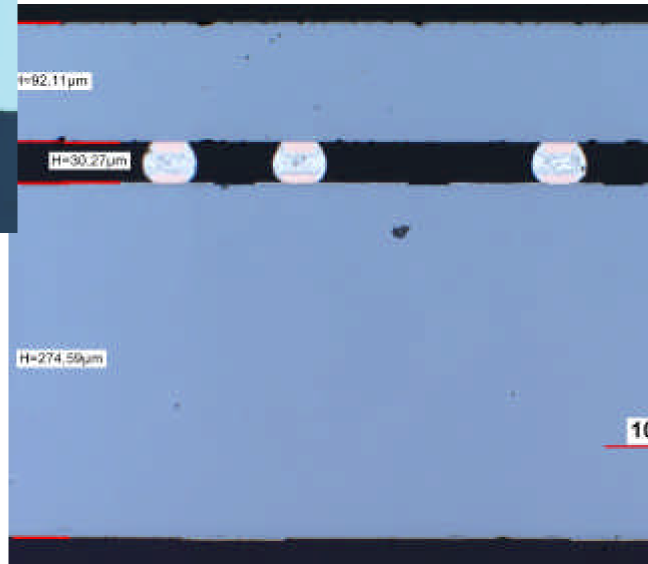
Future Requirements: Thin Silicon

hinning of bumped wafers:









m FE Chips
ssembled

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Handling of thin Wafers

- Support Wafer
- Support Foils
- Mobile Electrostatic Carrier

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Mobile Electrostatic Carrier Technology

h temperature removable
rier technology
 to 400°C)

nning, plasma-CVD,
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 wafers

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mobile ESC

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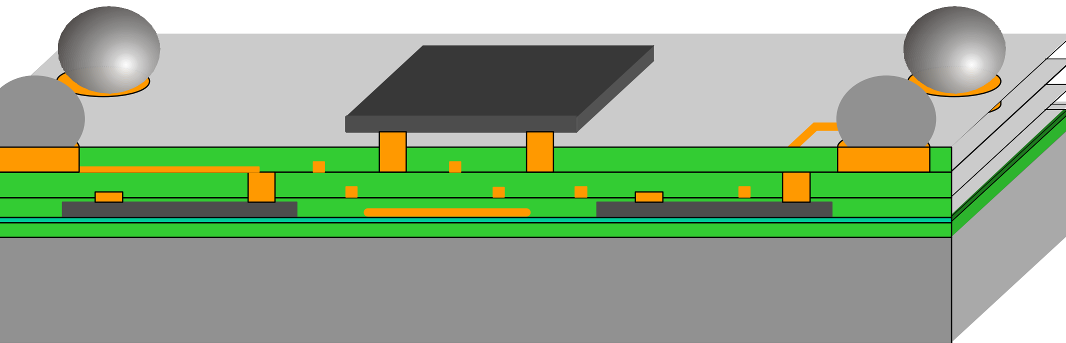
/L Thin Chip Integration –Basic Characteristic

icon on silicon

e thickness (embedded): 20µm- 50µm
add prepar of I/O pads (e.g.Cu)
electric: BCB
etallization: ep.Cu (5µm)
erlayer dielectric thickness: 5 µm



Layer configuration TCI:

dielectric
silicon
- polymer dielectric
- metal (RDL, passive #1)
- polymer dielectric (pas)
- metal (passive #2)
- polymer dielectric

metal (UBM)
solder ball (leadfree)

Flip Chip

- bumped thinned silicon
- leadfree soldering

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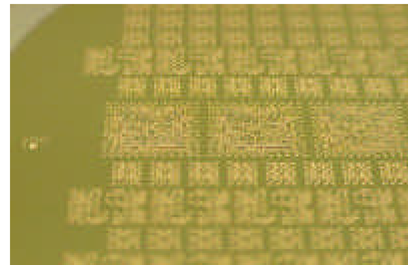

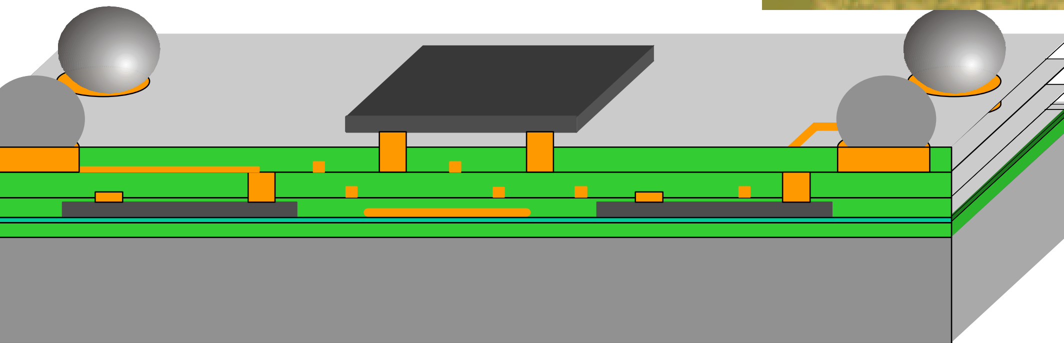

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Flip Chip
- bumped thinned silicon
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Fraunhofer Institut
Zuverlässigkeit und
Mikrointegration

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E-Mail: oswin.ehrmann@izm.fraunhofer.de

TCI - Processflow

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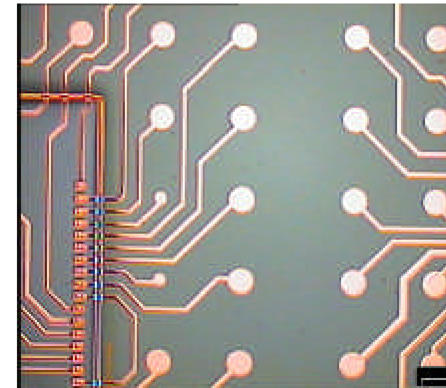
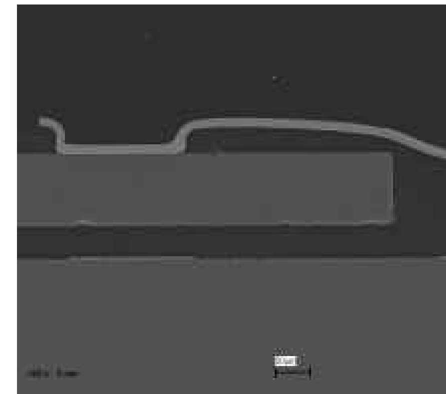
Thin Chip Integration on Wafer Level

Silicon Chip/Wafer





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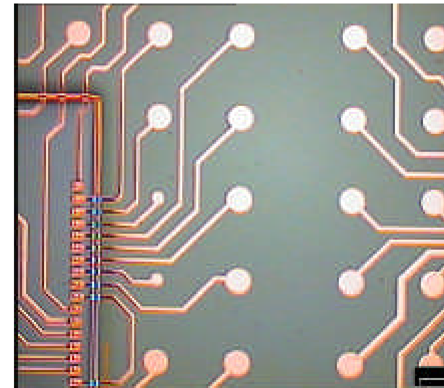

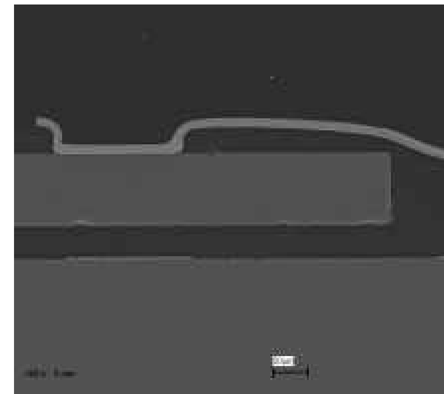

thin chips [40 µm]
embedded into redistribution BCB/Cu

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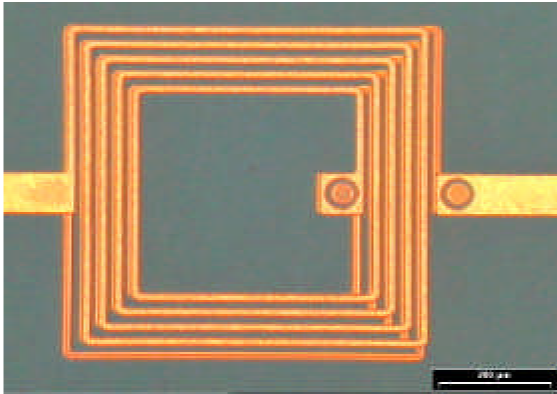
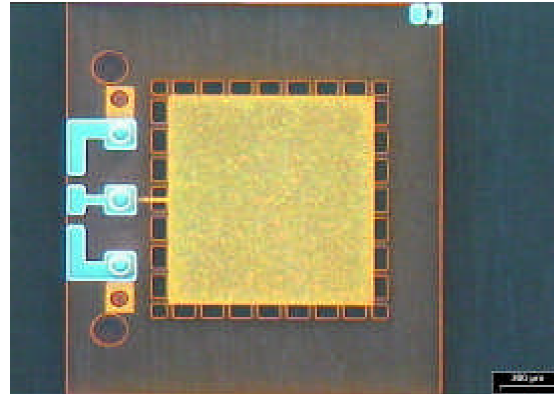
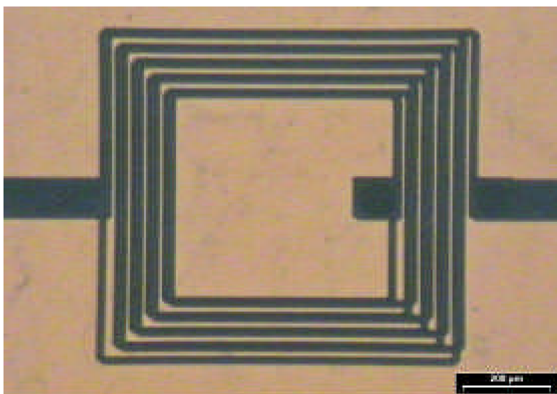
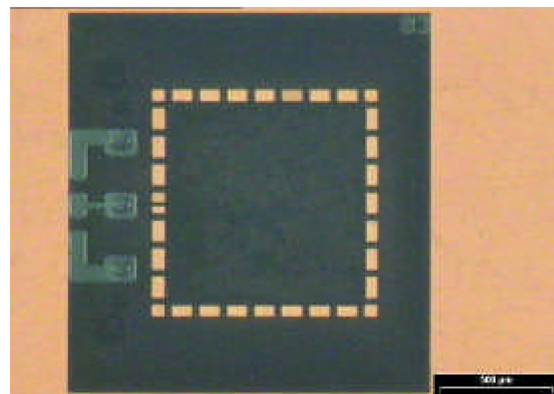
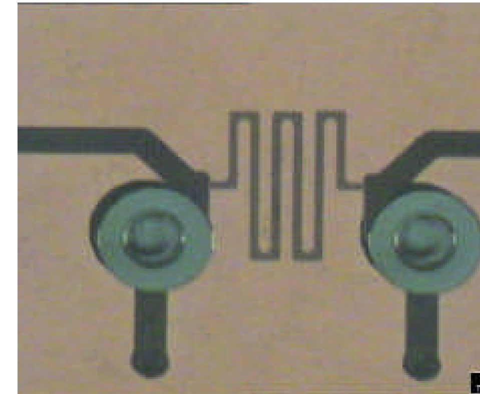
Cu / Polyimid Technology

	Coils	Capacitors	Resistors
de ation			
Side ation			
	L= 1 nH – 80 nH	**C= 0.3 pF – 4.5 pF**	**R= 100 W– 125 kW**

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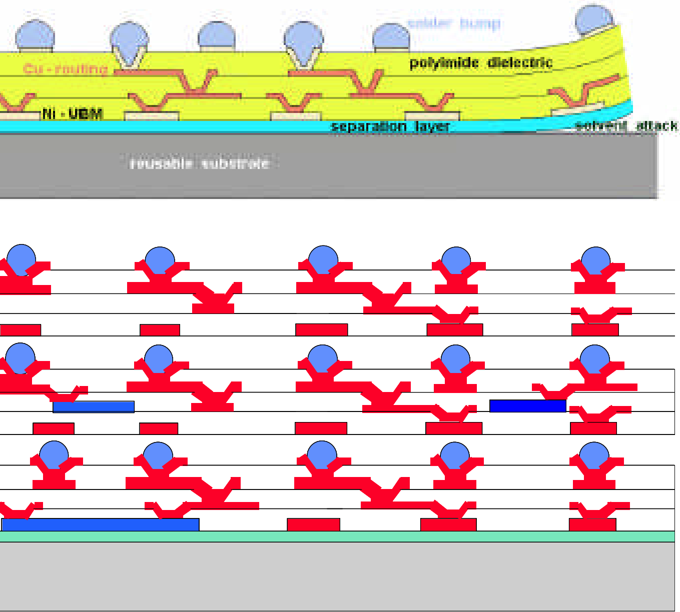
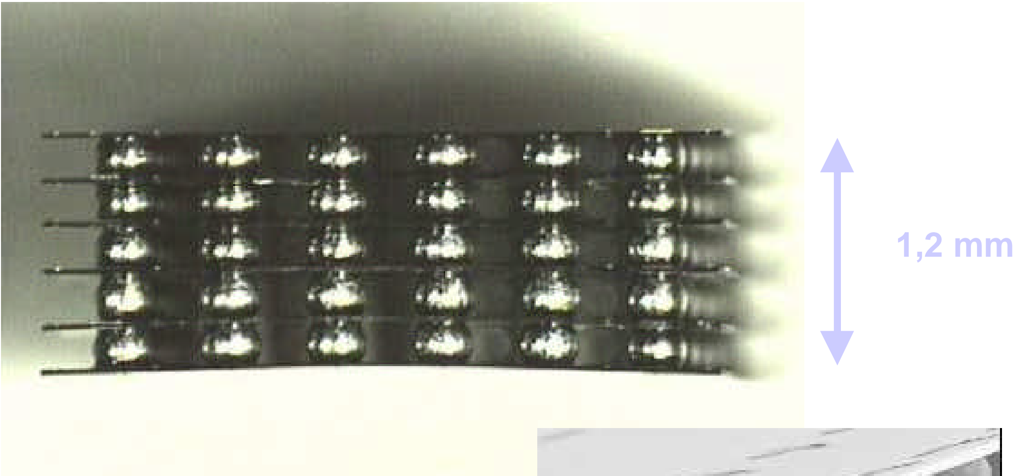
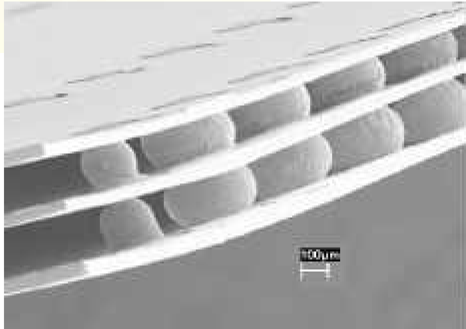
Stacked flex layers with vertical solder joints





Flex-stack - 6 layer



n polyimide layers with a 2-layered Cu-routing and integrated passive devices R, L, C

cked and interconnected with 200 µm solder balls

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3D - Stacked Silicon Systems with Embedded Thin Chips

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SV

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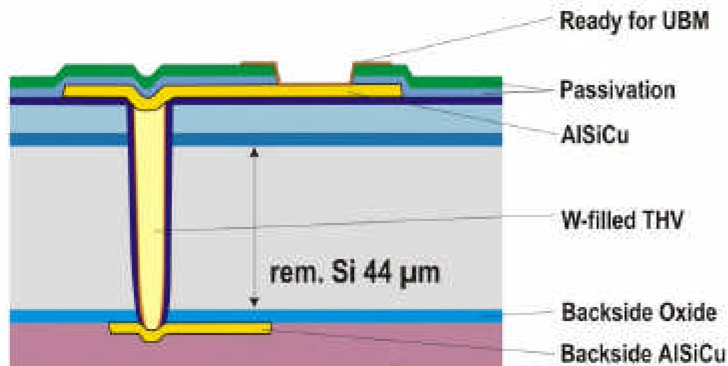
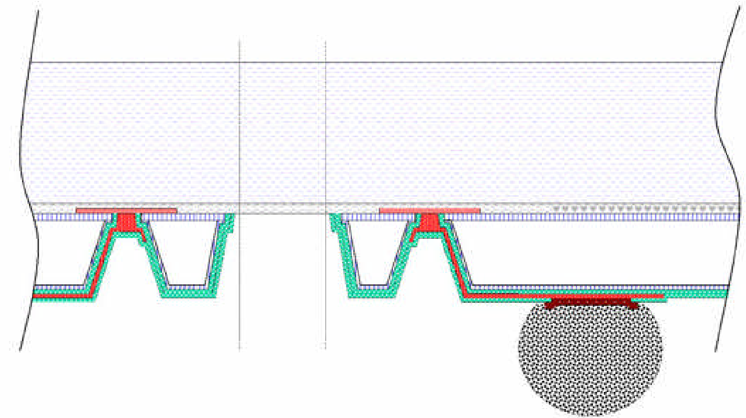
ough Silicon Vias: Basic Questions

Wafer Front Side Processing - Wafer Back Side Processing





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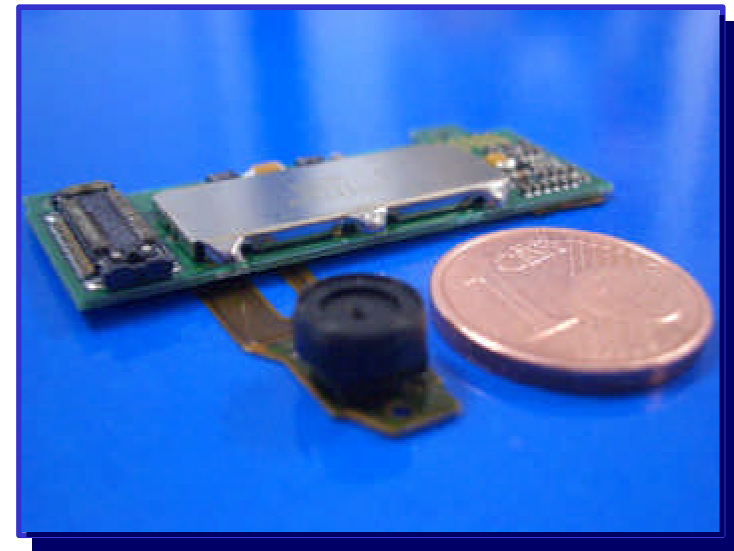
Camera Module

Lens Barrel
Lens 1
Lens 2
Mount
IR Filter
Image Sensor
Substrate
Solder Joints
Flex Circuit

Taken from: www.nokia.



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Wafer-Level-Packaging for Optical Applications

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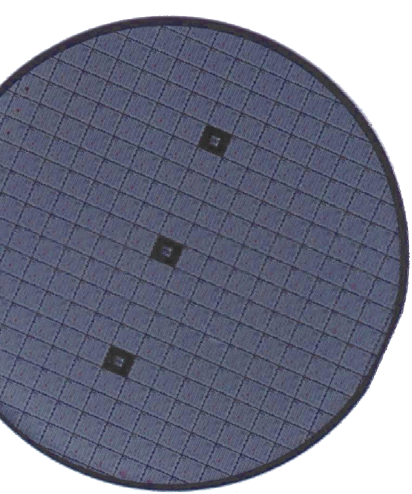
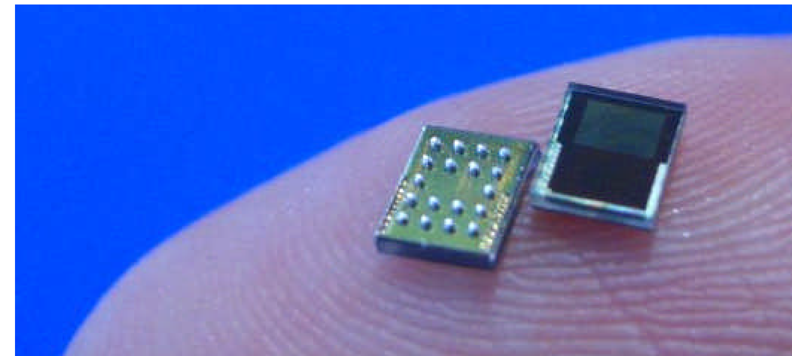


Process Flow



major process steps
different machines

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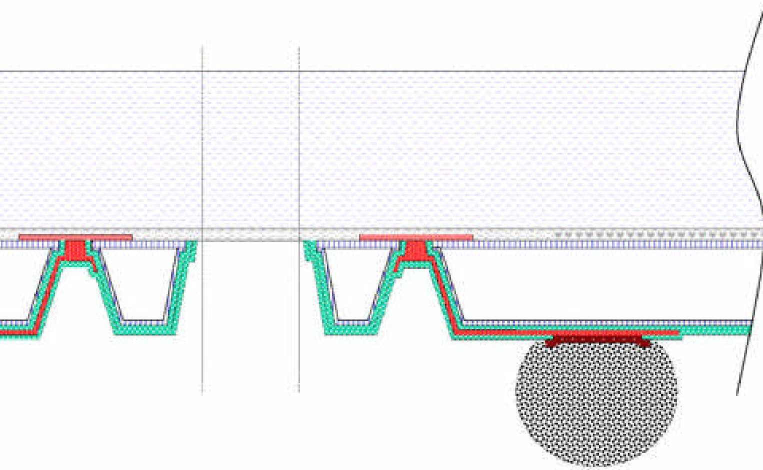
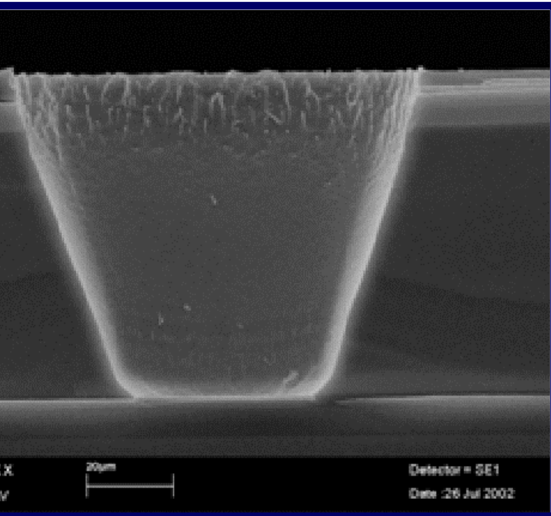
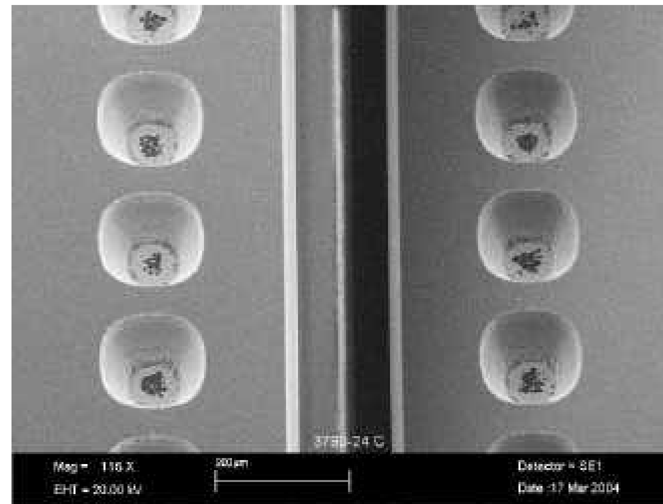
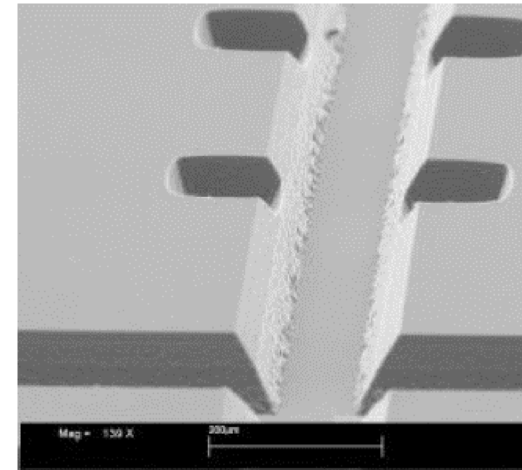
Wafer-Level-Packaging for Optical Applications



- **Tapered Vias & Streets**
- **controlled sidewall angle for sribe line**
- **controlled sidewall angle for via holes**







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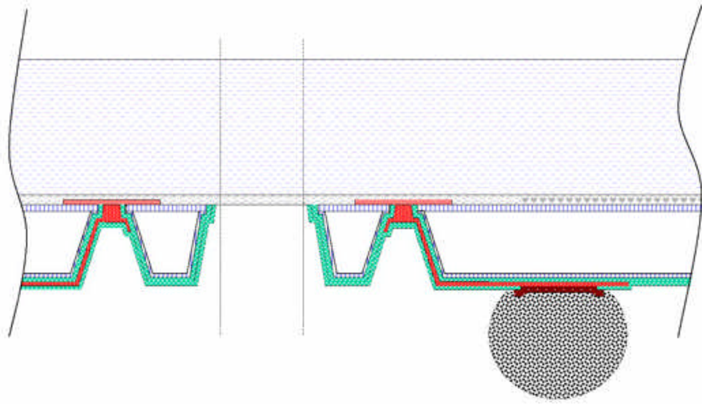
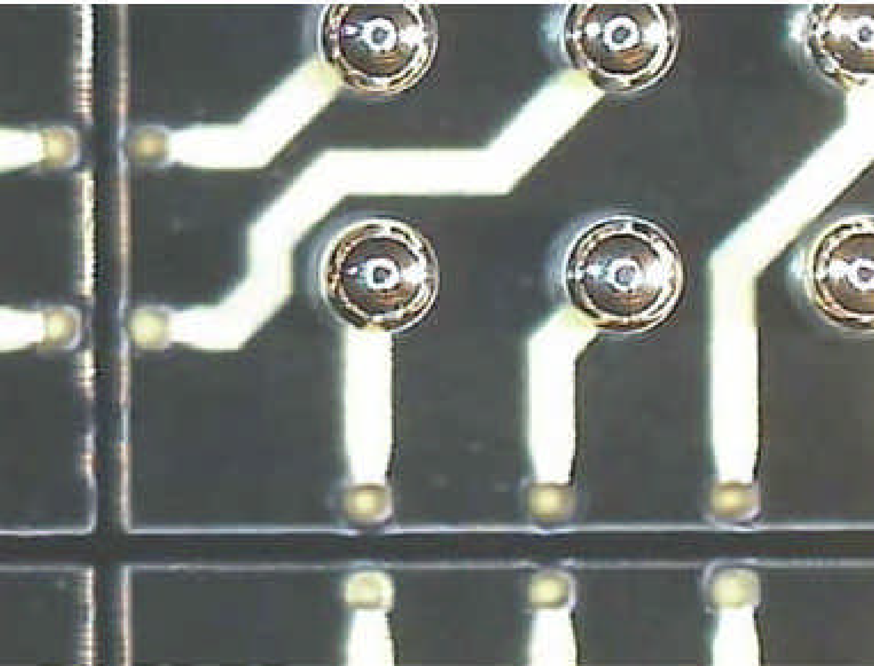
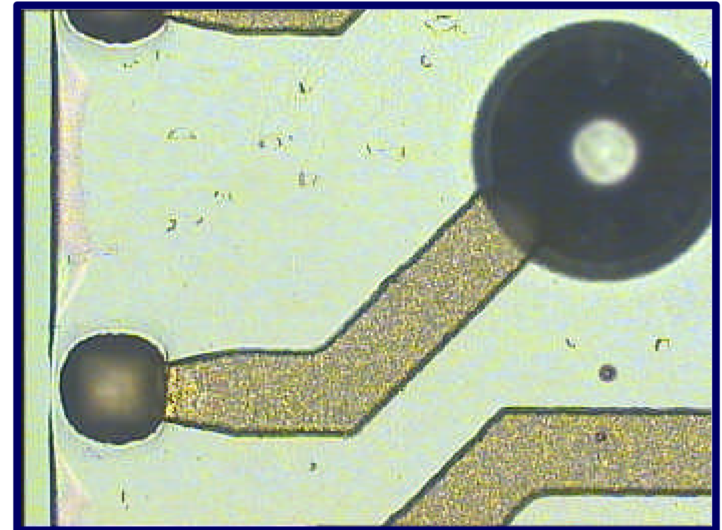


Ball Grid Array on the backside with Silicon Via Contacts





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Wafer-Level-Packaging for Optical Applications

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TSV – Formation and Metallization

- Deep Via High Aspect Ratio Etching (h >20 µm – 150 µm)
- Side Wall Insulation
- Deposit Seed- and Barrier Layers
- Via Filling by W-CVD/
- Via Filling by Cu-Electroplating
- Via Filling by Cu - CVD

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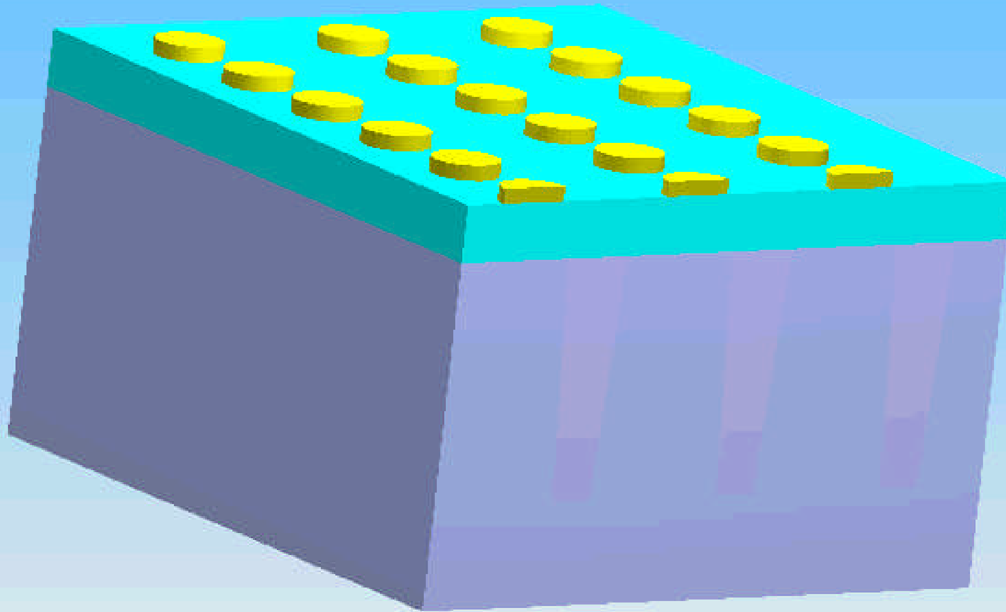
Back End Process Flow Through Silicon Via



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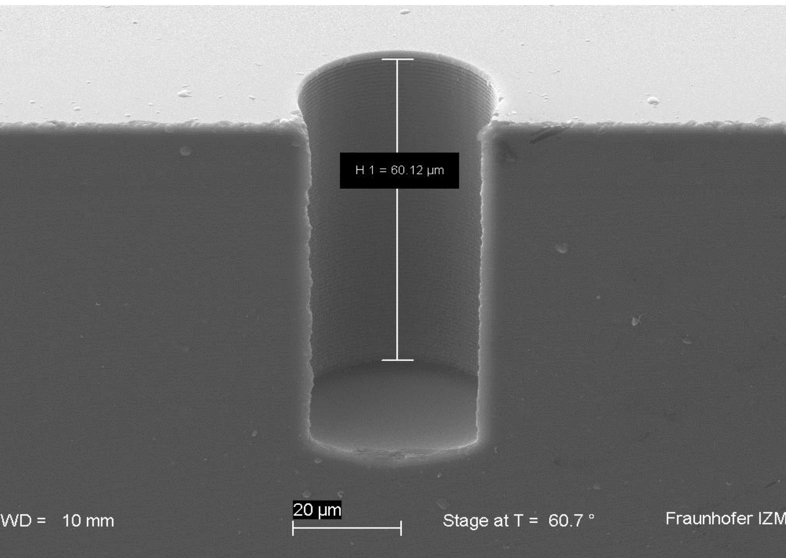
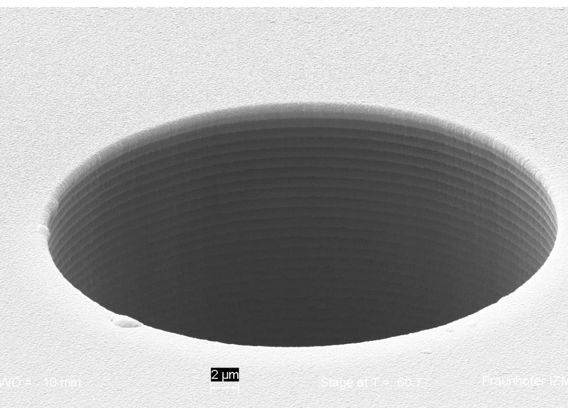
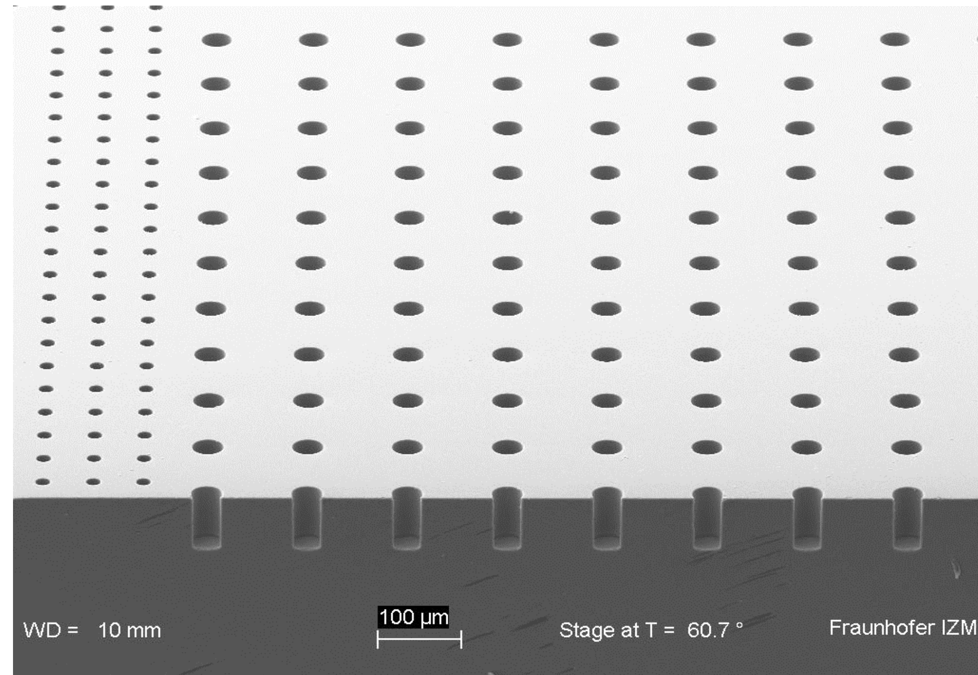
Deep Via Etching
TSV- Test Device – different Via Sizes



40 µm Vias
80 µm pitch
depth: 60 µm
CVD-Oxid: 120 nm





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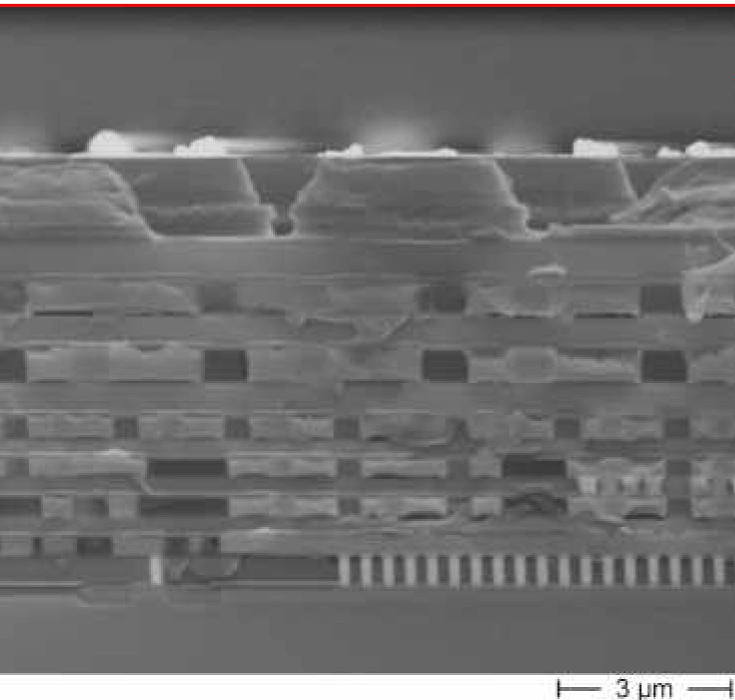
Via Etching

SEM of 54 µm deep TSV

10 x 3 µm (nominal size)

etched in Product-test chip of IFX



7,11 µm

53,72 µm

TSV

IFX 070901 Dem 1 #06

20 µm

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W- Fill of High Aspect Ratio Trench

ICV-Dimensions:
3 µm x 10 µm x 50 µm

300 nm SACVD TEOS
20 nm TiN CVD
900 nm W CVD und W Backetch
800 nm M1 (AlSiCu, structured)
850 nm PN/POX (Passiviation)

Trench #11

10 µm

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CVD TiN (60 nm)

Oxide (150 nm)

x50000 500nm 1.00kV 3mm
#9002 TUC/ZfM/Henker 18466
512 x 512 18466-01.TIF

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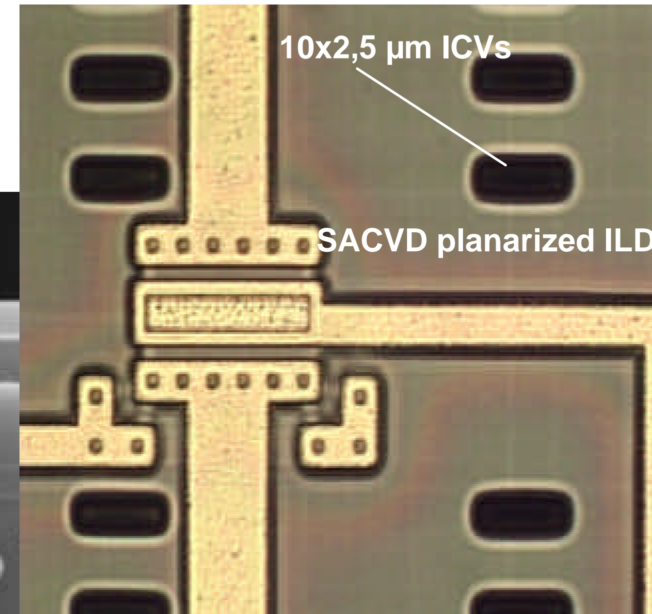
CMOS Top Wafer prior to Thinning



TEOS
M2-AlSiCu
TEOS
Therm. Oxide
O3/TEOS Spacer
MOCVD-TiN/W
2µM 20KV 18 026 S

10µM 20KV 18 026 S

- ICVs 10 x 2,5 µm,
  20 µm deep, AR 8:1
- Distance between W-filled
  ICVs and Transistors:
  ~ 4 µm to Source/Drain Ar
  ~ 11 µm to Gate Area

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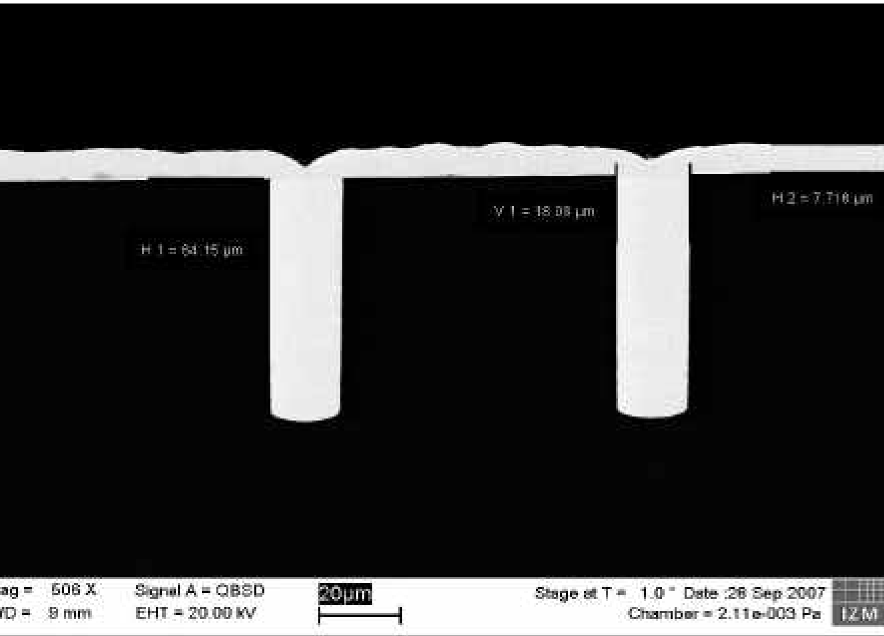
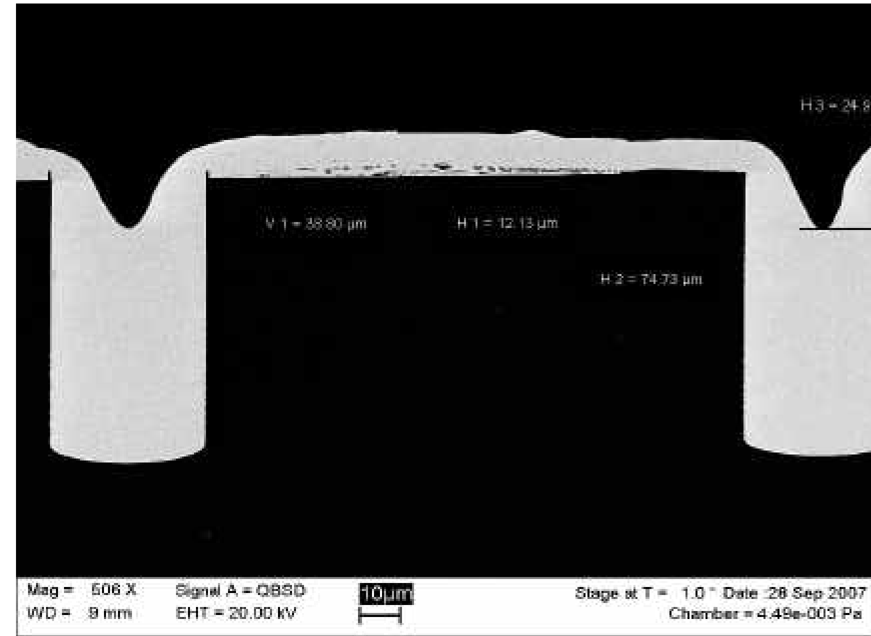
Cu-TSV using ECD



TSV. diameter 18 µm, 65 µm depth



TSV. diameter 38 µm, 75 µm depth

Cu Filled TSV by Electrodeposition Seed layer W-CVD

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Cu-TSV using ECD

H 1 = 7.209 µm

V 1 = 16.22 µm

V 2 = 36.27 µm

µm

µm

µm

H 2 = 63.30 µm

H 3 = 72.77 µm

Mag = 509 X Detector = QBSD 20µm
WD = 9 mm EHT = 20.00 kV

Stage at T = 0.0 ° Fraunhofer IZM
FIB Imaging = SEM Date :19 Sep 2007

Cu Filled TSV by Electrodeposition
(Via Size. diameter 18/35 µm, depth> 60 µm; Seed layer sputtered T.W/Cu

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Cu-TSV using Electro Plating

Cu Filled TSV by Electrodeposition
(Via Size. diameter 15 µm, depth> 60 µm; Seed layer sputtered T.W/Cu

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rough Silicon Vias: Via Filling

opper CVD

Y 2.5u

X 2.0u

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Wafer Level Assembly

CMOS Wafer Stack, ICV-SLID

ICVs

Top Si

Cu_3Sn

Bottom Si

20 µm

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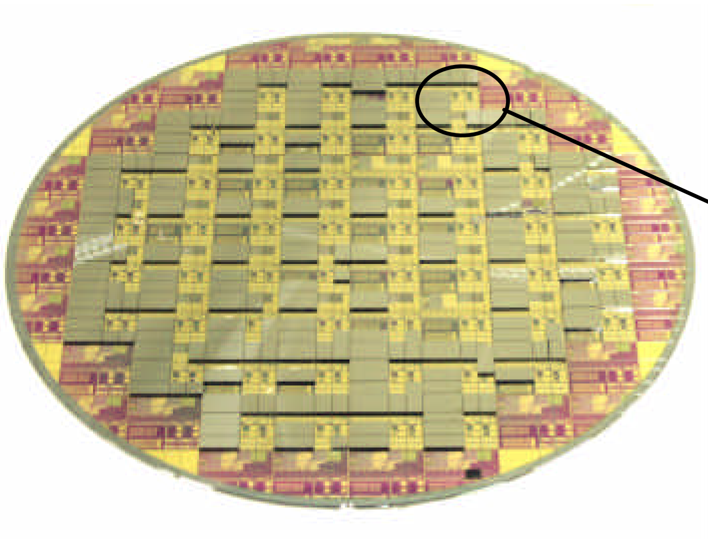
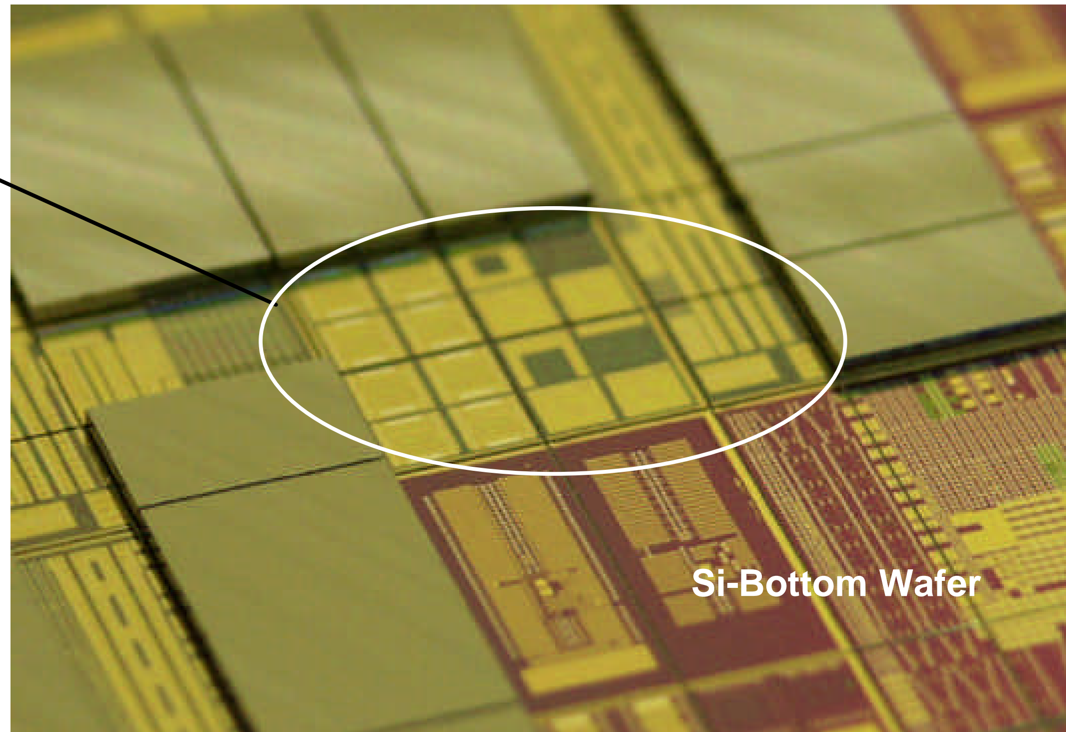
Chip-to-Wafer Bonding of thin Chips with Support Die





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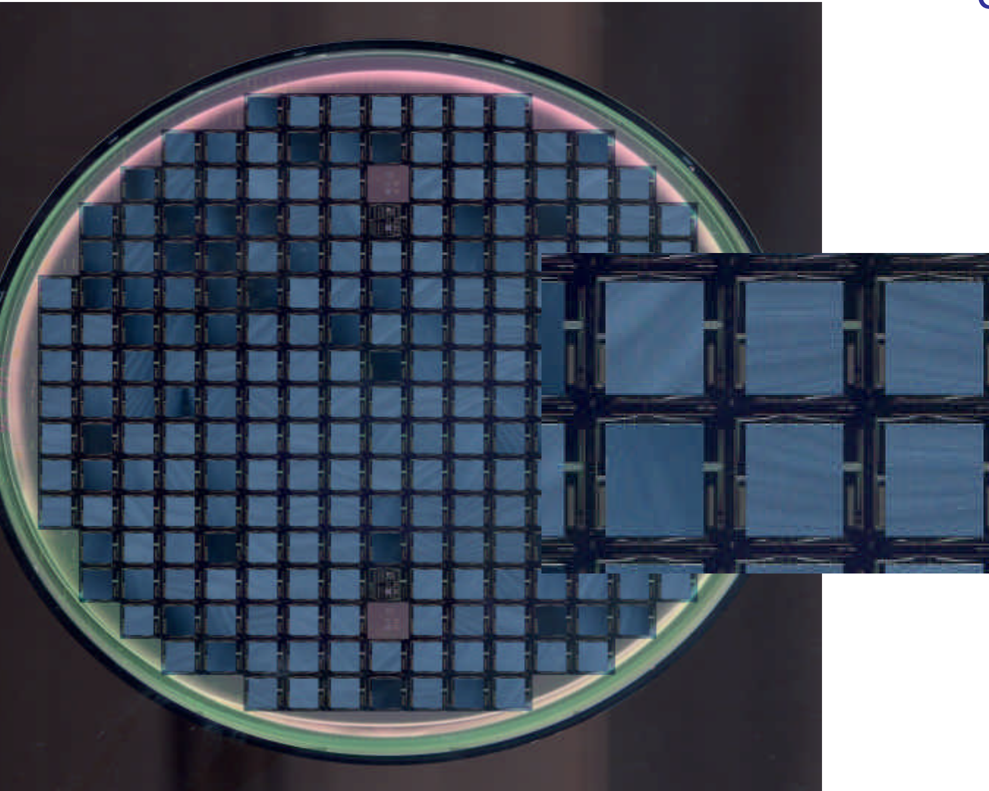
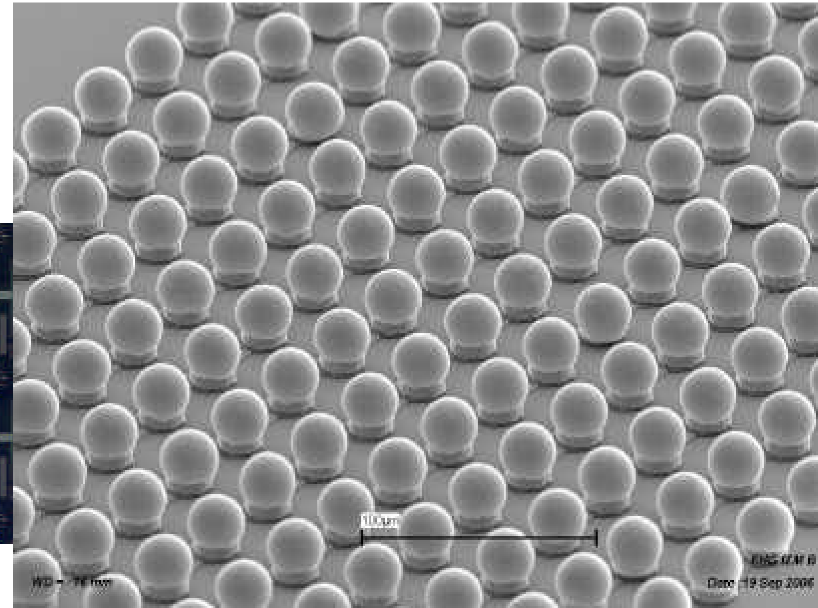
Wafer Level Assembly FC-Modul with TSV

250 Si devices (d~200 µm)
with SnAg Bumps (20µm, 13264 IO´s/die)
on Si Substrate with Trough Si-Via´s





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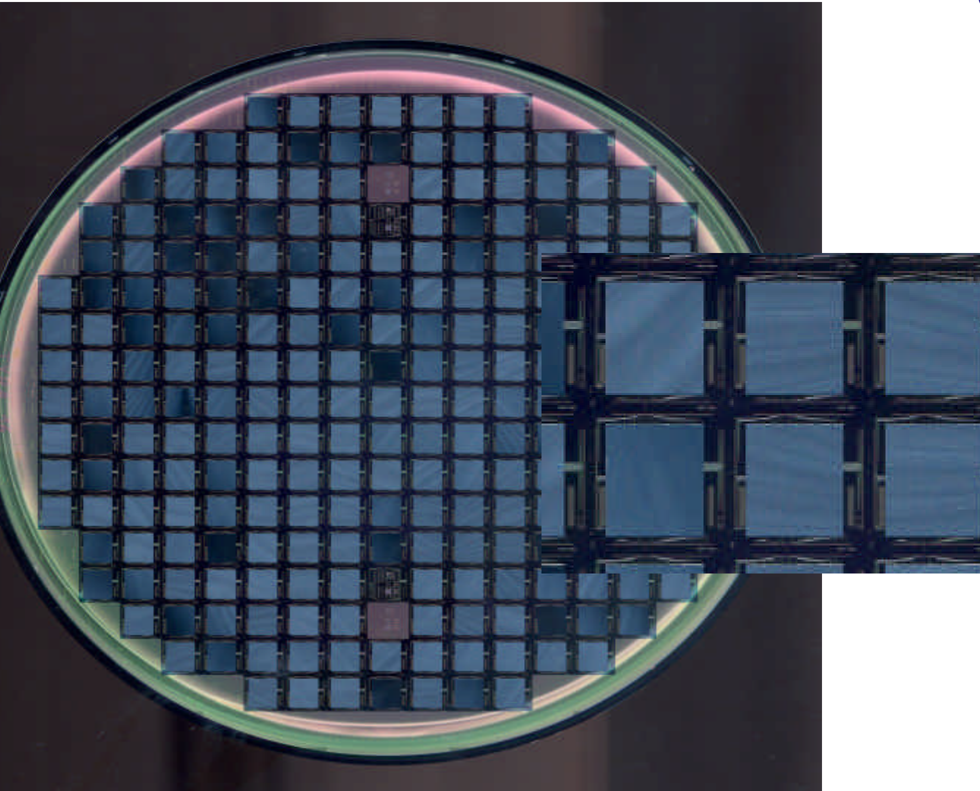
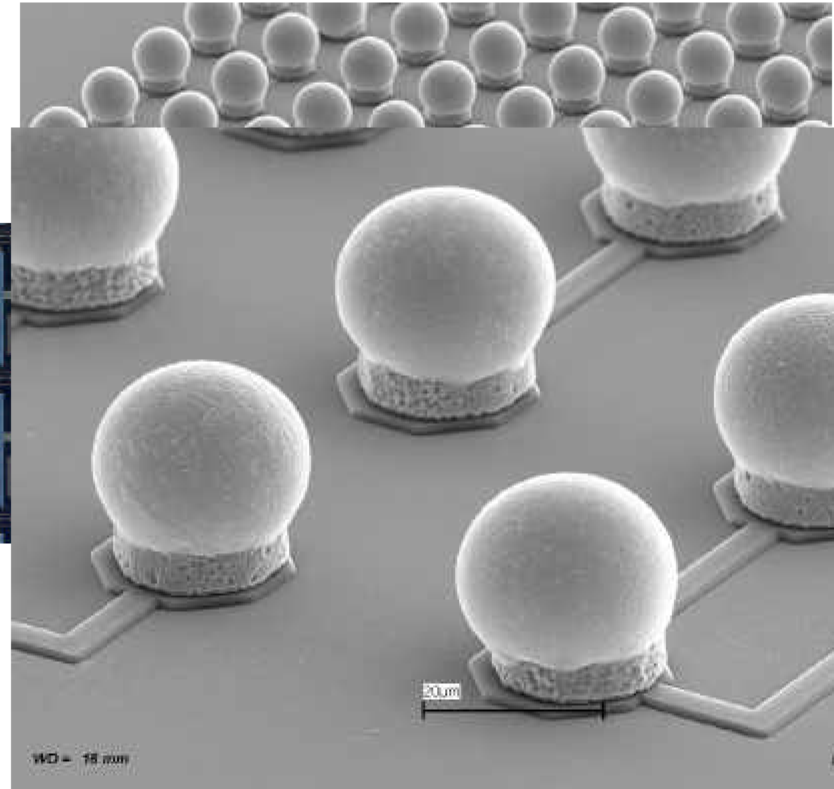
Wafer Level Assembly FC-Modul with TSV

250 Si devices (d~200 µm)
with SnAg Bumps (20µm, 13264 IO´s/die)
on Si Substrate with Trough Si-Via´s





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Wafer Level Assembly - FC-Modul with TSV

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Wolf, Oppermann

WL Assembly

FC of thinned die on 8“ Wafer

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Pixel Detector related 3D Developments:

TSV for FE Dies

TSC for MPEC Dies

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EMC 3D Industrial Consortium

Memb

Equipment

Materials

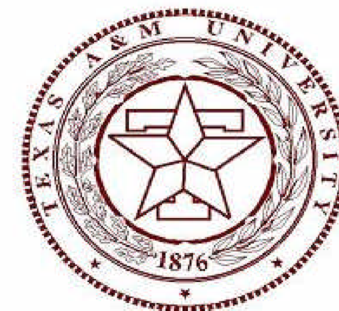
(Wafer Service)

Technology

Fraunhofer Institut Zuverlässigkeit u
Mikrointegration

SAMSUNG ADVANCED INSTITUTE OF TECHNOLOGY

Leading the Next



Founders

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thank you for your attention

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TSV Formation / Metal Filling

0 µm	3.5 µm	5 µm	10 µm	....	100 µm	Via-Diameter

CVD of
- copper
- tungsten
- TiN

Electroplating of
- copper

&

PVD of Seedlayer
- Ti:W / Cu

Processes for Via Ho Filling

10 µm		70 µm	....	100 µm	Via-Depth
0:1 3:1	2:1	7:1		1:1	Aspect Ratio

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