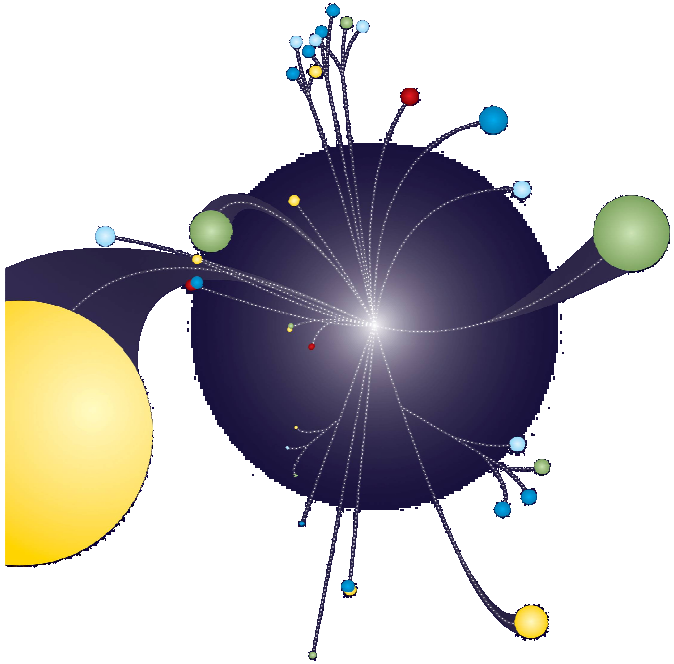
3D Integrated Technology at Fermilab

Activities and Plans



Marcel Demarteau

For the Fermilab Detector & Physics R&D Group

3D Integrated Technologies Perspectives
First workshop on LHC-ILC prospects
November 29-30, 2007

Fermilab

- Located in the western suburbs of Chicago, Illinois, on 2750 hectares site
- 1950 employees; 2500 users of whom 1000 from abroad
- Currently highest energy machine in the world: the Tevatron
- Currently highest intensity neutrino beam in the world
- A world class astrophysics program

- **Fermilab's Scientific Program**
  - Energy Frontier
  - Neutrino Frontier
  - Particle Astrophysics

- The only US lab. solely devoted to particle physics

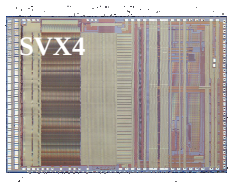
Fermilab Organization

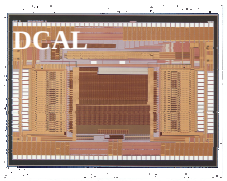
- **Most of the detector R&D carried out in the Particle Physics Division**
  - **~150 physicists associated with experiments**
  - **84 employees in Mechanical Department**
    - 12 designers/drafters
    - 28 engineers
  - **54 employees in Electrical Department**
    - 6 ASIC designers
    - 6 ASIC testing engineers

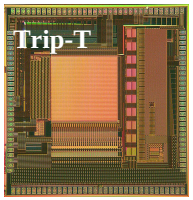
- **R&D supported by user facilities**
  - **Silicon Detector Facility**
    - 4000 sq. ft of cleanrooms
    - Wirebonding facilities
    - Large number of coordinate measuring machines
  - **Test Beam Area**
    - Energy range
      - protons: 1 – 120 GeV
      - pions: 1 – 66 GeV
      - $e^{\pm}$: 1 – 35 GeV

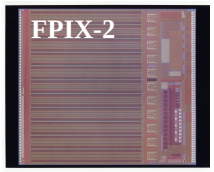
Past Projects

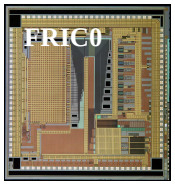
- **ASIC Designs for silicon strip and pixel detectors, digital calorimetry, trigger pipeline, voltage control and generation and monitoring**
  - **CDS, analog pipelines, Wilkinson ADCs, data sparsification**

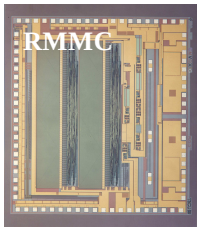




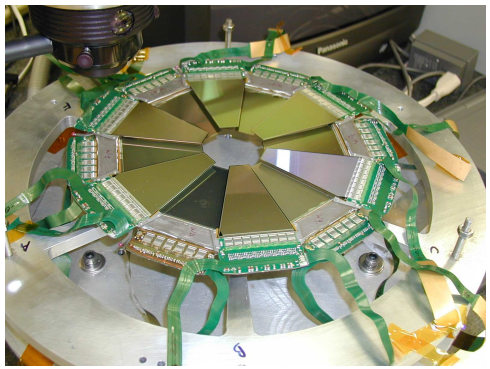


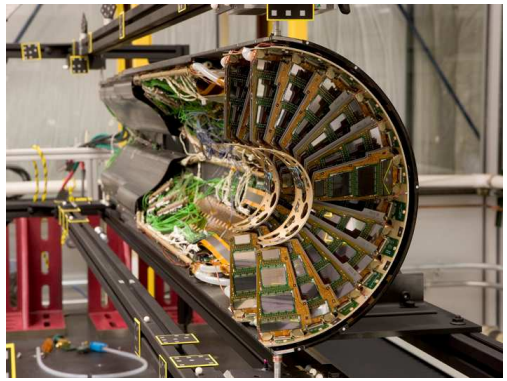


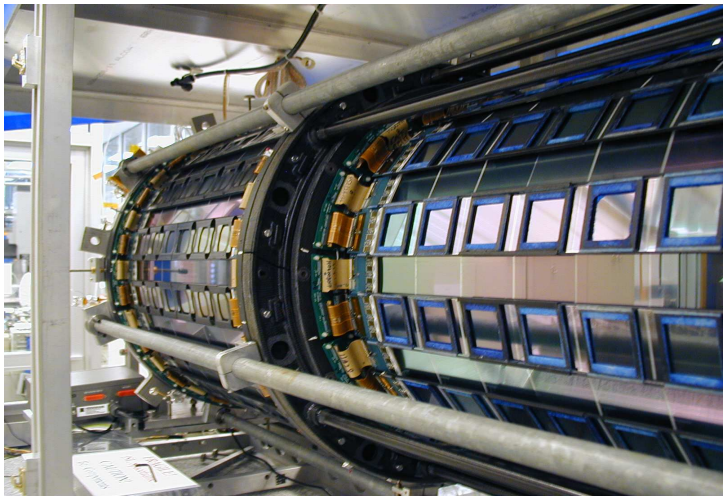


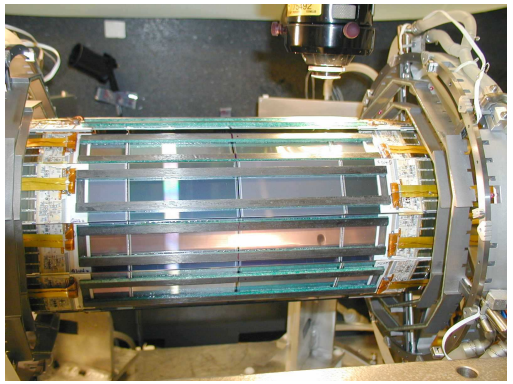


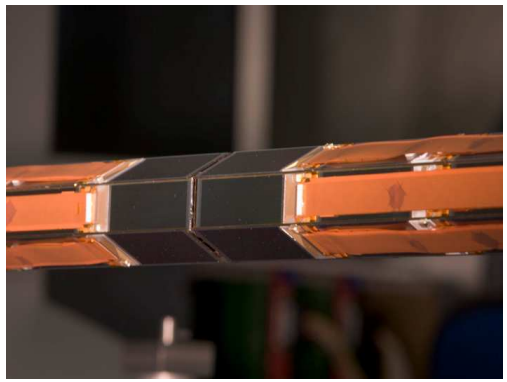
- **Silicon Strip and Pixel Detectors**











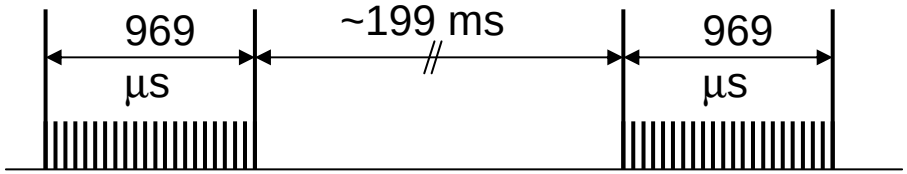
Fermilab Perspective

- **Our philosophy: detector R&D that is of high enough caliber will be applied in any future experiment**
  - **Focus on what we believe are the most promising technologies**
  - **Build on our significant strength and strong expertise in engineering for silicon particle detectors – both electrical and mechanical**
  - **All detector R&D is carried out with a long time scale in mind and within a broad context: ILC, LHC upgrade and applications beyond**
  - **Adopt a fully integrated approach: sensor development, associated readout, power delivery, mechanical support, beam tests**

- **Fermilab effort in 3D Integrated Technology**
  - **Context of our initial effort: ILC challenge**
  - **3D and SOI**
    - **SOI Technology**
    - **3D Technology**
  - **Thinned sensor R&D**
  - **Laser Annealing**
  - **Power distribution**
  - **Mechanical Support**

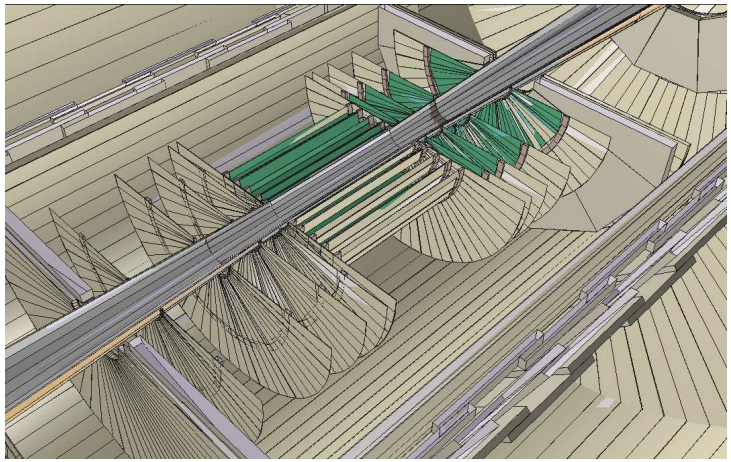
ILC Pixel Detector

- **Pixel detector requirements**
  - **Very low mass: 0.1% X_0 per layer (equivalent of 100 μm of Si)**
  - **Low power consumption (~50 W for 1 Giga pixels)**
  - **High resolution thus small pixel size**
  - **Modest radiation tolerance for ILC applications**



ILC Beam structure:
Five trains of 2625 bunches/sec
Bunch separation of 369.2 ns

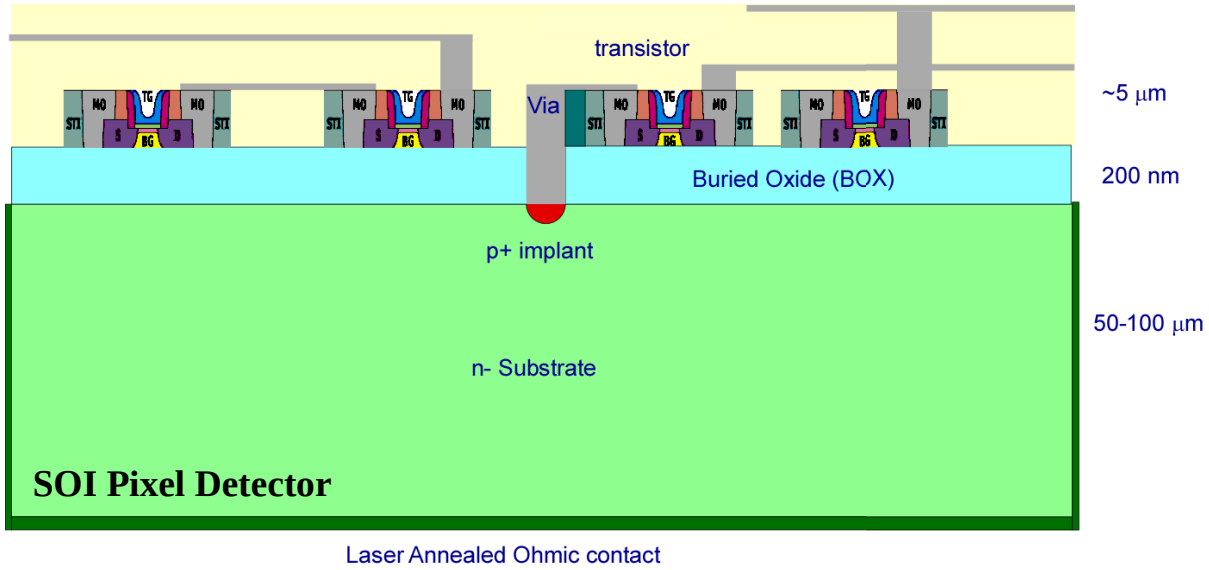
- **Combination of small pixels, short integration time, low power required for ILC is difficult to achieve**
  - **Small pixels tend to limit the amount of circuitry that can be integrated in a pixel**
  - **Small pixels also mean that the power/pixel must be kept low**



- **The low occupancy/pixel/train (~0.5%) means that a sparse scan architecture would be appealing if:**
  - **Signal/noise is high**
  - **Enough electronics can be integrated on a pixel**

- **We feel that the best prospects for an optimal vertex detector are the vertical integration (3D) and related SOI technologies. These offer the prospect of thin, densely integrated, devices with excellent signal/noise and low power. 3D also offers prospects for integration of power management into the pixel structure.**

SOI Detector Concept



Advantages

- 100% fill factor
- Large and fast signal
- Small active volume: high soft error immunity
- Full di-electric isolation: latchup free
- Low Junction Capacitance: high speed, low power

- **Bonded Wafer: low resistive top layer + high resistive substrate, separated through a Buried OXide (BOX) layer**
  - **Top layer: standard CMOS Electronics (NMOS, PMOS, etc. can be used)**
  - **Bottom substrate layer forms detector volume**
  - **The diode implants are formed beneath the BOX and connected by vias**
- **Monolithic detector, no bump bonds (lower cost, thin device)**
- **High density and smaller pixel size is possible**
- **Small capacitance of the sense node (high gain V=Q/C)**
- **Industrial standard technology (cost benefit and scalability)**

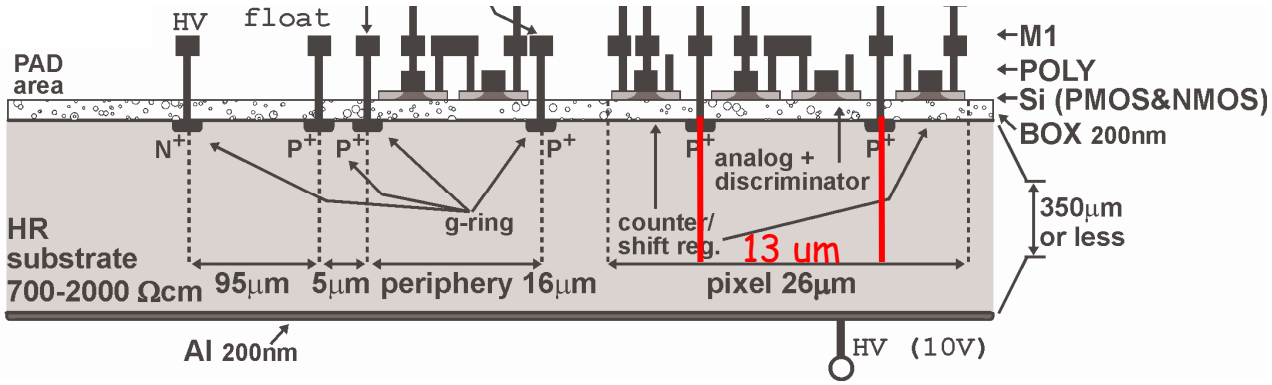
SOI Detector Development

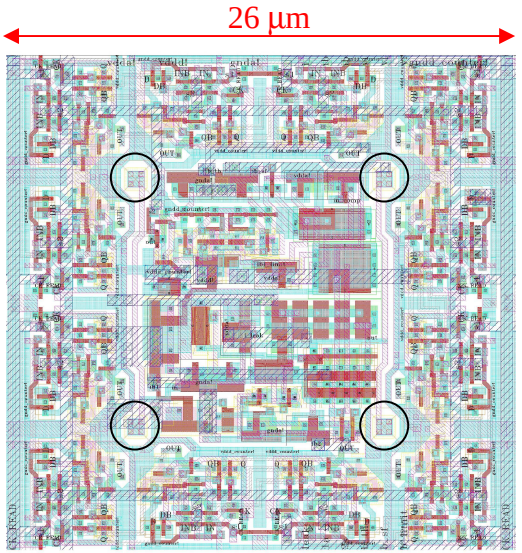
- **SOI detector development is being pursued by Fermilab at three different foundries:**
  - **MIT-Lincoln Laboratory through Multi-Project Wafer submission (DARPA funded)**
  - **OKI Electric Industry Co. Ltd. in Japan through Multi-Project Wafer submission (KEK)**
  - **American Semiconductor Inc. (ASI) in US, through SBIR phase I grant (Cypress semiconductor)**

	OKI	MIT-LL	ASI
Feature size (nm)	150 200	180 150	180
Wafer Ø	150 mm	150 mm	200 mm
Transistor type	Fully depleted	Fully depleted	Partially depleted dual gate
Buried Oxide	200 nm	400 nm	200 nm
Work underway	Test Struct. Mambo I Laser anneal	Test Struct. 3D chip	Conceptual design Simulation
Work planned	OKI: Mambo II	MIT-LL: 3D Run II 3D Dedicated	Test Structures Sensors

Pixel Design in OKI Process

- **MAMBO Chip: Monolithic Active pixel Matrix with Binary cOunters**
  - **A wide dynamic range counting pixel detector plus readout circuitry, sensitive to 100-400 keV electrons, high energy X-rays, and minimum ionizing particles, designed in the OKI 0.15 micron process**
- **OKI process incorporates diode formation by implantation through the BOX**
- **Chip architecture (simplified due to design time constraint): amplifier – shaper – discriminator – binary counter**
- **Design submitted Dec. 15, '06**
- **Chip delivered June '07**
- **Characterization of test structures underway**
  - **Array size 64x64 pixels, 26μmx26μm**
  - **13 μm implant pitch, to minimize the "back gate" effect**
    - 4 diodes per pixel
  - **350 micron detector thickness**

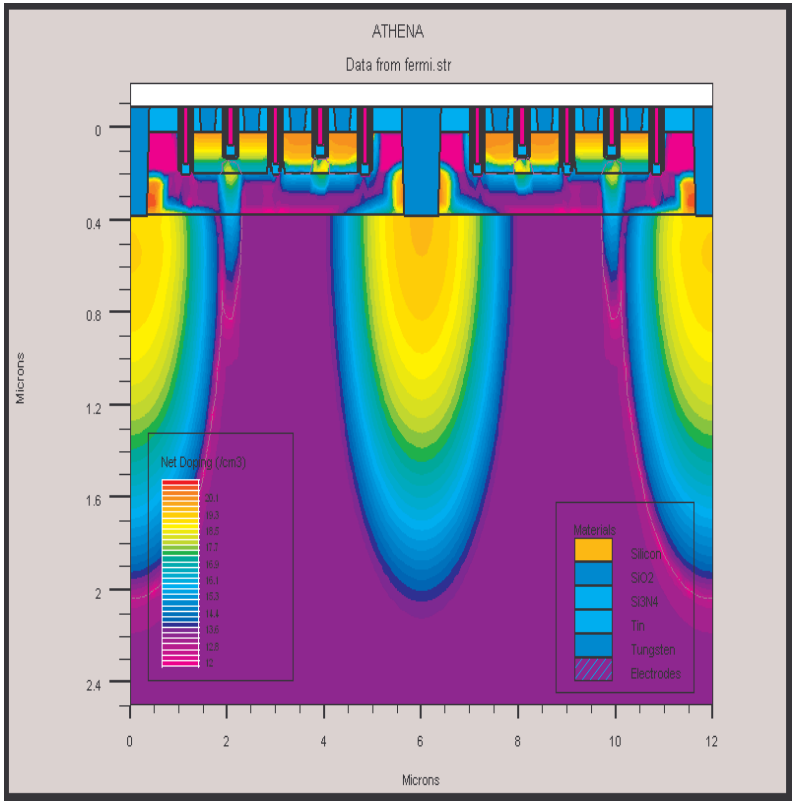




see talk by Ray Yarema

Pixel Design in ASI Process

- **SBIR Phase I grant with American Semiconductor (ASI), Boise, Idaho**
- **ASI process (0.18μm) based on an SOI dual gate transistor called a Flexfet™**
  - **Flexfet has a top and bottom gate**
  - **Bottom gate shields the transistor channel from**
    - Charge build up in the BOX caused by radiation.
    - Voltage on the substrate and thus removes the back gate voltage problem
  - **Modeling and process simulation of a thinned, fully depleted sensor/readout device.**
  - **Circuit design for ILC pixel cell**
    - Voltage ramp for time marker
    - ~20 micron analog pixel
    - Sample 1 - crossing time
    - Sample 2 - time over threshold for analogue pulse height information
    - Coarse time stamp



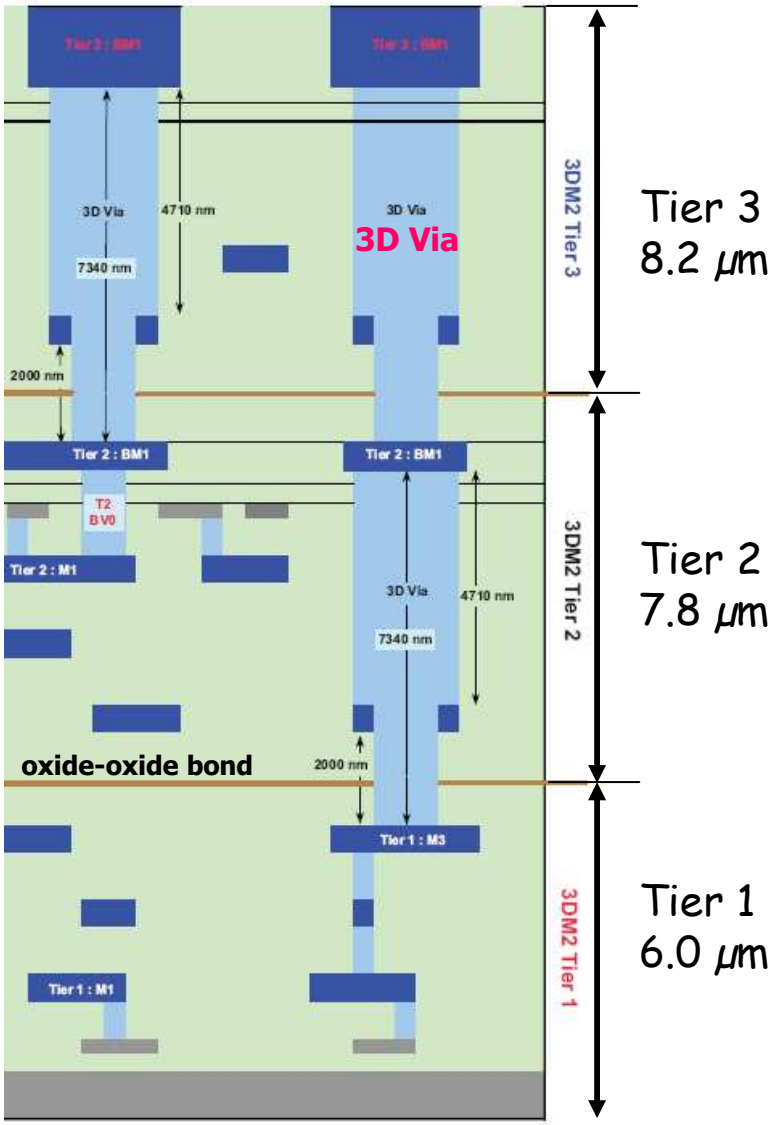
Diode simulation in Flexfet process

see talk by Ray Yarema

http://www.americansemi.com/

MIT-Lincoln Laboratory 3D Process

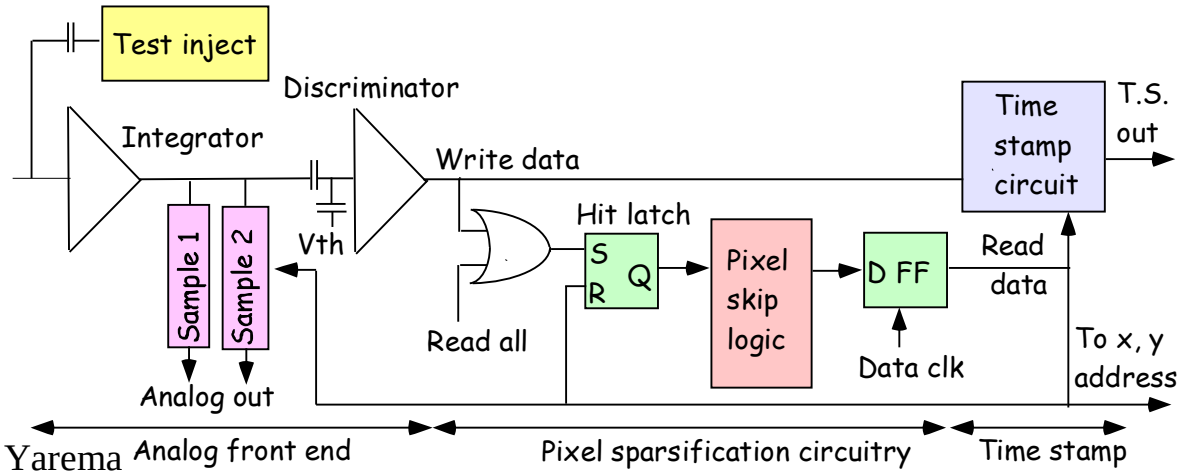
- MIT Lincoln Laboratories (MIT-LL) is a federally funded (Air force) research and development center of MIT
- It has developed the technology that enables 3D integration
  - Demonstrated the 3D technology through fabrication of imaging devices
- It offers a DARPA funded 3D Multi-Project Wafer Run
- We participated in the last MIT-LL three-tier multi-project run
  - 3D design to be laid out in MIT-LL 0.18 μm SOI process
    - SOI provides additional advantages: BOX, full isolation, direct via formation, enhanced low-power operation
  - 3 levels of metal in each layer
- VIP chip design submitted Oct. 15, 2006
- Pixel size 20 x 20 μm; 64 x 64 pixel array
- No integrated sensor



Pixel Design in MIT-LL Process

- **Design:**
  - **Analogue and binary readout information**
  - **Time stamping of pixel hit for ILC environment**
    - Divide bunch train into 32 (5 bit) time slices
  - **Sparsification to reduce data rate**
    - Use token passing scheme with look-ahead to reduce data output
      - During acquisition, a hit sets a latch
      - Sparse readout performed row by row with x- and y-address stored at end of row and column
  - **Chip divided into 3 tiers**
    - Design for 1000 x 1000 array but layout only for 64 x 64 array.
  - **Chip received Nov. 20, 2007; being tested**

- **First design which, in principle meets 'all' of the ILC requirements for thickness, resolution, power dissipation, time stamping**
  - **Power is 0.75 microwatt/pixel ~ 18.75 microwatts/mm^2 (after pulsing)**
  - **Noise is ~30-40 e$^-$**
  - **S/N = 100-200:1**



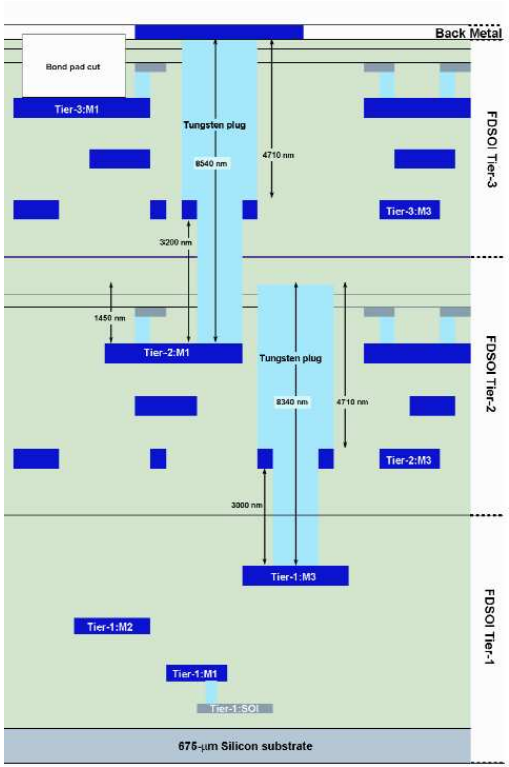
Schematic pixel cell block diagram

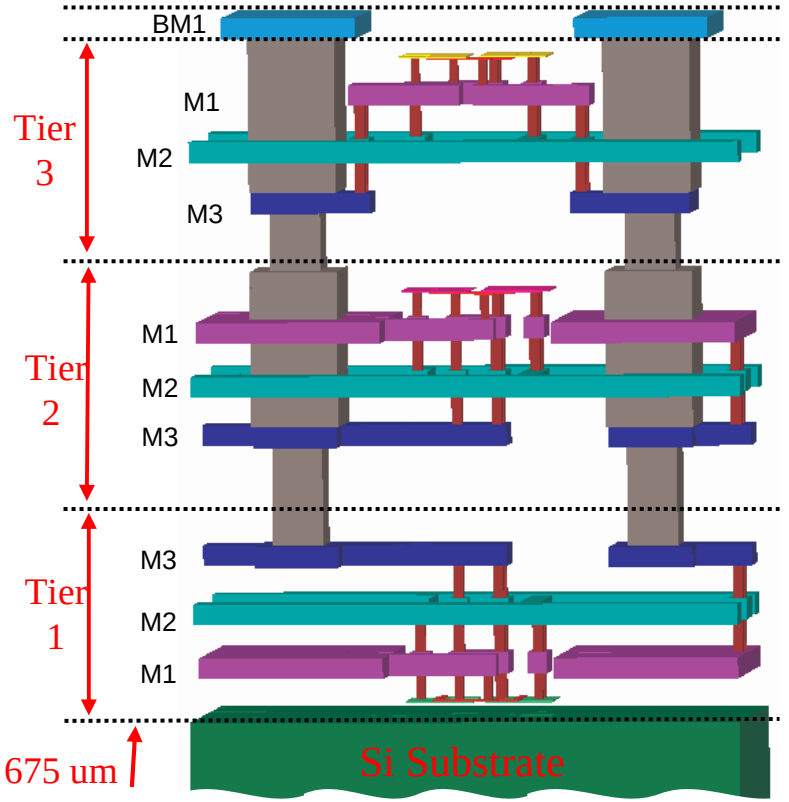
see talk by Ray Yarema

Modeling 3D Circuits

- **Applied for an SBIR Phase I grant with CFD Research Corporation (www.cfdrc.com) to develop automated design tools for detector and electronics integration which will allow the extraction of physical parameters of these devices based on the integrated circuit layout**
  - **Modeling and analysis of radiation effects**
  - **Modeling of thermal and mechanical properties**

MIT-LL 3D Layer Description

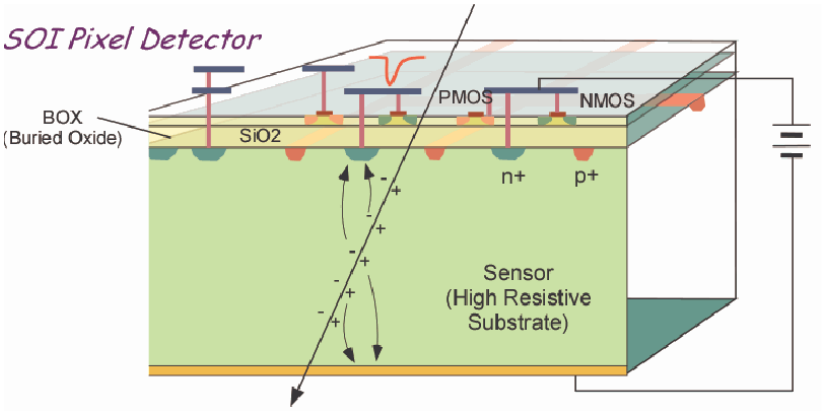




CFDRC Full 3D Model

Towards Integrated Detectors

- In the SOI process, the handle wafer can be high quality, detector grade silicon: integration of electronics and fully depleted detectors in a single wafer with very fine pitch – our ultimate goal
- In our applications the detector layer is at most 50μm thick

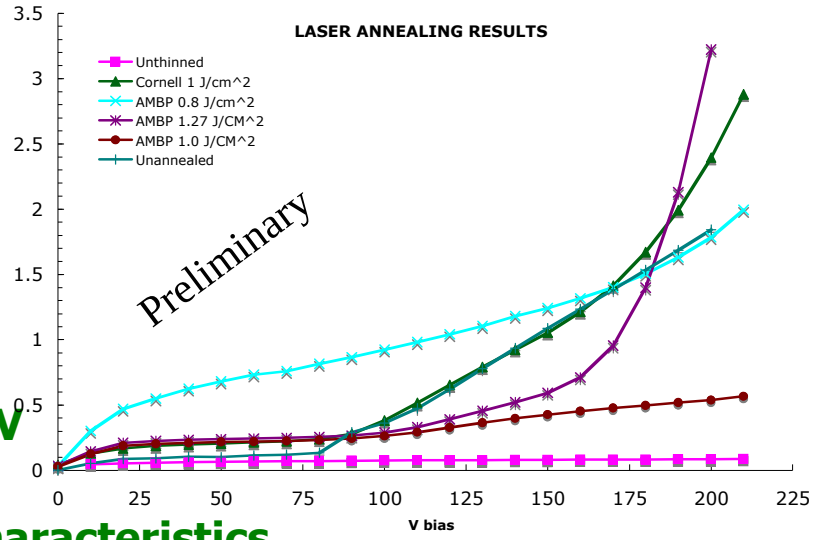


- Sensor Issues:
  - SOI processes which include processing of the handle wafer as part of the fabrication process often need thinning of the backside
  - After thinning a backside contact must be formed.
  - The current MIT-LL MPW run did not provide us with a detector tier

- Sensor R&D
  - Laser annealing
  - Development of edgeless sensors
  - Device bonding

Laser Annealing

- **Problem: After thinning provide a backside Ohmic contact while keeping the topside below ~500 deg C to protect topside CMOS SOI circuitry**
  - **Usually done by implantation and high temperature furnace annealing**
- **We, in collaboration with Cornell University, are developing a laser annealing capability of backside implantation:**
  - **Use a raster scanned Excimer Laser to melt the silicon locally**
    - This activates the Ohmic implant and repairs the implantation damage by recrystallizing the silicon
- **Study and qualification of process**
  - **300 μm thick silicon strip detectors (Hamamatsu), 4x10 cm^2 with low leakage current**
  - **Backgrind by ~50 microns to remove back implant and aluminization**
  - **Polish, re-implant detector using 10 KeV phosphorus at 0.5 and 1.0x10^{15}/cm^3**
  - **Laser anneal and measure CV and IV characteristics**
    - AMBP - 0.8, 1.0, 1.2 J/cm^2, 248 nm laser
    - Cornell - 1.0 J/cm^2 305 nm laser



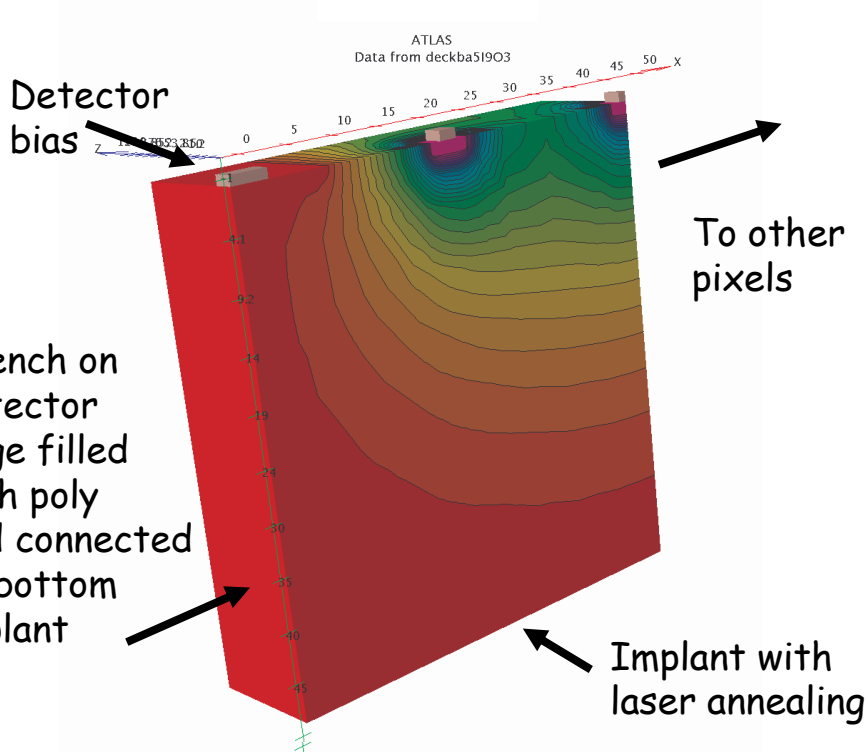
Development of Thinned Edgeless Sensors

- **3D chip provides only readout. In parallel we have designed mating sensors on 6”, high resistivity, float-zone, n-type wafers to be bonded to 3D chips**

- **Sensor fabrication performed at MIT-LL**
  - **Thinned to 50, 75, 100 microns**

- **Sensors sensitive to the edge, 4-side abuttable, i.e. no dead space**
  - **Deep trench etch, n doped poly-silicon fill provides edge doping**

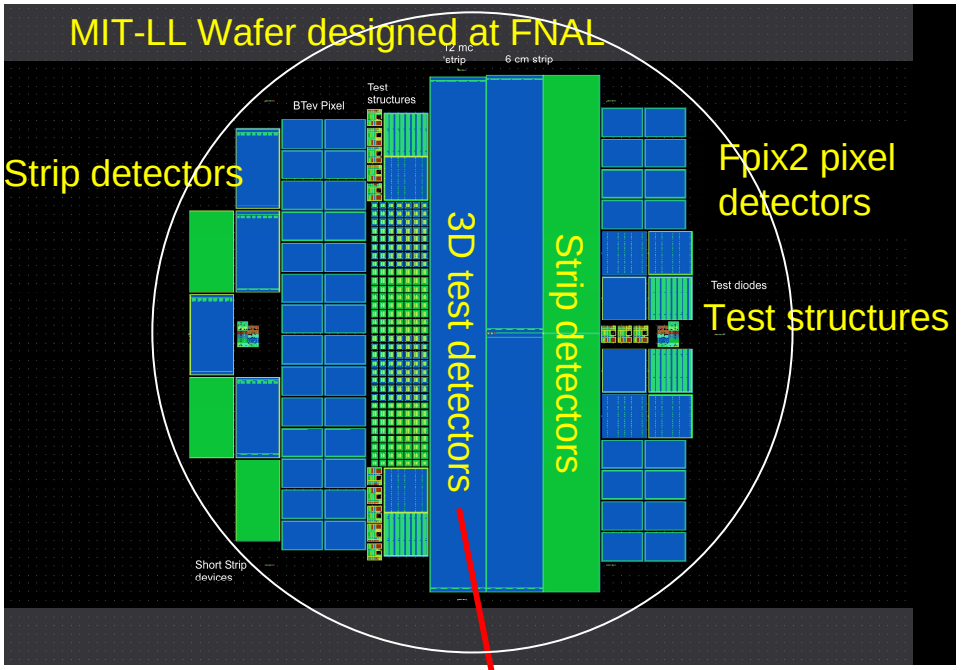
- **R&D Program**
  - **Validate and develop thinning process with laser annealing**
  - **Validate the technology which provides thinned detectors sensitive to the edge**
  - **Measure the actual dead region in a test beam**
  - **Study radiation effects (SLHC)**
  - **Understand performance**
  - **Bond with VIP readout chip**
  - **Use in construction of mechanical prototype detectors**



Detector Cross section near one detector edge

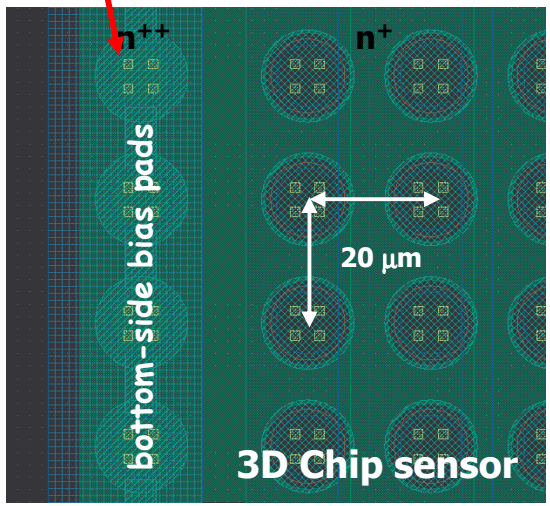
Development of Thinned Edgeless Sensors

- **Masks designed at FNAL**
  - **Test structures**
  - **Strip detectors**
    - 12.5 cm long
    - 2 cm long
  - **FPiX2 pixel detectors**
    - 50 x 400 μm pixels
    - Bonding studies
    - Beam tests
  - **Detectors to mate to 3D chip**
    - 20 x 20 μm pixels



- **Wafers received at Fermilab Nov. 2007**
  - **Growing pains removing handle wafer**
  - **VI measurements being carried out**

- **Next step is to bond sensor to readout chip**



Device Bonding

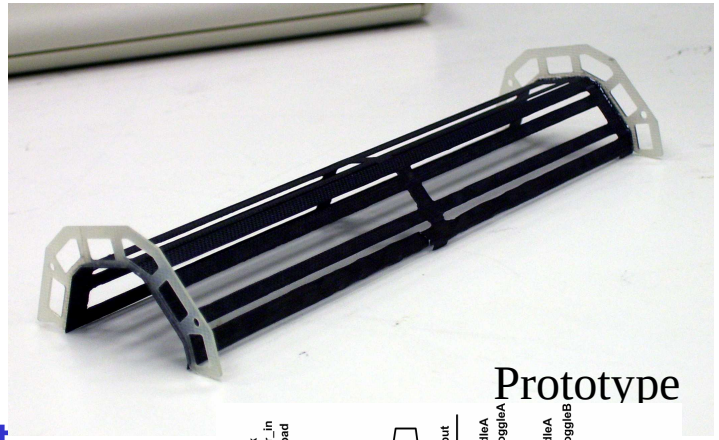
- **Sensor production provides**
  - **50 x 400 μm² pixel arrays**
  - **20 x 20 μm² pixel arrays**
- **Need to bond sensor with readout chip**
  - **50 x 400 μm² ➠ FPIX 2 chip**
  - **20 x 20 μm² ➠ VIP 3D chip**
- **Pursuing two technologies: Cu-Sn (RTI) and DBI (Ziptronix)**

Bonding Techniques

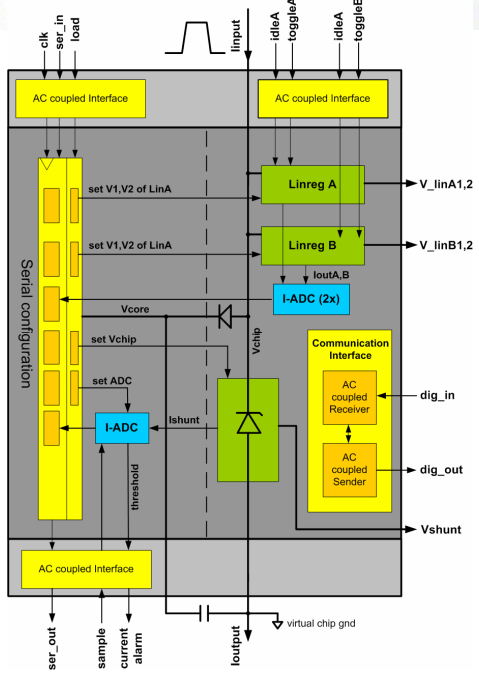
- **RTI: Cu-Sn Bond procedure**
  - **Technique uses Cu pillars with diameter limited to 7 μm**
    - Test placing pillars on test Si wafers using FPix pattern
    - Bond FPIX ROIC to pixel array using Cu-Sn bonding technique
- **Ziptronix: Direct Bond Interface**
  - **Technique uses "magic metal" plus oxide bond**
    - Process sensor and readout wafers
    - Mount sensor chips on the readout wafer
    - Thin sensor chips to 50 μm and readout wafer to 100 μm
    - Implant and laser anneal sensor
    - Dice bonded pairs

Mechanical Design and Serial Power

- Developing techniques for fabricating and handling thin-walled carbon fiber structures
- Multi-layered, high precision, very thin, low mass detectors
  - ILC goal: layer thickness of 0.1% X_0 per layer, equivalent of 100 μm of Si
  - LHC goal: lowest material budget as possible
- Prototypes of carbon-fiber support structures
  - Fabrication of prototype half-shell structures for evaluation and testing
  - Comparison with FEA analyses


Prototype

- Peak and average power are crucial issues for the next generation of particle detectors
- Serial powering can lower instantaneous current
- Fermilab is designing a serial powering chip in collaboration with Penn/RAL
  - Design of a shunt regulator being capable of regulating up to 1A @ 2.5V
  - Two linear regulators (analog and digital) switchable between two downloadable voltages
  - Core voltage for chip control (1.5 to 2.5V)
  - TSMC 0.25 micron (radiation tolerant design)
- Concerns:
  - Current balance and torques

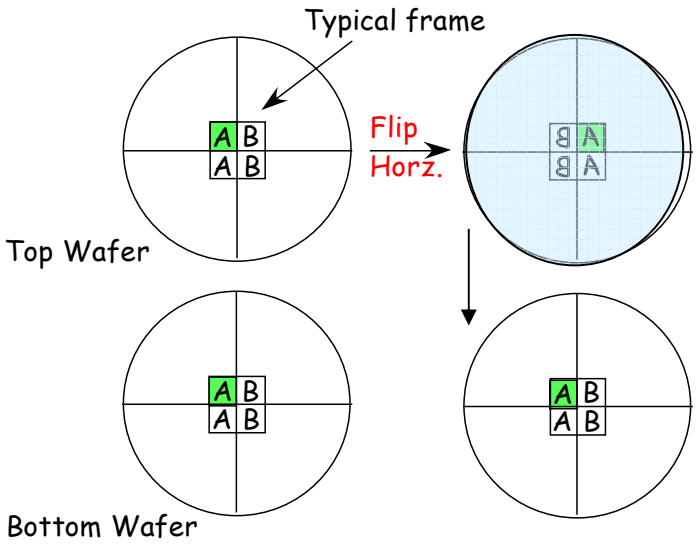


Summary of Current Projects

- **SOI**
  - **OKI Multi Project Wafer run; test of Mambo chip**
  - **OKI test structure irradiation**
  - **MIT-LL test structures**
  - **ASI sensor design with dual gate transistor**
- **3D**
  - **Studies of devices thinned at IZM**
  - **VIP1 chip tests**
  - **Bonding Studies**
    - Cu-Sn with RTI
    - DBI interconnect with Ziptronix
- **Sensors**
  - **Hamamatsu sensor thinning and laser anneal studies**
  - **OKI wafer thinning and laser anneal studies**
  - **MIT-LL sensor testing**
- **Power and Mechanics**
  - **Serial power chip (Fermilab, Penn, RAL)**
  - **Fabrication and testing of thin carbon fiber support structures**
- **Test Beam**

Future Projects

- **SOI**
  - **OKI has 2nd MPW run, 200nm SOI process; submit Mambo II chip**
  - **Through Phase II SBIR grant, obtain sensors from ASI**
- **3D**
  - **Expect third MIT-LL Darpa 3D MPW run; submit VIP-II chip**
  - **3D simulation studies with CFDRC**
  - **Considering dedicated 2-Tier 3D run, with layout on one wafer**
    - Exploring interest, collaboration, funding and technical options



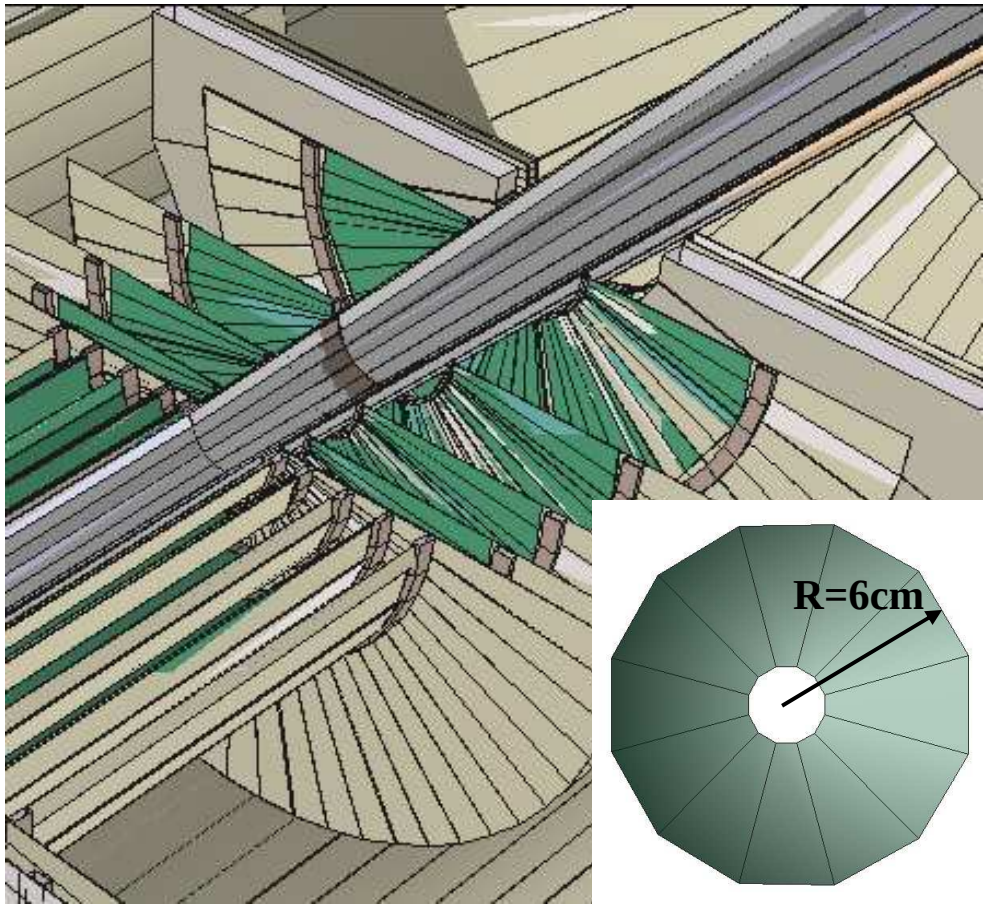
Note: top and bottom wafers are identical.

- **Sensors**
  - **Continued R&D on thinned sensors**
- **Power and Mechanics**
  - **Submission of serial powering chip**
  - **Development of thin carbon fiber support structures**
- **Test Beam**
  - **Expect to have beam test of all components**

Far Future

- **Forward pixel detectors are notoriously difficult to build in low mass, low power configuration with very little additional mass due to cables**

- **Maybe, one day, a full 3D wafer will be developed that contains all the functionality needed for a tracking pixel detector**
  - **Shaper, amplifier, DCS**
  - **ADC, pipeline**
  - **Hit addressing**
  - **Time stamping**
  - **Sparsification**
  - **Continuous readout**
  - **Deadtime less operation**
  - **Low power**
  - **…**
  - **…**



Summary

- We see the development of the 3D technology as holding a lot of promise for the development of particle physics detectors
- Very active R&D program at Fermilab on the development of 3D technology covering all aspects of its design as particle vertex detector:
  - Readout and sensor development
  - Device characterization
  - Power and mechanical support
  - Beam tests
- The R&D program builds on the existing strengths at the laboratory
- This work has an initial focus on the ILC but we view it in as broad a context as possible within the laboratory including LHC, synchrotron radiation x-ray detectors as well as medical applications
- All detector R&D is carried out with a long time scale in mind and we are willing to partner with collaborators from industry, universities and other research institutions