

3D DRIE Activities & plans of Alcatel

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3 DIT Workshop Palaiseau Nov. 29th 2007

ALCATEL
Micro Machining Systems

Part of a Worldwide Leader, High Tech, Multinational Corporation



P. RUSSO



Enterprise Business Group



Vacuum Group

- Annual Revenues: > 200 M€ (CY06)
- Employees >980

Alcatel Vacuum Technology France (AVTF)
JY. GUEGAN

Alcatel Micro Machining Systems (AMMS)
G. BELLINI



100% **adixen**

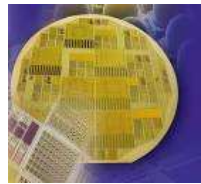


- ◆ Introduction
- ◆ DRIE: Semiconductors and Microsystems
- ◆ Majors Achievements
- ◆ Trends & perspectives
- ◆ Conclusion



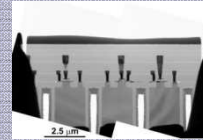
S.C. Etching tools & Microsystems

Semiconductor



1 μ m technology
RIE

Dry Etch technology
expertise

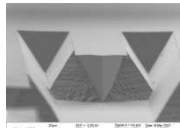


Moore law
Toward
nanotechnology

Microsystems

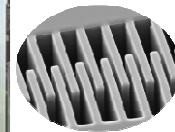


100 μ technology
Wet Etch



High AR and High
ER requirements

Deep RIE Technology
Bosch Process



MEMS Law
One process = one product

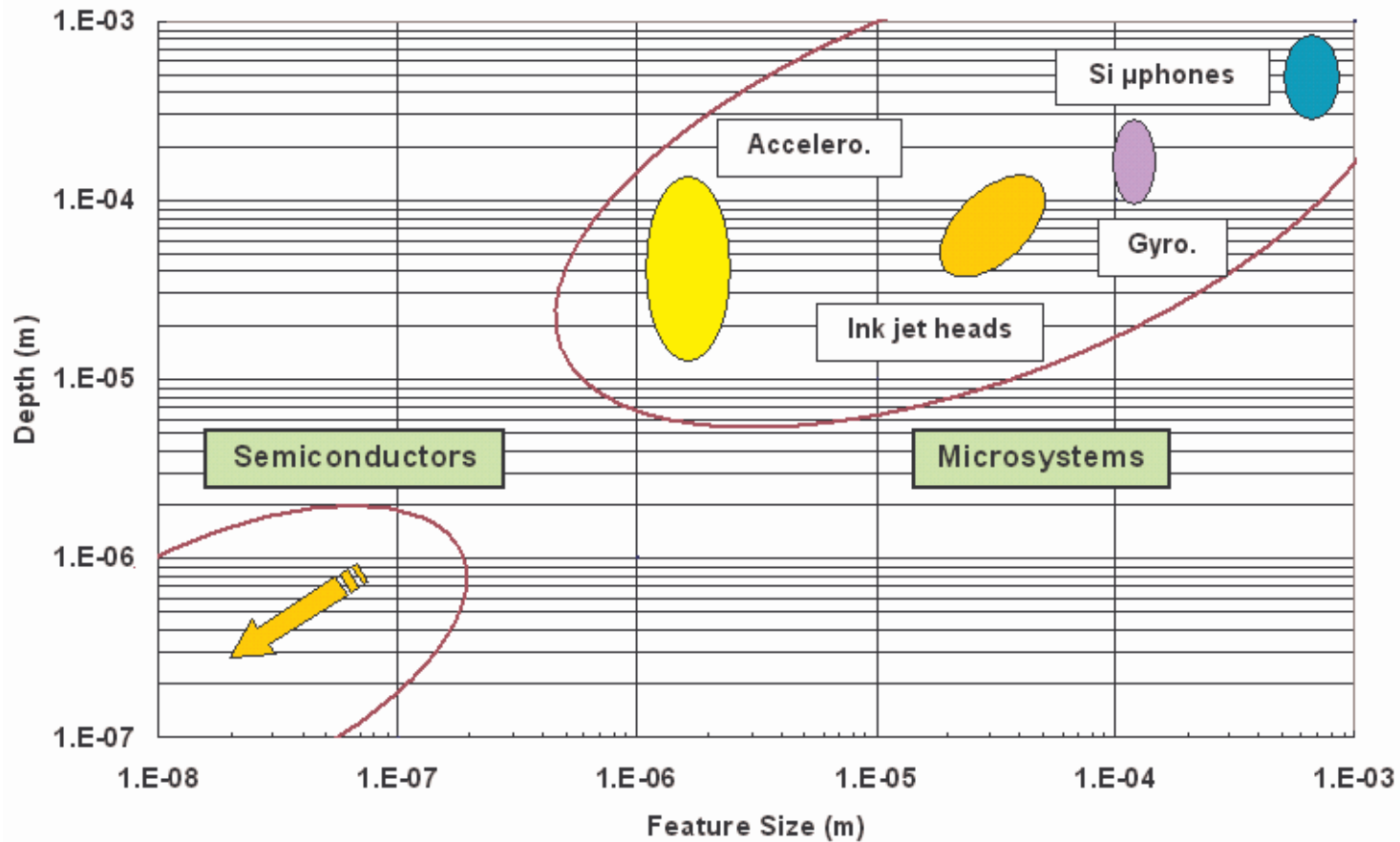
1990

1993

>1998

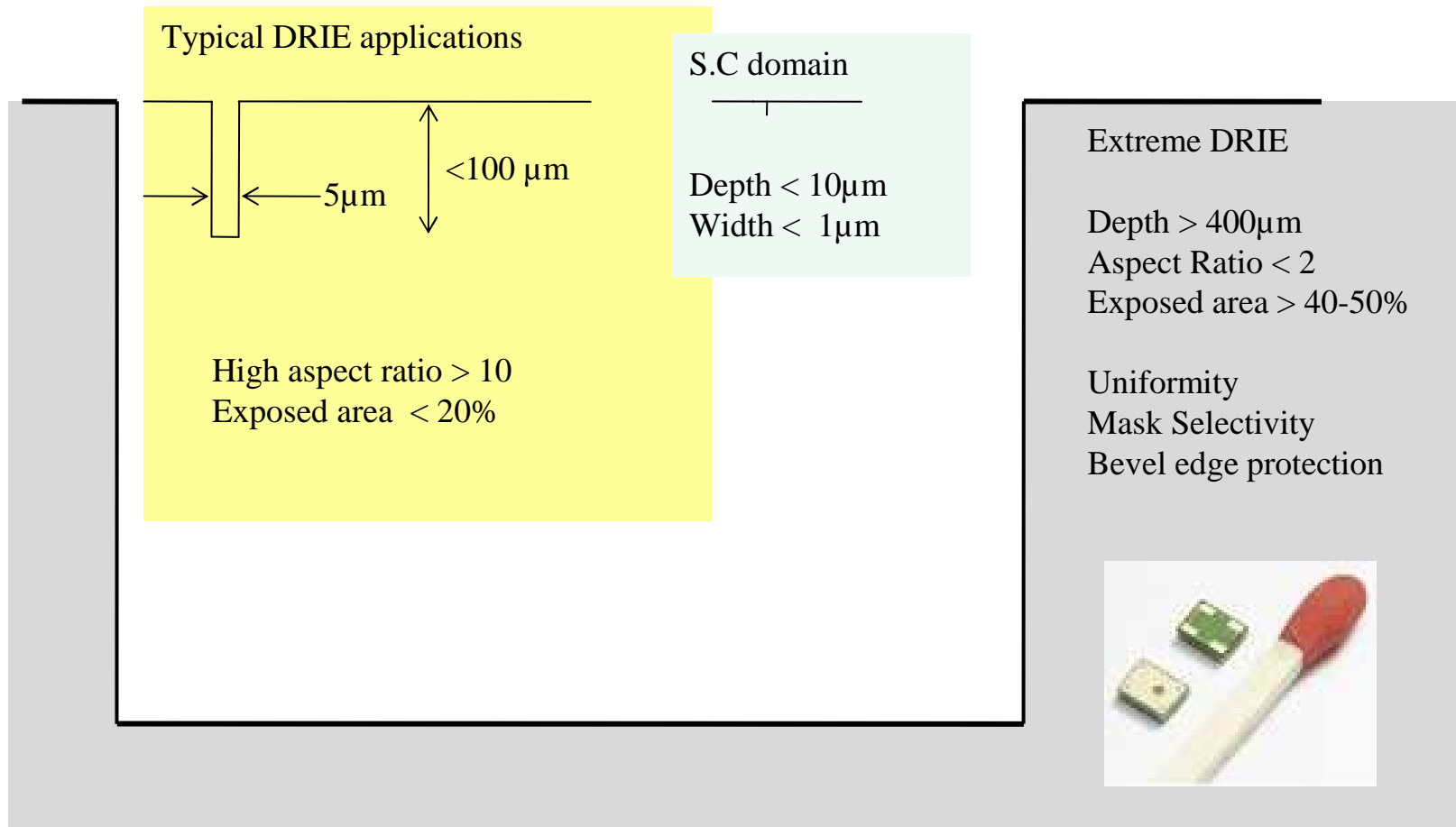
Microsystems & Semiconductors

- ◆ Microsystems: a wide range of size & depth !



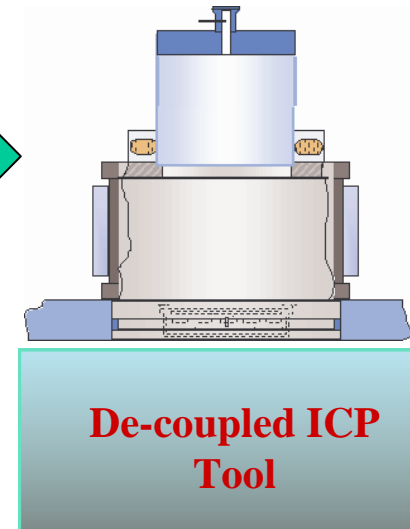
DRIE requirements for MEMS

- ◆ Microsystems: a huge volume of Si to remove !

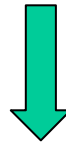


DRIE requirements for MEMS

Very High Selectivity	Low Plasma potential Independent Bias control
Very High Etch Rate	High Density Plasma "F" Chemistry
Anisotropy	Passivation mechanism



**De-coupled ICP
Tool**



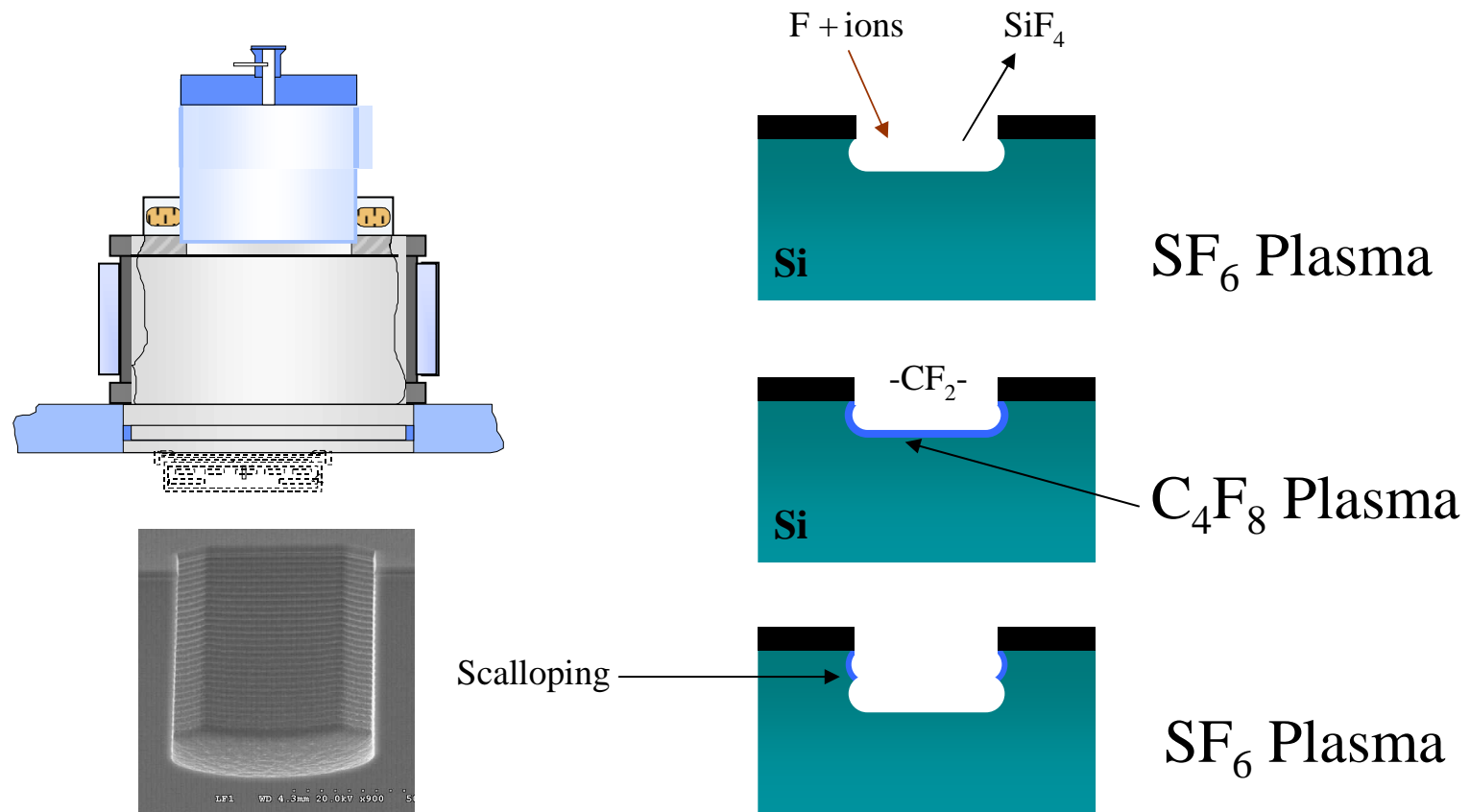
Simultaneous etching:
with SF₆ and sidewall
passivation with O₂ and
Cl₂, HBr

OR

Bosch Process:
Short cycling steps of isotropic
etching with SF₆ and Polymer
Deposition with C₄F₈

The "Bosch*" Process

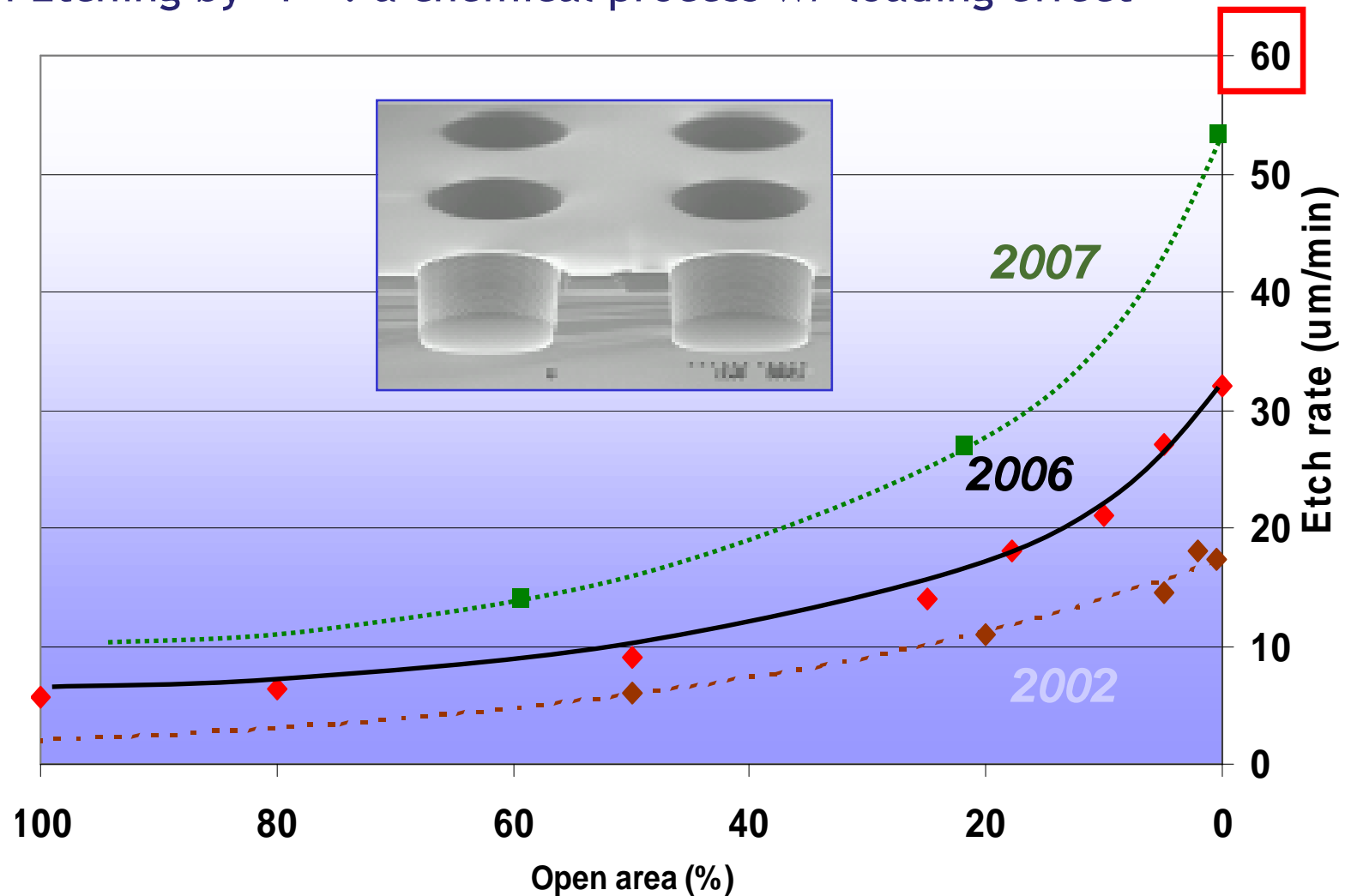
- ◆ A time multiplexed process between Etch & Passivation



*US pat. 5,501,593 Publi. Mar. 26, 1996

The Race Toward Higher Etch Rate

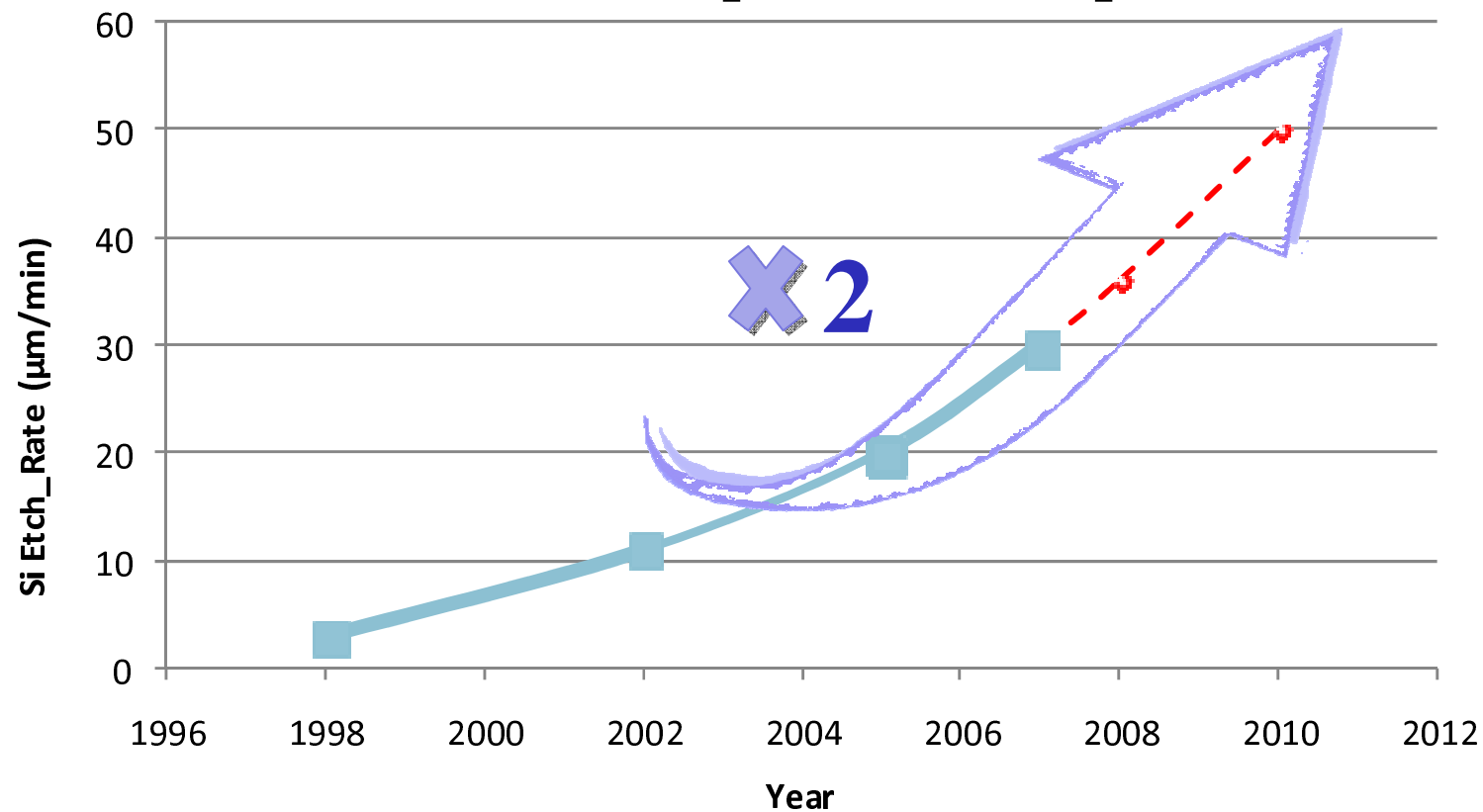
- ◆ Si Etching by “F” : a chemical process w/ loading effect



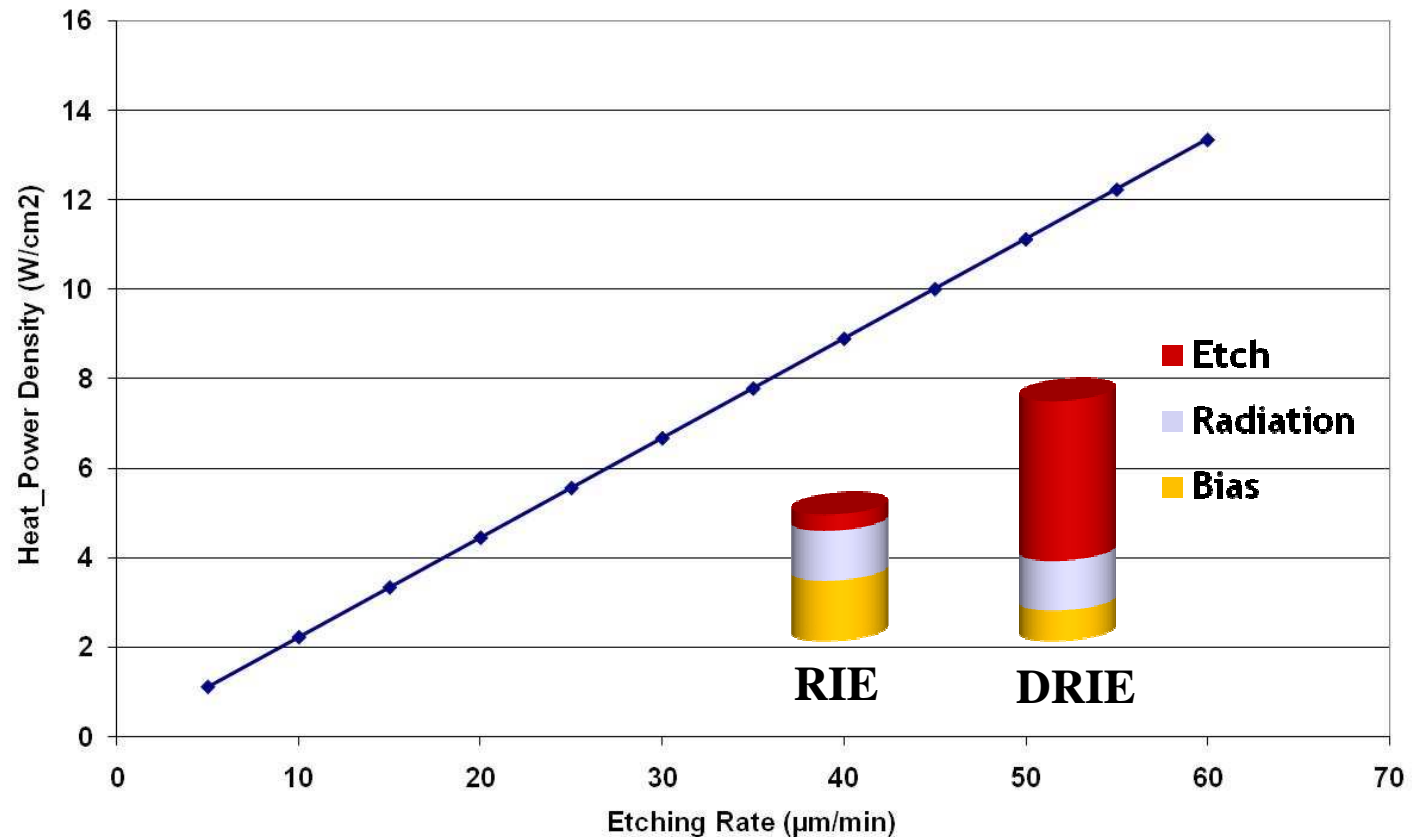
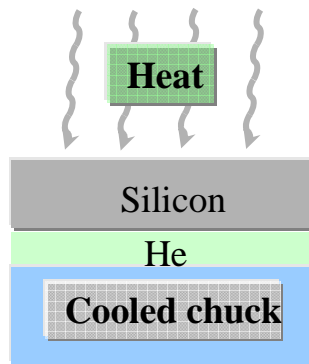
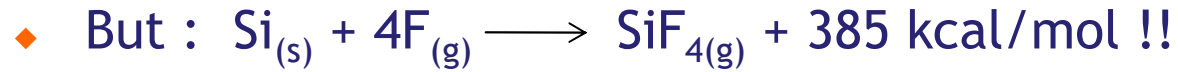
The Race Toward Higher Etch Rate

- ◆ Higher gas flow / pressure, Better gas utilization
- ◆ Higher RF Power

Etch rate Roadmap on >20% exposed area



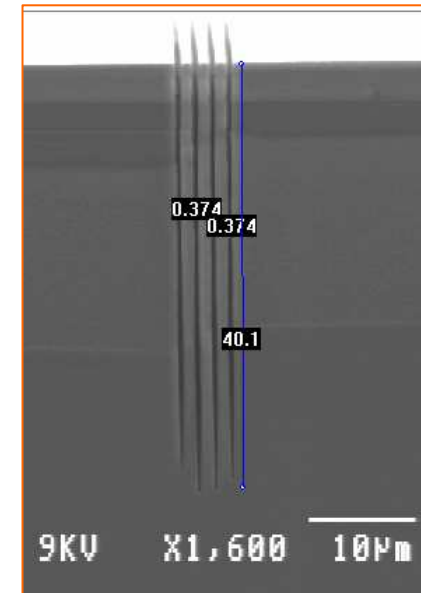
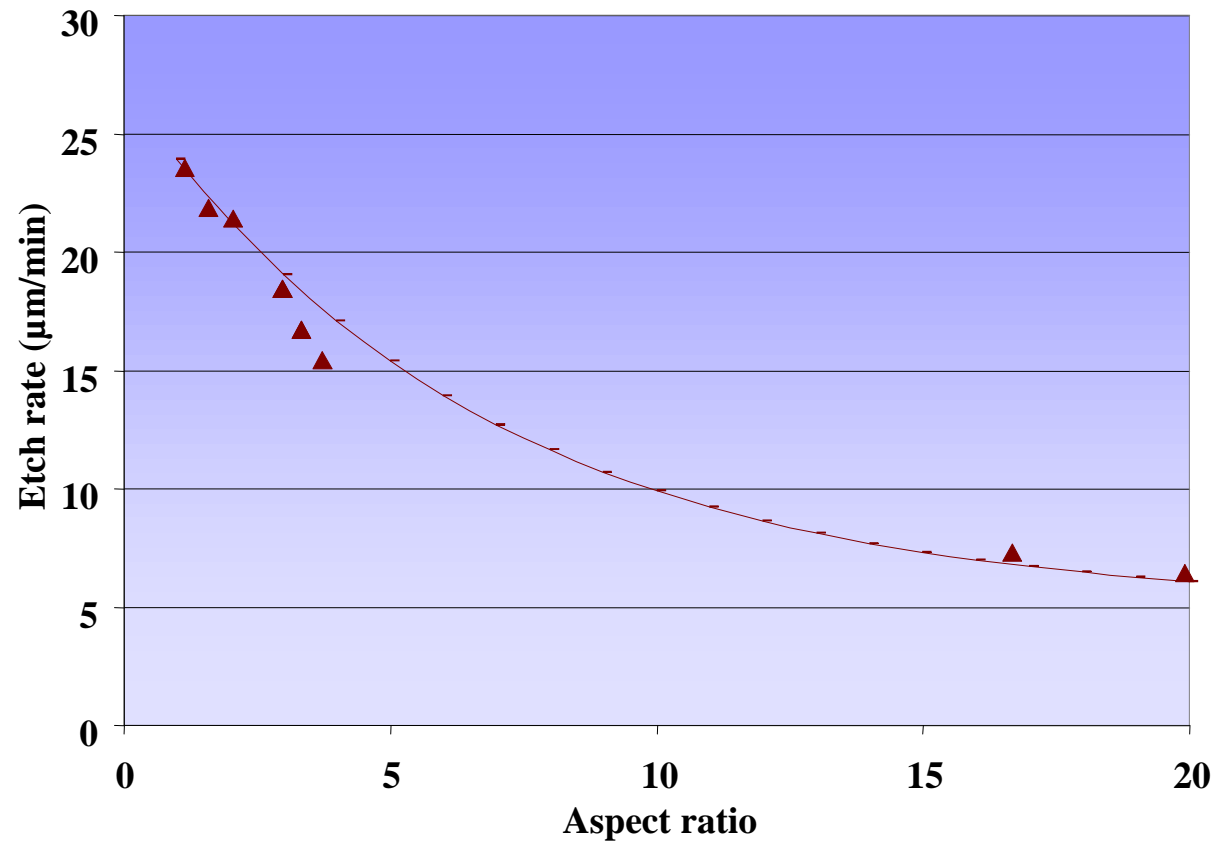
Thermal Budget issues



Aspect Ratio Dependent Etching

- ◆ Silicon Etch rate is sensitive to Aspect ratio (species transport limitation)

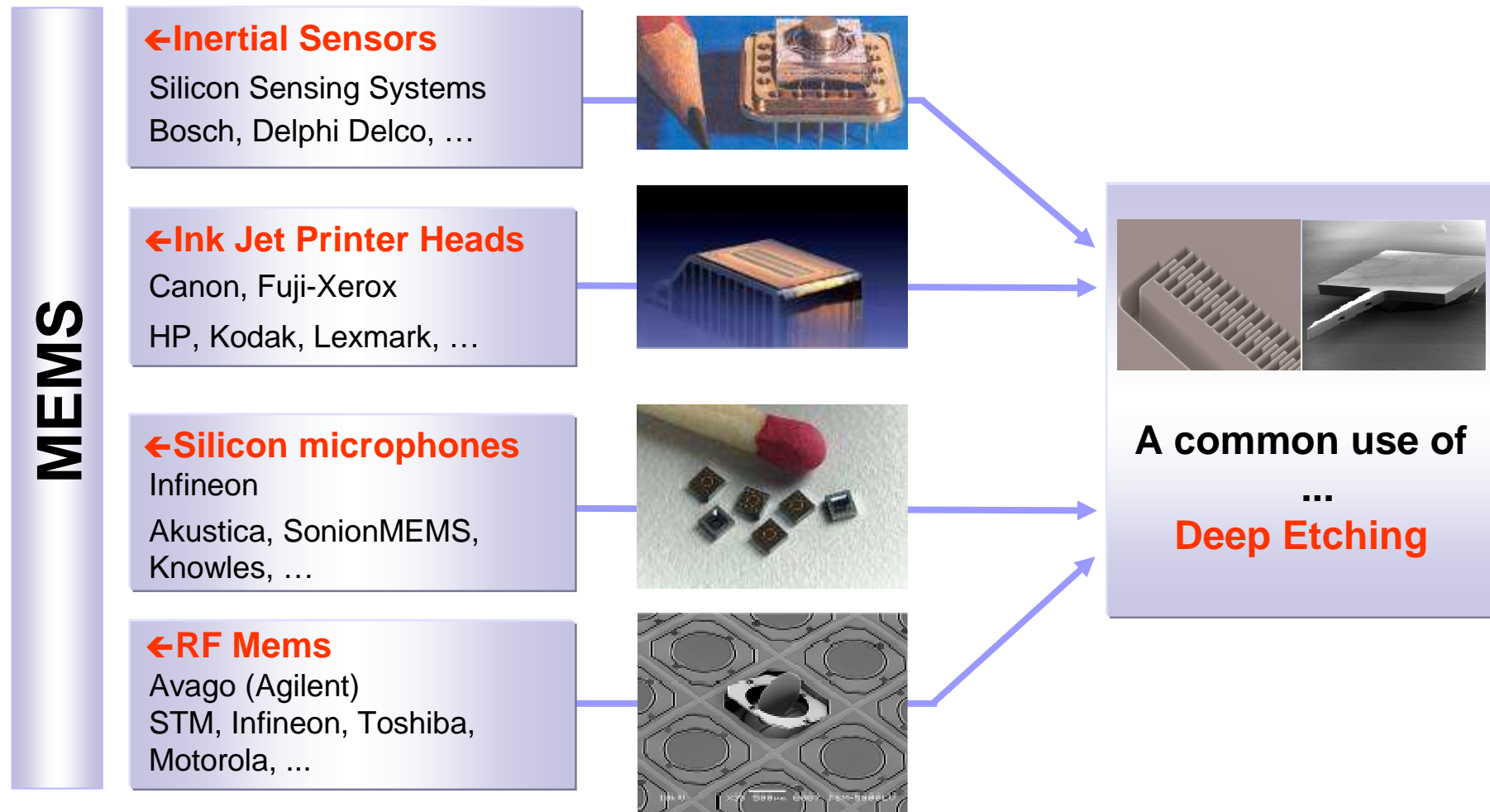
Etch rate versus the aspect ratio
for an exposed area around 25 %



Alcatel Patented process
(S.H.A.R.P. process)
Achieving Aspect Ratio
> 110

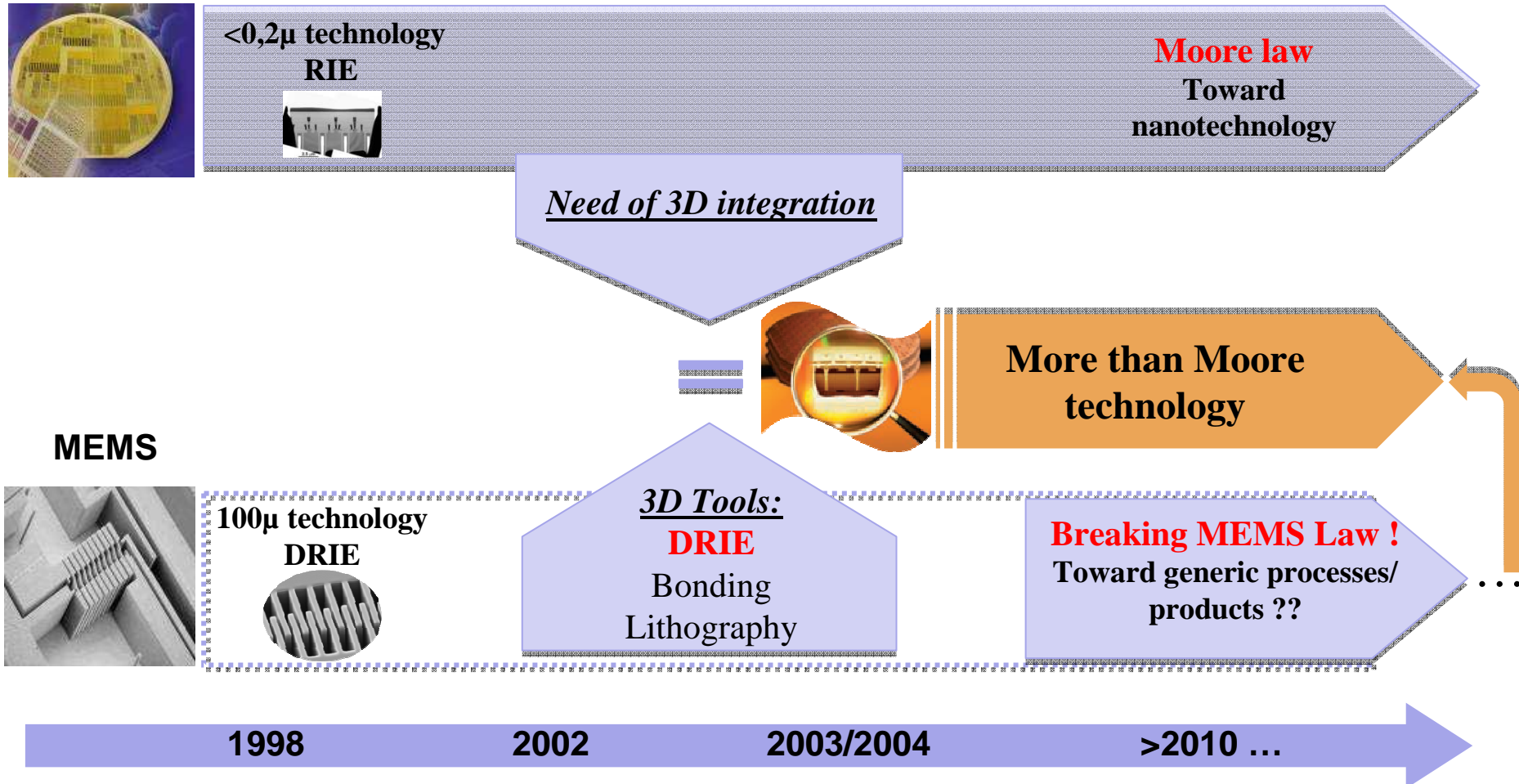
New perspectives for the DRIE

- ◆ DRIE: a key technology to address the 3rd dimension



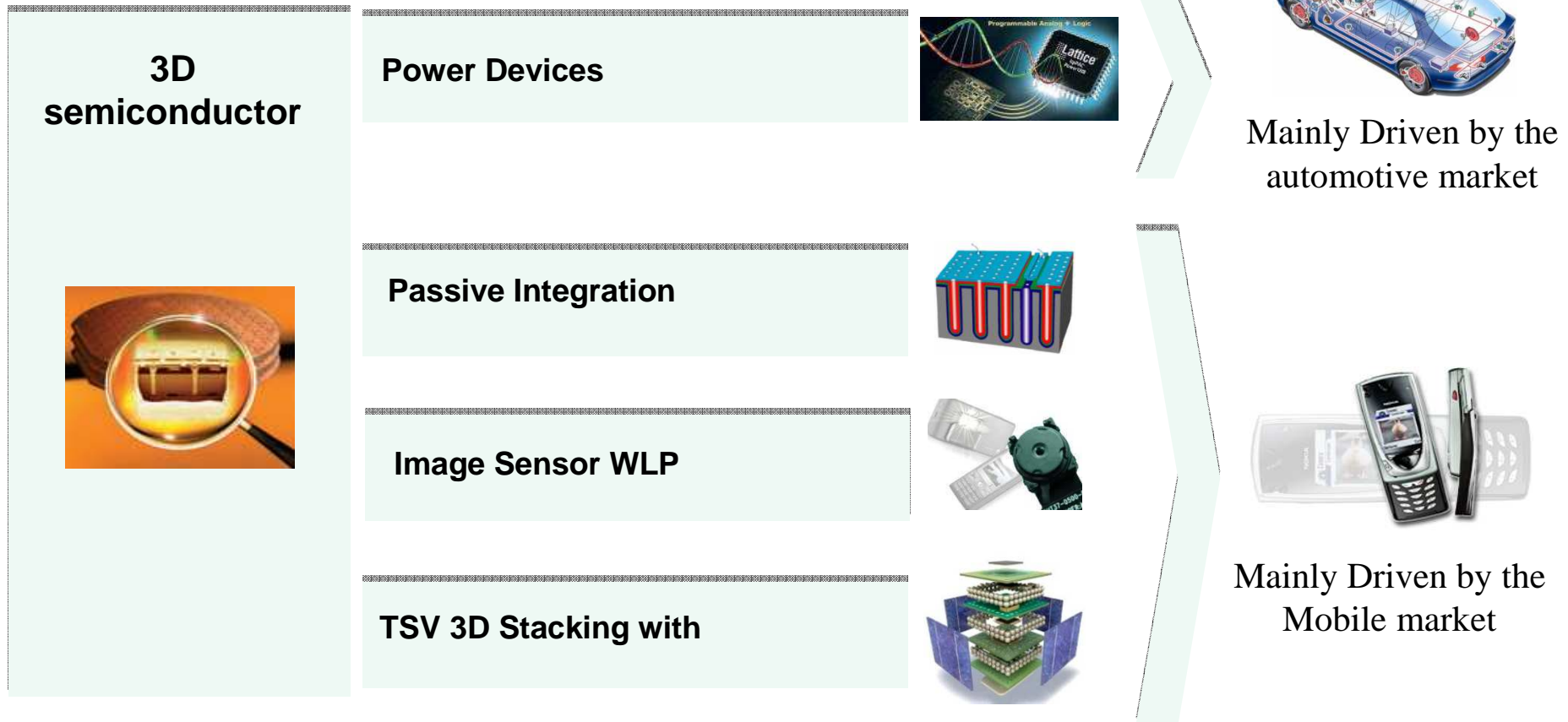
Interest from S.C

Semiconductor



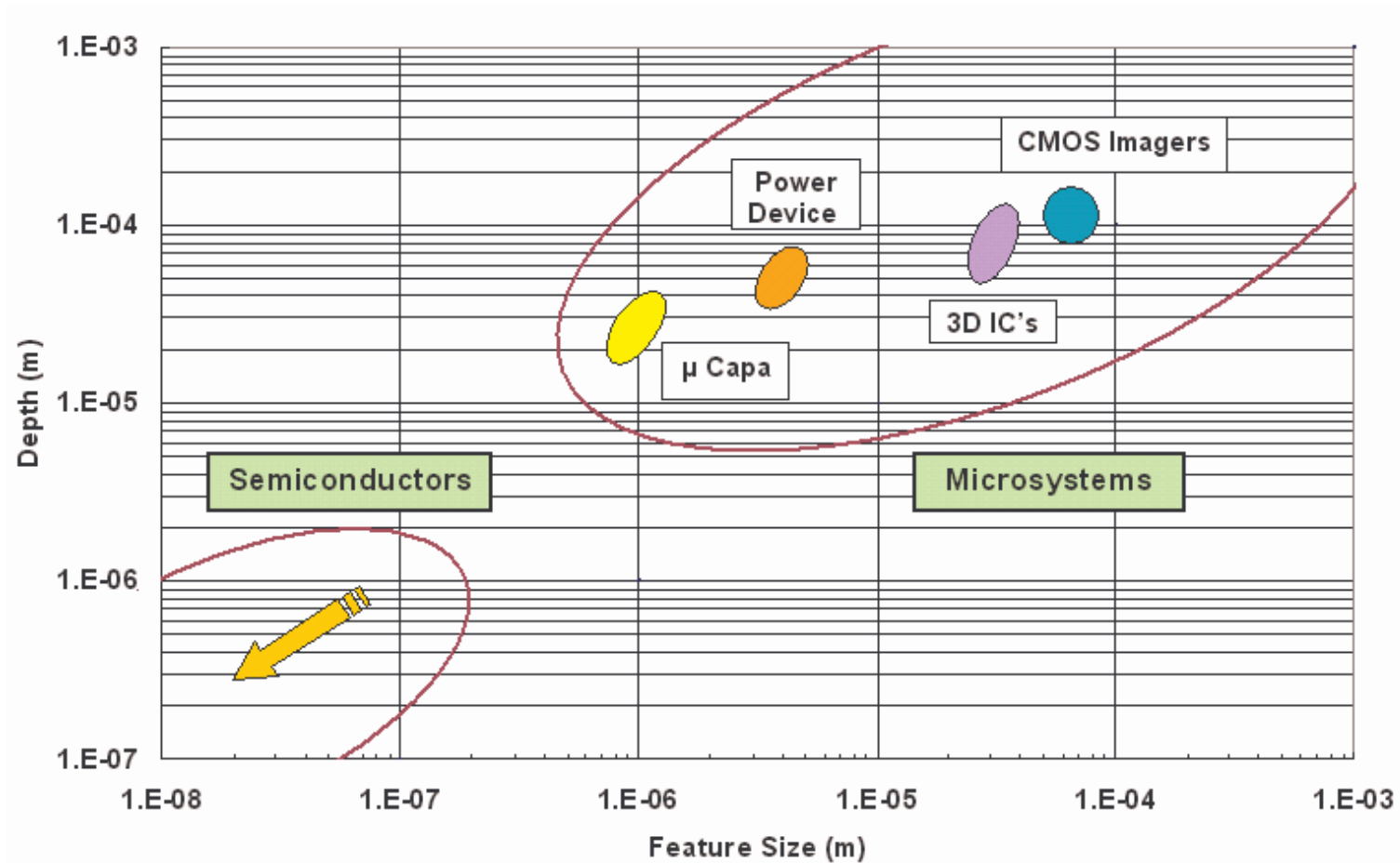
Interest from S.C

- ◆ Common need of Deep etching and LT-PECVD :



3D SC within the scope of DRIE

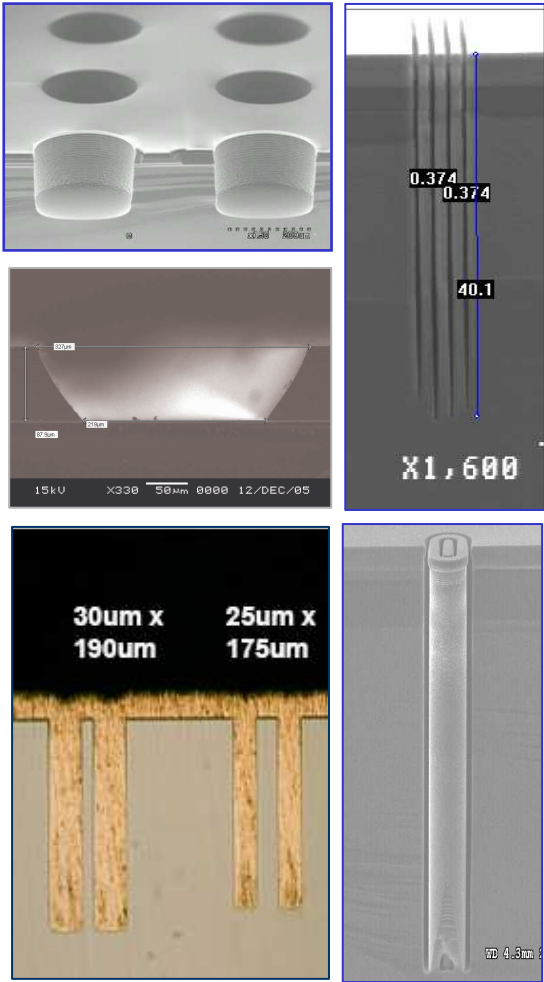
- ◆ 3D S.C fall into the micro-systems domain !



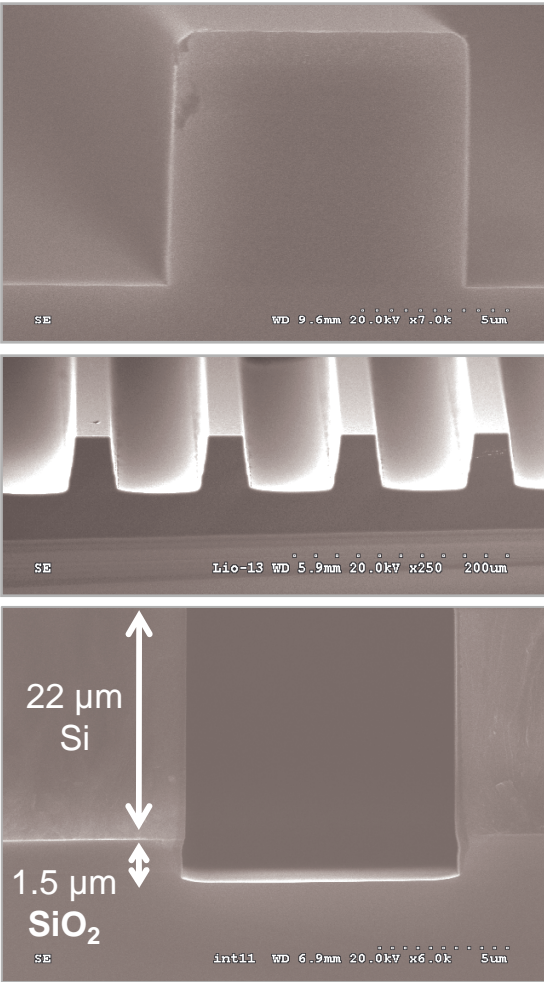
Process Range

... addressing 3D integration applications

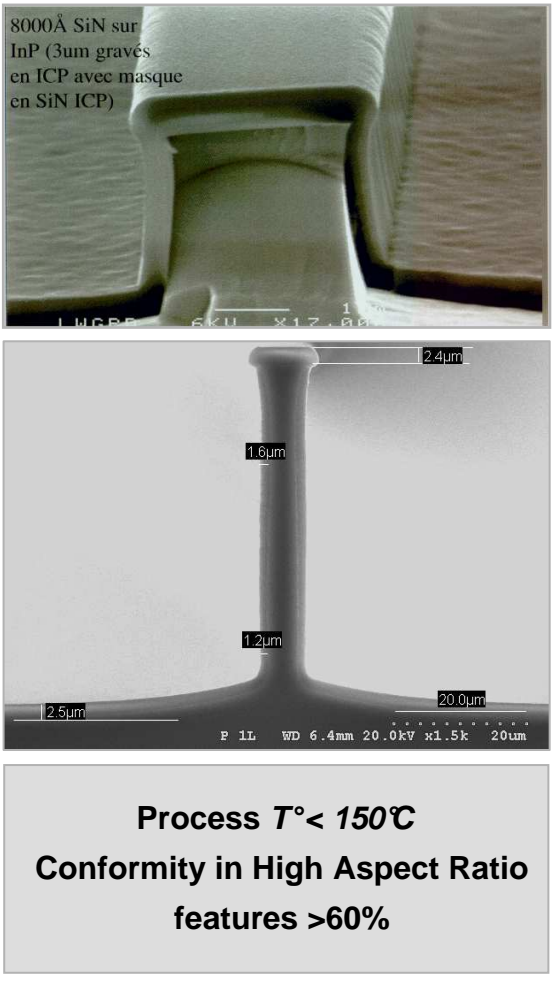
Silicon Via etch



Thick SiO2 Etch



Low Temperature PECVD



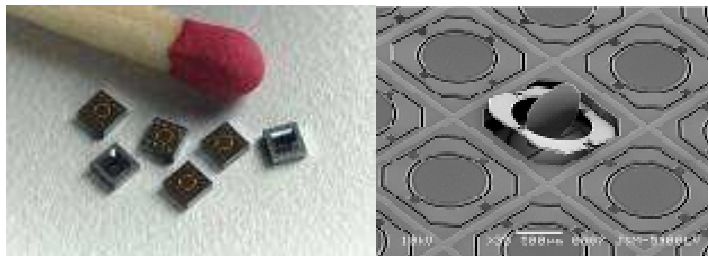
Process $T < 150^\circ\text{C}$
Conformity in High Aspect Ratio
features >60%

Transition to 300 mm

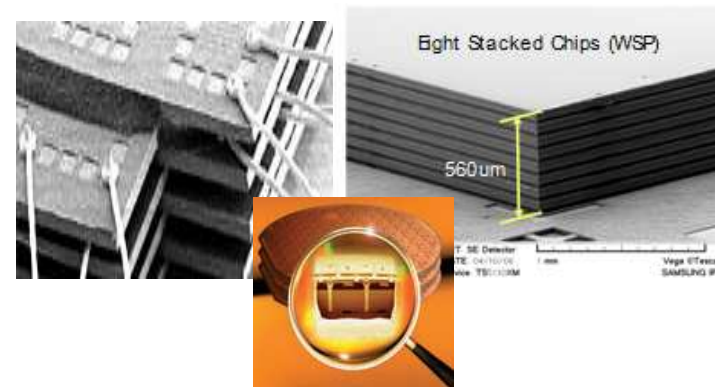
- ◆ 300 mm transition driven by mobile applications



- MEMS
- Power Devices
- Passives integration



- WLP CMOS image sensors
- 3D integration/ Device Stacking





Conclusion

- ◆ DRIE of silicon became a key enabling technology for MEMS.
- ◆ Within a decade, DRIE increased productivity by almost a factor of 10.
- ◆ New process challenges have been quickly addressed.
- ◆ Semiconductor supply chain is looking to DRIE for the emerging 3D semiconductor applications
- ◆ Microsystems should take benefits from those new applications

www.alcatelmicromachining.com

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