3D integration activities and plans at IMEC

Piet De Moor

Introduction

- Evolution in radiation detection/imaging:
  - single pixel → linear array → 2D array
  - increase in resolution = decrease in pitch (down to few um)
- = thanks to development in **microelectronics fabrication technology**:
  - CMOS scaling
  - hybridisation using solder bumps
- Question: what's next ?
  - which new technologies become available ?
  - what are the benefits ?
- Answer:
  - 3D integration
  - advanced packaging

Overview

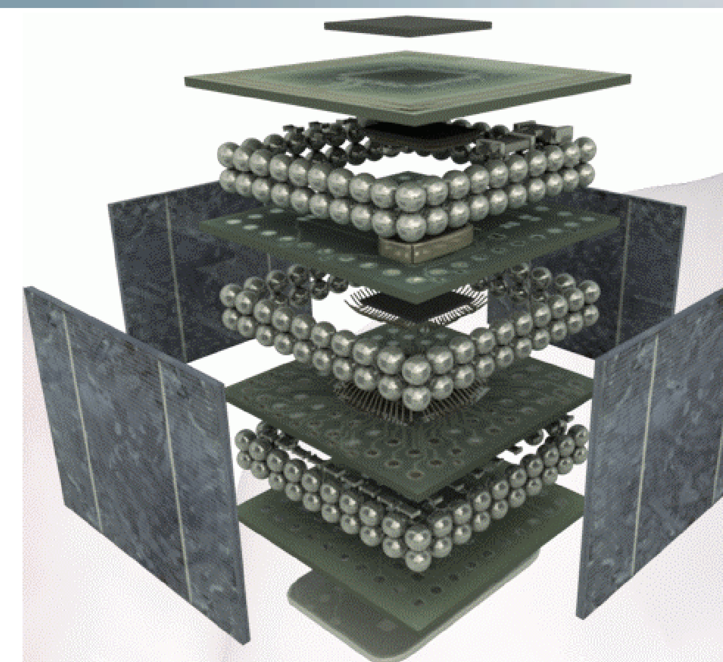
- Introduction
- 3D integration:
  - 3D-"System-in-Package" (3D-SiP)
  - 3D-"Wafer-Level-Packaging" (3D-WLP):
    - die stacking
    - thin chip embedding
  - 3D-"Stacked-IC" (3D-SiC)
  - IMECs 3D integration roadmap
- Detector application examples
- Conclusions & outlook

3D Integration approaches:
Introduction

- 3D integration drivers:
  - miniaturization
  - high density hybrid interconnection
  - interconnect speed and power
- 3D interconnects can be realized at different **levels** of the micro-electronic system, corresponding to different existing (commercial) microelectronic technology **platforms**:
  - die/package level → traditional packaging & interconnection technologies
  - post-processing of wafers → wafer-level packaging technologies
  - CMOS fabrication → IC-foundry technologies
- These technologies result in different 3D-interconnect densities and capabilities
- Choice of technology depends on the **interconnect requirements** of a given **application**

3D-SIP approach: Traditional packaging & interconnection

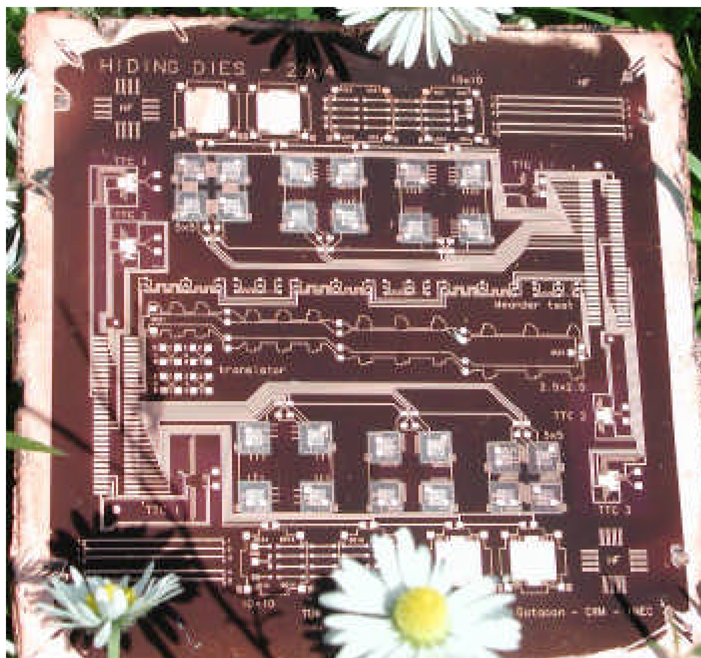
- Stacking of 2D-SIP “sub-systems”
  - each layer is an SIP PCB
  - different assembly technologies can be used
  - interconnect density: 2-3/mm, 4-11/mm^2
- Advantages:
  - generic 3D technology
  - each layer is fully tested before final assembly
  - best yield and manufacturability
- Limitations :
  - relatively low 3D interconnectivity
  - lack of standardization of package sizes
- Application:
  - intelligent/autonomous wireless sensor nodes
  - miniaturized detector systems

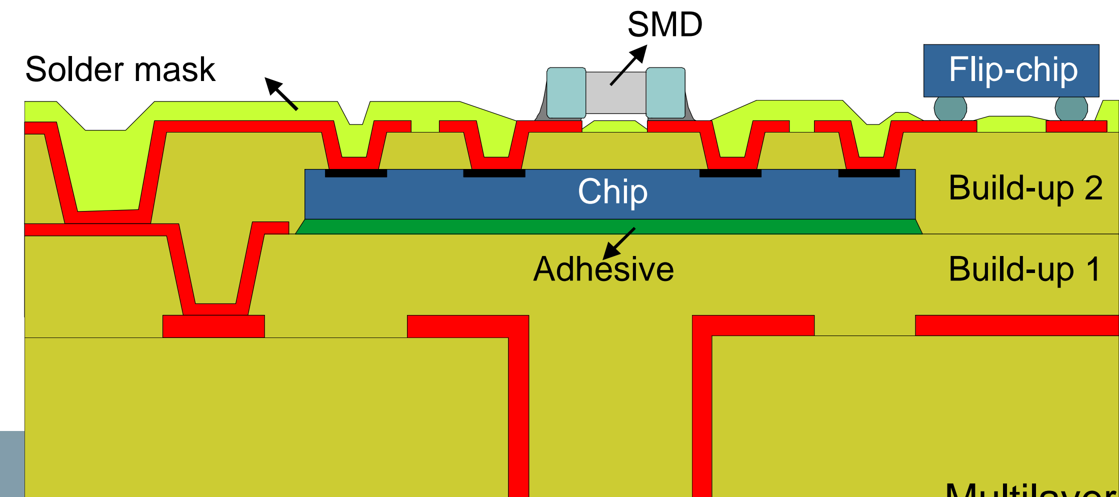


IRIS-2 CMOS camera

3D–SiP:
Example: PCB with embedded components

- Technology:
  - embedding of a 50 um thin die in a laminated PCB
  - interconnects made in PCB technololgy
- Applications:
  - very thin systems
  - flexible/foldable systems





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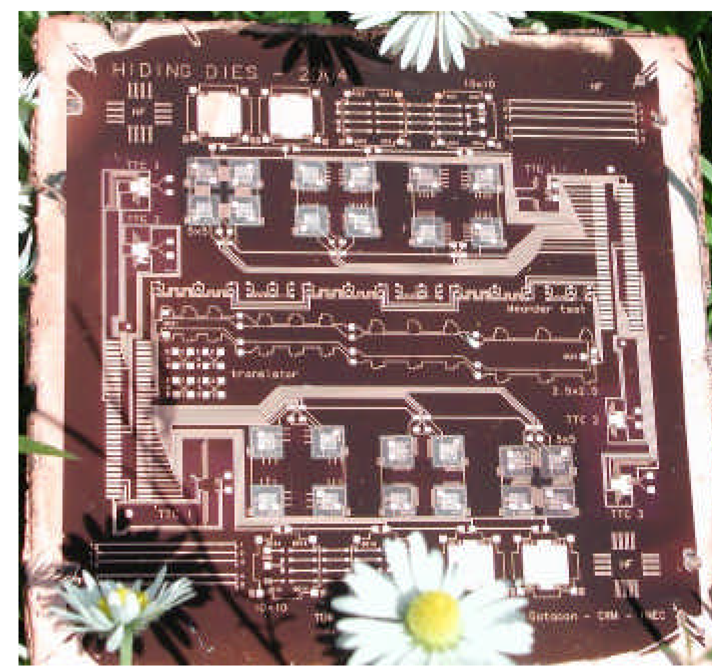
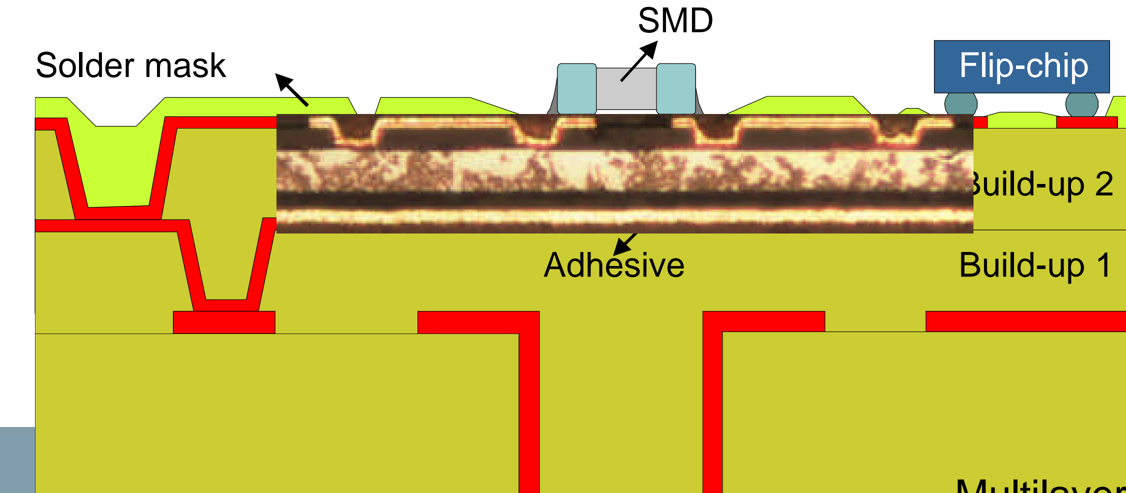
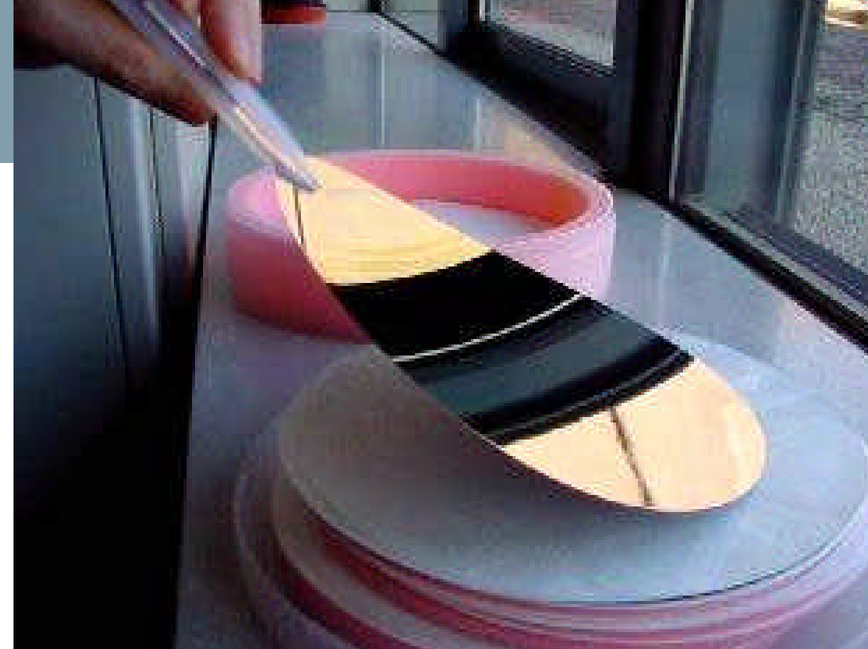
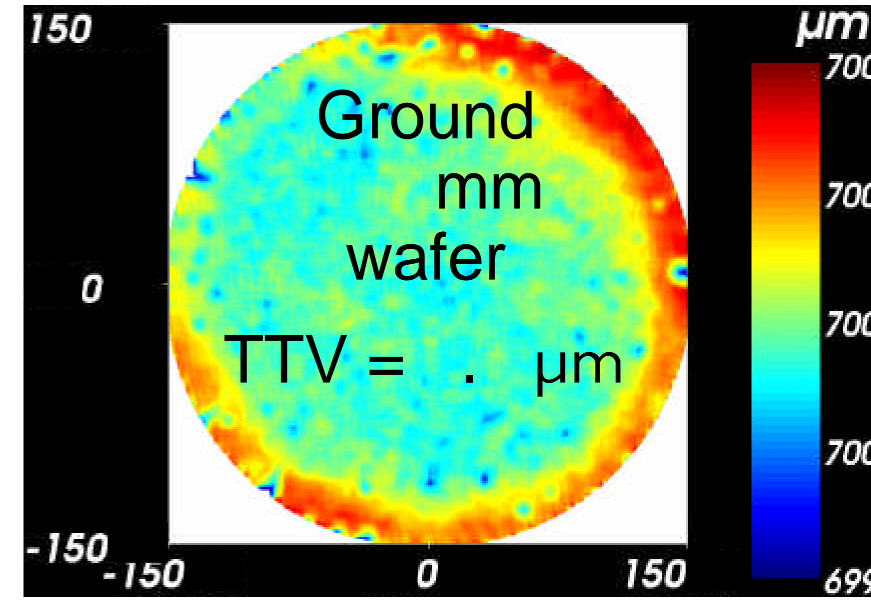




Technology enablers: Wafer thinning

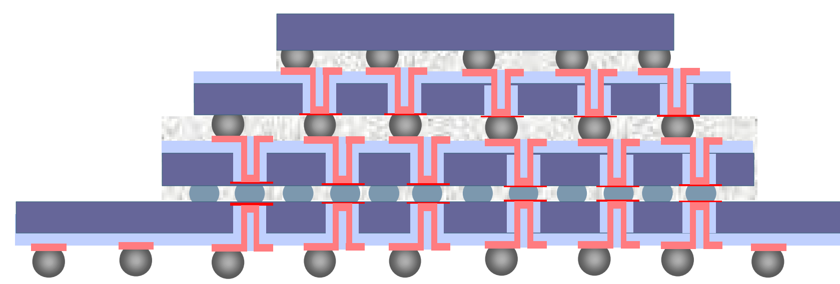


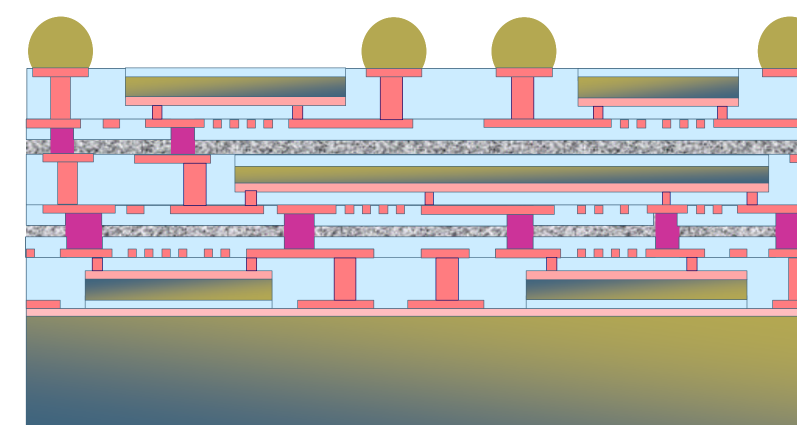
- Technology:
  - rough/fine grinding, dry/wet etch
  - Si, glass, GaAs, ...
  - critical: thinning damage, impact on devices
  - very thin wafers (< 100 um): use of carrier wafers and temporary (de-)bonding technology
- Features:
  - thinning down to 15 um
  - total thickness variation < 1 um
- Applications:
  - 3D stacking, enabling through Si interconnects
  - ultra thin chip embedding
  - thin substrates: backside illuminated imagers, ΔE detectors, ...



3D-WLP approach:
Wafer-level-packaging technology

- 3D interconnects:
  - realized at wafer level
  - processed on fully processed wafers
- Interconnect density:
  - 10-50/mm, 100–2.5k/mm^2
- Advantages:
  - no interference with process of individual layers
- Limitations:
  - not the highest interconnect density
- 2 technology approaches:
  - die stacking
  - ultra thin chip embedding
- Applications:
  - 3D sensor/imager systems allowing tiling/full buttability
  - thin flexible/stretchable systems





3D-WLP approach: Process and specifications

3D-WLP chip stack process:

- die/wafer thinning
- through silicon vias (TSV)
- micro-bumps

Via last approach:

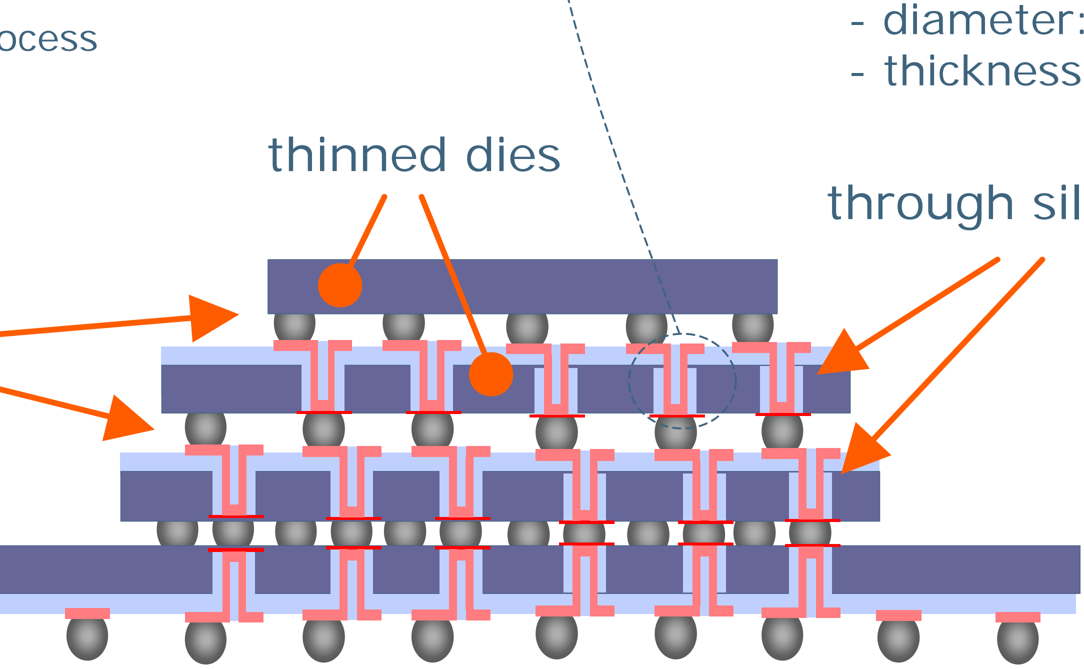
- backside thinning
- followed by TSV process

Assembly:

- micro-bumps

TSV specifications:

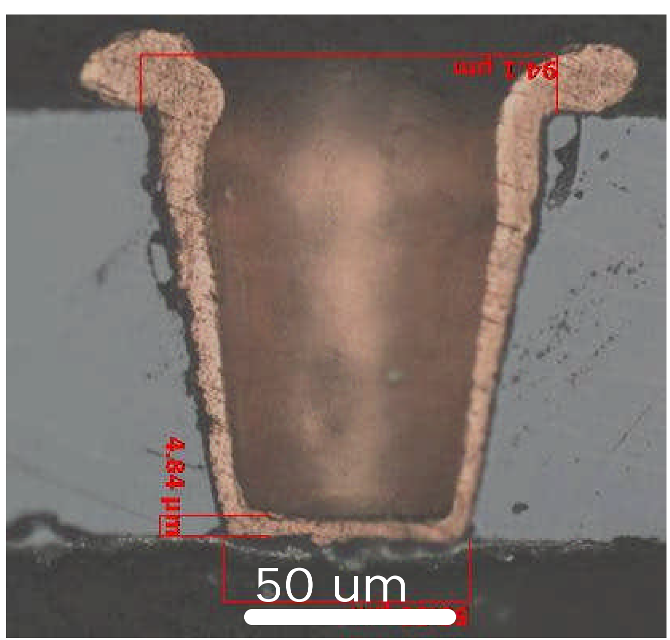
- pitch: 40-150 um
- diameter: 25-100 um
- thickness: 50-100 um

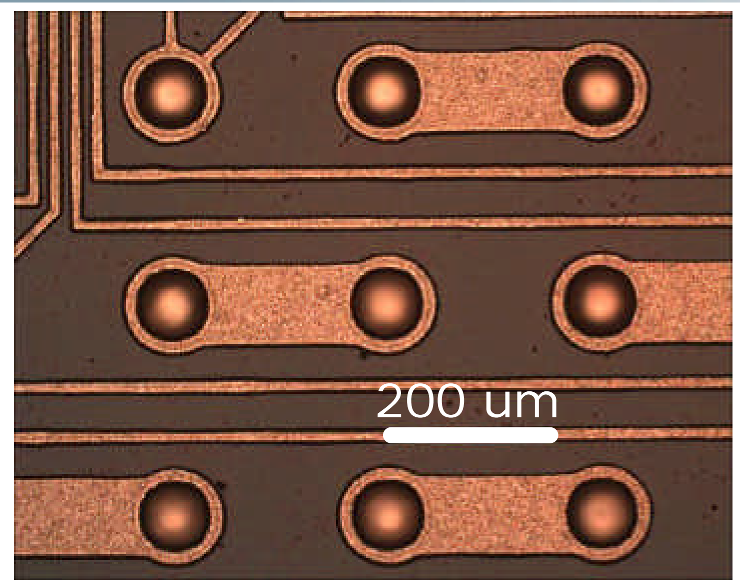


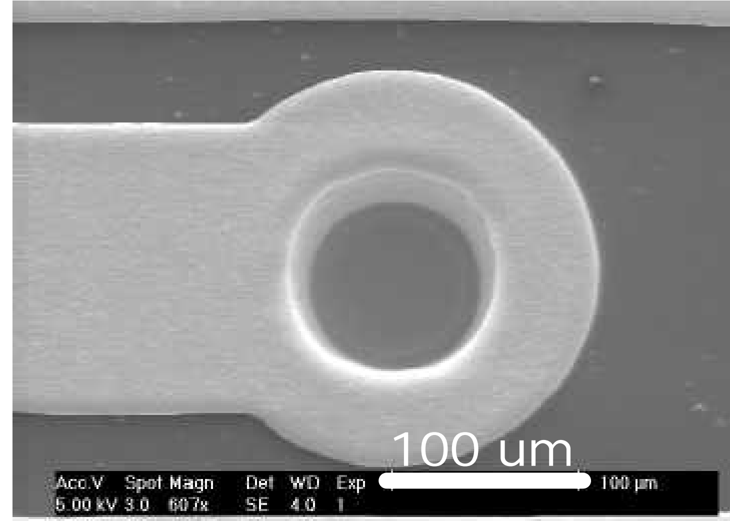
3D-WLP approach: Results

- Through wafer via:
  - resistance <= bond wire resistance

	3D-WLP via	1mm wirebond
R	20-30mW	~40mW *(25µm wire)*

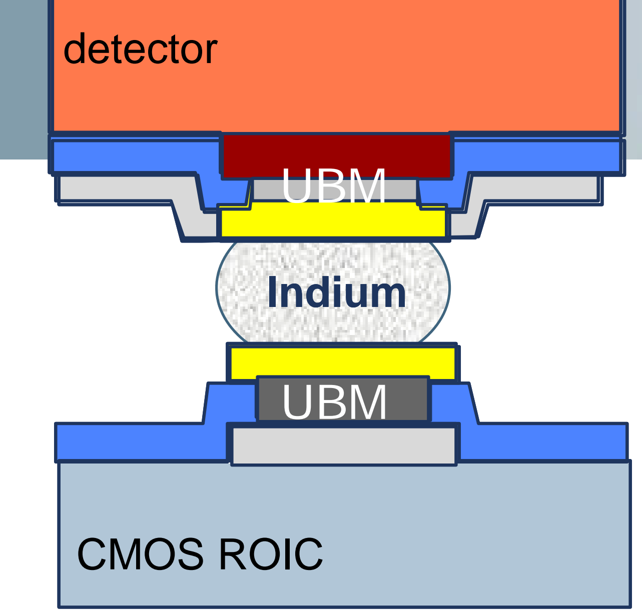




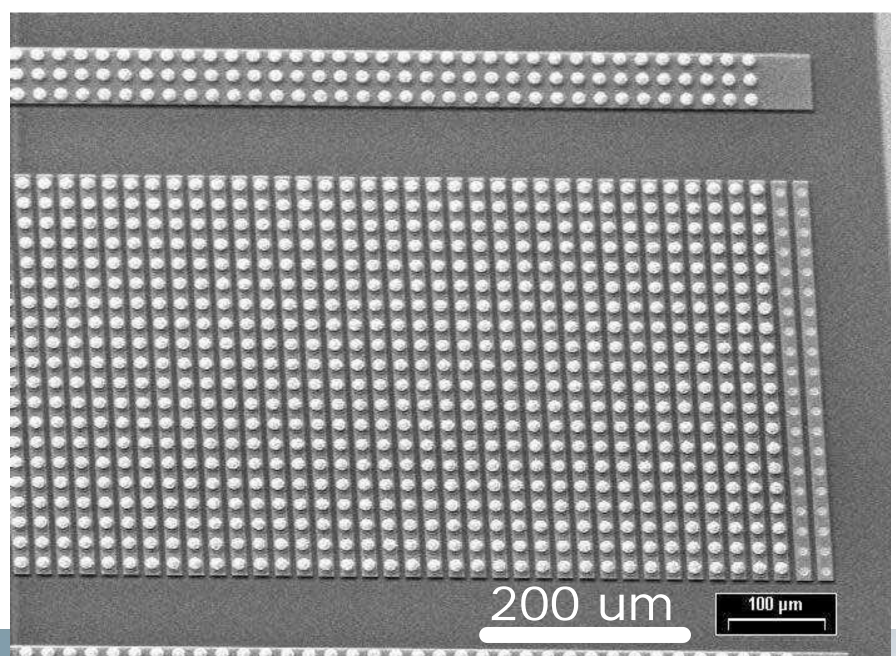


D. Sabuncuoglu et al., ECTC 2007

Technology enablers: (Micro-)bumping



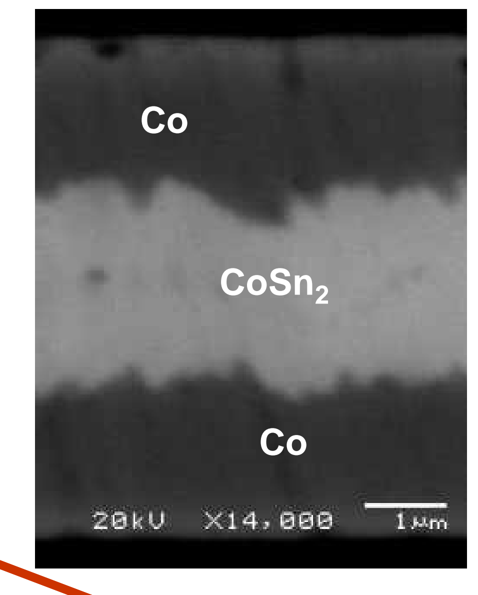
- Technology:
  - (post-)processing Si, CMOS
  - under bump metallization (UBM)
  - solder (e.g. In, Sn, ...) deposition using electroplating or evaporation
  - flip-chip bumping
- Features:
  - bump size ~ 10 um
  - pitch ~ 20 um
  - 1 Mpixel 2D arrays
- Applications:
  - hybrid interconnect between substrates of different technologies with low parasitics/microphonics
  - high density interconnect between imagers and read-out



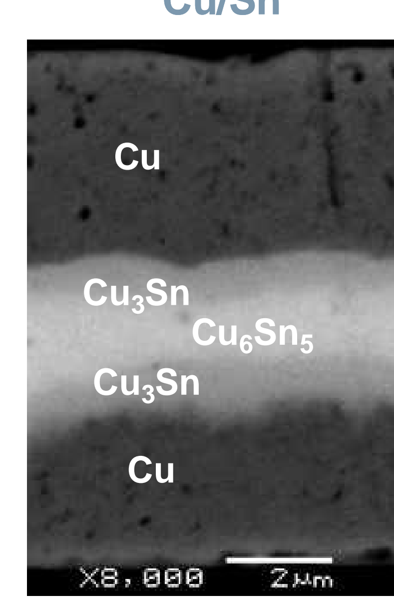
Technology enablers:
(Micro-)bumping: Transient Liquid Phase bumping

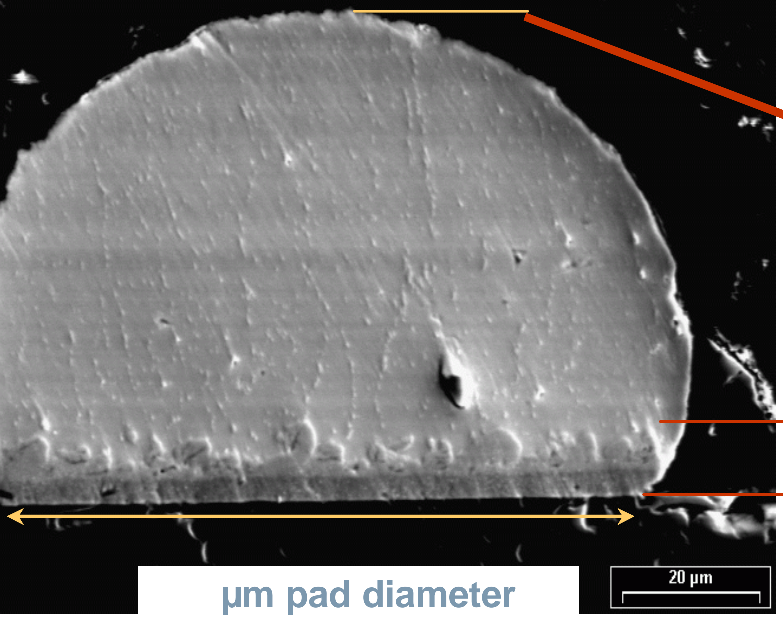
- Small bumps:
  - no solder
  - Inter Metallic Compound (IMC)
- Advantage:
  - higher melting point allows 3D stacking
- Disadvantage:
  - multiple (brittle) phases
  - reliability issues

Co/Sn



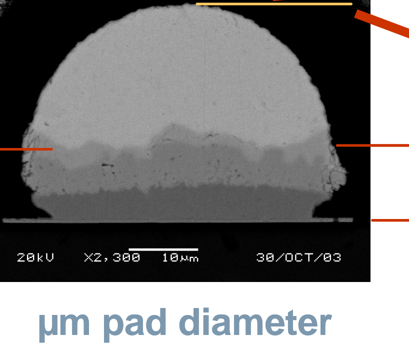
Cu/Sn





μm pad diameter

\- μm bump pitch



μm pad diameter

μm bump pitch

IMC

μm pad

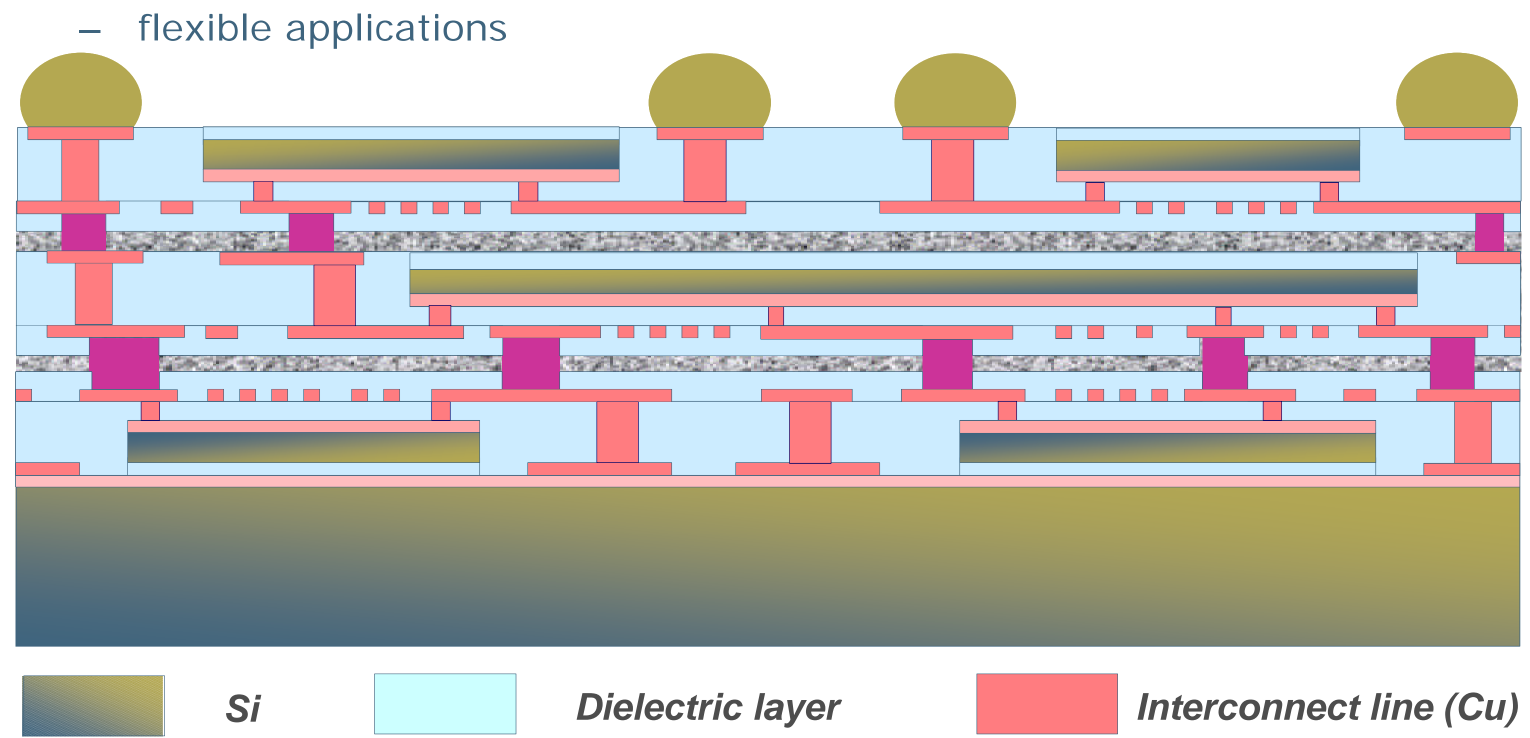
μm pitch

μm pad

μm pitch

3D-WLP:
Ultra Thin Chip Embedding

- Approach:
  - ultra thin 10 to 20 µm thick die
  - embedded in a multilayer thin film build-up
- Advantages:
  - allows different die size
  - flexible applications



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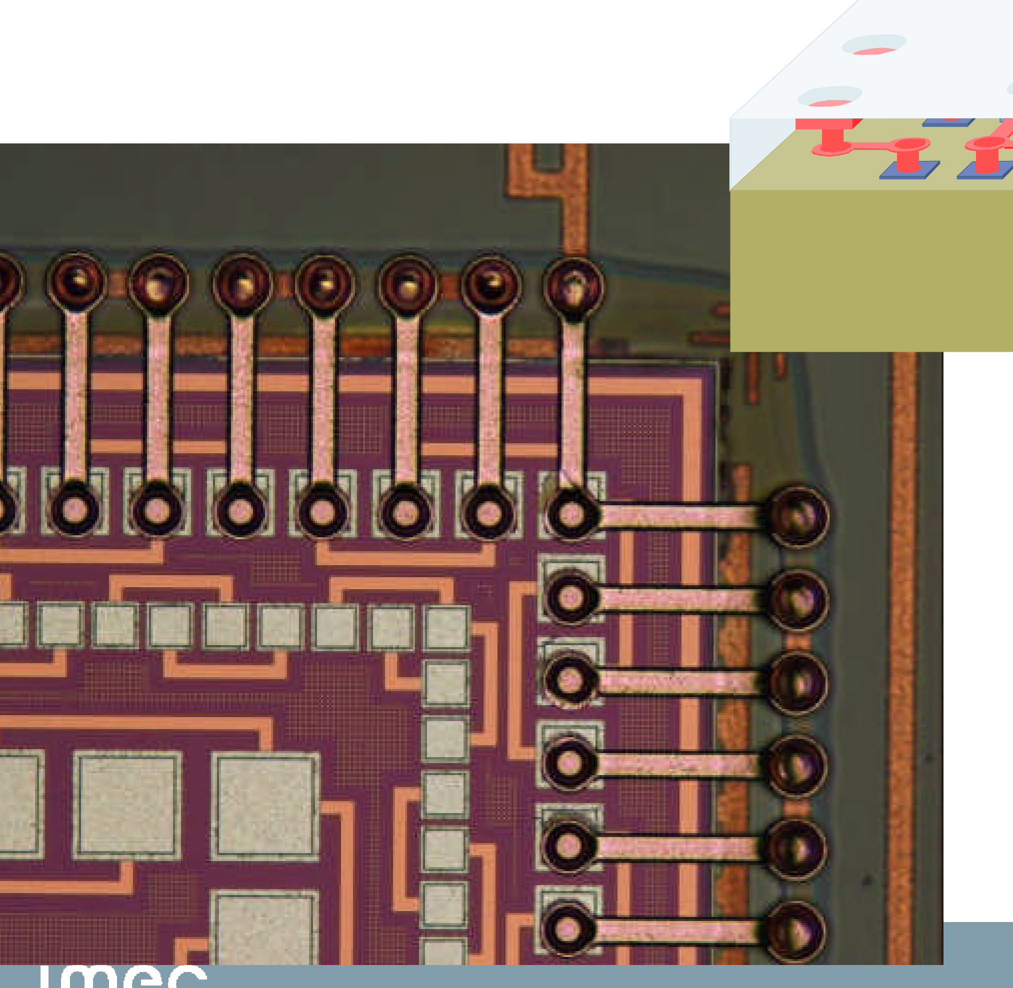
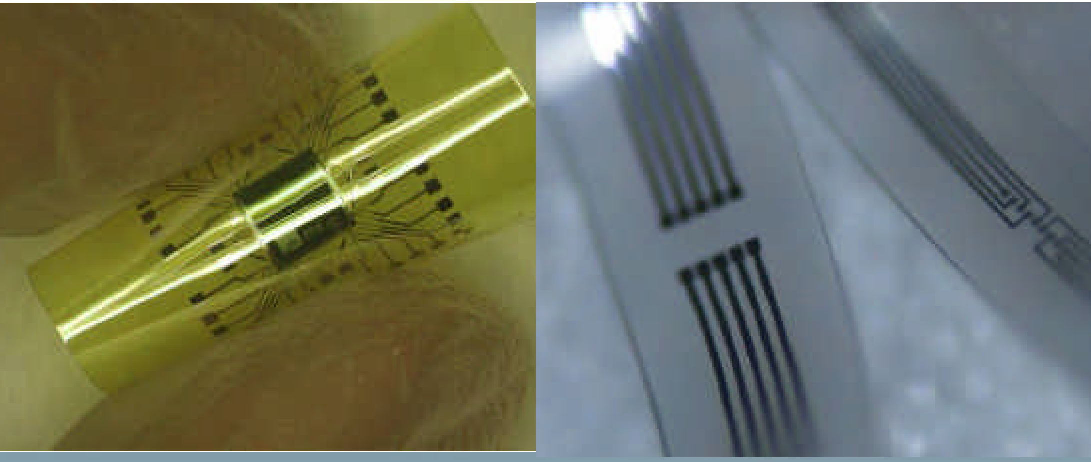


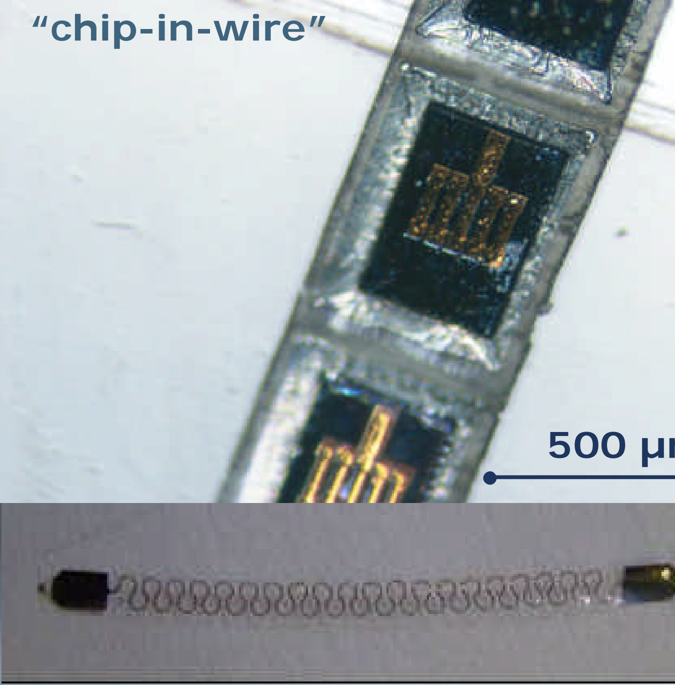
- UTCS example:
  - 20µm thin Si-die,
  - 40µm pad pitch connections

3D-WLP: Ultra Thin Chip Embedding: Flexible electronic systems

- thin chip embedding on sacrificial layer
- release of sacrificial layer: chip-in-flex
- result: flexible/stretchable embedded electronics using e.g. Silicone dielectric

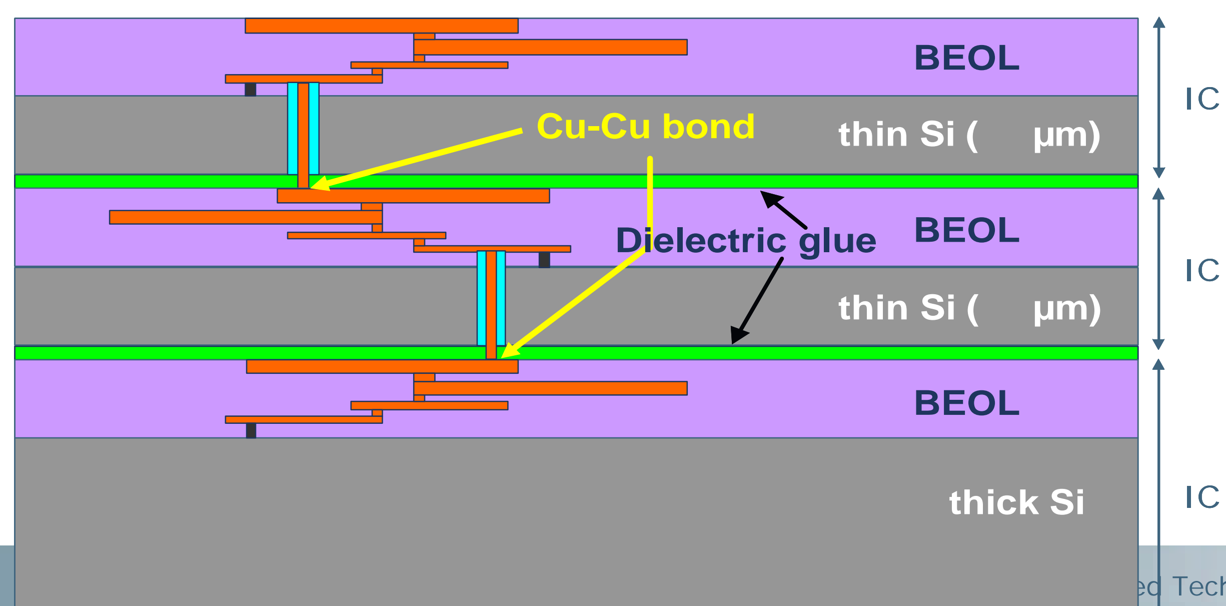
M. Vanden Bulcke et al., IEEE-EMBC 2006





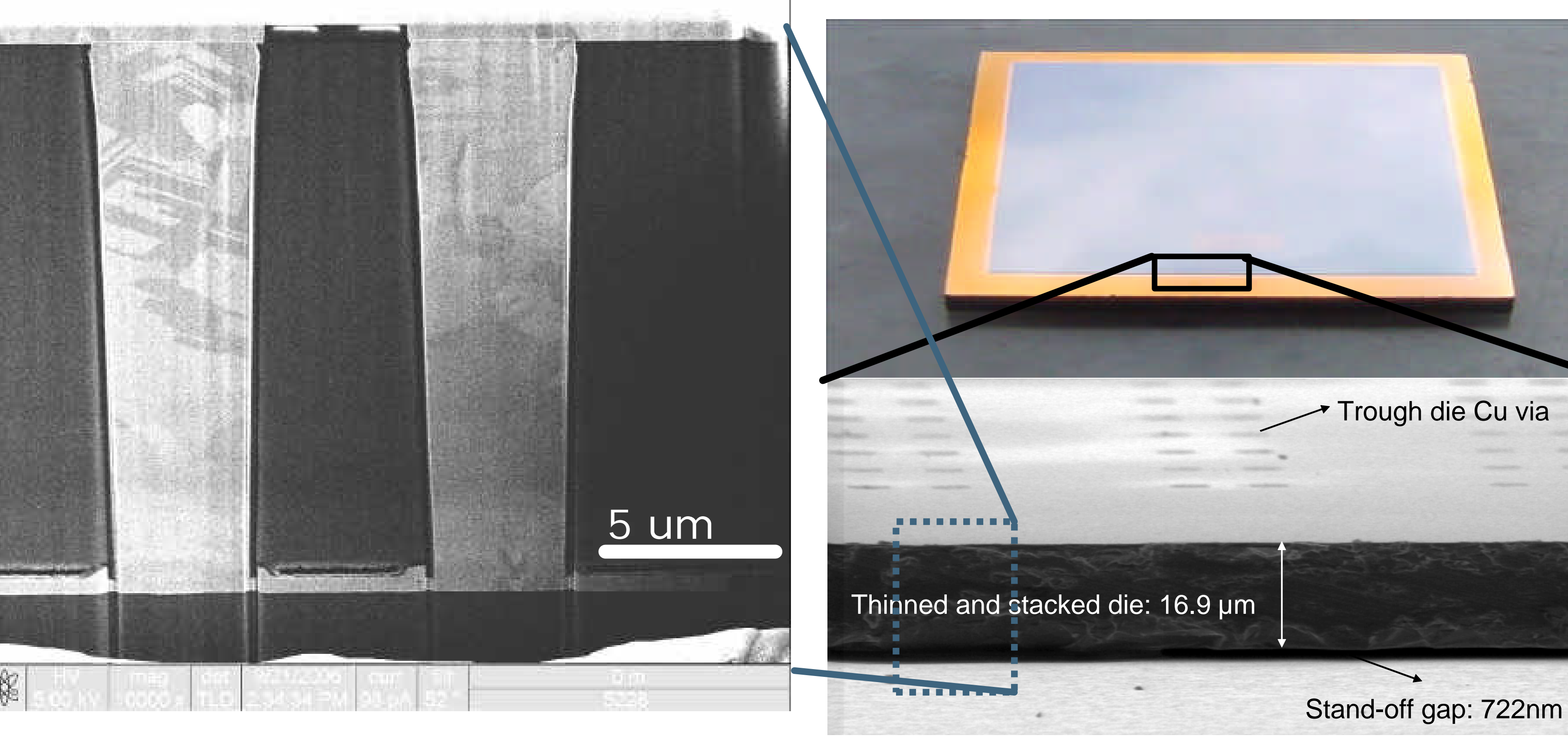
3D-SiC approach:
Introduction

- Technology:
  - fabrication at device level, i.e. as a part of (CMOS) flow
- Specifications:
  - Si thickness: 10 – 20 um
  - via diameter: 3 – 5 um
  - via pitch: 10 um
- Applications:
  - CMOS/memory/imager stacking



3D-SiC approach: Results

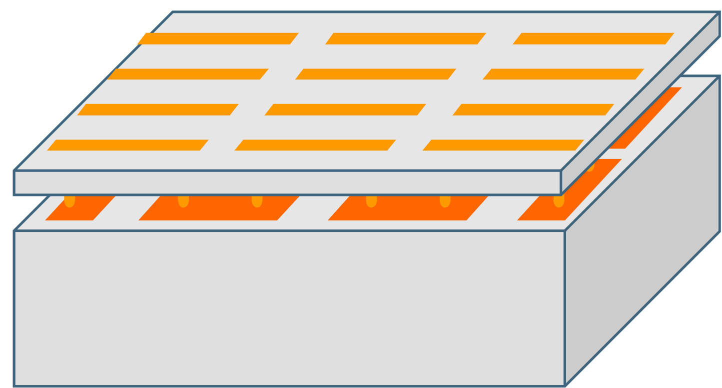
- Through Si vias:
  - Pitch 10 micron, via diameter: 5 micron

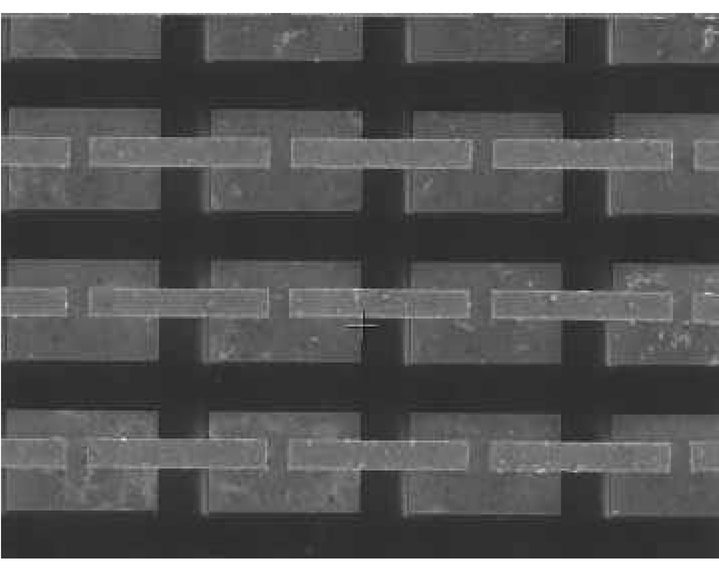


B. Swinnen et al., IEDM 2006

3D-SiC approach:
Results

- Visualization of daisy chain by etching of top substrate in KOH:

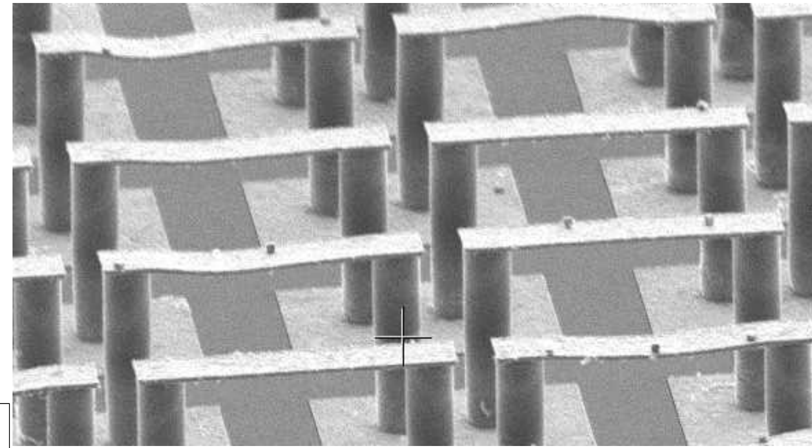


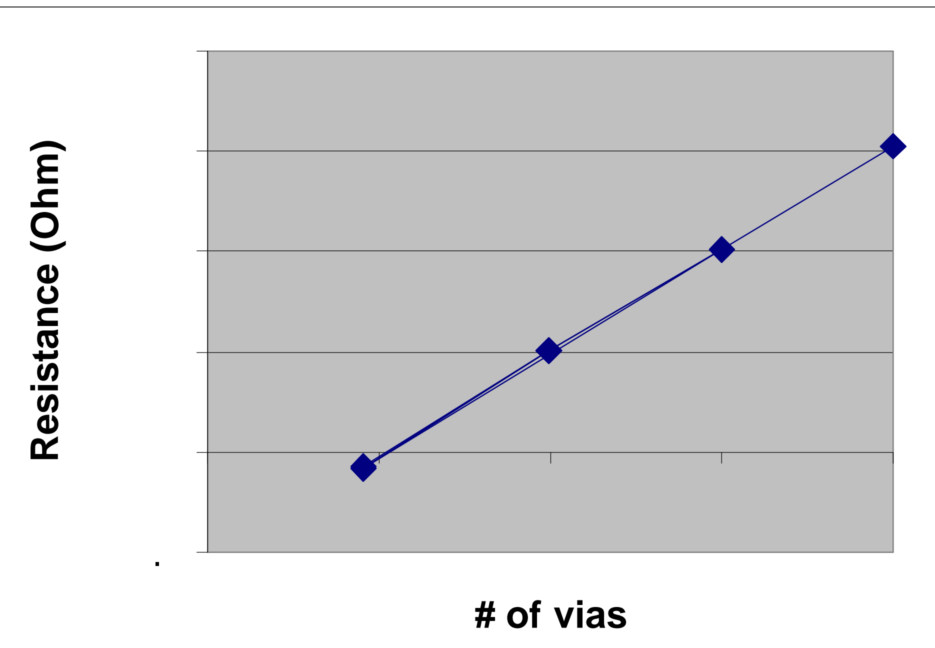


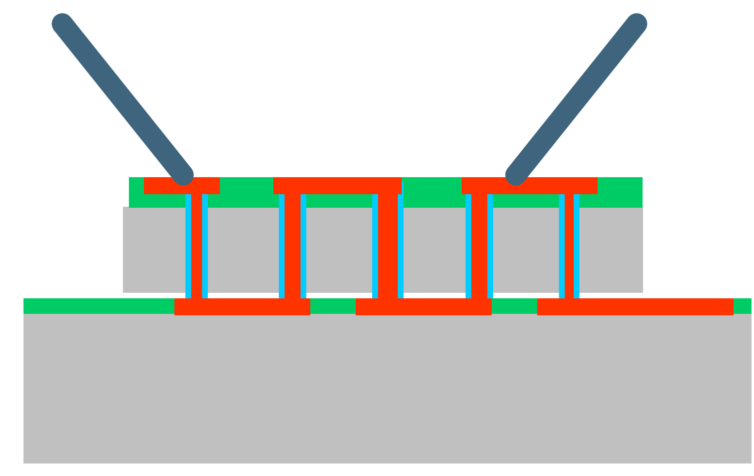
4/25/2006 4:06:29 PM | HV 5.00 kV | spot 3.0 | mag 1 915 x | WD 2.2 mm | det ETD | pressure 1.85E-8 bar | 30 µm | IMEC Cu NAIL

3D-SiC approach:
Results

- 10000 Cu vias in series yielding
- Linear I-V curve
- Via resistance ~ 30 mOhm
- close to bulk Cu resistance







IMEC's 3D Interconnect R&D Roadmap

3D interconnect complexity

3D-SIC

3D-SIC 2-layer

3D-SIC n-layer

n-layer UTCS 3D-SIC

3D-WLP

Ultra Thin Chip embedding 2-layer UTCS

Chip-in-Flex UTCF

n-layer UTCS

n-layer UTCS 3D-WLP

Face-to-face Flip-chip

Face-to-face Micro-bumps

3D-WLP 2-layer Through-Si

3D-WLP n-layer

3D-SIP

Stacked-IC Package

3D-SIP BGA

3D-SIP CSP

3DSIP Die-in-board

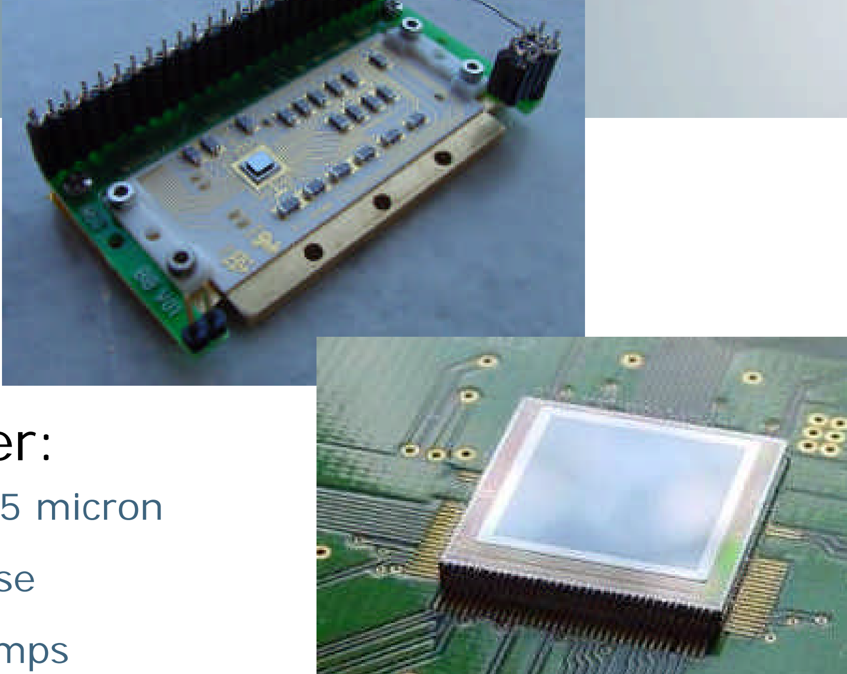
2004 2005 2006 2007 2008 2009

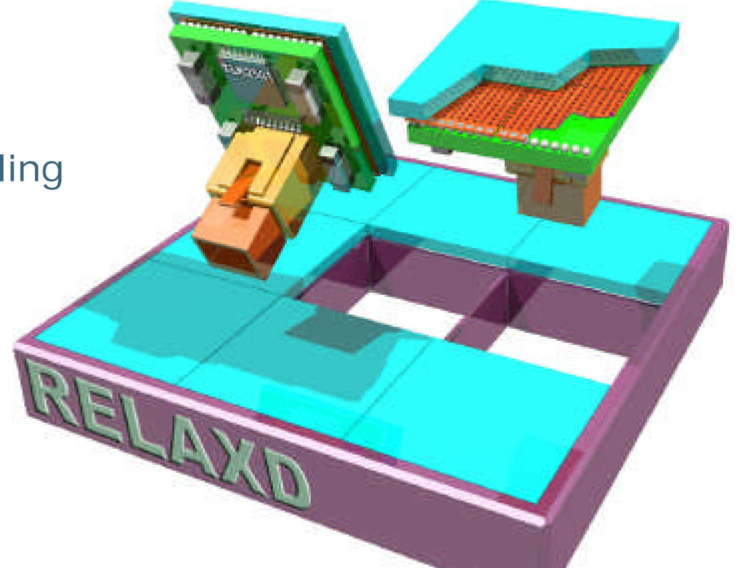
Positioning different 3D approaches

	3D-SIP	3D-WLP		3D-SIC
Technology	Package interposer	WLP, Post-passivation		Si-foundry, Post FEOL
3D interconnect	Package I/O	UTCS Embedded die	Si-through vias	Si-through “Cu nail” vias
Intercon. Density *Peripheral* *Area-array*	‘package-to-package’ 2 - 3 /mm 4 - 11/mm^2	‘around’ die 10 - 50 /mm 100 -2.5k/mm^2	‘through’ die 10 - 25 /mm 16 - 100/mm^2	‘through’ die 25 -100 /mm 400-10k/mm^2
3D Si Via pitch 3D interconnect pitch	- 300 – 500 µm	- 20 – 100 µm	40 – 100 µm -	< 10 µm -
3D Si Via diameter	-	-	25 - 100 µm	1 - 5 µm
Die thickness	> 50 µm	10 - 20 µm	50 - 100 µm	10 - 20 µm

Detector Applications: Examples

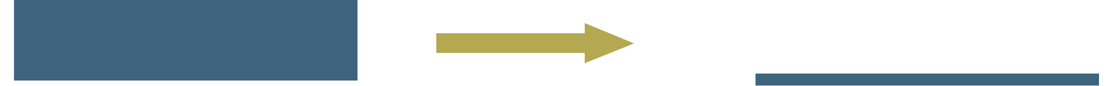
- Cryogenic far IR detector:
  - Linear array of blocked impurity detectors
  - Hybridized on cryogenic read-out
- Backside illuminated CMOS imager:
  - 1 Mpix, 22.5 um pitch, thinned down to ~35 micron
  - 100% fill factor, High QE, high blue response
  - Both monolithic and full hybrid using In bumps
- RelaxD: tilable X-ray sensors:
  - 3D stack of X-ray 2D array, Medipix read-out, system board
  - In combination with edgeless detectors allows tiling of imager modules
- Analog read-out design for imaging:
  - Cryogenic and radiation tolerant design using standard CMOS





Conclusions & outlook I

- 3D integration technology is developing fast and will become commercially available in the coming years
- It will allow manufacturing of advanced detection systems:
  - highly **miniaturized**, i.e. very small in vertical dimension

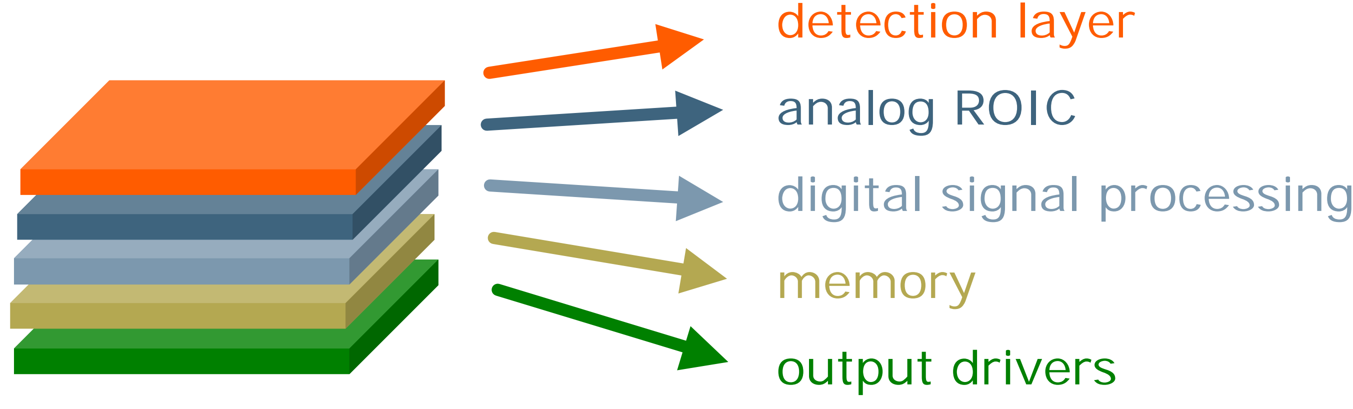


  - **tilable**, i.e. enabling large area detection with minimal non-sensitive area

  - **very thin**, e.g. **flexible** detector systems, for e.g. non-planar 4π detection, ΔE detectors

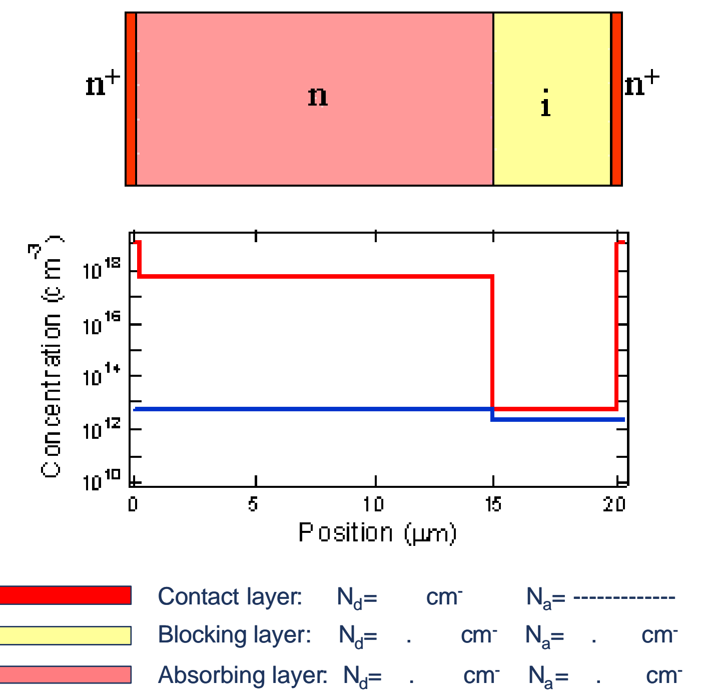
Conclusions & outlook II

- 3D integration technology will allow manufacturing of advanced detection systems:
  - **complex** imaging detectors using high density 3D interconnects (=1 per pixel) between different intelligent layers:



aspire invent achieve

Detector applications:
Cryogenic BIB detector



- Far IR detection: 6 – 18 um wavelength
- Si:As Blocked Impurity Band (BIB) detector array operating at 4 K
- Backside illuminated through high resistivity Si

BIB Detector

Readout Chip

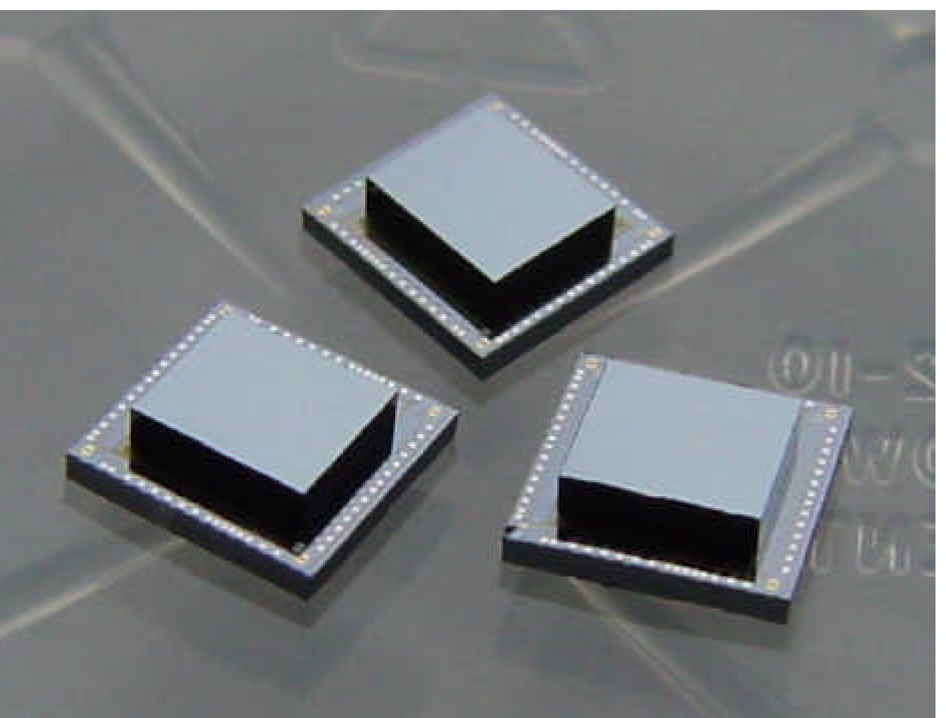
- Hybridization on cryogenic ROIC using In bumps

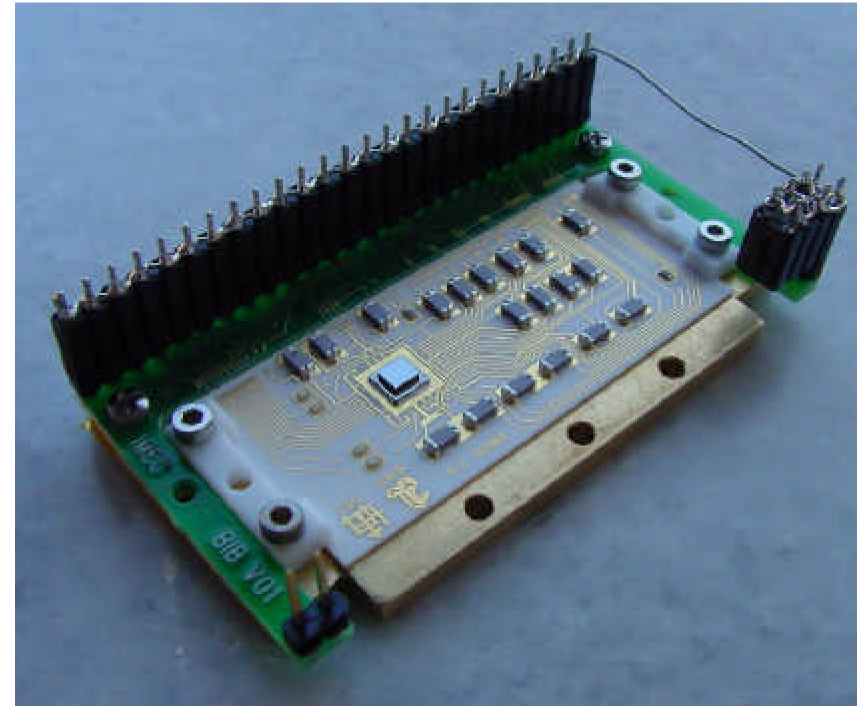
imec

esa

Detector applications:
Cryogenic BIB detector

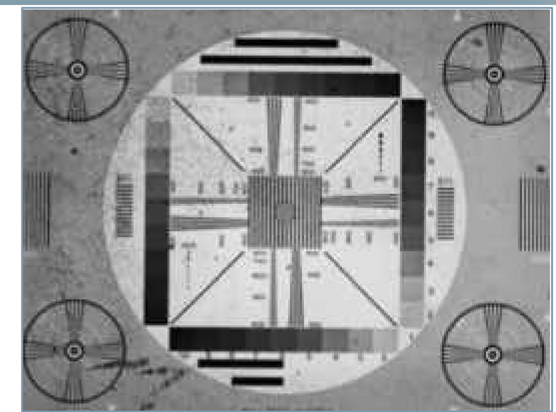
- Linear array: 2x 88 pixels
- Pitch: 30 um
- Application:
  - DARWIN mission: search for exoplanets

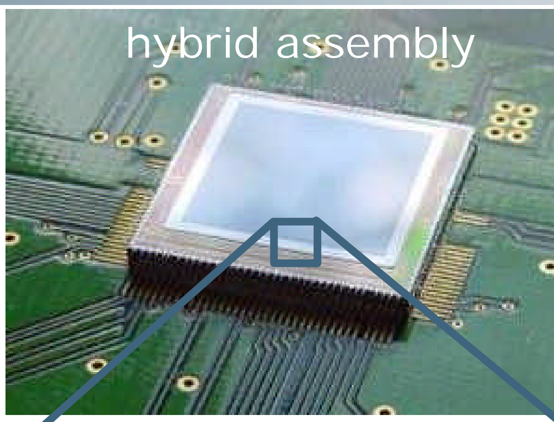


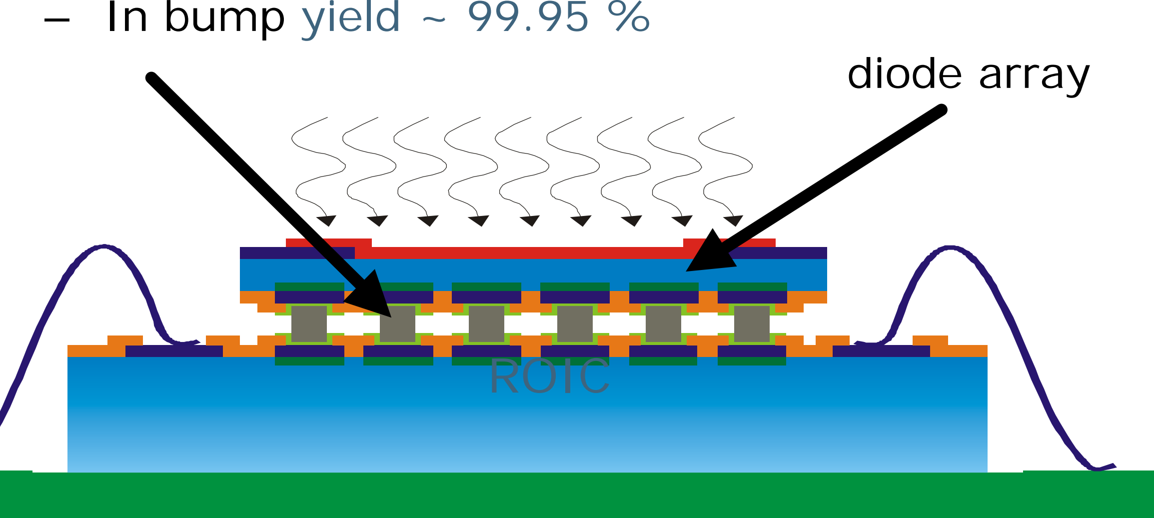


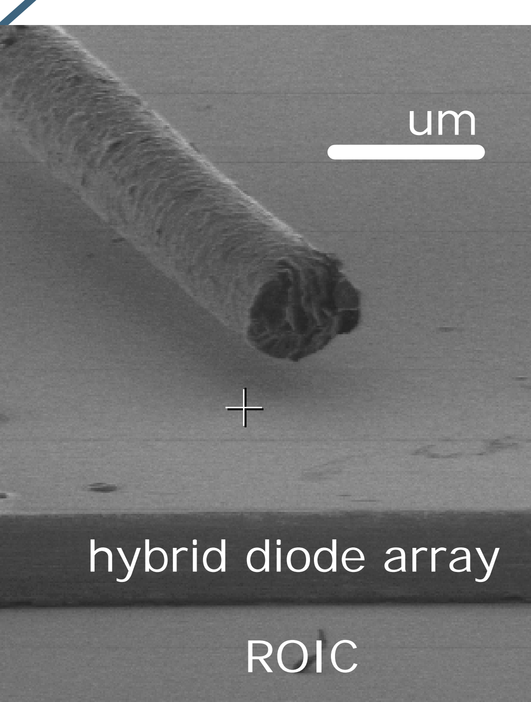
Applications: Backside illuminated CMOS imager

- Specifications:
  - 22.5 um pitch
  - 1 Mpixel
  - thinned down to +/- 35 um
  - In bump yield ~ 99.95 %





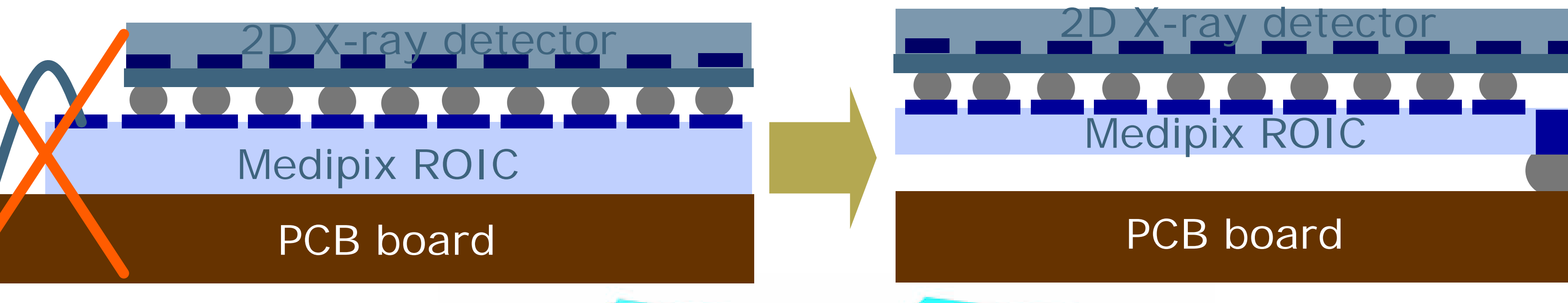


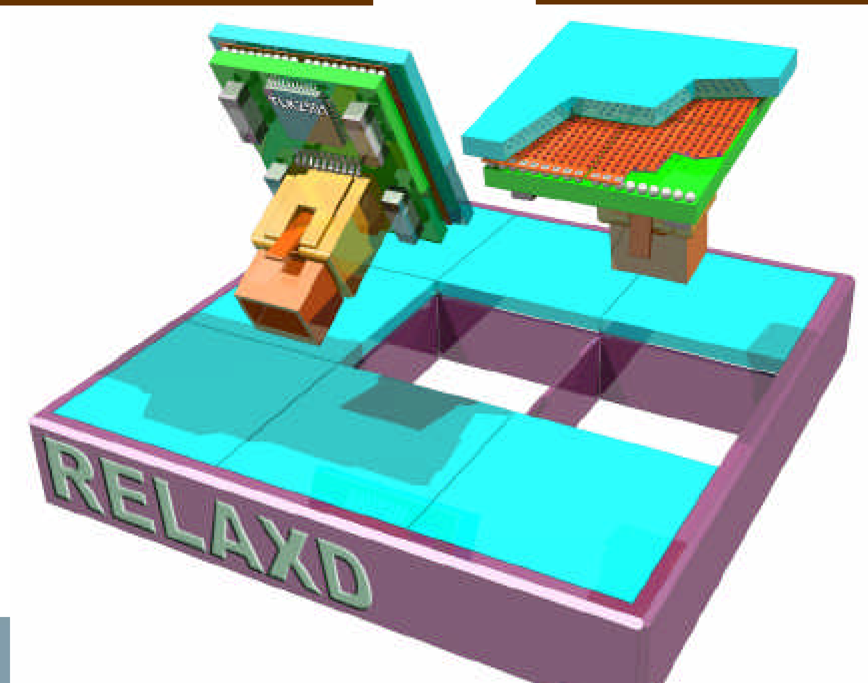


K. De Munck et al., IEDM 2006

Detector applications:
RelaxD: tilable X-ray imagers

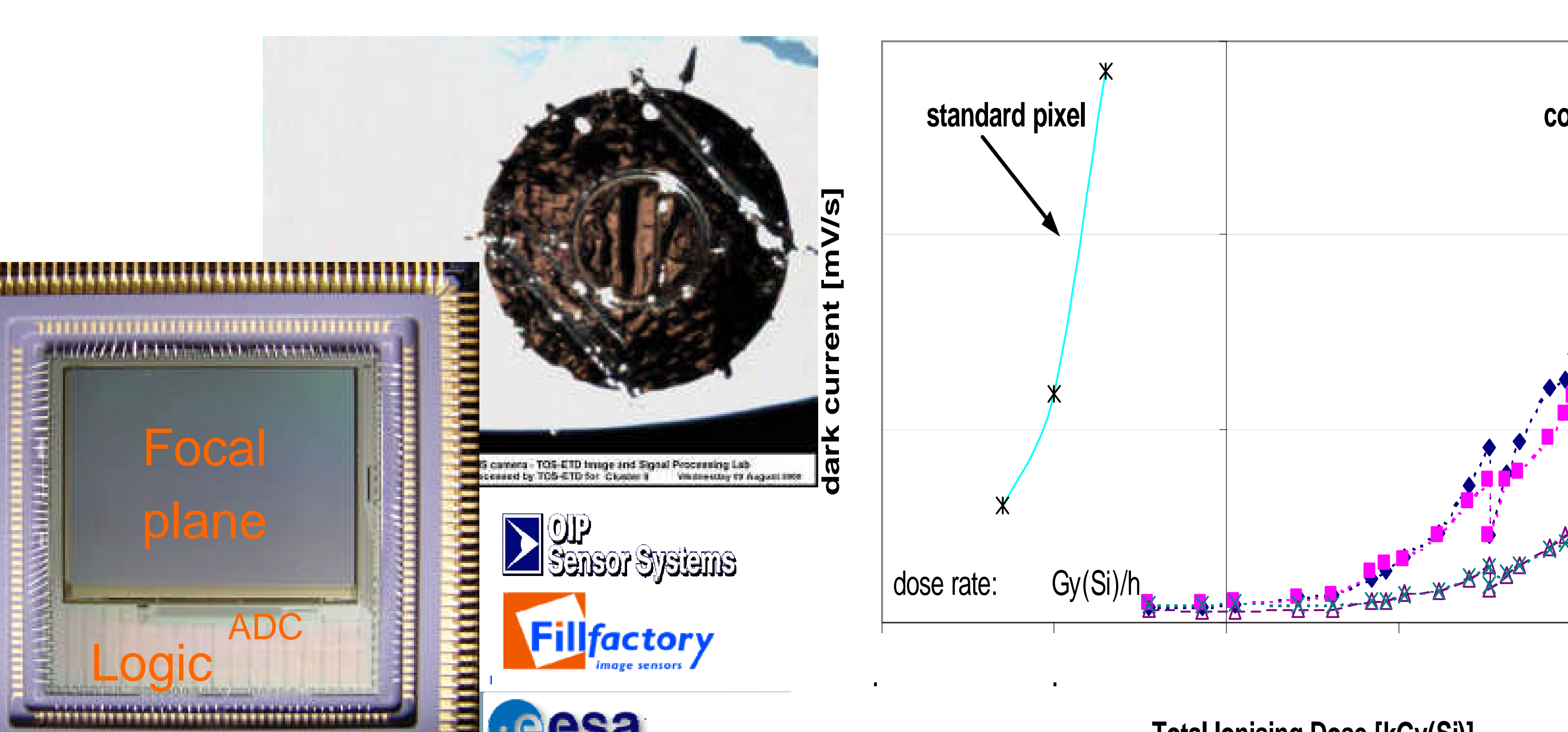
- 3D integration of 2D X-ray imager
- tiling of modules for large area detection





Enablers:
Custom analog design: radiation tolerant

- Radiation-tolerant analog ROIC design:
  - nMOS pixel design (using 0.7µm Alcatel Microelectronics Technology)
  - 2-3 orders of magnitude less sensitive to total dose
- Example: Flight Model IRIS3
  - CMOS camera for imaging in space



Enablers:
Custom analog design: cryogenic ROICs

- Analog design for 4 Kelvin operation:
  - special design to avoid anomalous behavior of standard CMOS < 20 K
- Example: PACS-CRE: ROIC for a far-infrared detector array
  - ~ 200 qualified assemblies delivered to ESA
  - Herschel satellite to be launched in 2008
  - very low noise: measures 10 fA – 100 pA
  - very low power consumption: 80 μW
  - irradiation tolerant @ 4 K