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# Technical approach for 3D integration

**Gilles Poupon**

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# Contents

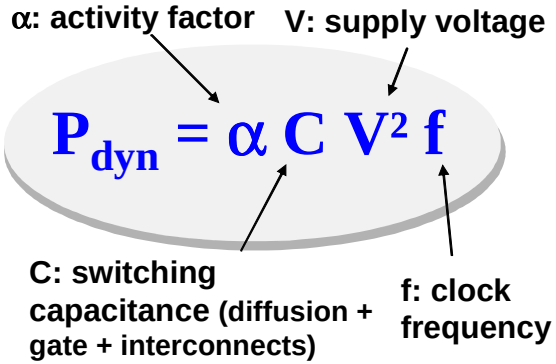
- 3D integration : motivation / challenges
- Technology roadmap : A 3D generic tool box
- Applications
- Summary/prospects

# 3D integration challenges & interests

## ➢ Interconnects challenges :

✓ **Today, More than 50% of dynamic power consumption is due to interconnects. This rate is projected to increase.**

*[Nir Magen et al, Proc. of the 2004 international workshop on System level interconnect prediction, France, pp 7-13, 2004]*




✓ **Interconnects are the main issue in term of :**

- **Power consumption**
- **Frequency limitation**
- **Signal integrity**
- **Thermal management**

✓ **Same issue for every levels of interconnects:**

- **IC level**
- **Component level**
- **System level**

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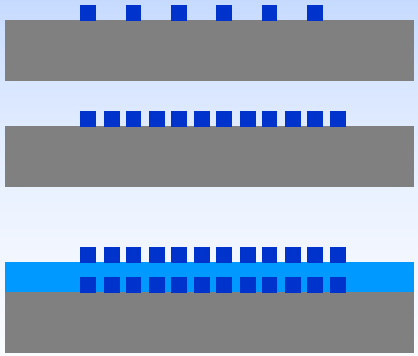
# Motivation for 3D

## *Front-end world*

- *The end of scaling*
- *The end of the « Great SOC Euphoria »**

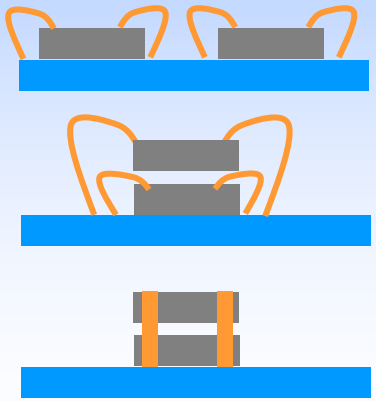
*Need 3rd dimension to increase IC performances*



## *Packaging world*

- *Need for compact systems*
- *Limit of classic wire bonding techniques*

*Need 3rd dimension to reduce packaging cost & dimension*



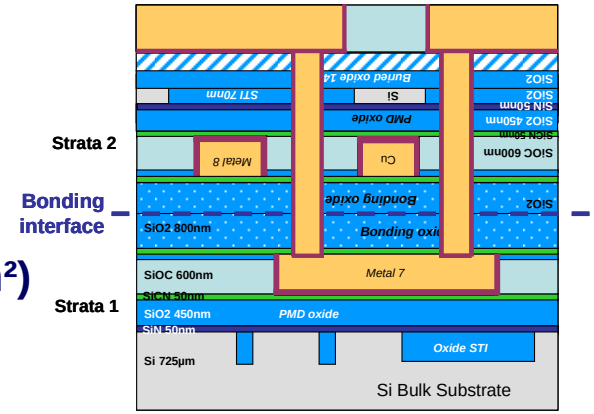
***2 different world => 2 different targets… but a common technologic toolbox***

# 3D integration challenges & interests

## ➢ Different challenges to solve at different levels :

### ✓ IC level

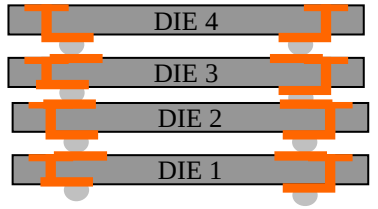
- ✓W2W or C2W bonding
- ✓ High accuracy alignment (+/- 1µm)
- ✓ High density TSV pitch 5µm (~$10^6$ vias/cm²)
- ✓ Vias first or last – Cu filling




### ✓ Homogeneous component level

- ✓ W2W or C2W bonding
- ✓ Temporary bonding
- ✓ Medium density TSV (~$10^5$ vias/cm² , pad pitch >50µm)
- ✓ Vias first or last
- ✓ Components stacking

3D stacking



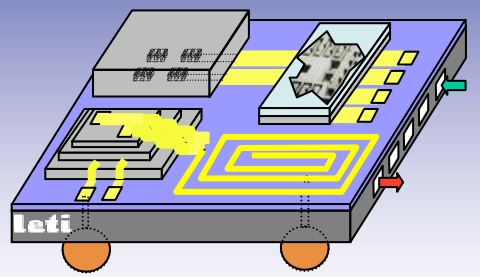
# 3D integration challenges & interests

➢ **Different challenges to solve at different levels :**

✓ **Heterogeneous components level ➔ System**

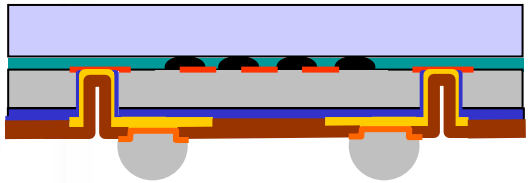
- ✓ **Temporary bonding**
- ✓ **W2W or C2W bonding – High accuracy alignement**
- ✓ **Heterogeneous materials**
- ✓ **Components stacking**
- ✓ **Vias first & last**
- ✓ **Redistributive Layer**

**SoW**
**System On Wafer**



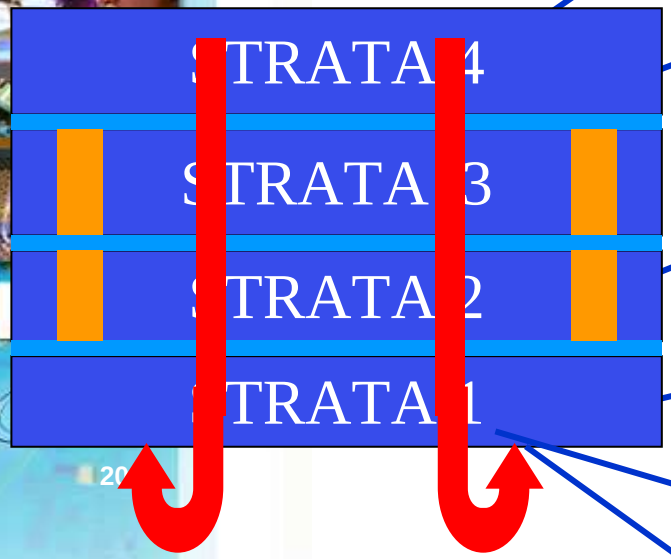

**Chip on wafer**
**All Silicon**

CMOS devices packaging



MEMS packaging

# 3D Generic toolbox




- ***Bonding / Alignment***
- ***Interstrata connexions***
- ***Intrastrata connexions (TSV, …)***
- ***Thinning & handling***
- ***Chip on wafer planarization***
- ***Thermal management***

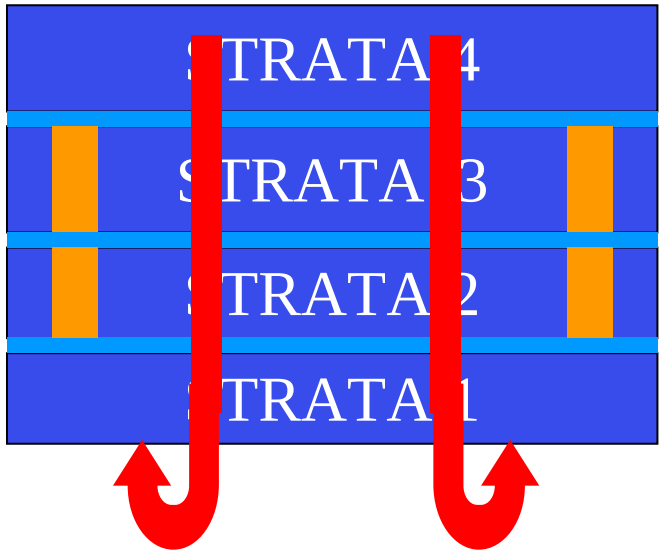
*3D DESIGN*

*COST ANALYSIS*

*TEST & RELIABILITY*

# Technology options / Tool box

- Integration level
  - Wafer  to wafer
  - Chip to wafer
- Face to face / back to face
- Through silicon vias
  - First
  - Last
- Materials
  - Si
  - SOI
  - Bulk
  - MEMS
- Bonding / Alignment / Thinning / Handling



# Bonding & alignment

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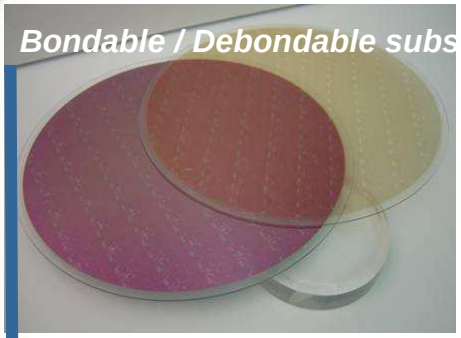
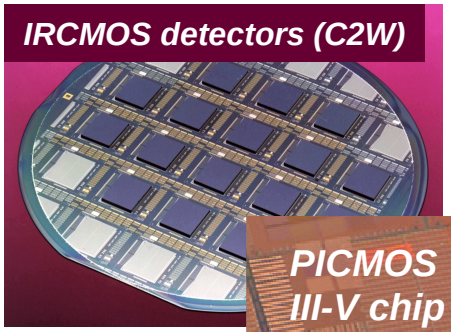
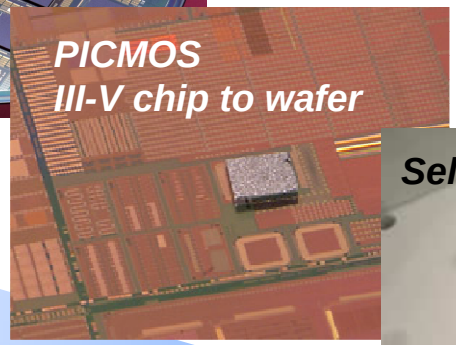
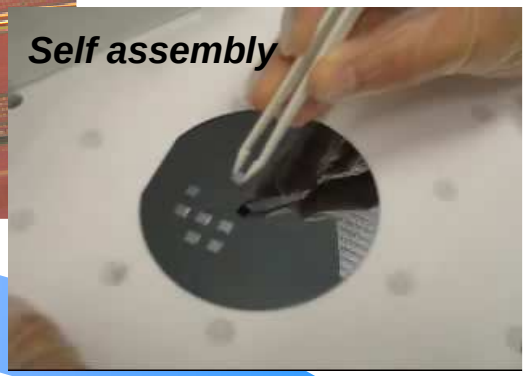
Pitch reduction




Technology available

Applied research

Advanced research

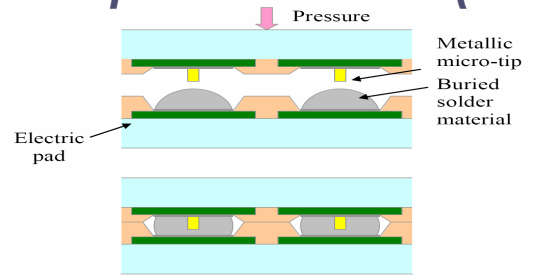
# Bonding & alignment

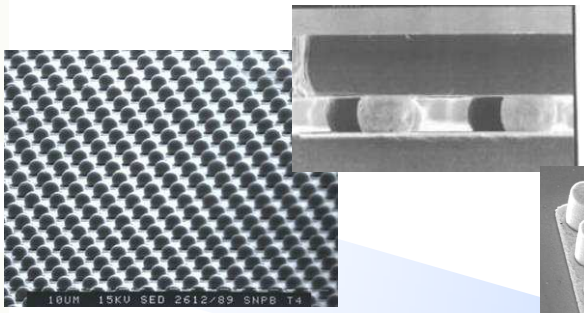
| | W2W | C2W |
|---|---|---|
| Bonding | Polymer<br>Direct (isol. / ohm)<br>Low temp (150℃ / 400℃) | Polymer<br>Direct (isol. / ohm)<br>Low temp (150℃ / 400℃) |
| Alignment | 2008 : +/-1µm<br>2010 : ~0.5µm | 2008 :<br>-<10µm (High Throughput)<br>- <1µm (Low throughput)<br>Ratio speed / accuracy<br>Self assembly |
| | | |

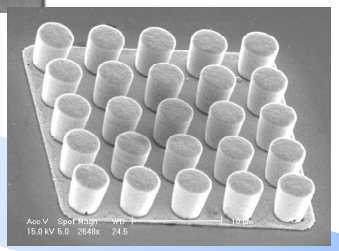
# Interstrata connection for 3D


Pitch reduction

## Low pitch insertion (TB2)



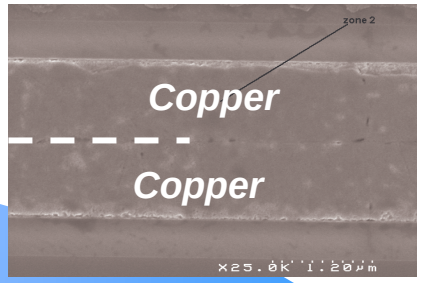





## Classic Flip chip
*(Ball or stud bump)*

## µbumps

## Direct Metal Bonding (DMB)




## Nanointerconnects

Technology available

Applied research

Advanced research

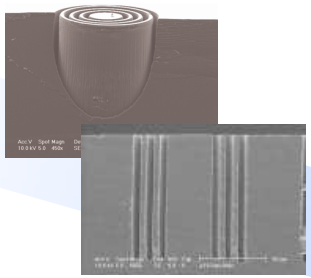
Joint lab leti axalto

## Capacitive coupling by Direct bonding

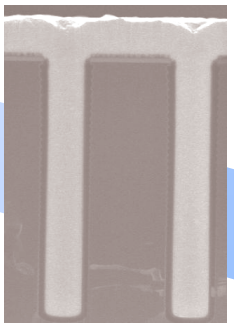
# Intrastrata connection for 3D

*TSV (pre-process vs mi-process vs post-process)*
*Density / diameter*
*Filling or not*
*Using : Static : R - Dynamic : RC / band width*

*Cu TSV (3µmx15µm)*



4 µm rings



*Pitch reduction*

*Technology available*

*Applied research*

*Advanced research*

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# Through Silicon Vias highlights

## 2 different concepts : Vias first & vias last

***Technologies***

***Highlights***

**Vias first**

**Vias last**

| *Pre process vias* | *Mid process vias* | *Post process vias* |
|---|---|---|
| Via Structuration | FEOL | FEOL |
| FEOL | Via Structuration | BEOL |
| BEOL | BEOL | Vias |
| Via Exposure | Via Exposure | Packaging |
| Packaging | Packaging | |
| FEOL/BEOL comp. | BEOL comp. | Ultra Low resistance |
| Technology cost | Technology cost | Low temp. process |
| Yield | Yield | Low AR |
| Design flexibility | Low resistance | Techno. Flexibility |

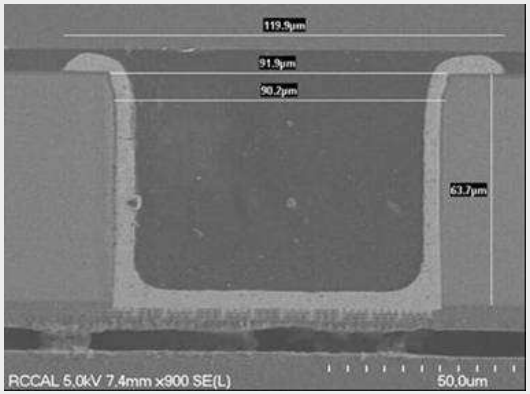
# Thru-Si-Via realization

**TSV diameter**

100µm | 10µm | 1µm

Aspect Ratio

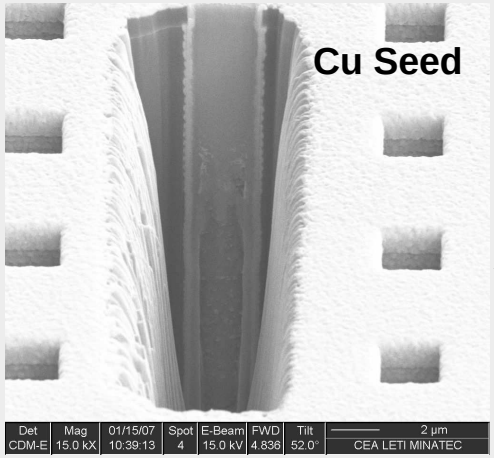
1




90µ-wide / 80µm-deep

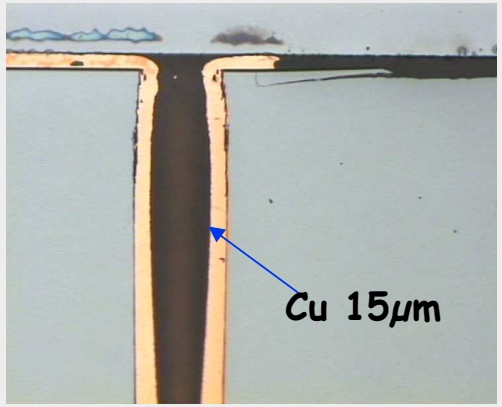
AR=1

**High density TSV**




3µm-wide / 15µm-deep

AR=5




80µm-wide / 500µm-deep

AR=7

10

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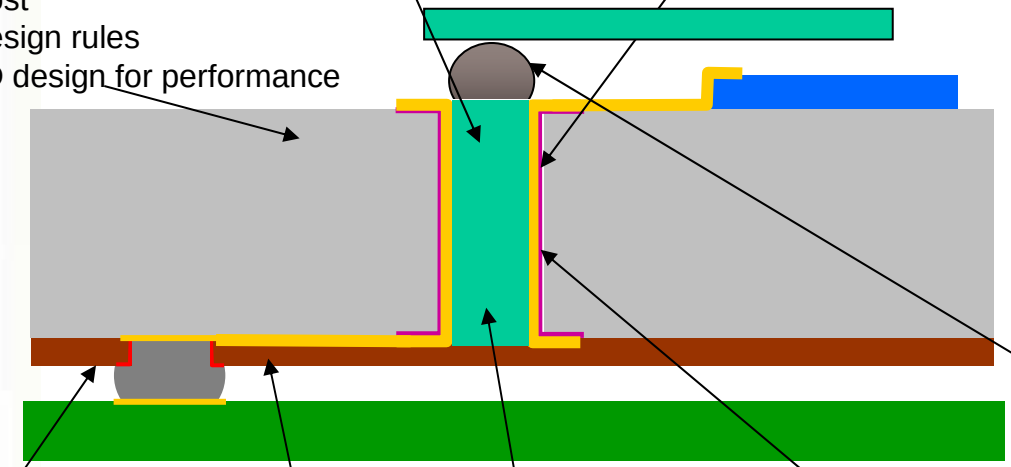
# TSV : a complex system



**Through hole isolation**
-Methodology
-Material
-Thickness uniformity
-Barrier & adhesion properties

**Vias filling / Plating** :
- Voïds Free Filling / Plating

**Design :**
-Cost
-Design rules
-3D design for performance

**Thermal/reliability**
-Thermal management
-2nd level joint reliability
-RDL integrity
-Through via reliability performance

**Interconnections :**
-Die to wafer
-Wafer to wafer (wafer alignment)
solder vs Au stud vs metal to
-Metal diffusion bond
-With or without underfill
-High alignment accuracy
-High breakdown voltage
-Low leakage

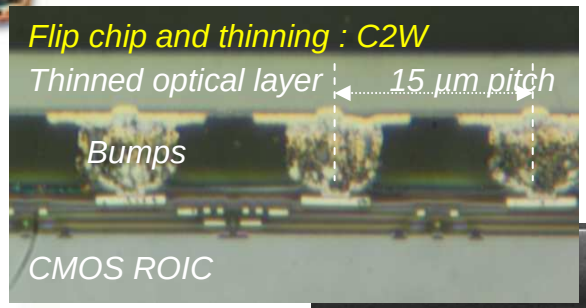
**RDL** :
-Routability
-Fine pitch (<100µm)
-Fine pitch & space

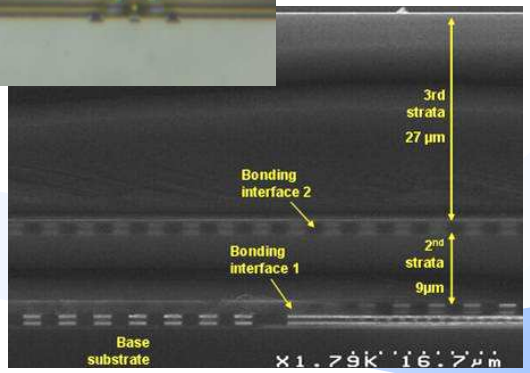
**Cost / test / yield**
-Cost
-Know good die
-RDL integrity
-Via quality assurance
-Thin film interconnection quality

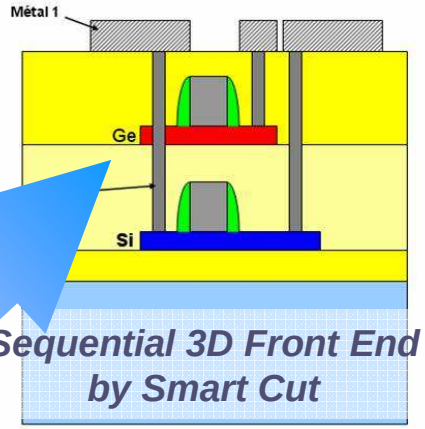
**Deep Si etching**
-Via size & depth uniformity
-High-aspect ratio etching
-Through hole scallop control
-Sidewall profile control

**Seed layer**
-Conformity
-Thickness uniformity

# Thinning & handling for 3D


*Sequential 3D Front End by Smart Cut*

*G ing + ESL technique op layer / other and c aper than SOI)*

*200mm wafers & Down to 10µm*

*300mm wafers (2008)*

*Smart cut applied to circuit transfert*
*➔Ultra thin chip or wafer (<4µm)*
*➔planar technologies*
*(Thick Handel & Thin Chip : TH&TC)*

*Technology available*

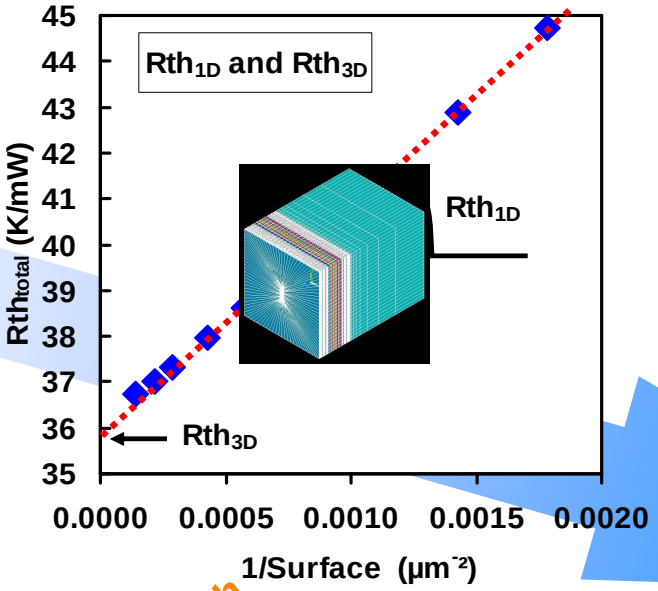
*Applied research*

*Advanced research*


# Thermal management

*Thermal spreader (interstrata)*
*Hot spot cooling*
*Active system*

## *Local 3D simulation*




*Pitch reduction*

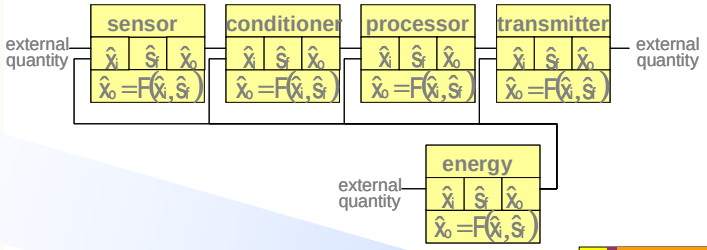
*Technology available*

*Applied research*

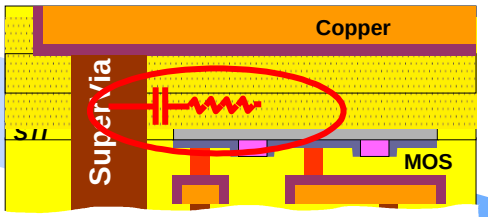
*Advanced research*

# 3D Design Methodologies

## *Heterogeneous Design*




## *3D partitioning*




*Pitch reduction*

*Full Custom CAD Flow*
*3D Parasitics*
*3D design rules*

*Technology available*

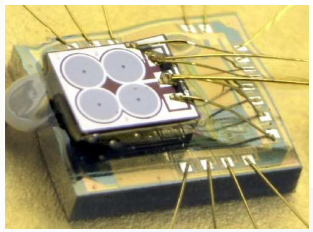
*Applied research*

*3D Floor planning*
*3D Place&Route*
*3D thermal Aware analysis*

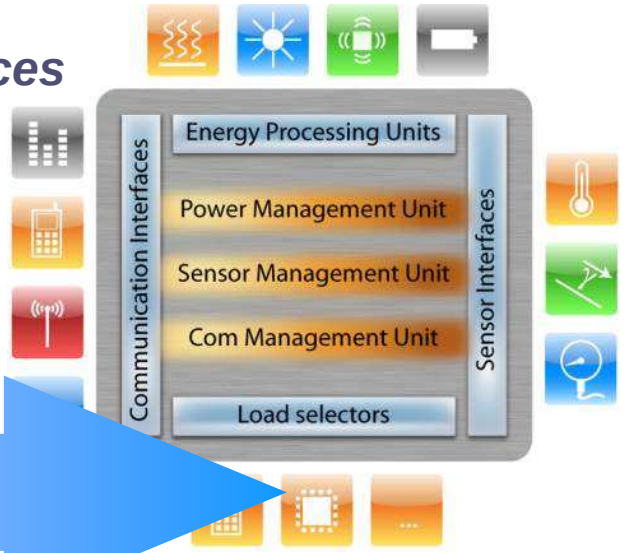
*Advanced research*

# 3D Design & Architectures


***Sensor Interf.***
***Power Managt.***



***Multi Energy sources***
***Multi Sensors***
***Wireless interface***
***Stacked antenna***
***(Energy Managt.)***




***Memory on top***
***Of Computing***

***Capacitive or***
***Inductive interstrata***
***communications***

***3D Network on Chip***
***Computing & Memory***
***Deeply interacting***

*Technology available*

*Applied research*

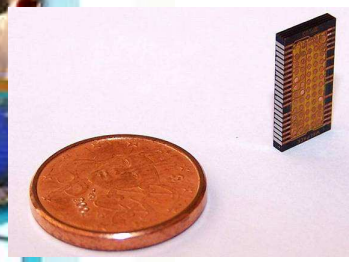
*Advanced research*

# 3D concept : exemple of implementation at LETI

## 3D Integration level

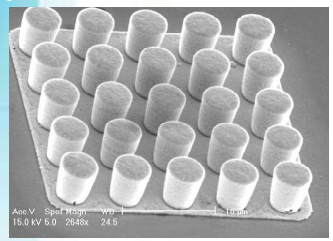
chip → wafer

### Advanced Packaging



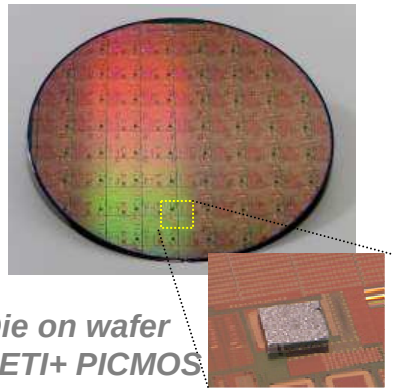
***Packaging by neo-wafer concept (LETI + 3D PLUS)***

2007

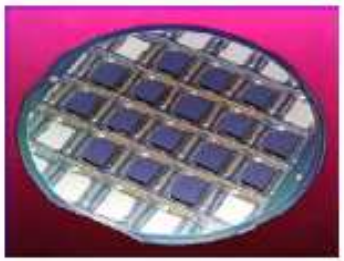


***Electroplated Micro-bumps***

### Die or chip on Wafer

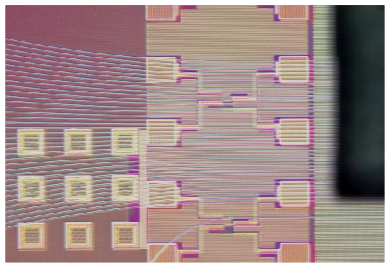


***Die on wafer LETI+ PICMOS EU PROG.***



***Chip on wafer (LETI)***

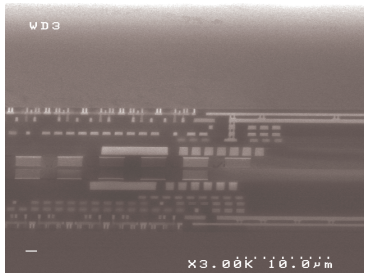
### Above IC Devices



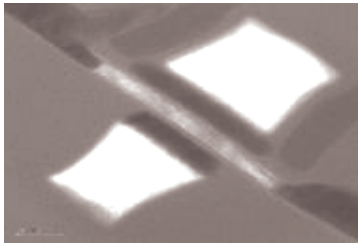
***Optical waveguides on CMOS***

***BAW filters on CMOS LETI+ STM***

### Wafer on Wafer

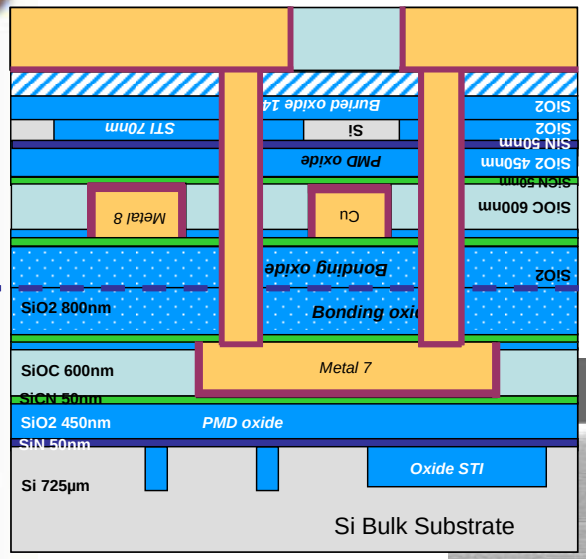


***Capacitive interconnect (LETI Hi3 EU prog.)***



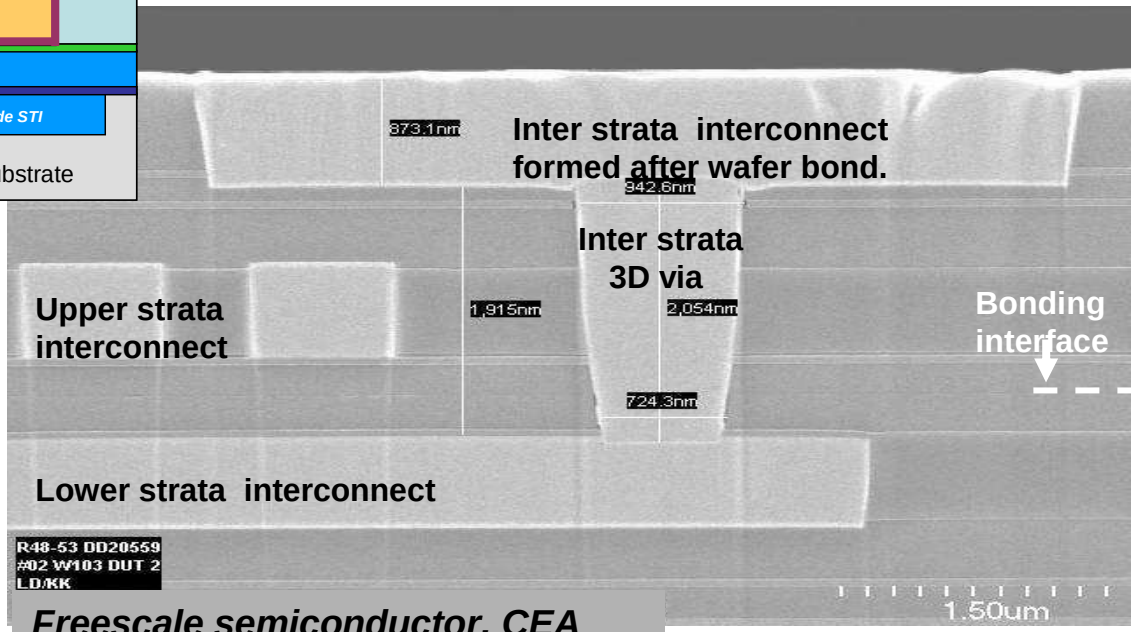
***Double gate MOS (BDGMOS) FEOL architecture***

# 3D Application : IC integration


**Wafer Level Assembly, Cu Interconnect:**

- Water to wafer, face-to-face, molecular $SiO_2$ bonding
- SOI Substrate removal
- Cu supervia post-process, 5µ pitch



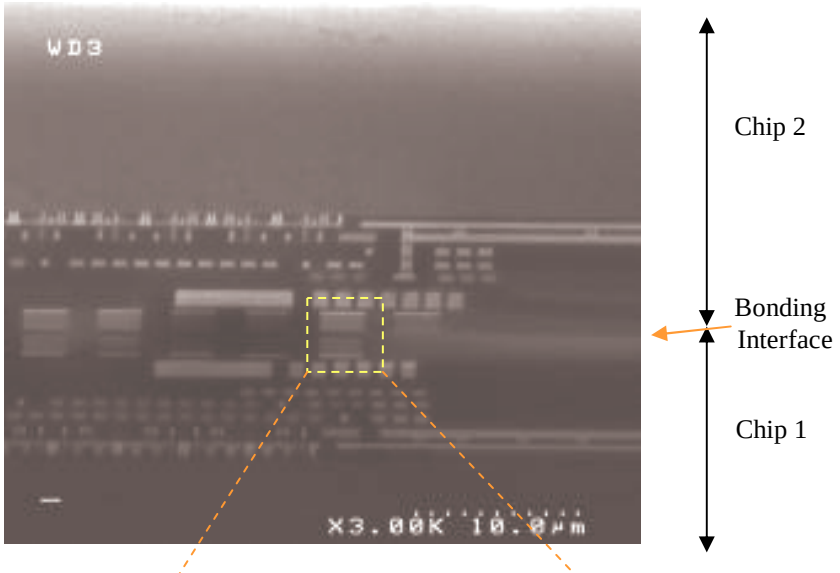

***Freescale semiconductor, CEA Leti - Minatec***

# 3D Application : $SiO_2$ bonding & Capacitance coupling

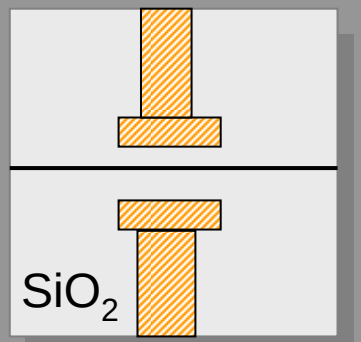
**B. Charlet et al., MAM 2006**

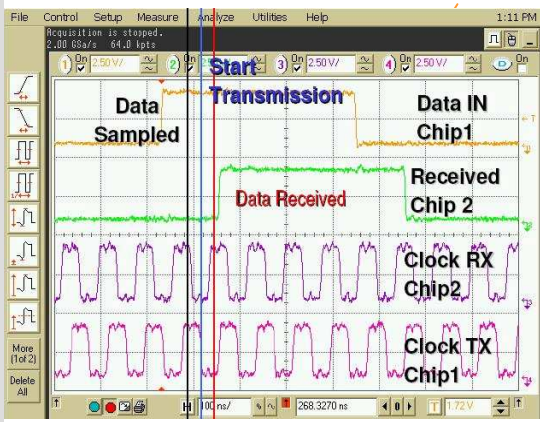
## Wafer Level Assembly, Capacitive Interconnect

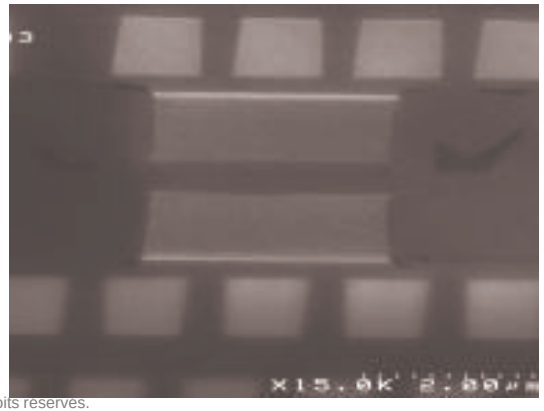
- CMOS compatible design and technology
- Capacitor integration by Direct SiO2 bonding with alignment
- I/O vias achievement
  - Adjusted top wafer thinning
  - Thru-Si-Vias etching




**Capacitance interconnect (SiO2 bonding)**

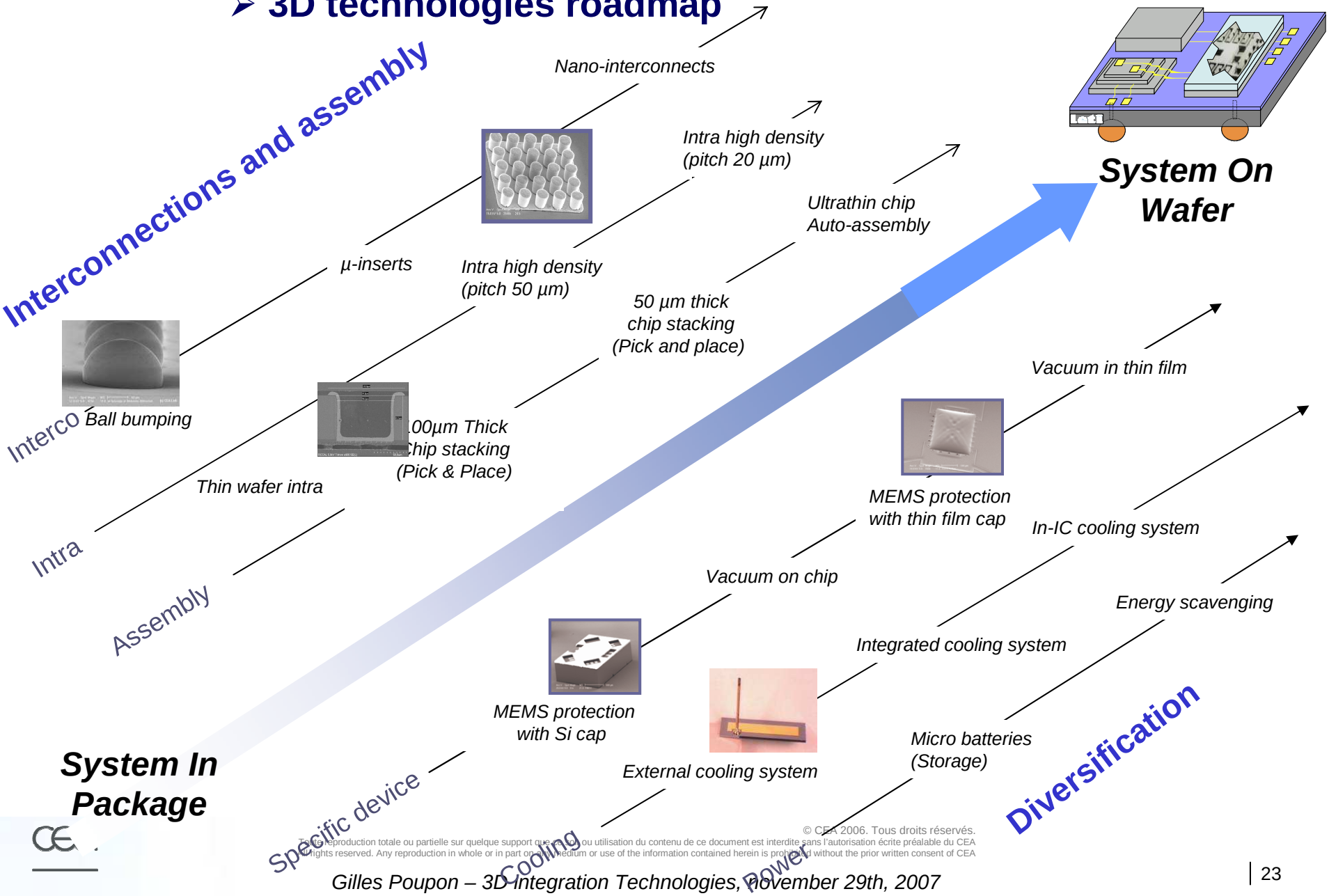


# 3D integration challenges & interests

## ➢ 3D technologies roadmap



# Multipurpose MEMS 200mm platform
## a unique environment in Europe for the development of microsystems technologies

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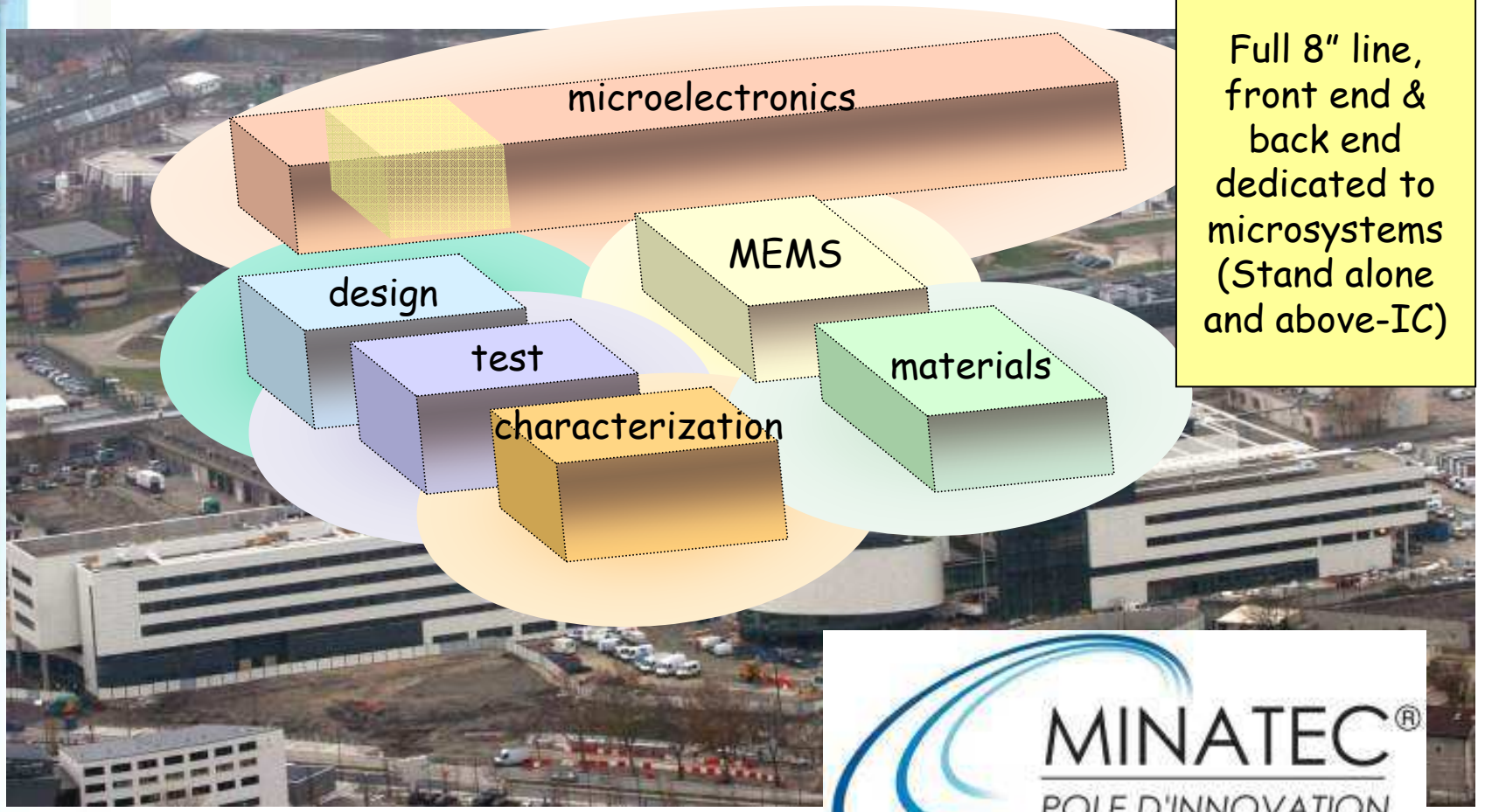


Full 8" line, front end & back end dedicated to microsystems (Stand alone and above-IC)

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# Summary

- 'More Moore' high-density interconnect challenges and 'More than Moore' functionality challenges are leading to 3D technology development
- Main common enabling technologies are TSV, bonding, handling,
- Many approaches of these technologies are possible ➔ LETI proposes a tool box for customer requirements adaptation
- Technologies available or in development at LETI:
  - Low temperature Direct SiO2 bonding with alignment
  - Substrate thinning (SOI and Si bulk)
  - Through Silicon Via realization (etching / isolation / filling / CMP)
- In parallel, design and thermal simulation studies are carried out

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Loyalty
Entrepreneurship
Team work
Innovation

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