Status and plans in 3D Technologies; summary - EMC-3D

Paul Siblerud

EMC^{3D} Program Manager

V.P. Electrochemical Deposition

Semitool, Inc.

www.emc3d.org

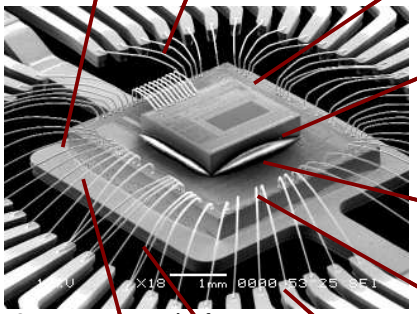
Semiconductor 3-D Equipment and Materials Consortium

SEMITOOL®

Contents

- EMC^{3D} Introduction (Brief)
- Packaging and Interconnects Common Challenges/ Interests
  - Challenges of Interconnects
  - Direction of Packaging
  - ‘Fusion’ Era
- Enabling Technologies
- 3D CoO – The ultimate driver
- Summary

TSV (Through-Silicon-Via) electrodes can provide vertical connections that are both the shortest and the most plentiful.



Source : Fraunhofer-IZM

High Power consumption

Long Connection

Low Density

Poor Heat Dissipation

RC Delays

High Impedance

Large Area

Challenging Interposers

I/O Pitch limitations

Low Power consumption

Short Connection

High Density

Good Heat Dissipation

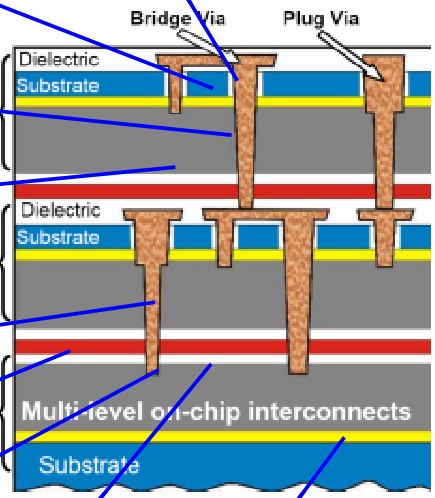
Reduced RC Delays

Low Impedance

Smallest Area

Simple Interposers

Less I/O Pitch limitations

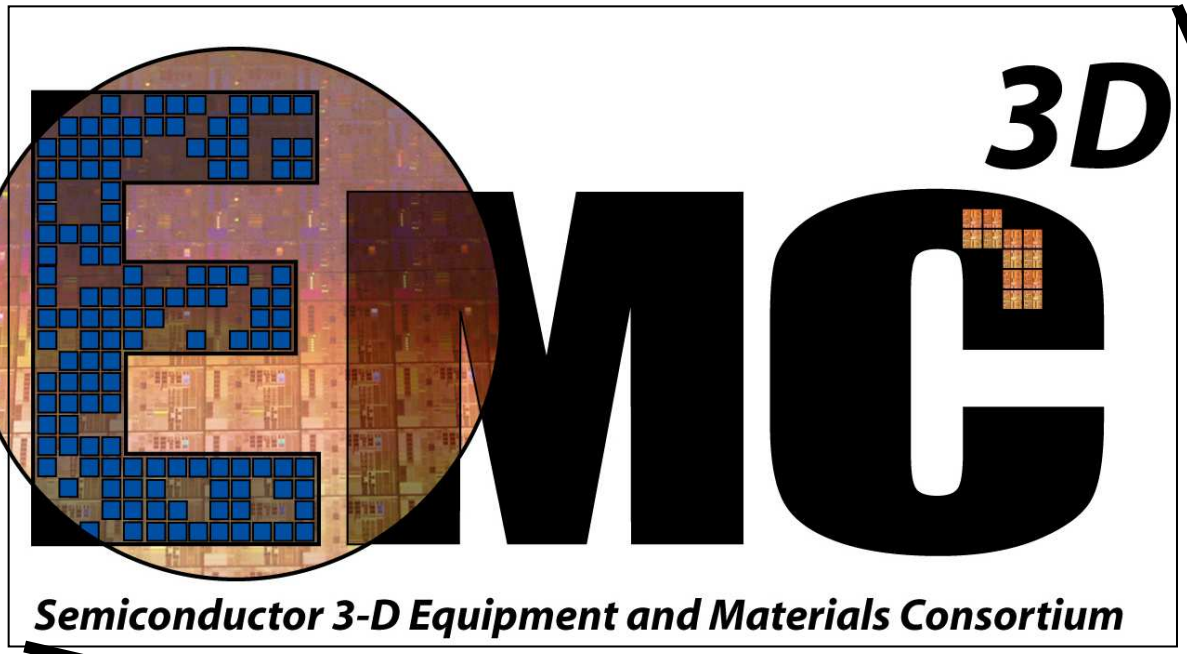


James Lu, RPI, Peaks in Packaging, 2003

TSV interconnects provide solutions to many limitations of current SiP and Chip Stacking methods.

Comparison of SoC, SiP and 3D IC

YOLE DÉVELOPPEMENT



			3D IC
Manufacturing cost in low/medium quantities	B	M	W
Manufacturing ready (2007)	M	B	W

B: Best
M: Medium
W: Worst

- *For high manufacturing quantities of high performance, heterogeneous products, 3D ICs have a significant potential advantage*
- *SiP and 3D ICs have complementary characteristics. SiP has poor performance but manufacturing is today ready*
- *The debate is rather SoC vs. SiP*

Ecole Polytechnique Paris - 3D Technical Symposium; November 2007

SEMITOOL

Announcement ; Oct. 11th, 2006

EMC-3D consortium created for the development of cost-effective 3D Thru-Silicon-Via interconnect

Equipment providers, materials companies and researchers join in an international consortium to address complex integration of TSV 3D chip interconnect.

SALZBURG, Austria, October 11th, 2006. EMC-3D is a new consortium created to address the technical and cost issues of creating 3D interconnects using TSV technology for chip stacking and MEMS/sensors packaging. Several major equipment manufactures have joined with material companies to work with key research groups to address the issues of cost-effective manufacturing and integration. Equipment companies initiating the consortium are Alcatel, EV Group, Semitool and XSiL.

Associate research members include Fraunhofer IZM, SAIT (Samsung Advanced Institute of Technology), KAIST (Korea Advanced Institute of Science and Technology) and TAMU (Texas A&M University). Material members include Rohm and Haas, Honeywell, Enthone, and AZ with wafer service support from Isonics.

The consortium will develop processes for creating micro vias between 5 and 30um on thinned 50um 300mm wafers using both via-first and via-last techniques. Major processes being integrated into the EMC-3D program are via etch and laser drill, insulator/barrier/seed deposition, micro via patterning with RDL capabilities, high aspect ratio Cu plating, carrier bonding, sequential wafer thinning, backside insulator/barrier/seed deposition, backside lithography, backside contact metal plating, chip-to-wafer placement and attach, and dicing. In addition, wafer-to-wafer attach, dicing and de-bonding will also be demonstrated. Cost of ownership goal for the integrated 3D process is $200usd per wafer.

EMC3D (or EMC^{3D})

Mission

Develop/demonstrate a cost-effective TSV interconnect technology (unit processes + integration) and provide manufacturable processes, equipment, and materials.

Equipment

ALCATEL

Micro Machining Systems

XSiL Enable

SEMITOOL

Technology That Works

EVG®

Materials

ROHM and HAAS ELECTRONIC MATERIALS

PACKAGING AND FINISHING TECHNOLOGIES

enthone

AZ Electronic Materials®

brewer science

Isonics corporation

wafer service

Technology

IZM

Fraunhofer Institut Zuverlässigkeit und Mikrointegration

cea leti

SAMSUNG

SAMSUNG ADVANCED INSTITUTE OF TECHNOLOGY

KAIST

TEXAS A&M UNIVERSITY 1876

SEMITOOL®

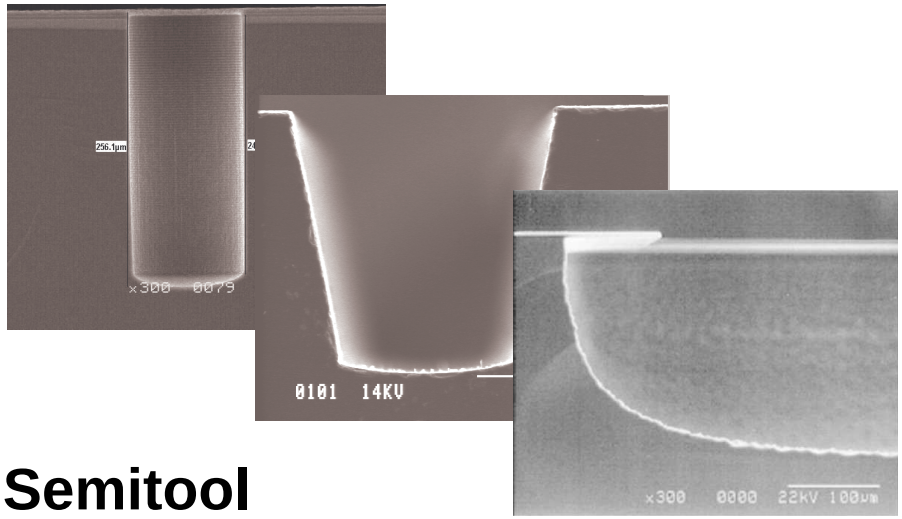
Board Members

GMC 3D

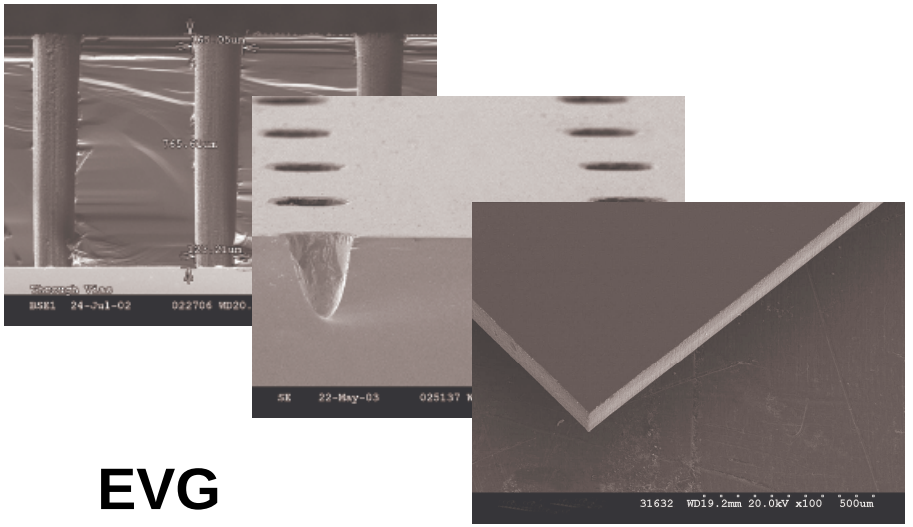
Semiconductor 3-D Equipment and Materials Consortium

Ecole Polytechnique Paris - 3D Technical Symposium; November 2007

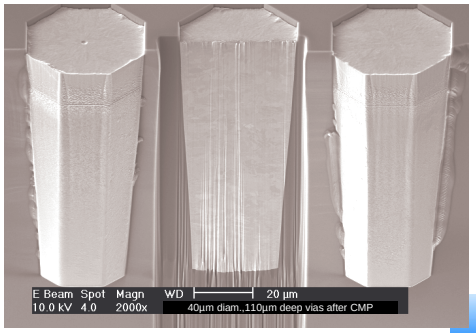
Alcatel

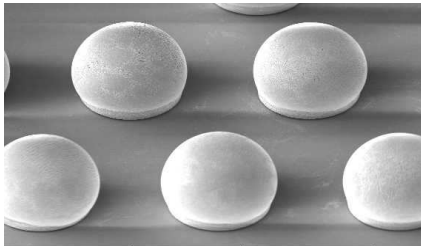


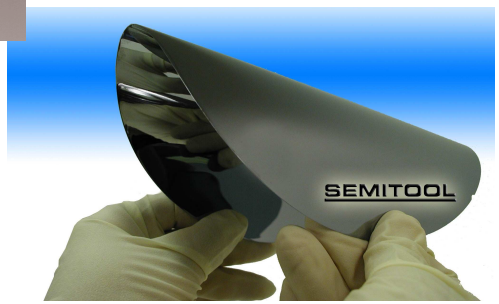
XSiL

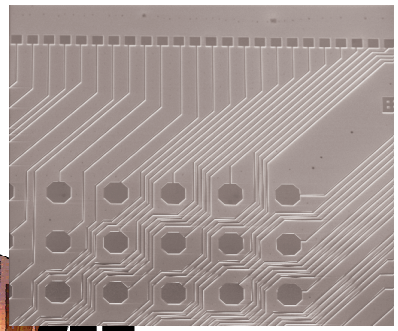


Semitool

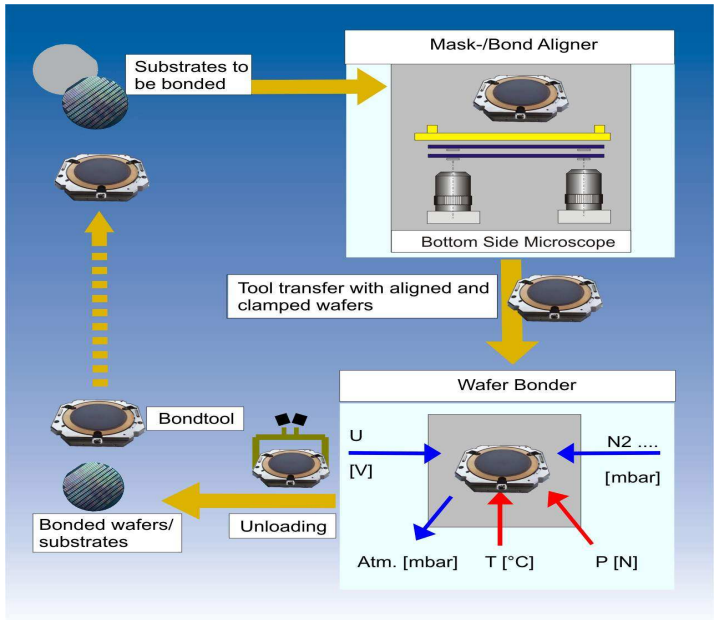




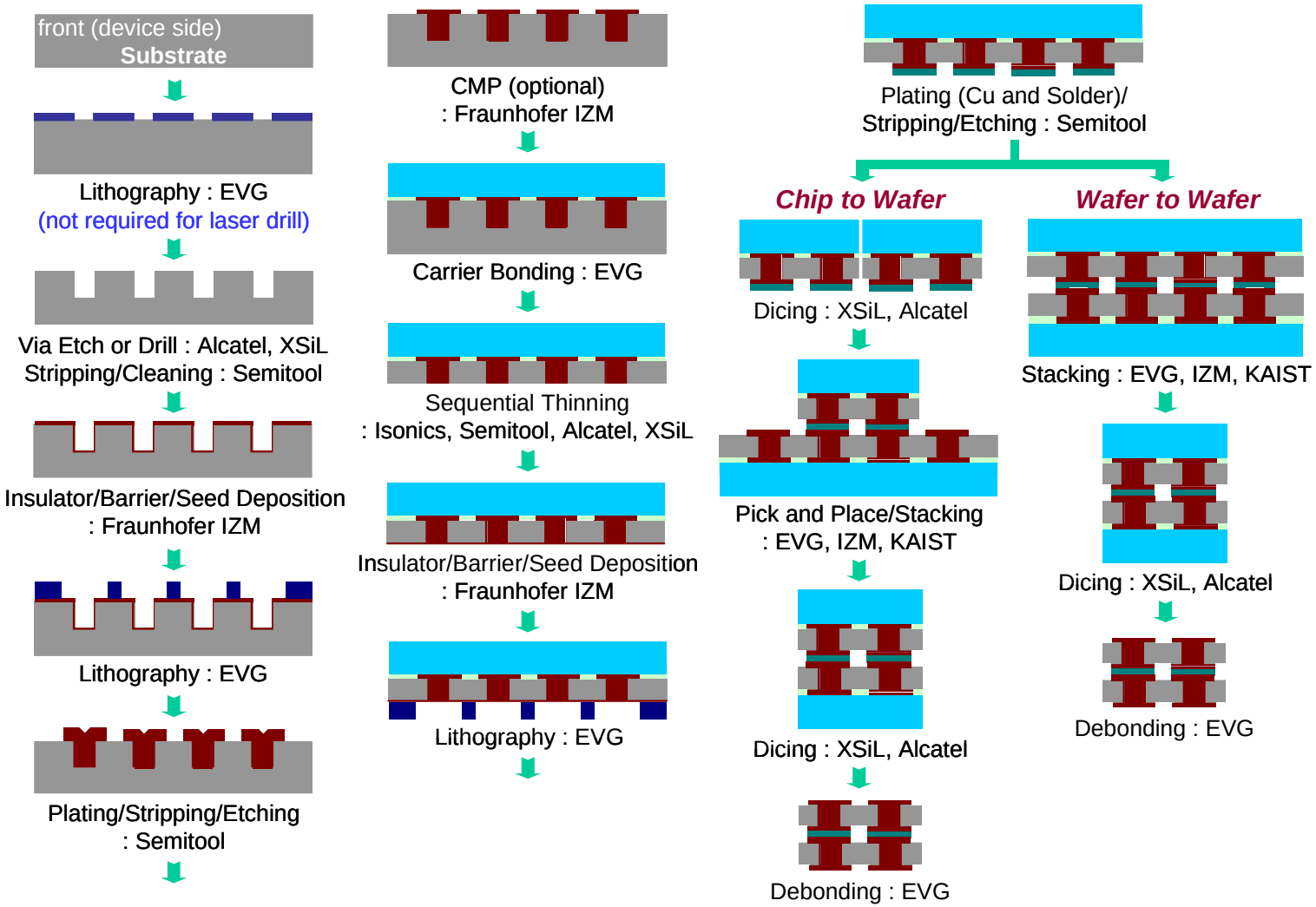




EVG



EMC-3D Process and Equipment Flow



We are considering both via-first and via-last approaches (start with via-first approach). This process flow is not for licensing, but is an example of process and equipment flow for demonstrating chip integration with consortium members' technologies.

First Year

Develop unit processes and demonstrate integration (or stackability) of via-first TSV technology on 200mm wafers with CoO ≈ 400-500usd per wafer.

Second Year

Demonstrate integration and reliability of TSV technology (via-first or via-last depending upon technology trends) on 200mm wafers with CoO ≤ 300usd per wafer.

Third Year

Demonstrate seamless integration and reliability of TSV technology (via-first or via-last depending upon technology trends) on 300mm wafers with CoO ≤ 200usd per wafer.

Contents

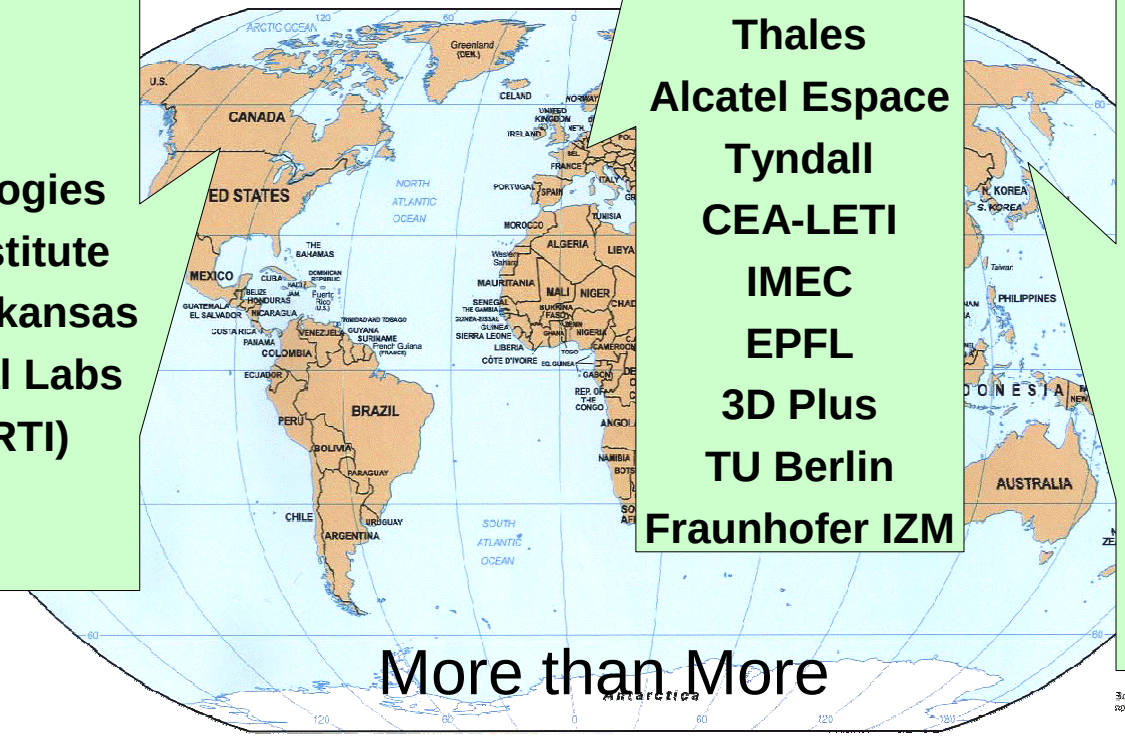
- EMC^{3D} Introduction (Brief)
- Packaging and Interconnects Common Challenges/ **Interests**
  - Challenges of Interconnects
  - Direction of Packaging
  - ‘Fusion’ Era
- Enabling Technologies
- 3D CoO – The ultimate driver
- Summary

Global Activities in 3D Integration

Irvine Sensors
IBM
Intel
Texas Instruments
Vertical Circuits
Amkor
Tessera
Tezzaron
Tru-Si Technologies
Rensselaer Institute
University of Arkansas
Sandia National Labs
MCNC-RDI (RTI)
MIT
Ziptronix

Infineon Technologies
Philips
NXP
Thales
Alcatel Espace
Tyndall
CEA-LETI
IMEC
EPFL
3D Plus
TU Berlin
Fraunhofer IZM

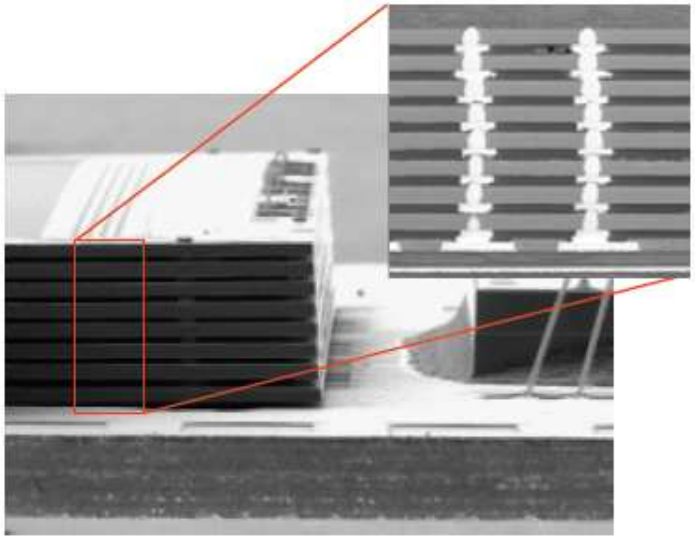
ASET
NEC
Tohoku University
University of Tokyo
ZyCube
CREST
Fujitsu
Sanyo
Sony
Toshiba
Denso
Mitsubishi
Sharp
Hitachi
Matsushita
Samsung



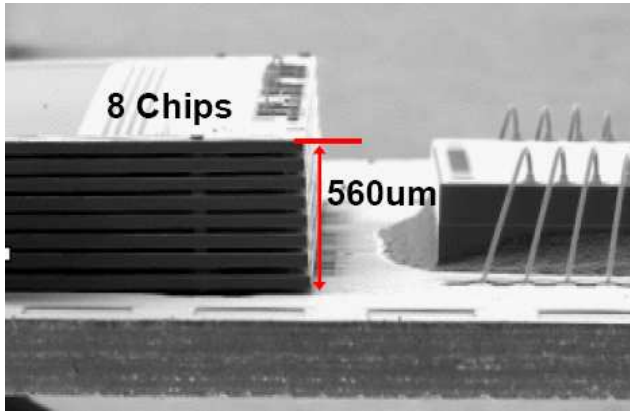
More than More

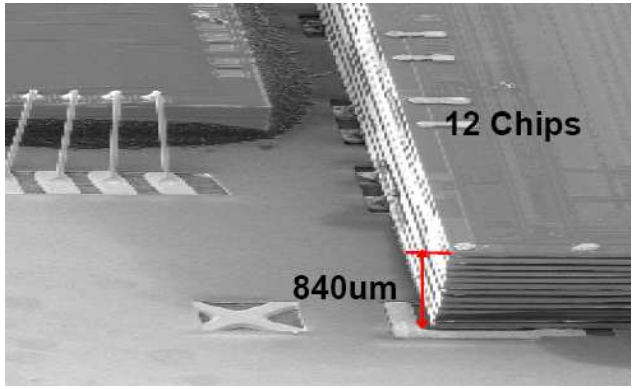
Is TSV 3D-IC Manufacturable?

Samsung's WSP



Source : Samsung Electronics

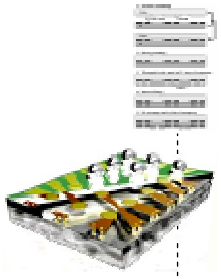




Announced on April 2006

WSP (wafer-level processed stack package) with TSV interconnects

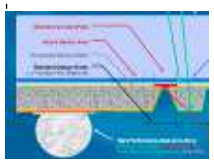
Company roadmaps
for through-holes on CIS mobile imagers



Fujikura (development of through-holes for CCDs, 8'' wafers)

Sanyo (through hole in R&D)

STM (image sensors WLP planned for 2007)



Schott (technology IP, fab sold in Singapore)

Xintec (Wet etch to be followed by WLCSP with DRIE)

Micron (use WLP for imagers)

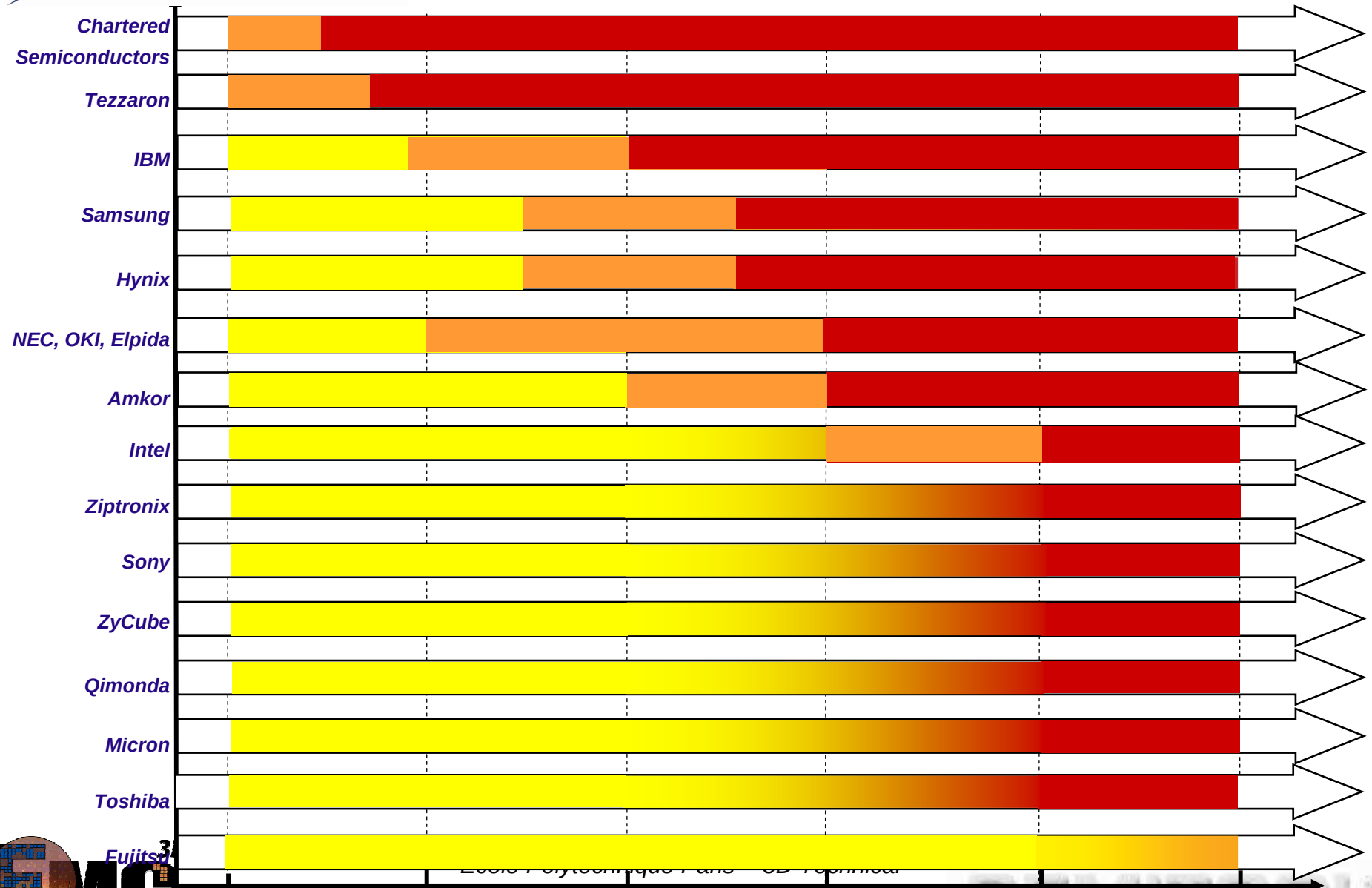
TSMC (Shellcase license)

< 2004 *2005* *2006* *2007* *2008* *2009* *2010*

→ Matsushita, Sharp & Sony have also been reported as having through-holes developments for imagers.

→ Schott fab in Singapore has been sold to StatsChippac that will make it a research center for the development of the TSV technology

Roadmaps of some 3D-IC players



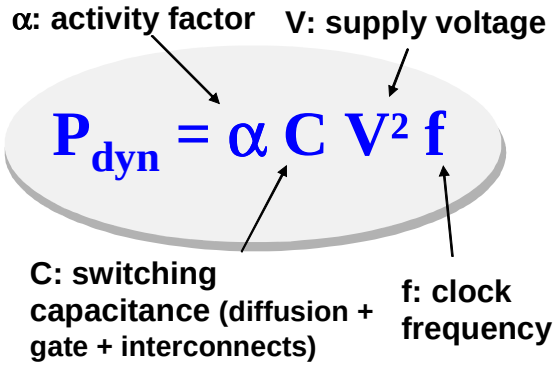
Contents

- EMC^{3D} Introduction (Brief)
- Packaging and Interconnects Common Challenges/ Interests
  - Challenges of Interconnects
  - Direction of Packaging
  - ‘Fusion’ Era
- Enabling Technologies
- 3D CoO – The ultimate driver
- Summary

Challenges of advanced interconnects

• **Today, More than 50% of dynamic power consumption is due to interconnects. This rate is projected to increase.**

[Nir Magen et al, Proc. of the 2004 international workshop on System level interconnect prediction, France, pp 7-13, 2004]



• **Global Interconnect length doesn't scale with transistors and local wires. Because of functionality increase, chip size remains relatively constant.**

[Havemann et al., IEEE, Vol. 89 (5), May 2001]

• **RC delay is increasing exponentially. For 65nm node, RC delay in 1mm global wire at minimum pitch is ~100 times higher than NMOSFET intrinsic delay [ITRS07].**

[ITRS 2007]

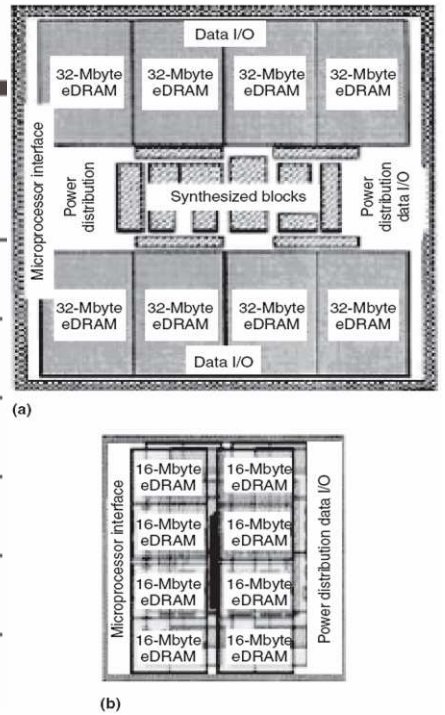
source:

Logic (Processor with cache memory)

- **Processor with cache memory** : Example of 16-Mbyte SRAM cache design (*Rensselaer Polytechnic Institute*)

Table 5. Performance comparison of 2D and 3D implementations for 130-nm, 16-Mbyte L2 cache ($\lambda = 0.1$).

Characteristic	2D design	3D design: Two-wafer stack	3D design: Four-wafer stack
Access time (ns)	5.09	2.73 (-46%)	2.04 (-60%)
Cycle time (ns)	1.27	0.68	0.5
Operating frequency (GHz)	0.79	1.47	2.0
Dynamic energy (nJ)	4.49	2.38 (-47%)	1.37 (-69%)
No. of repeaters on critical I/O channels	1,216	768	224
No. of banks	16	64	128



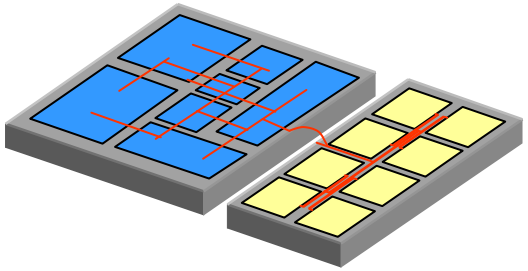
A. Zeng, J. Lü, K. Rose, and R. Gutmann (Rensselaer Polytechnic Institute), IEEE Design & Test of Computers, 2005, pp. 548-555

IC floorplan of graphics rendering processor with 256-Mbit eDRAM: 2D (a) and 3D (b).

source:

Why 3-D?

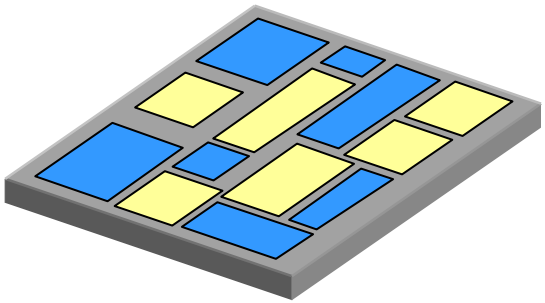
"More than MOORE"



2D interconnect:

- Large form factor
- Long lines / shared bus

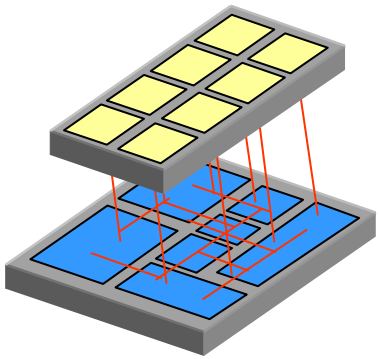
3.8mm X 2.9mm



SOC solution:

- Reduced system size
- Increased performance
- Increased device cost

15%	**Size Reduction**
30%	**Power/signal Improvement**
5%	**Cost Increase**

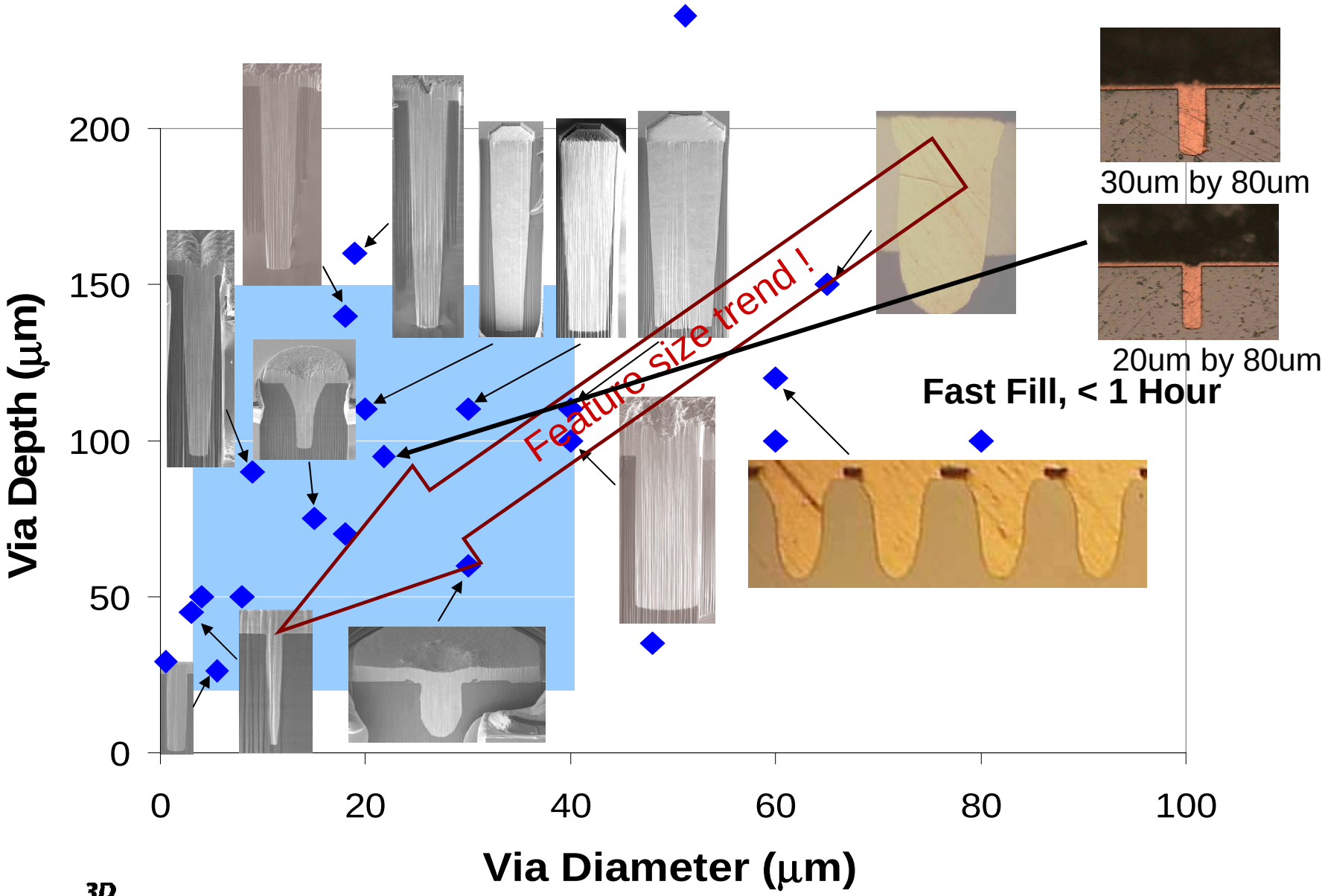


3D stack:

- Reduced system size
- Short interconnects
- Reduced packaging cost

35%	**Size Reduction**
40%	**Power/signal Improvement**
45%	**Cost Reduction**

Void-free Filling at Optimized Conditions

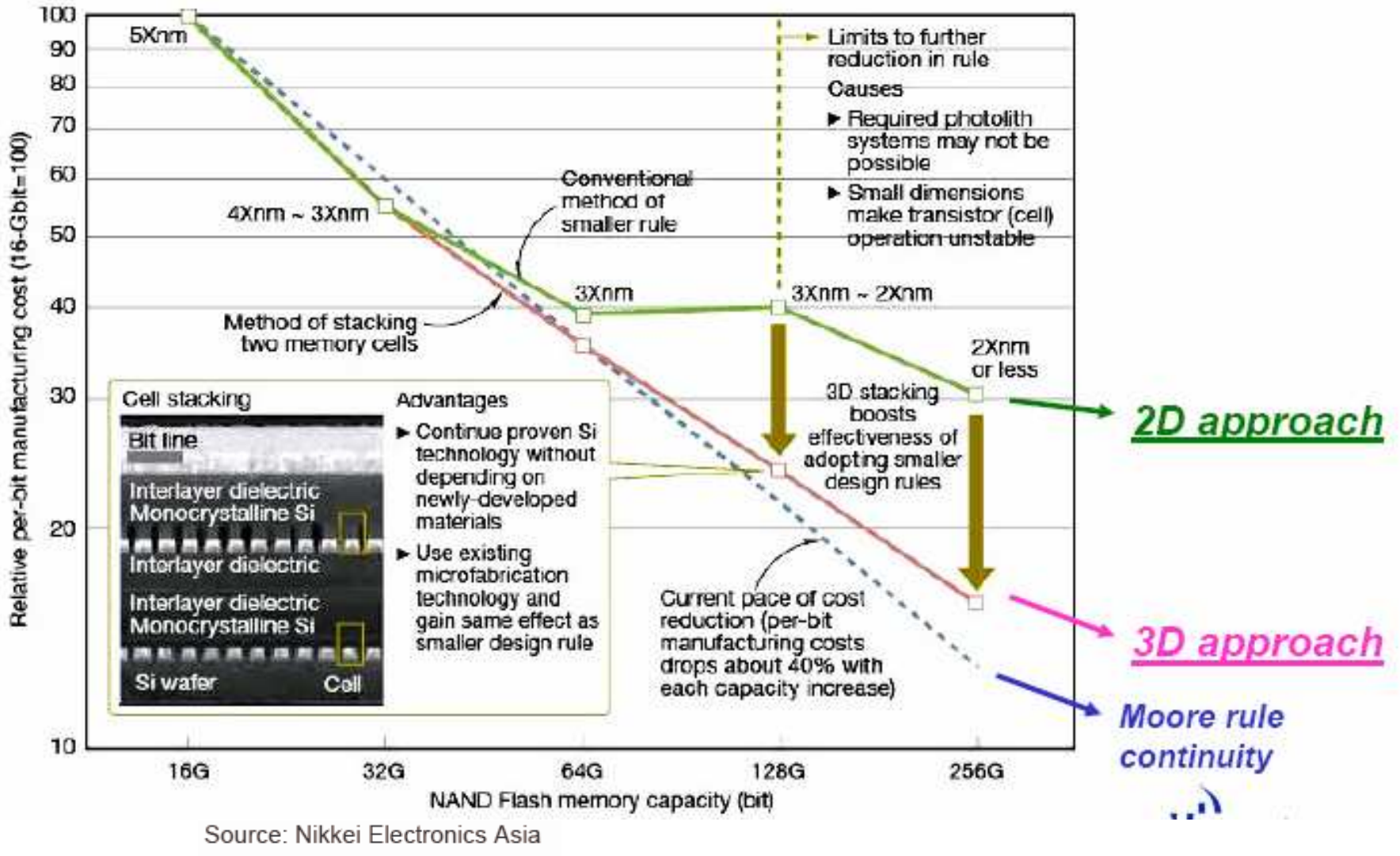


“Fusion Era”

- “We are at the doorstep of the largest shift in the semiconductor industry ever, one that will dwarf the PC and even the consumer electronics eras”
- “The core element needed to usher in the new age will be a complex integration of different types of devices such as memory, logic, sensor, processor and software, together with new materials, and advanced die stack technologies, … all based on 3D silicon technology”

Dr. Chang-Gyu Hwang, president-CEO, Samsung Semiconductor, IEDM conference, Dec. 2006

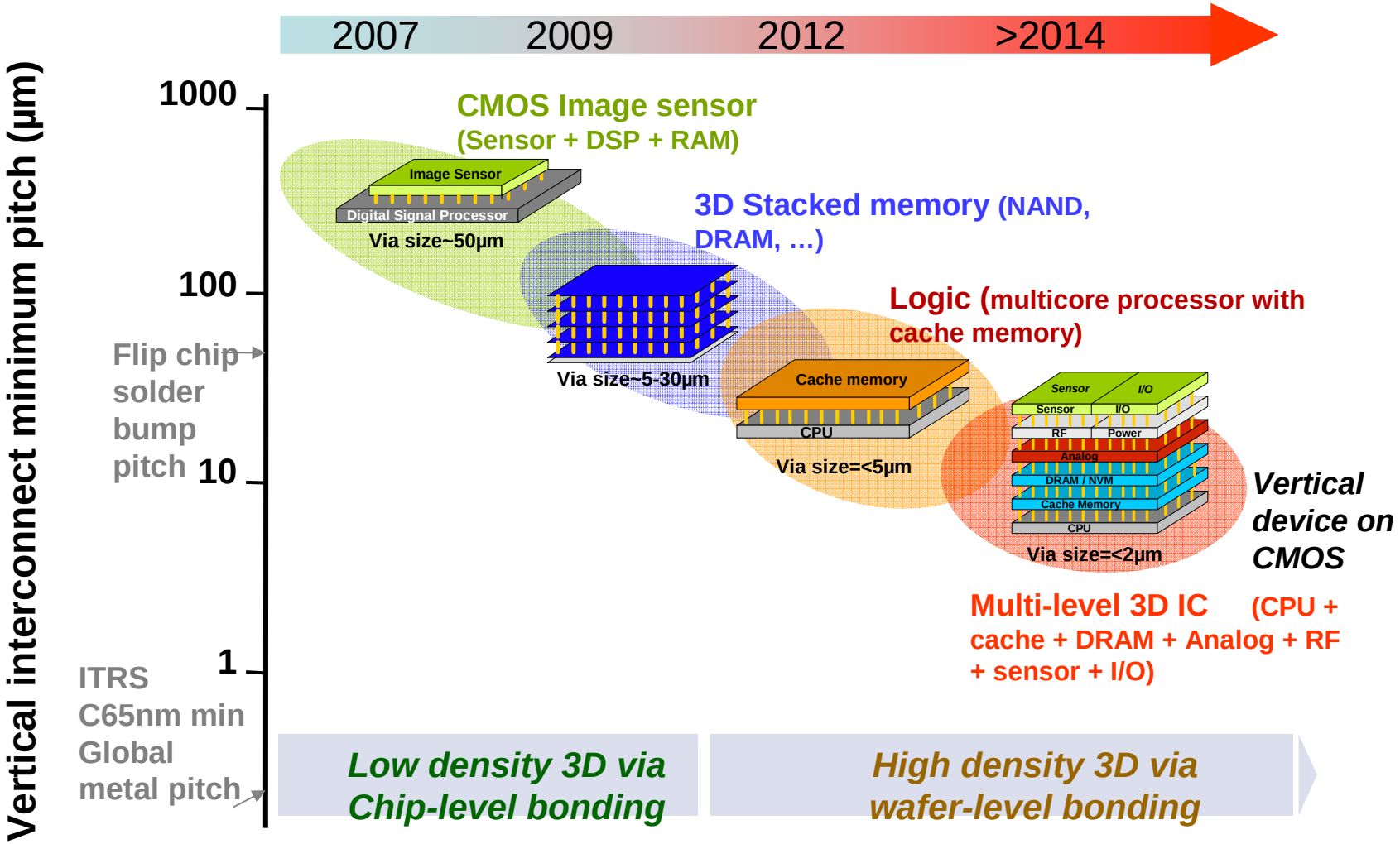
source:



Source: Nikkei Electronics Asia

At flash capacity >64 Gb, expect to see a big cost differential between 2D and 3D

Applications of 3D Si integration



source:

Memories (Flash and DRAM)

- Samsung (**NAND**)

K. Lee (Samsung), Conference on 3D Architectures for Semiconductor Integration and Packaging, 31oct-2nov 2006, SF, CA

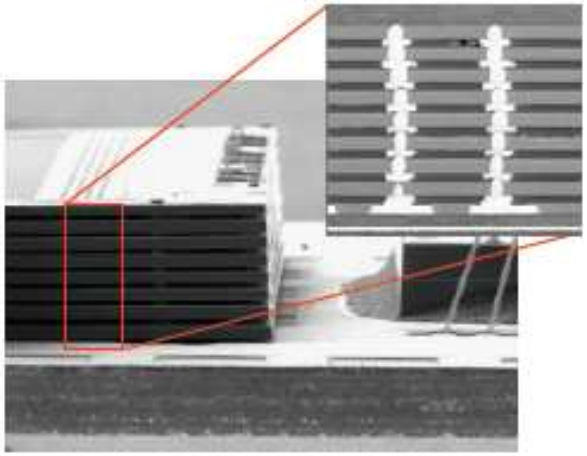


Photo : Samsung

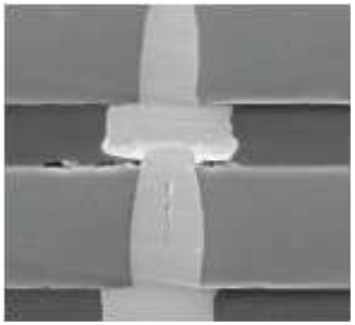
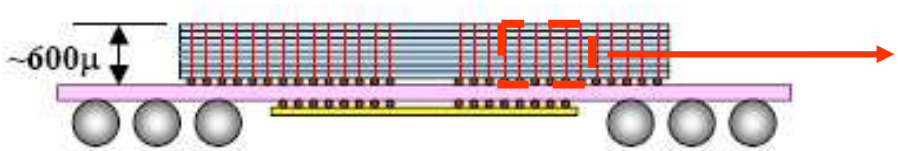


Photo : Samsung

- ***Through Silicon Via Formation (~ 30µm diameter) : Laser Drill, Electroplating Via Filling***
- ***Die-to-die bonding : micro-bump bonding***
- ***Wafer Thinning : ~ 50µm***

- Elpida Memory (**DRAM**)



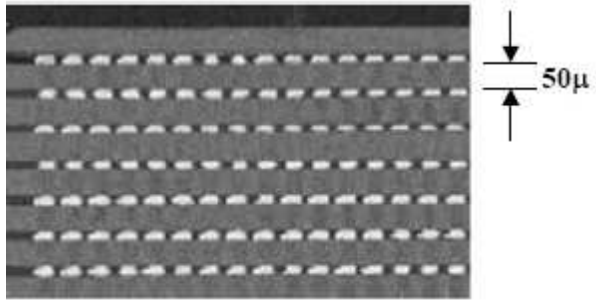
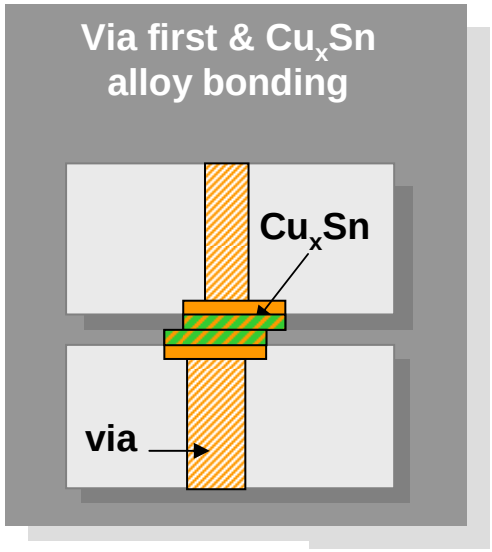


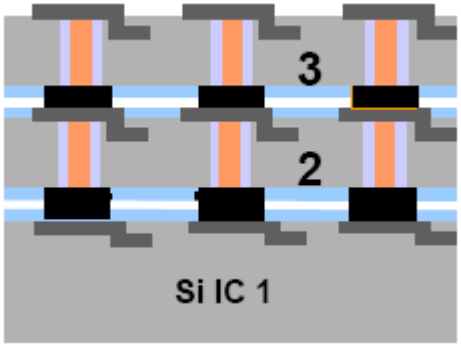
Photo: Elpida memory

H. Ikeda (Elpida Memory, Inc.); Conference on 3D Architectures for Semiconductor Integration and Packaging, 31oct-2nov 2006, SF, CA

source:

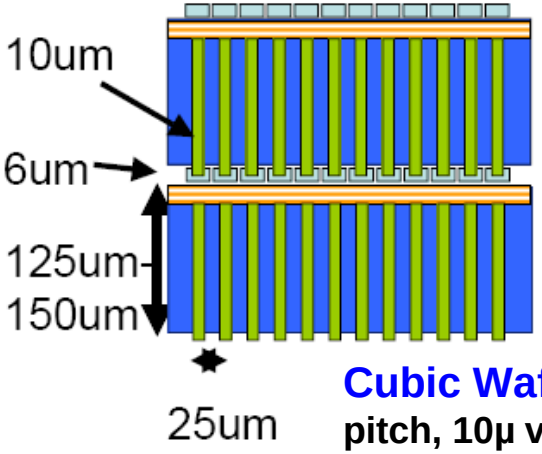
Via first & CuxSn bonding (w/ or w/o glue)

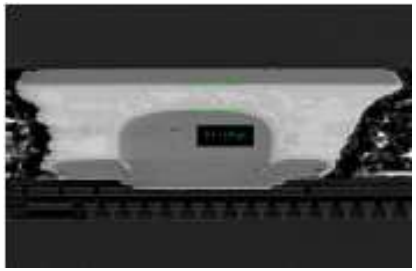




K. Williams et al., 3D Architectures for Semiconductor Integration and Packaging Conf., 31oct-2nov 2006, SF, CA

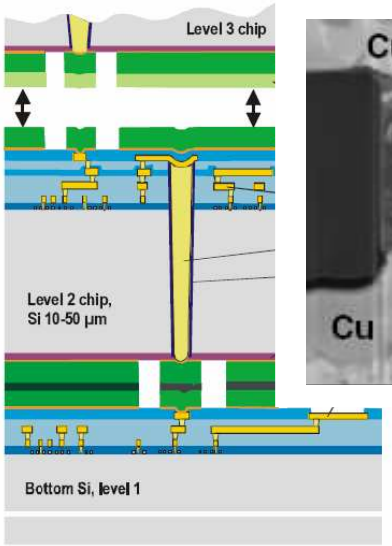
RTI, Pitch ~20µm, die-to-wafer, glue layer for fine pitch

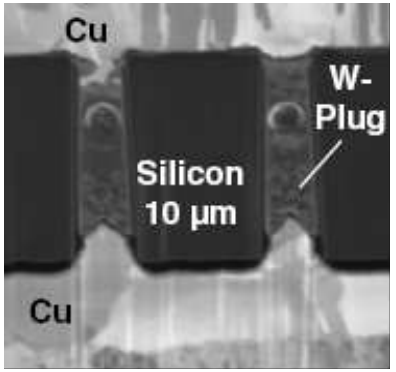




Cubic Wafer, die-to-wafer, 25µm pitch, 10µ via diameter, no glue

J. Trezza et al., 3D Architectures for Semiconductor Integration and Packaging Conf., 31oct-2nov 2006, SF, CA



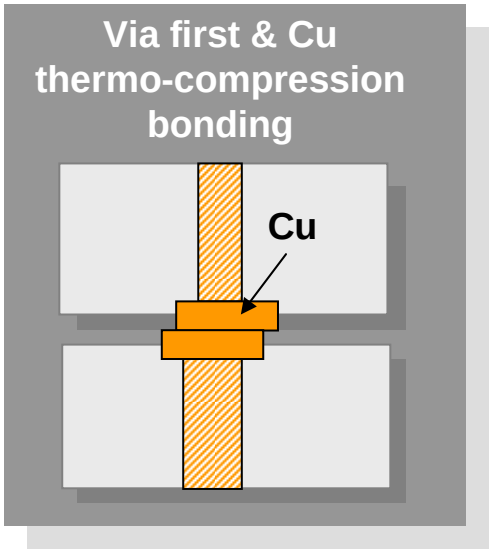


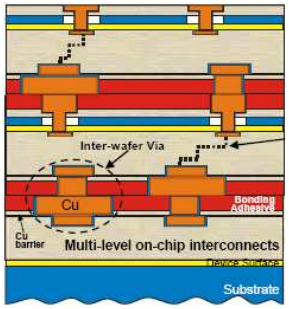
Fraunhoffer IZM, Pitch <15µm

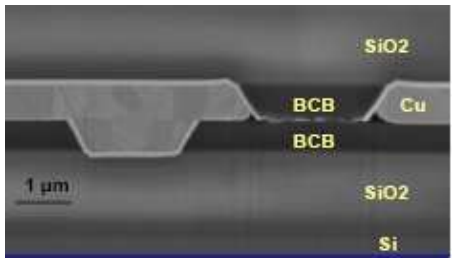
B. Wunderle et al, MRS fall 2006

source:

Via first & Cu thermo-compression (w/ or w/o glue)

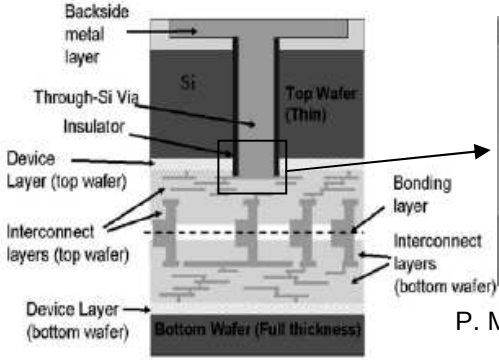






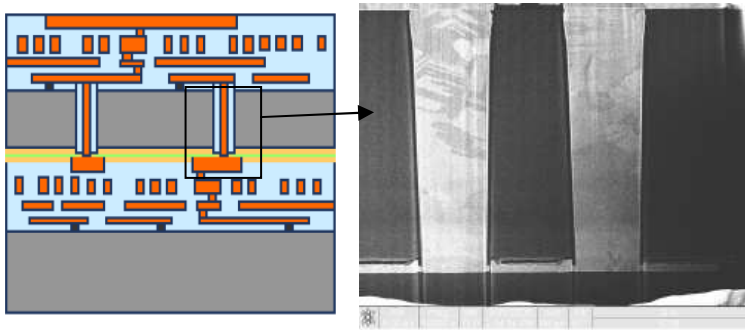
RPI, with glue

J. Lu et al., MRS Spring 2005



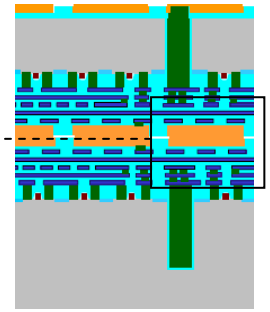
P. Morrow et al., AMC 2004

Intel, Pitch <10µm



IMEC, Pitch ~10µm, with glue

P. De Moor et al., MRS fall 2006

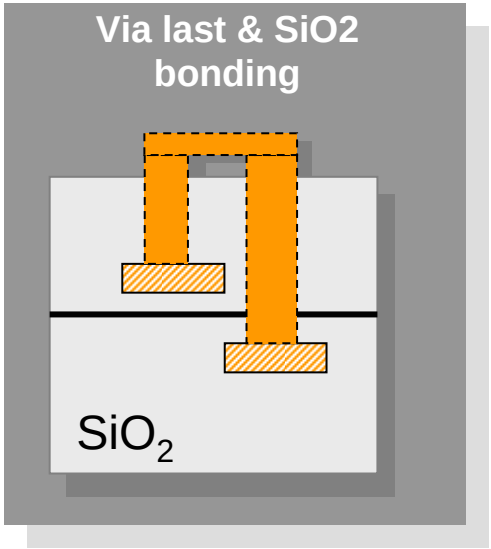


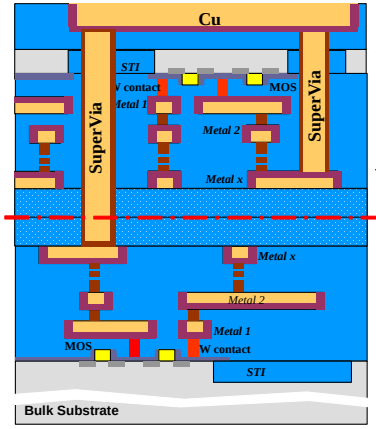
Tezzaron, Pitch ~10µm

R. Patti et al., RTI Conf., 2006,

source:

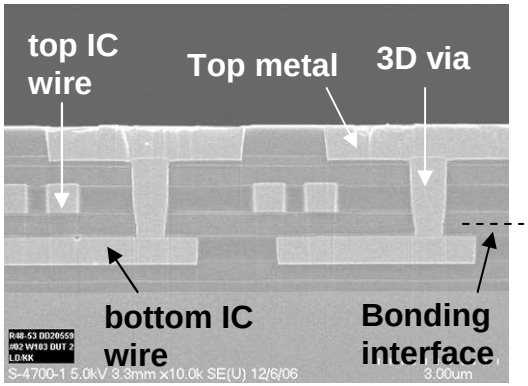
SiO2 bonding & via last



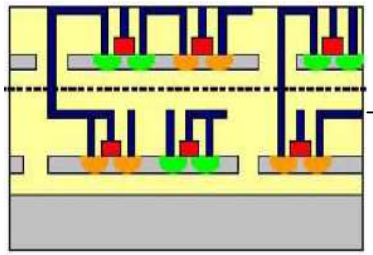


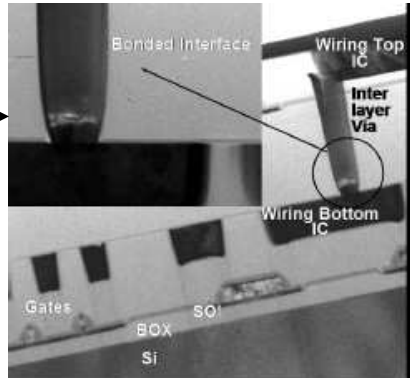
R. Chatterjee et al., IITC 2007 (To be published)

P. Leduc et al. IITC 2007 (To be published)



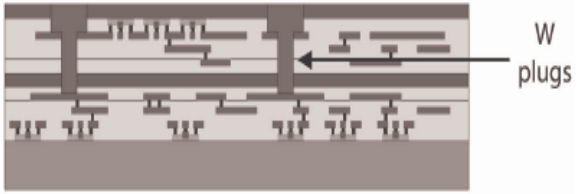
CEA Léti - MINATEC / Alliance, SiO_2 bonding, pitch ~5µm (SOI)

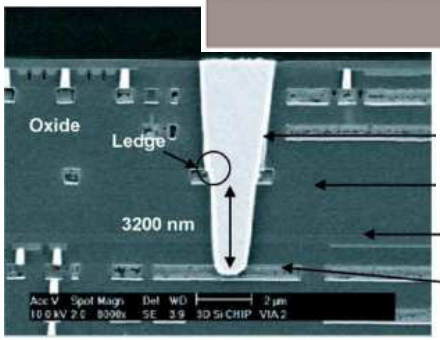




IBM, SiO_2 bonding, pitch <1µm (SOI)

A.W. Topol et al., IEDM 2006





J. Burns et al., IEEE Transactions on Electron Devices, Vol. 53 (10) OCt. 2006

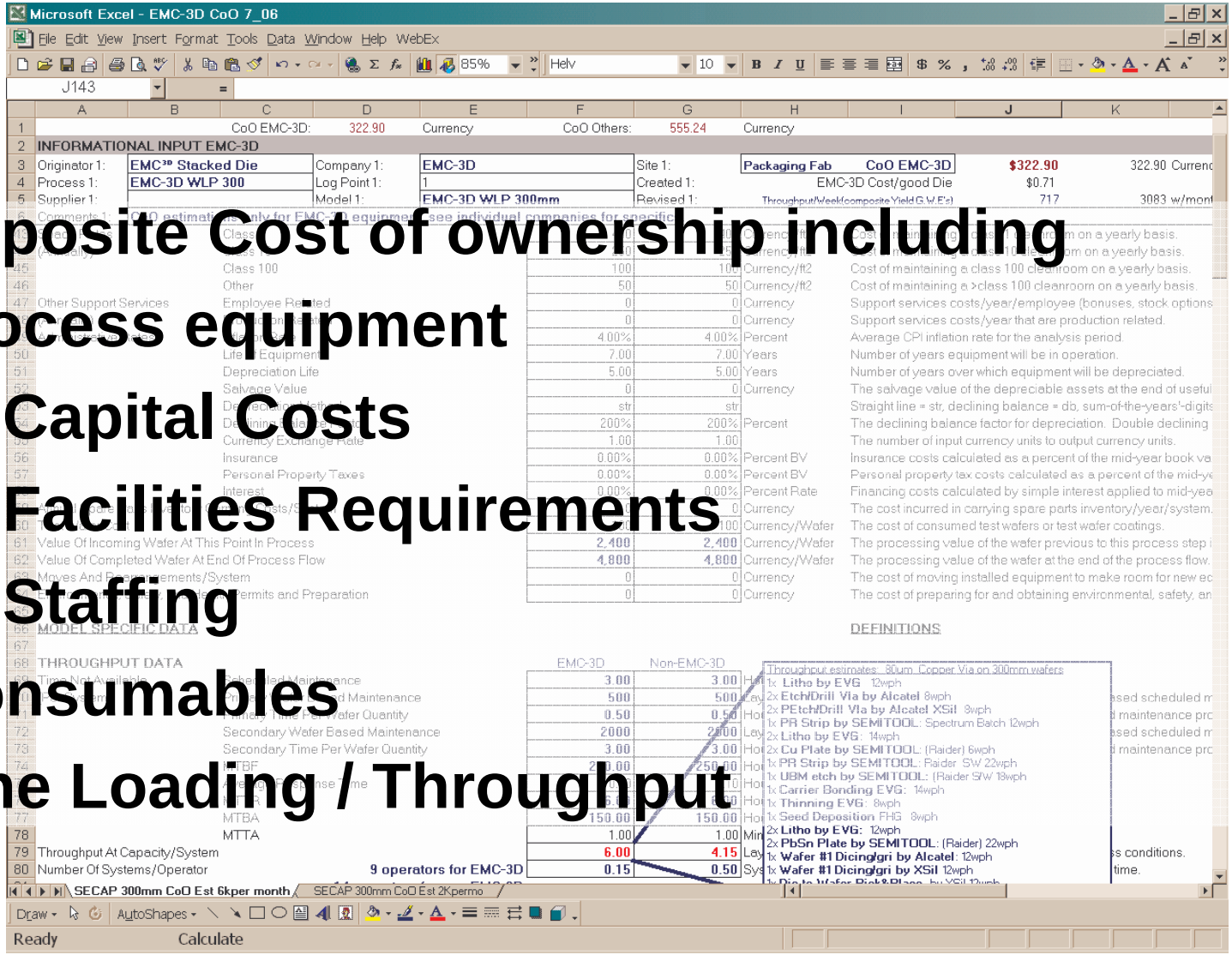
MIT Lincoln (SOI), 8µm pitch

source:

Contents

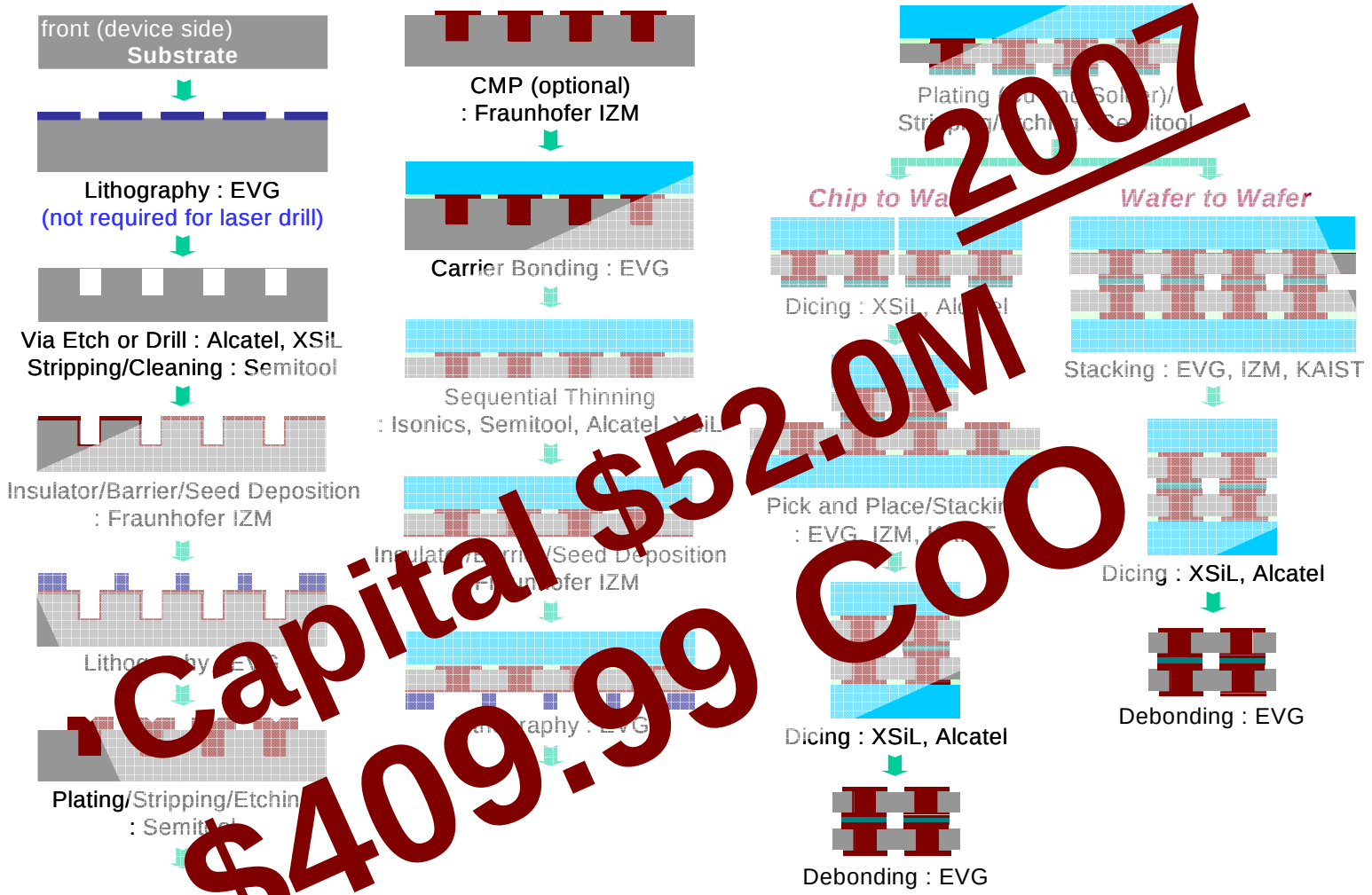
- EMC^{3D} Introduction (Brief)
- Packaging and Interconnects Common Challenges/ Interests
  - Challenges of Interconnects
  - Direction of Packaging
  - ‘Fusion’ Era
- Enabling Technologies
- 3D CoO – The ultimate driver
- Summary

CoO by SEMATECH's Model



- Composite Cost of ownership including
  - process equipment
    - Capital Costs
    - Facilities Requirements
    - Staffing
  - Consumables
  - Line Loading / Throughput

2007 CoO Expectation



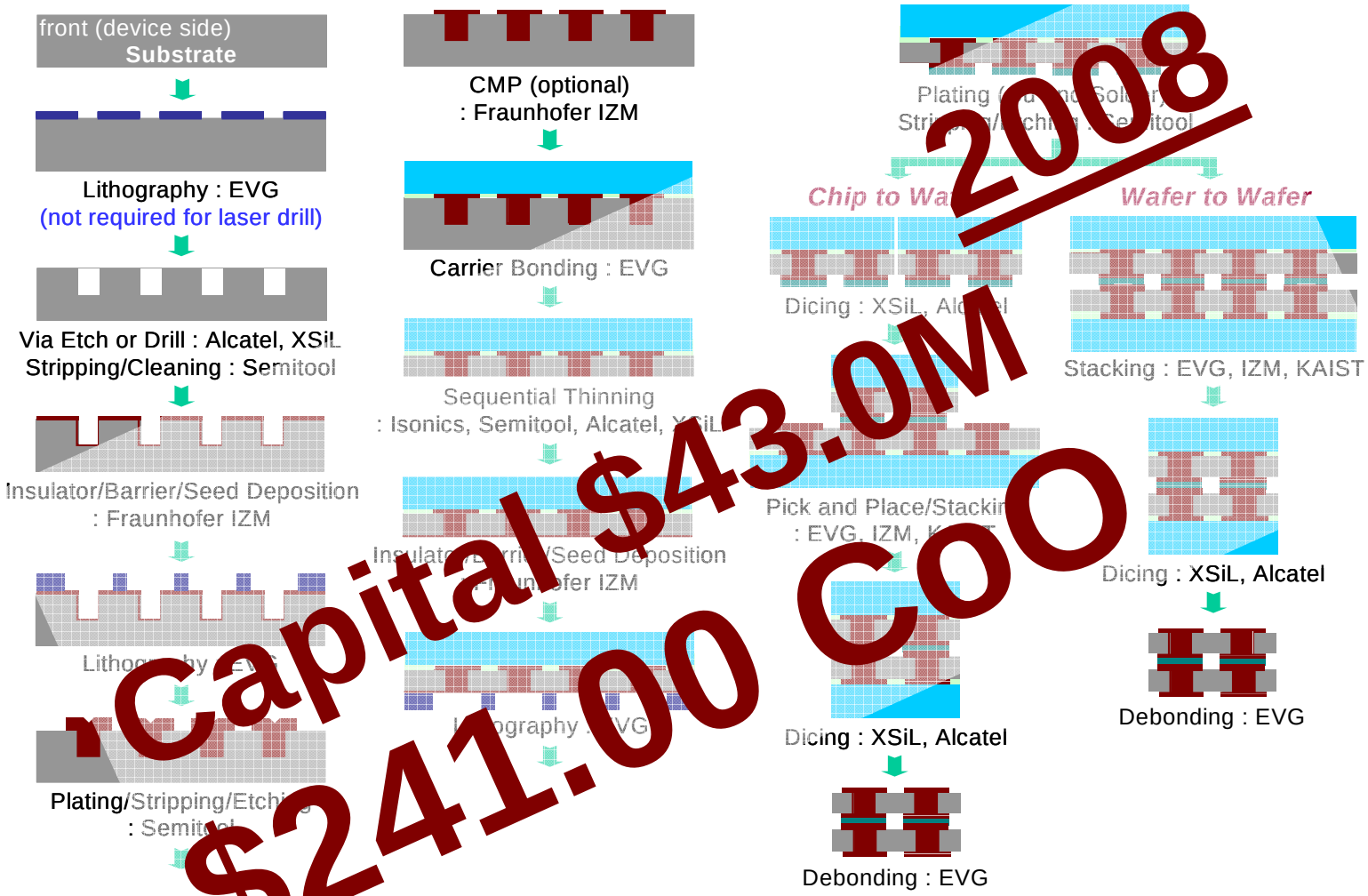
2007

Capital $52.0M

$409.99 CoO

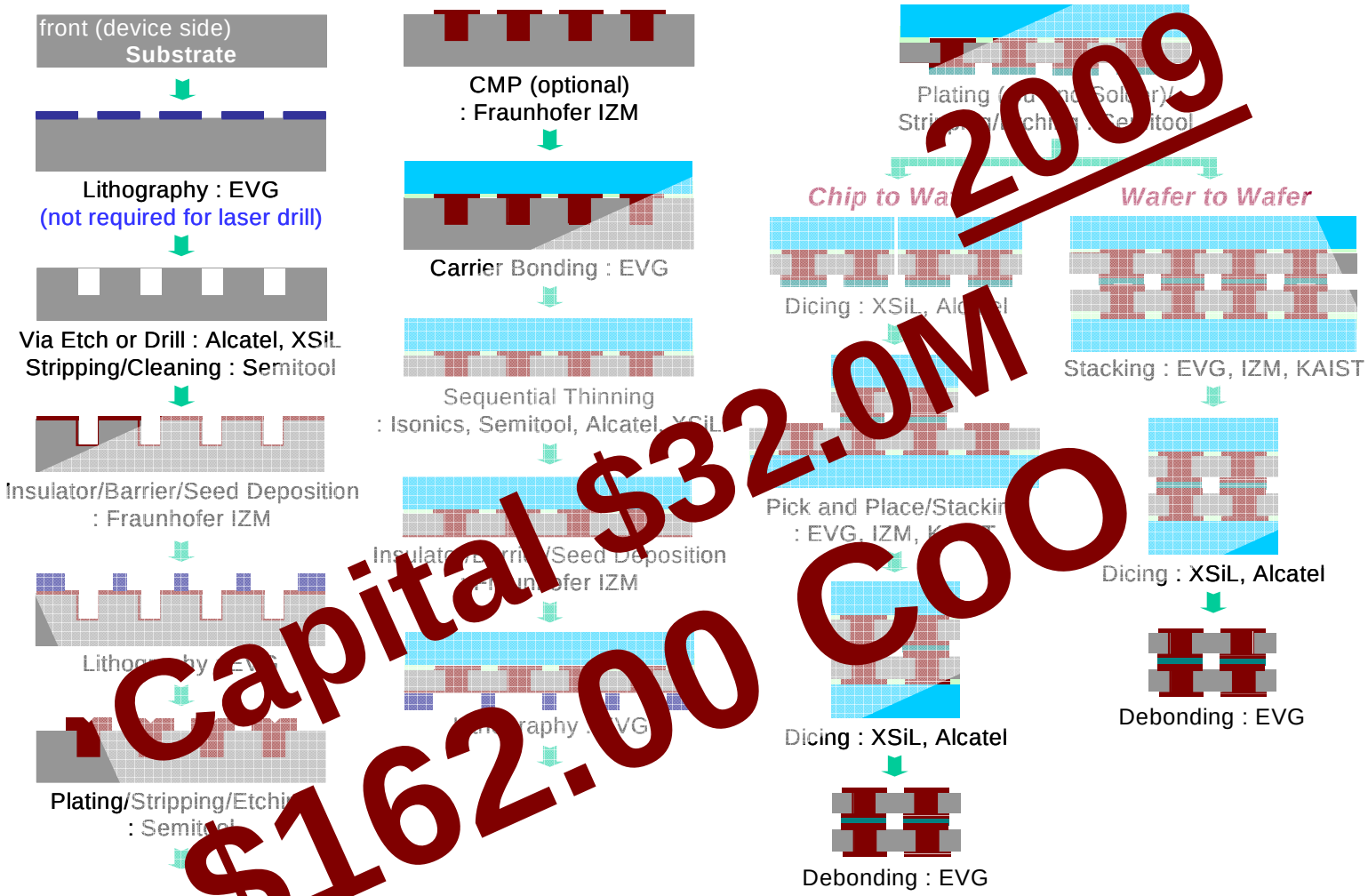
3,500 wafers/month – 200mm

2008 CoO Expectation



3,500 wafers/month – 200mm

2009 CoO Expectation



3,500 wafers/month – 300mm

CLEAR Objective :

Integrated and Cost-Effective Cu TSV for < $200/wafer by Year 2009

www.emc3d.org

Acknowledgements

- Barbara Charlet, Mark Scannell & David Henry — CEA/LETI
- Juergen Wolf, Peter Ramm — Fraunhofer IZM
- Dr. Christo Bojkov & Dr. Manuel Soriaga — Texas A&M
- Michel Puech and Hind Beaujon — Alcatel
- Tom Ritzdorf, Charles Sharbono & Rozalia Beica — SEMITOOL
- Markus Wimplinger and Paul Kettner — EV Group
- Delphine Perrottet, Dr Aleksej M. Rodin — XSIL
- Suk-Jin Ham, Yoon-Chul Sohn — SAMSUNG
- Dr. Kyung W. Paik — KAIST
- Dr. Vaidyanathan Kripesh ; — IME, Singapore
- Dr. Fred Roozeboom and Eric van Grunsven — NXP
- Stephen Christian, Bob Forman — Rohm & Haas
- Yun Zhang, Bioh Kim — Enthone
- Georg Pawlowski, C. Chen — AZ Electronic
- Paul Harris — Brewer Science
- Wilfried Bair — Ziptronix
- Jean-Christophe — Yole Développement

3D TSV Consortium

3D EMC

Semiconductor 3-D Equipment and Materials Consortium

Working together to enable low cost thru-silicon-via interconnection.