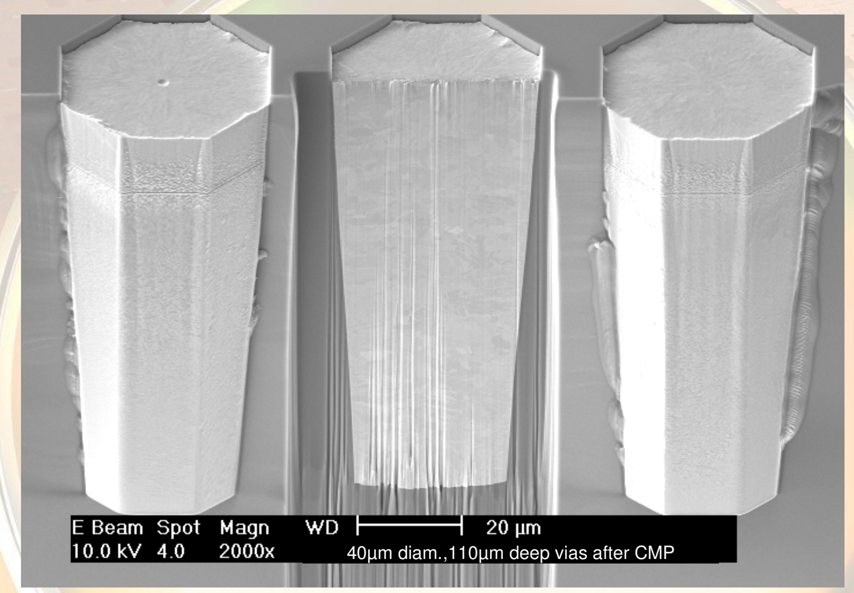
Void-Free Cu Filling within High Aspect Ratio TSVs



Tom Ritzdorf and Charles Sharbono

Semitool, Inc.

EMC-3D Japan/Korea Technical Symposium
April 23-27, 2007

Outlines

SiP and 3D Packaging

Through-Silicon-Via (TSV) Chip Integration

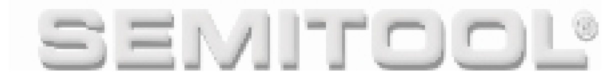
TSV Copper Filling

ECD fill mechanism

Factors affecting filling profiles

Void-free filling at optimized conditions

Conclusions



Demands from Consumer Electronics Market

Size, Weight, Cost, and Power ↓

Features and Functionality ↑

Incorporation of other circuit elements (MEMS, opto-electronics, and bio-electronics)

→

Product complexity ↑

Product life cycle ↓

→

System in a Package

(Multi-chip & 3D packages)

Cost / Function
Time to Market

System on Chip

Bio-Interface

Power Supply

MEMS

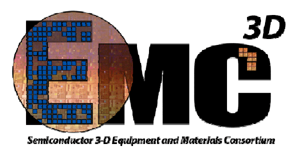
SiP and 3D Packaging

Source : ITRS

System Complexity

Compared to SoC, SiP offers

- greater flexibility
- shorter time to market
- less development cost.



SIP Technologies

Source : ITRS

Chip / Component Configuration	Technology
Side by Side Placement	**Substrate:** organic laminate, ceramic, glass, silicon, leadframe **Chip Interconnection:** wire bond and/or flip chip + passive components — integrated into the substrate / discrete (CSP, SMD)
Stacked Structure	**PoP PiP** **Stacked Die** — wire bond, WB+FC **Chip to Chip / Wafer** — flip chip, face to face / through silicon / WL 3D stack / wafer to wafer (W2W)
Embedded Structure	**Chip in PCB / Polymer** — single layer / multi-layer 3D stack **WL Thin Chip Integration** — single layer / stacked functional layers

Need strategies and solutions for test, yield, and rework.

Benefits of TSV Integration

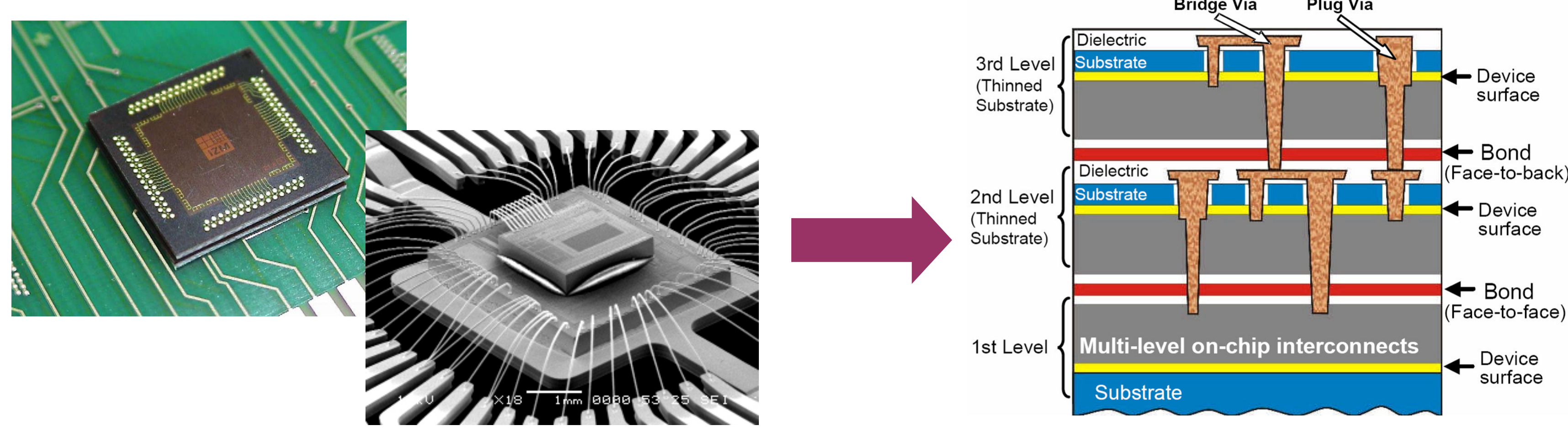
TSV electrodes can provide vertical connections that are both the shortest and the most plentiful.

Connection length ≈ chip thickness

High density, high aspect ratio, and small pitch connections

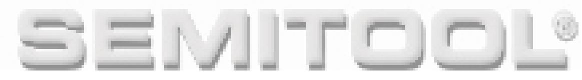
RC delays and power consumption are reduced

Therefore, TSV interconnection can overcome the limitations of typical SiP methods.



Source : Fraunhofer-IZM

James Lu, RPI, Peaks in Packaging, 2003



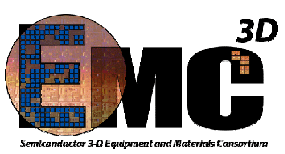
Void-free Filling at Optimized Conditions

Feature size trend !

Via Diameter (µm) axis	0	20	40	60	80	100

Via Depth (µm) axis: 0, 50, 100, 150, 200

Via Diameter (µm)



Requirements for TSV Integration

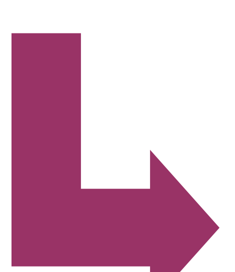
Robust and precise thinning process flow

Handling concepts for a thin wafer

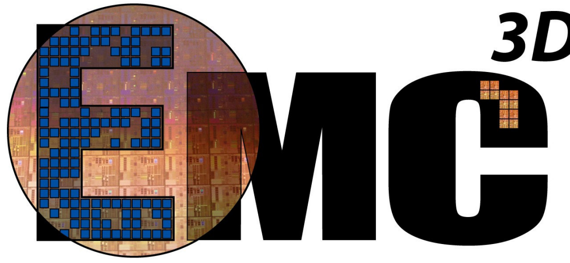
Electrical interconnects through a thinned wafer

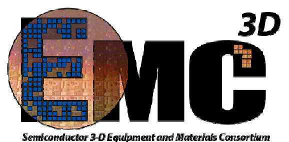
- Via etch : shape, angle, and scallop control
- Insulator/Barrier/Seed : conformality and adhesion control
- Copper fill : fill robustness and speed control
- Metal removal : surface smoothness and over-polish control

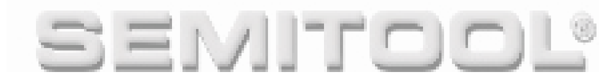
Suitable bonding process : alignment, bonding, and dicing



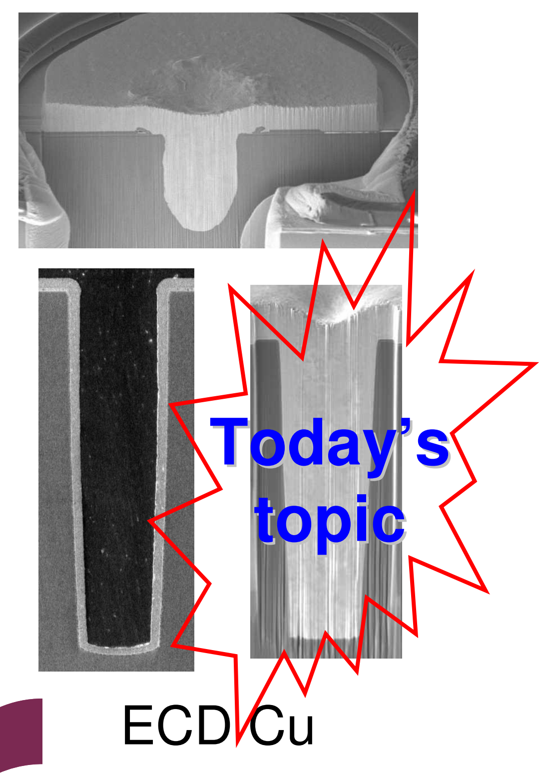
Need cooperation with industrial leaders in equipment, materials, and technology.



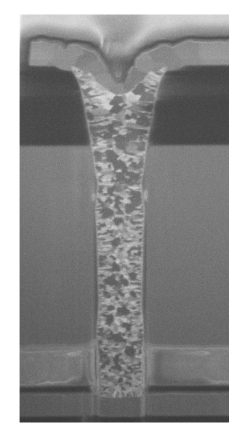




Various TSV Filling Methodologies

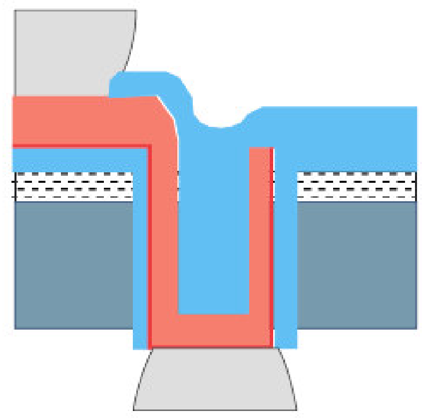


ECD Cu



Source : Fraunhofer-IZM

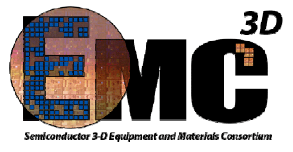
CVD W, Cu,
or Poly-Si



Source : IMEC

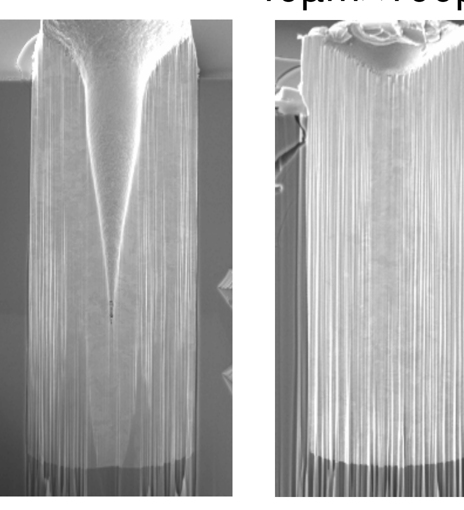
Conductive Polymer
or Conformal Cu/Polymer

High purity
Low resistivity
No size/shape limitation

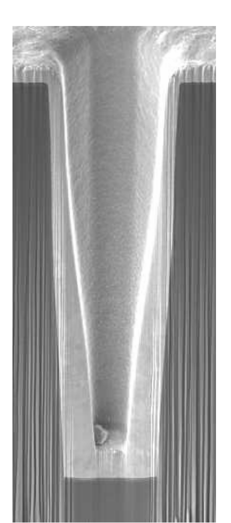


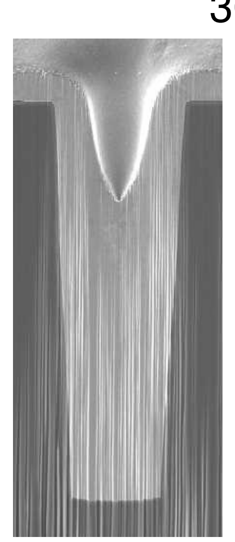
Void-free Filling with Various Dimensions

40μm×100μm

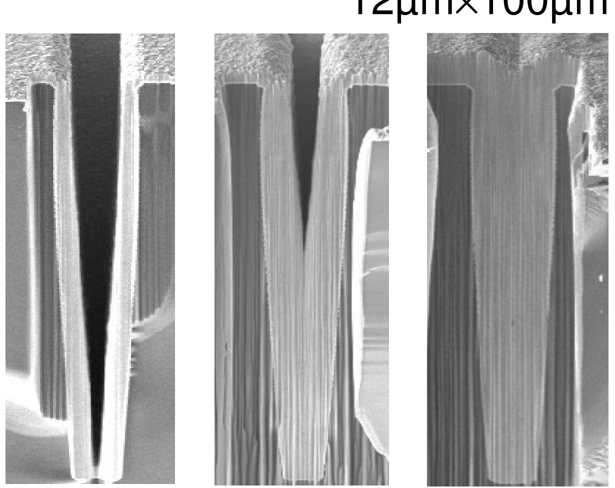


30μm×110μm

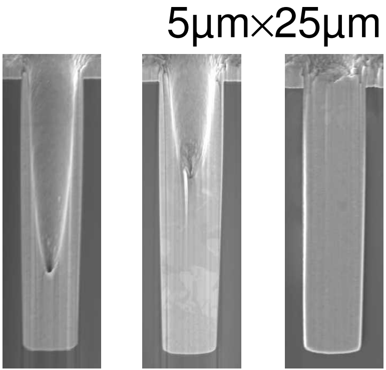


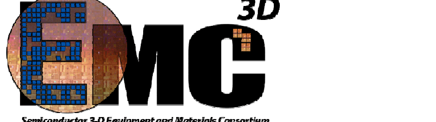


12μm×100μm



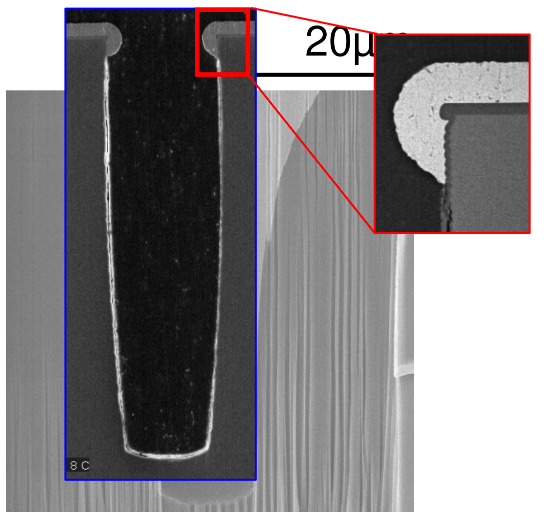
5μm×25μm

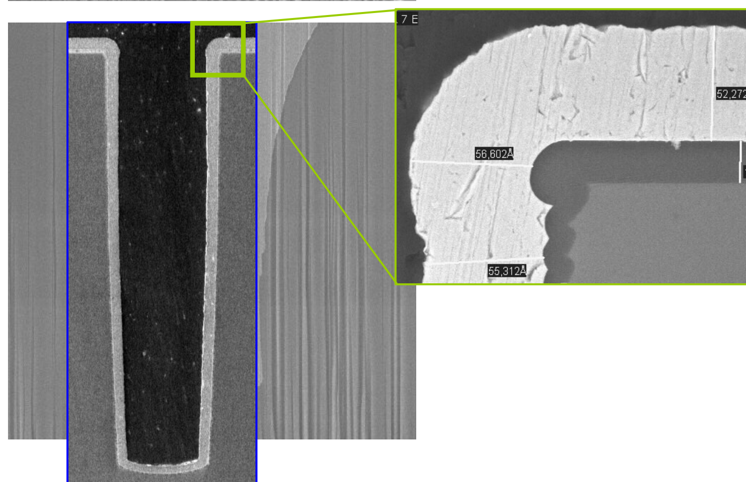




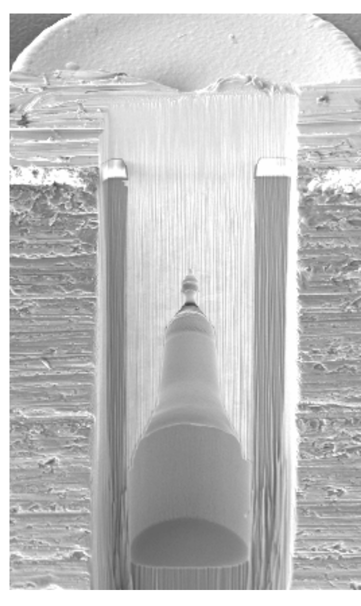
Prerequisites

Seed Continuity

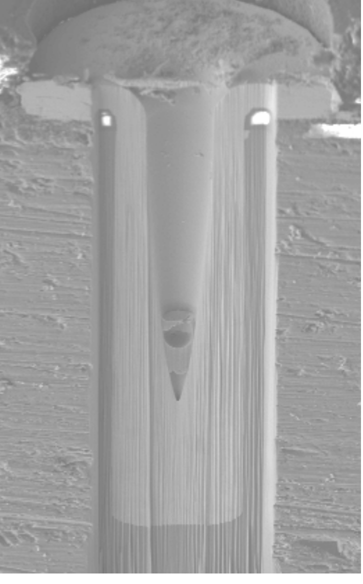




Surface Wetting



50µm×225µm



Via Filling Profiles

12μm×100μm

Charge Transfer

$$Cu^{2+} + 2e^{-} \rightarrow Cu^{0}$$

Mass Transfer

Void formation mechanism : Higher deposition rate near the via mouth due to faster charge and mass transfer, causing pinch-off

Potential Variation through a High AR Via

el_pot – Volt
0.096
0.094
0.092
0.09
0.088

250µm

el_pot – Volt
0.096
0.094
0.092
0.09
0.088

67mS/cm **247mS/cm**

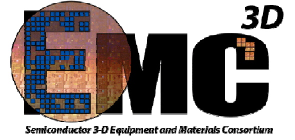
<u>Model Parameters</u>

- Uniform seed layer
- Constant current density

<u>Factors</u>

- Copper seed layer (thickness and coverage)
- Feature dimension
- Bath conductivity

Additive adsorption/desorption behavior is also dependent on local potential.



Mass Transfer in a High AR Via

Model Conditions : Steady state model fluid velocity, 50µm via diameter
Constant fluid velocity across feature top

Convection

Diffusion

200µm

50µm

AR = 4

100µm

AR = 2

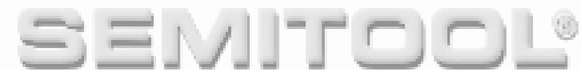
50µm

AR = 1

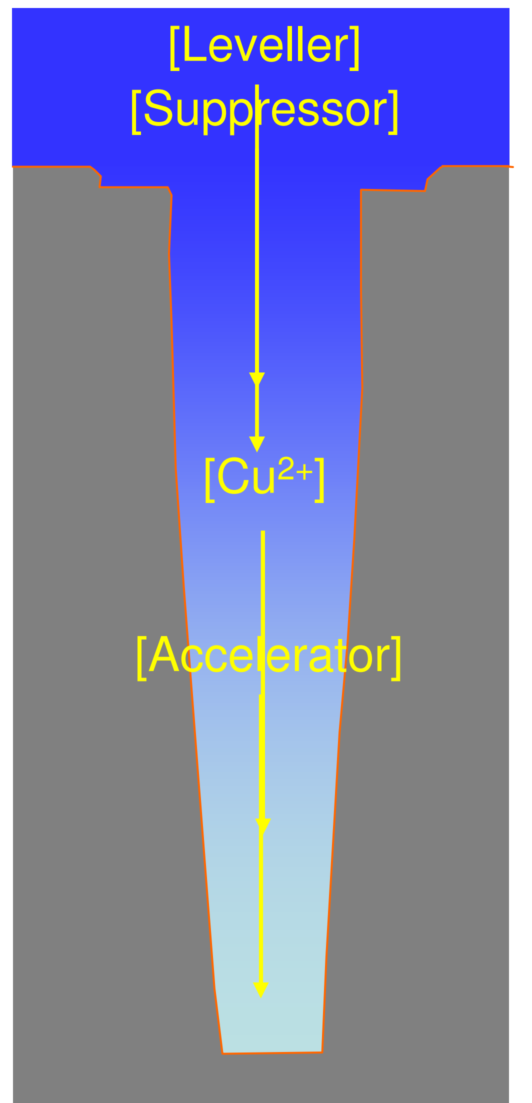
VelocityMagnitude – m/s

0 0.0005 0.001 0.0015 0.002 0.0025 0.003 0.0035 0.004 0.0045 0.005

As AR increases, a larger portion of the via becomes diffusion-controlled.



Via Filling Mechanism



Charge Transfer

$$Cu^{2+} + 2e^{-} \rightarrow Cu^{0}$$

Mass Transfer

How to Achieve Void-free Filling?

Prerequisites

Seed conformality for uniform charge transfer

Surface wetting for proper mass transfer

Impact of current density?

Reduce current crowding at the via mouth

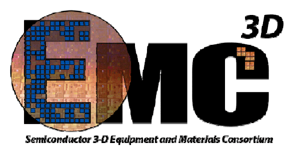
Waveform

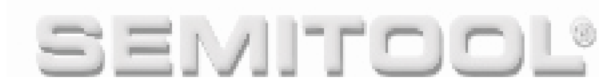
Bath composition

Reduce mass transfer limitation at the via bottom

Bath LCD

Flow mechanism





Reduce Current Crowding at Via Mouth

30µm×110µm

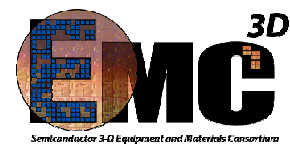
Chemical-induced

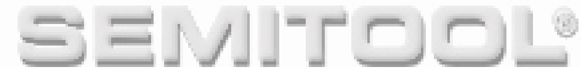
12µm×100µm

Waveform-assisted

PR is helpful for high AR, deep vias.

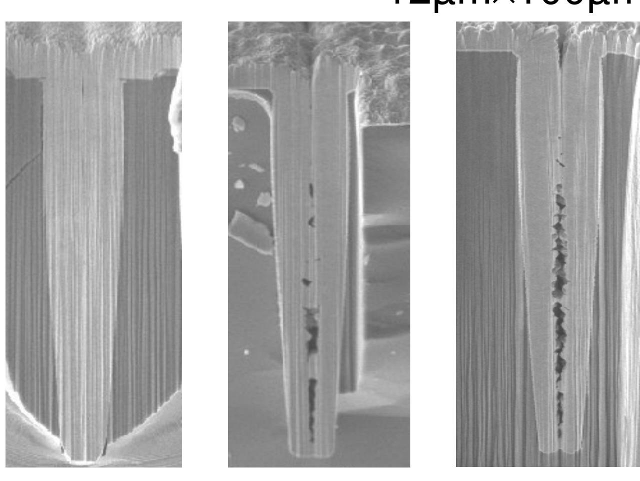
DC PR

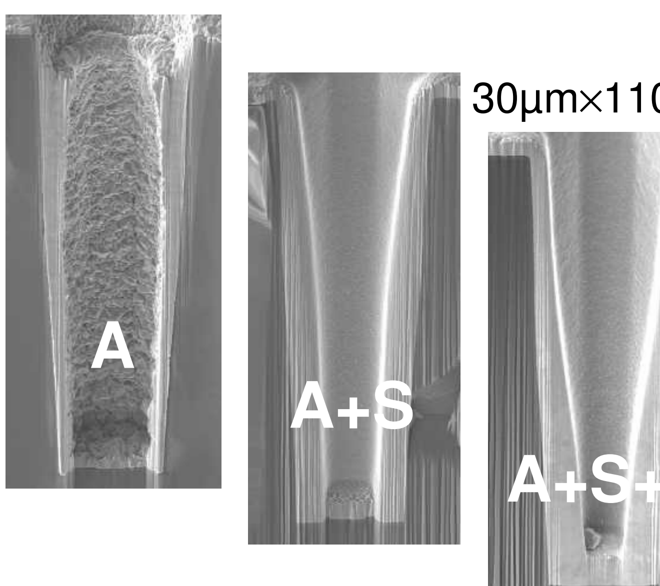


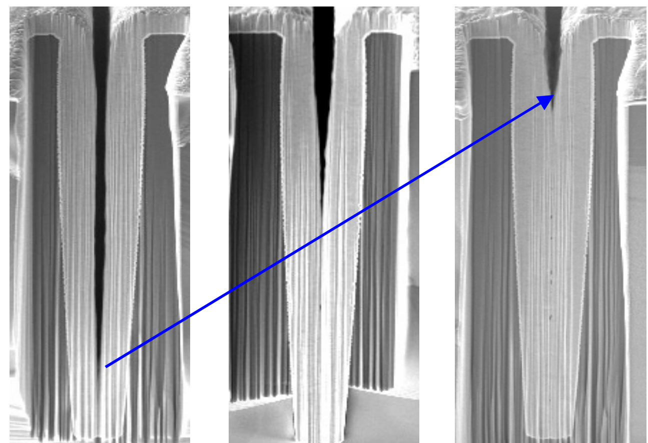


Reduced Current Crowding at Via Mouth : Chemical-induced

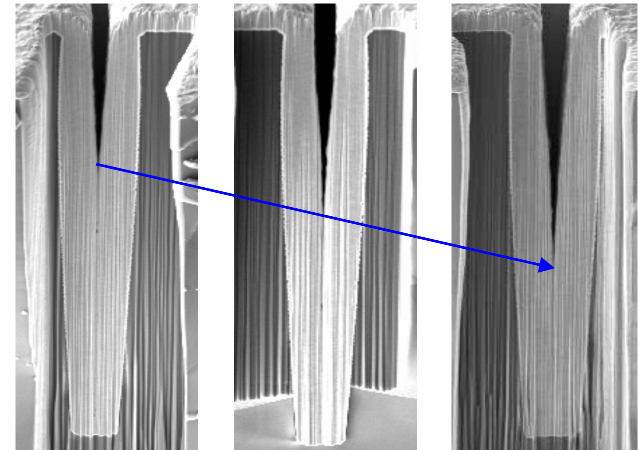
12µm×100µm



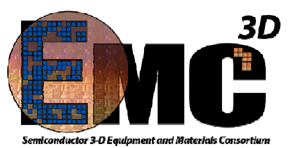


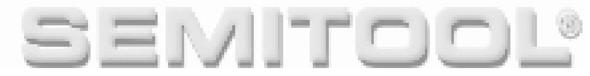


Increasing accelerator conc.



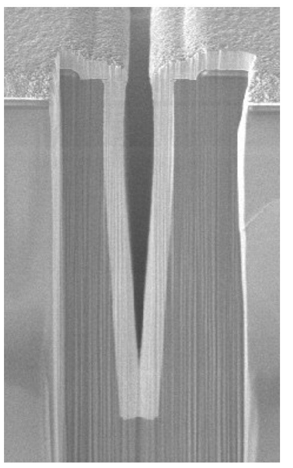
Increasing suppressor conc.





Reduced Current Crowding at Via Mouth: Waveform-assisted

DC

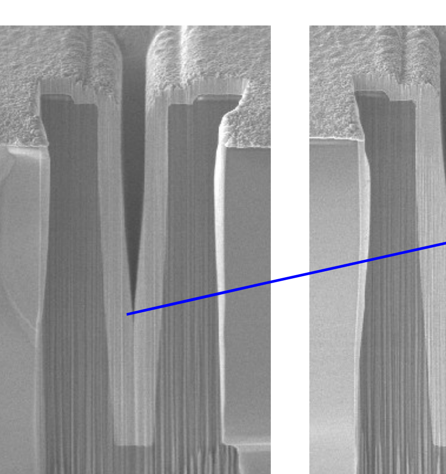


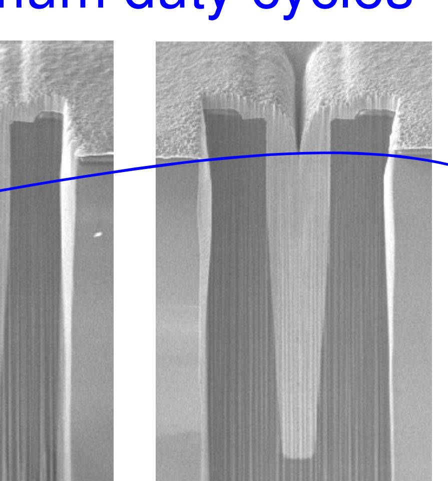
At a fixed amp-time and
bath composition

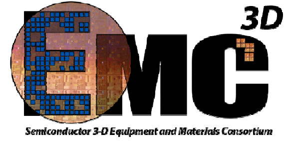
Optimum duty cycles

12µm×100µm

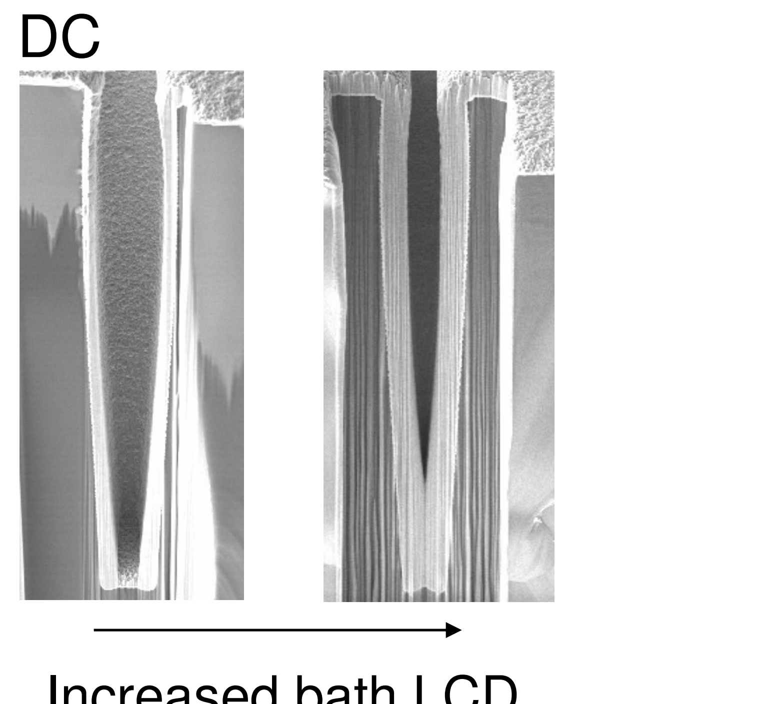
PR

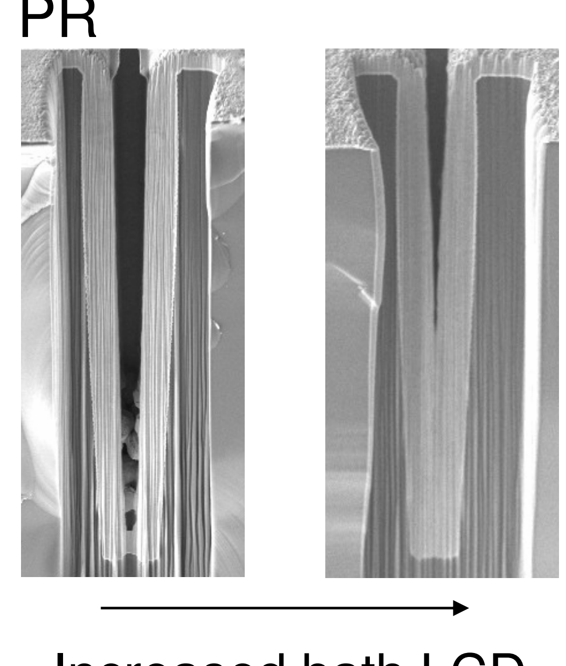






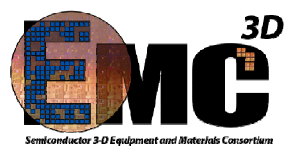
Reduced Mass Transfer Limitation at Via Bottom





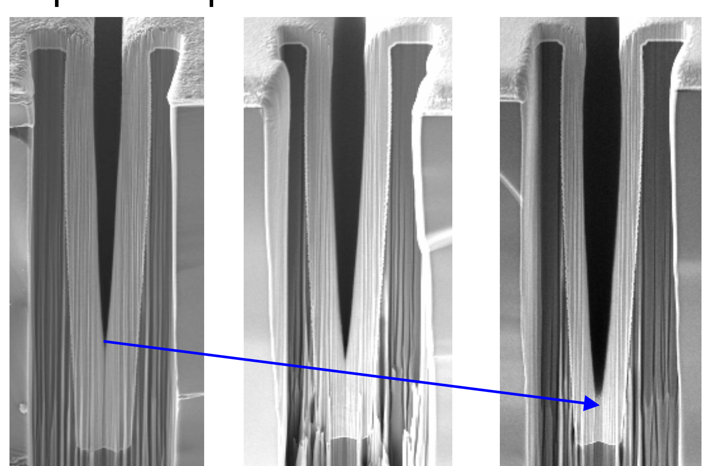
Bath LCD : A higher LCD bath is preferred.

Flow Mechanism : The ion transport within deep vias may not be substantially enhanced by the increased convection. But, a strong flow mechanism is still required for better transfer of organic components.

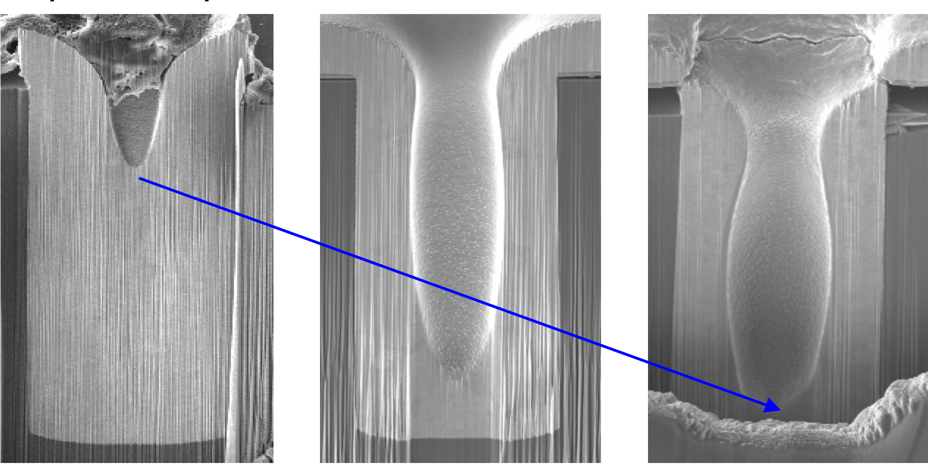


Current Density Effect

12μm×100μm



40μm×100μm



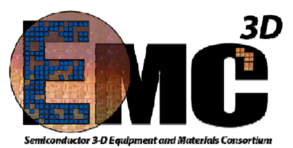
Current Density

Increasing Current Density

Increases current crowding at the via mouth

Approaches mass transfer limit at the via bottom

Reduces deposit within the via



Feature Dimension vs. Filling Time

Why is Smaller Feature Dimension preferred?

Fill Time (min)

160
140
120
100
80
60
40
20
0

5×25um

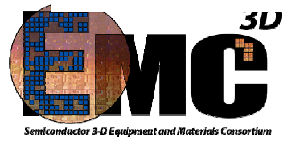
14×125um

30×100um

40×100um

0 1000 2000 3000 4000 5000

Feature Cross-Sectional Area (μm^2)



Filling Time vs. Manufacturability

Assumptions
1. Hardware : 6 CFD3m and 2 SRD
2. Operation : 500 hours/month
3. 200mm wafers with no PR pattern
4. Fixed current density

Cost of Ownership ($): 0, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100

Throughput (wafers/hour): 0, 2, 4, 6, 8, 10, 12, 14, 16, 18, 20

Filling Time per Wafer (min): 0, 30, 60, 90, 120, 150

5×25um

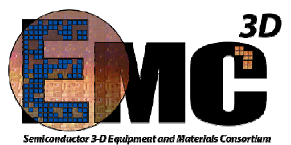
14×125um

30×100um

40×100um

Manufacturablity

Actual throughput & CoO varies with tool configuration and process conditions.
Resist pattern plating will have better overall cost of ownership.



Summary

Copper filling process with robustness and speed is among the most important to make TSV interconnection manufacturable.

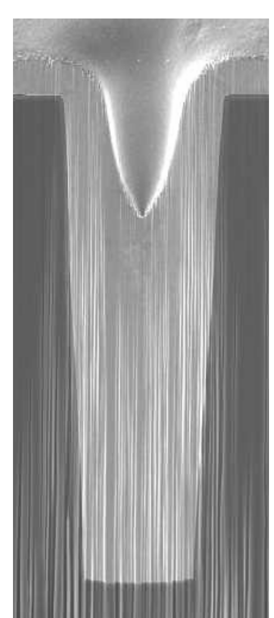
- Surface wettability
- Seed conformality

Prerequisites for proper mass transfer and current distribution

- Bath composition
- Waveform and current density
- Flow conditions

Eliminate mass transfer limitations at the via bottom

Reduce current crowding at the via mouth



Void-free Bottom-up Filling