Potential projects based on 3DIT for the ILC Detectors

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related talks: R. Yarema, L. Andricek, M.Demarteau

▷ More information on ILC Web site: http://www.linearcollider.org/cms/

CONTENTS

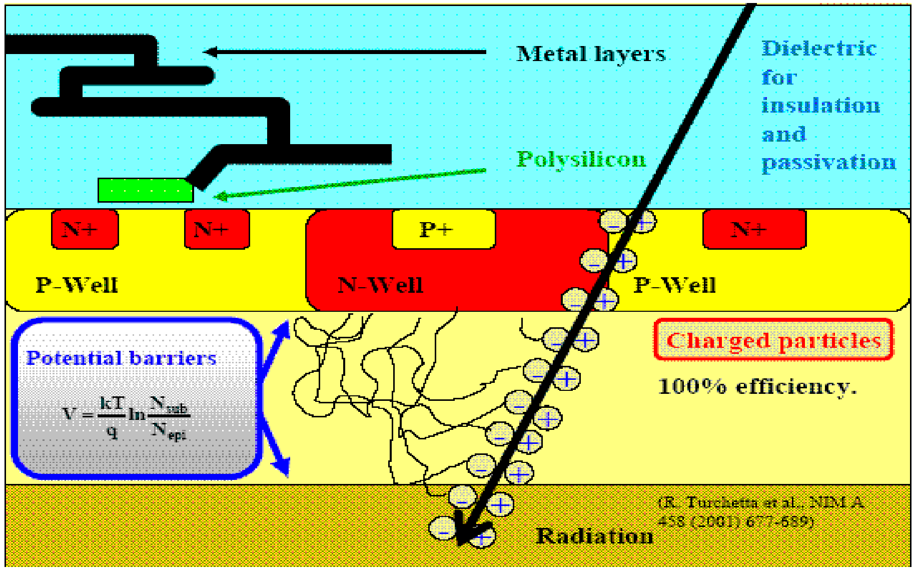
- Integration of data processing in small pixels
- System Integration problems addressed to 3DIT
- Application of 3DIT to light silicon ”strip” trackers
- Application of 3DIT to the pixellised read-out of a TPC
- Application of 3DIT to a small (beam monitor + shallow angle phys.) calorimetre
- Summary & Outlook

- **p-type low-resistivity Si hosting n-type "charge collectors"**
  - *signal created in epitaxial layer (low doping):*

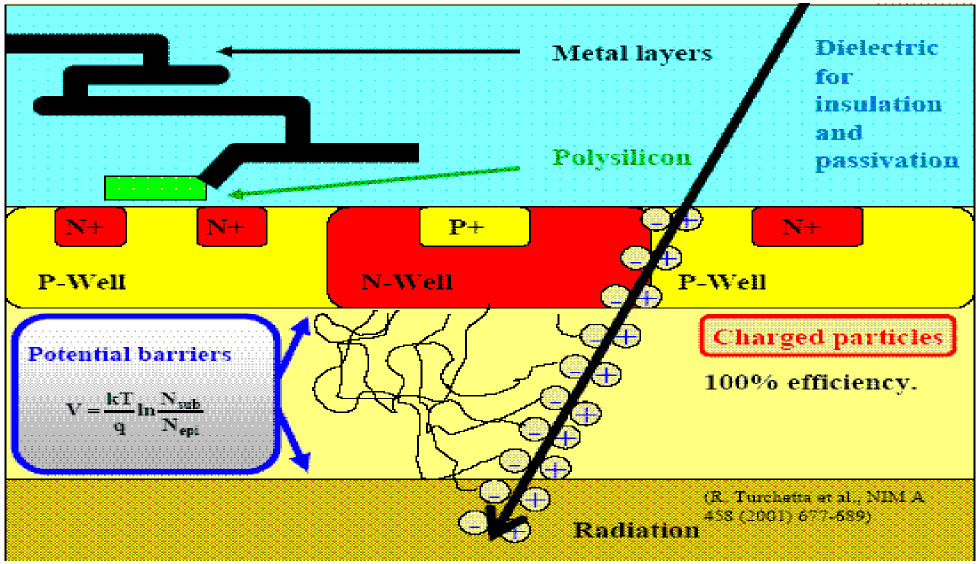
    $Q \sim 80$ *e-h /* $\mu m \mapsto$ *signal* $\lesssim 1000\ e^-$
  - *charge sensing through n-well/p-epi junction*
  - *excess carriers propagate (thermally) to diode*

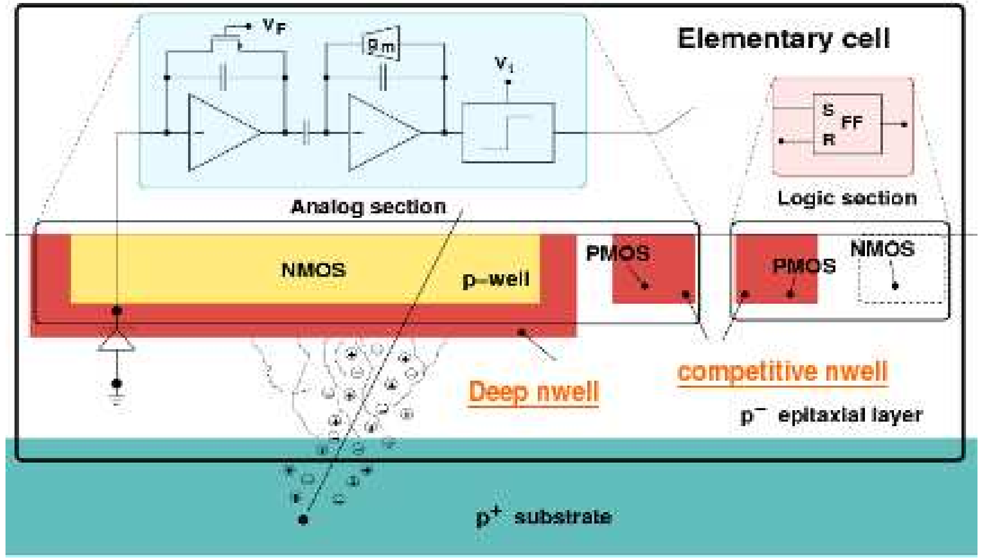
    with help of reflection on boundaries

    with p-well and substrate (high doping)



- **Specific advantages of CMOS sensors:**
  - ◇ *Signal processing* μ*circuits integrated on sensor substrate (system-on-chip)* $\mapsto$ *compact, flexible*
  - ◇ *Sensitive volume (*$\sim$ *epitaxial layer) is* $\sim$ *10–15* μm *thick* $\longrightarrow$ *thinning to* $\sim$ *30–40* μm *permitted*
  - ◇ *Standard, massive production, fabrication technology* $\longrightarrow$ *cheap, fast turn-over*
  - ◇ *Room temperature operation*



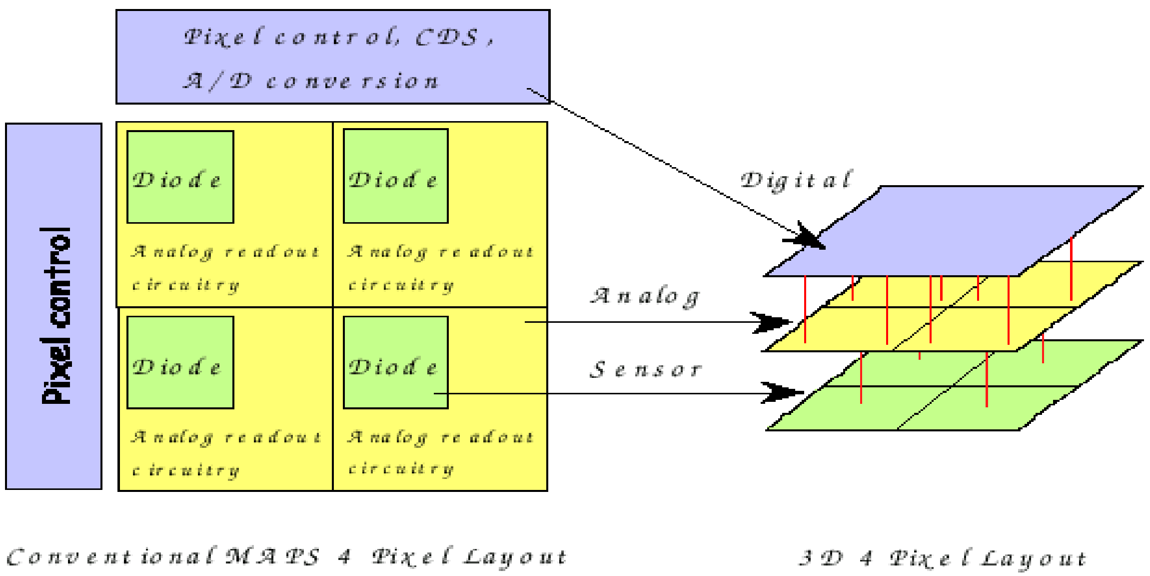


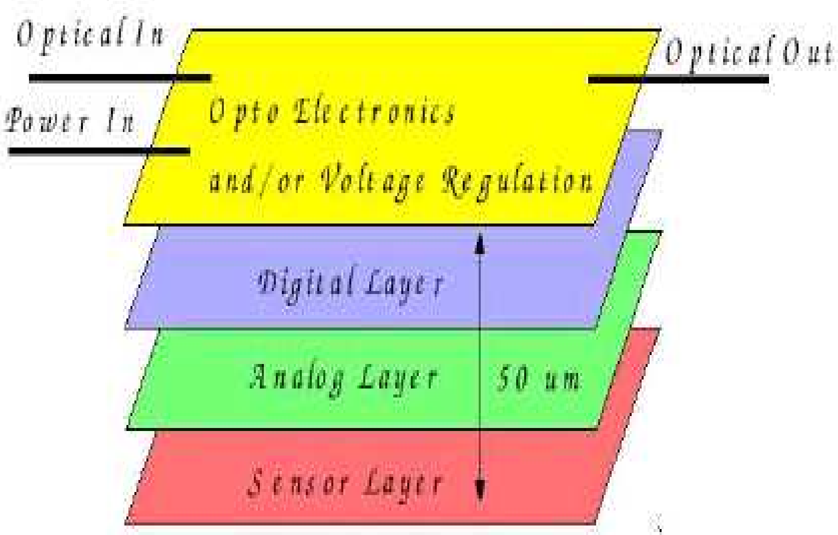
- Very thin sensitive volume $\rightarrowtail$ impact on signal magnitude (mV !)
- Use of P-MOS transistors difficult and exposed to drawbacks
- Sensitive volume almost undepleted $\rightarrowtail$ impact on radiation tolerance & speed
- Commercial fabrication (parameters)

  $\hookrightarrow$ Impact on : sensing performances (CCE),
  design of signal processing μcircuits (nb of metal layers),
  radiation tolerance

- **Split signal collection and processing functionnalities :**
  - *Tier-1: charge collection system*
  - *Tier-2: analog signal processing*
  - *Tier-3: mixed signal processing*
  - *Tier-4: digital signal processing*
  - *Tier-5: signal extraction (optical ?)*

- **Use best suited technology for each Tier :**
  - *Tier-1: epitaxy, deep N-well ?*
  - *Tier-2 & -3: analog, low leakage current, process (nb of metal layers)*
  - *Tier-4 & -5 : digital process (nb of metal layers)*





- **Labs involved :** *IPHC-Strasbourg, LPSC-Grenoble, CEA/DAPNIA-Gif, IPN-Lyon*

The Economy of Material Budget

- **Minimise multiple scattering inside detector material wherever possible ($b \searrow$)**

  $\hookrightarrow$ *thickness, amount and choice of material for mechanical support, gluing, electrical connexions, thermal conductivity, power dissipation (avoid active cooling), ...*

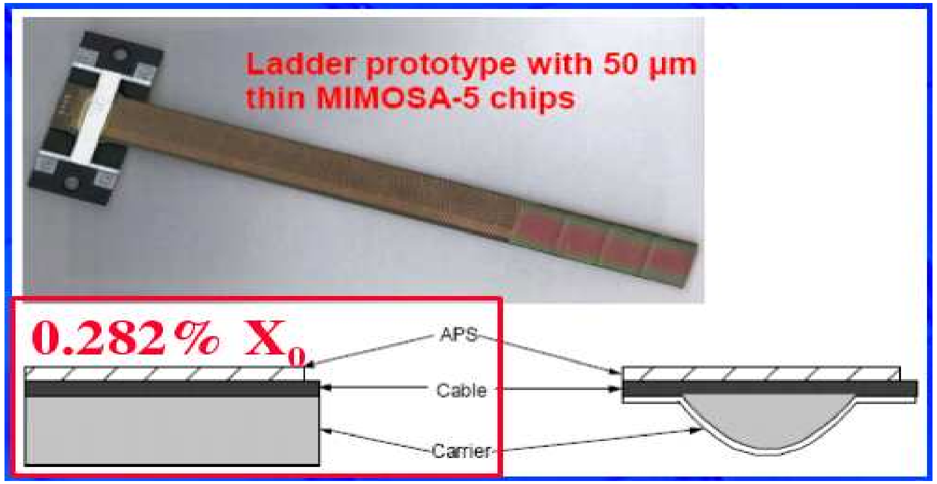
- **Goal : $<$ 0.2 % radiation length / layer** *(including chip + support + services) ($\Leftrightarrow$ $<$ 200 μm of silicon)*

- **Presently $<$ 3 % seems achievable** *(STAR vertex detector)*

- **STAR ladder : kapton cable contributes with 0.090 %**
  and carrier with 0.110 % of radiation length

  $\Rrightarrow$ **replace them with aluminised CVD diamond ?**

  $\hookrightarrow$ *bonus in thermal transport*

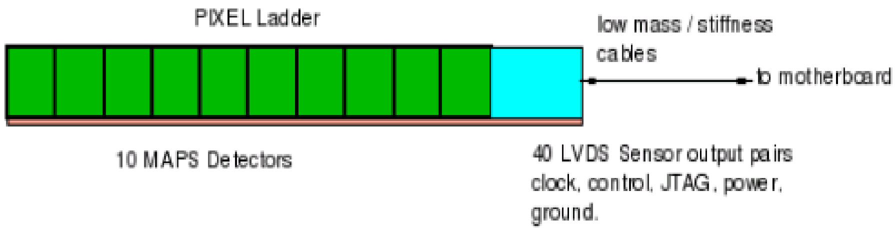


- **(CMOS) Sensor fabrication yield is a concern**

  $\Rrightarrow$ **diced sensors prefered to stitched sets of 5–10 sensors**

  $\hookrightarrow$ **inactive zones ($\gtrsim$ 40 μm wide) at sensor edge from dicing**

  $\Rrightarrow$ **can these zones be reduced to $\lesssim$ few μm with plasma etching ?**



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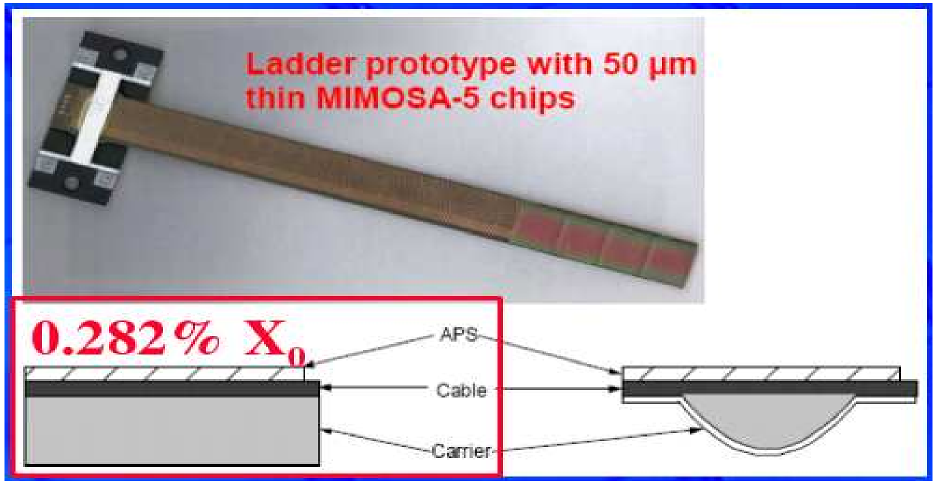

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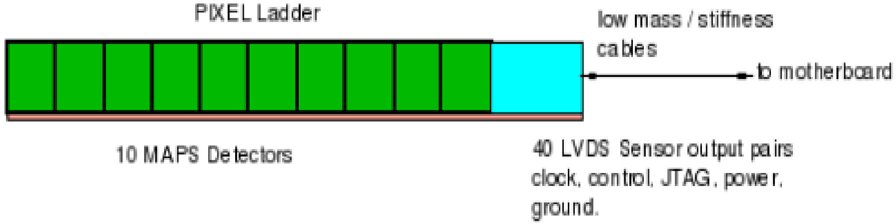
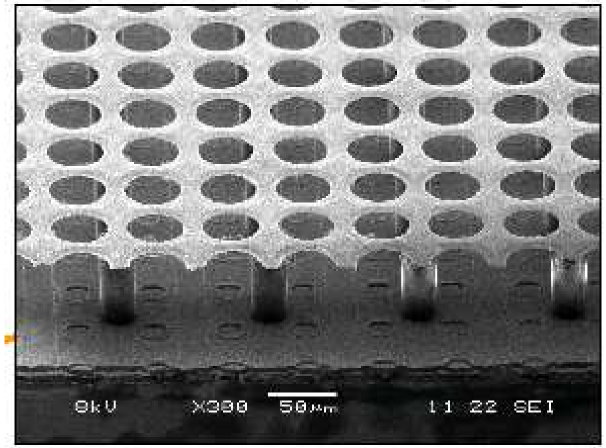


► **3D Integ. Techno. include thinning and dicing capacities of great interest**

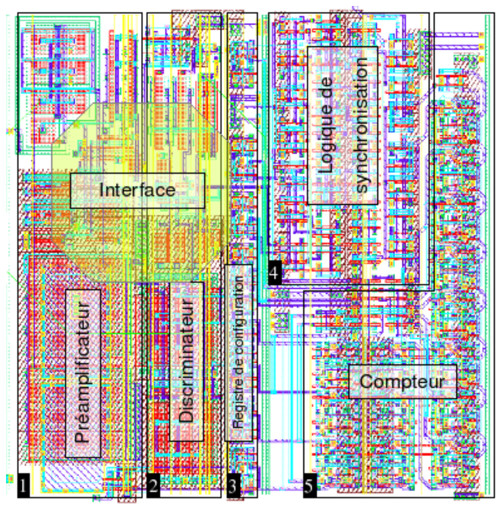
TPC Read-Out & End-Plate

- **TPC read-out via μMegas (signal amplification in gas) combined with pixellised anode plane hosting integrated signal processing μcircuits (TimePix)**

  $\hookrightarrow$ **Each pixel (55$\times$55 μm^2) contains μcircuits for pre-amp & shaping, discri., 14-bit counter, etc.**



- **3DIT expected to allow :**
  - ◇ **reduce complexity and improve performances of signal processing μcircuits**
  - ◇ **reduce material budget of TPC end-plate**
  - ◇ **reduce thickness of end-plate ($\equiv$ gap between TPC and Si detector behind end-plate)**

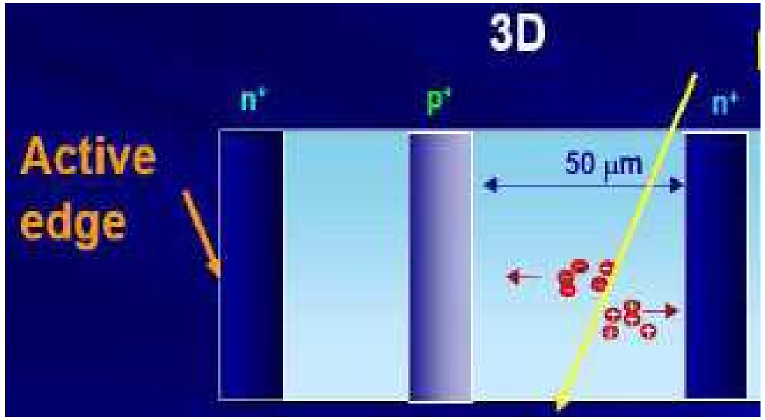


- **Objectives recover those for other applications of the chip** *(e.g. imaging)*

- **R&D to make Si-strip detectors evolve towards higher granularity and lower material budget**

  $\rightarrowtail$ **introduce alternated p- and n-type finger-shaped implants inside sensitive volume**

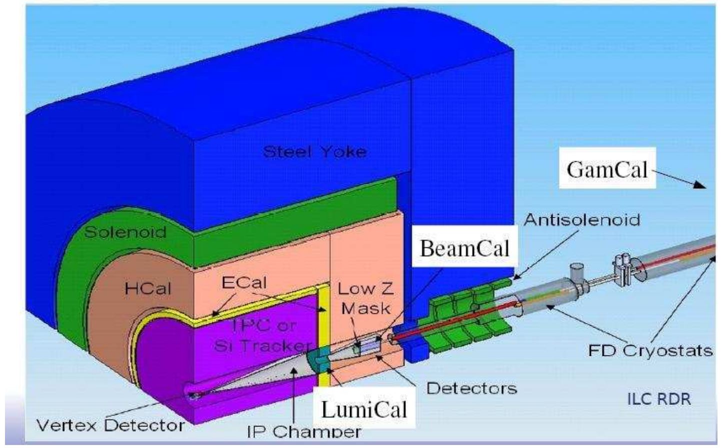
  $\hookrightarrow$ *relies on via technology*



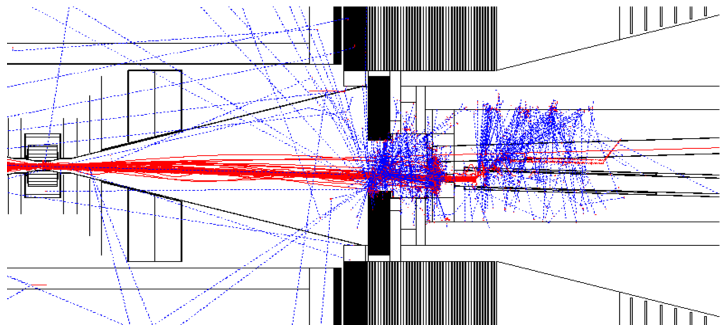
- **3DIT expected to allow :**
  - ◇ *improve read-out speed (ordre of mag.)*
  - ◇ *improve radiation tolerance*
  - ◇ *reduce material budget*
  - ◇ *larger active zone (active edges, etc.)*

	3D	Planar
Q collection path	50 μm	300 μm
V$_{Depletion}$	$<$ 10 V	70 V
Edge sensitivity	10 μm	500 μm
Q collection time	1–2 ns	10–20 ns

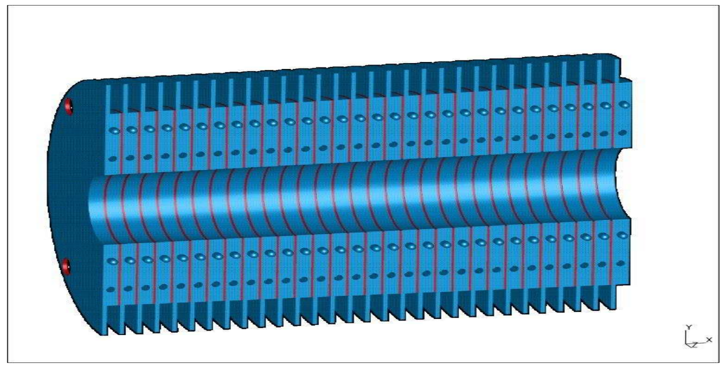
Forward Region Design



- **Small calorimetre installed near the beam pipe (5–30 mrad)**
- **Detect very energetic prompt electrons while swamped by gigantic electro-magnetic background from the beam**
  $\hookrightarrow$ **withstand O(1) MGy/yr !!!**
- **Provide fast (O(μs) info to beam monitoring system**



- **3DIT expected to allow :**
  - ◇ *reduce complexity and improve performances of signal processing μcircuits (avoid bump-bonding, cables, a.s.o.) integrated right behind the sensitive volume (e.g. diamond, AsGa)*
  - ◇ *reduce effects of bulk damage (cables, connectics)*
  - ◇ *reduce material sensitive to radiation*



- **Objectives recover those of R&D for LHC (fast and rad. hard)**

Summary $\rightarrowtail$ Common R&D Directions

- **several ILC groups are very concerned by the evolution of 3DIT ($\gtrsim$ 2015)**

  $\rightarrowtail$ *Expertise in Design and Characterisation*

  $\rightarrowtail$ *how can they contribute to the 3DIT devt ?*

- **2 areas where effort can be invested (substantial overlap with LHC, CLIC):**

  ▷ *Pixel & μcircuit integration $\rightarrowtail$ design kits, multiproject runs, rad. hard design ?*

  ▷ *System integration $\rightarrowtail$ studies of thinning & dicing, rad. hard material & fab. process ?*

- **2 types of activities in parallel :**

  ▷ *Technology surveys $\rightarrowtail$ we need to appreciate where we stand w.r.t. 3DIT*

  ▷ *Prototyping $\rightarrowtail$ design chips, make light material supports, dice chips, study connecting thinned sensors on thin mechanical supports, etc.*

- **Most activities supported by a large scale E.U. programme:** *EUDET/FP6 & its future/FP7*

- **Combine effort with world wide R&D for ILC and with spin-offs (***imaging applications, etc.)*

BeamCal: Need for Highly Integrated Rad. Hard Electronics

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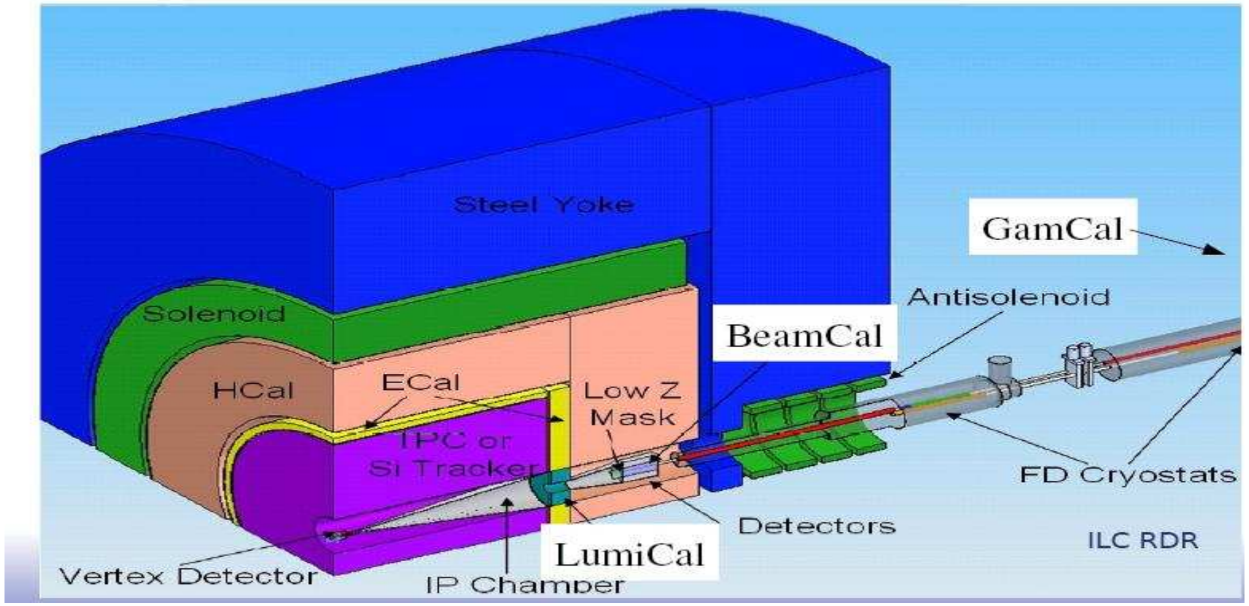
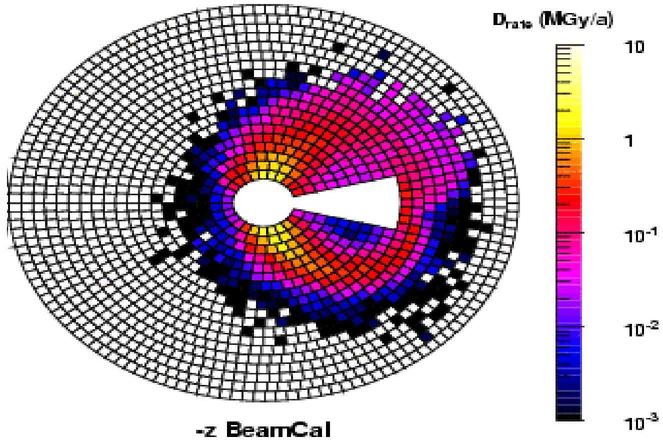
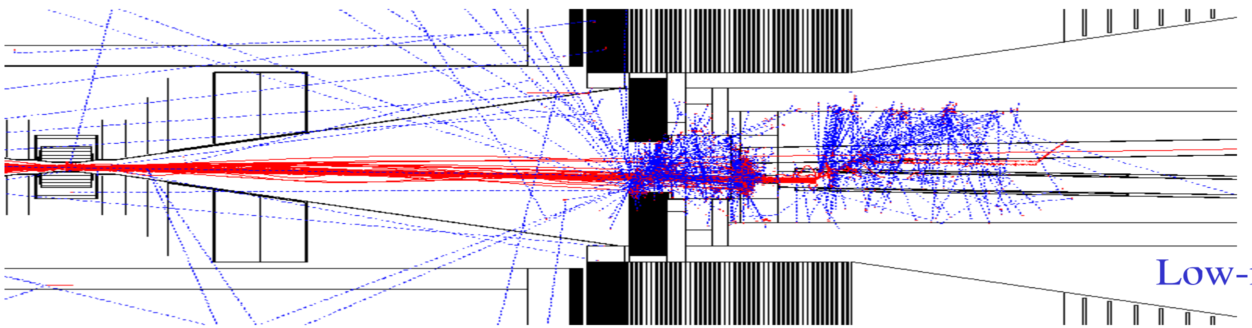


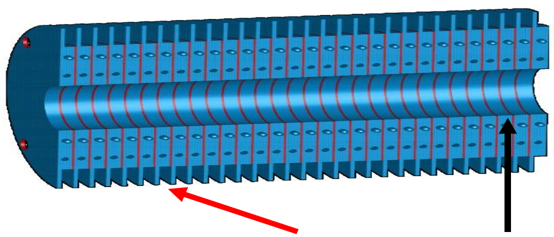


Radiation hard sensors
→ 100 Mrad / year

1. **Hermeticity : efficient electron veto in high background region → 10^5 channels / 200 msec**
2. **Bunch-to-bunch luminosity monitoring and feedback → 3000 channels / 100 nsec**



W-sensor sandwich, 30 one-X_0 layers



Low-noise electronics → outside or **in situ** ?