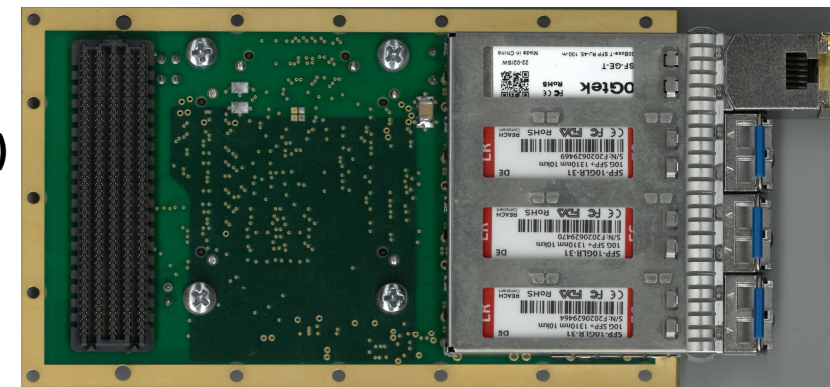
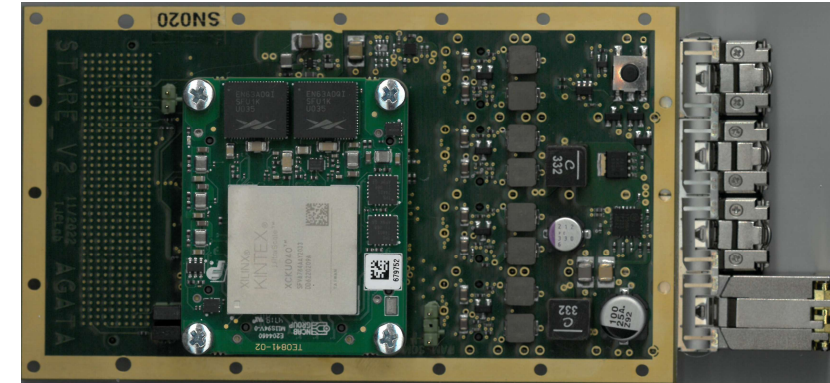
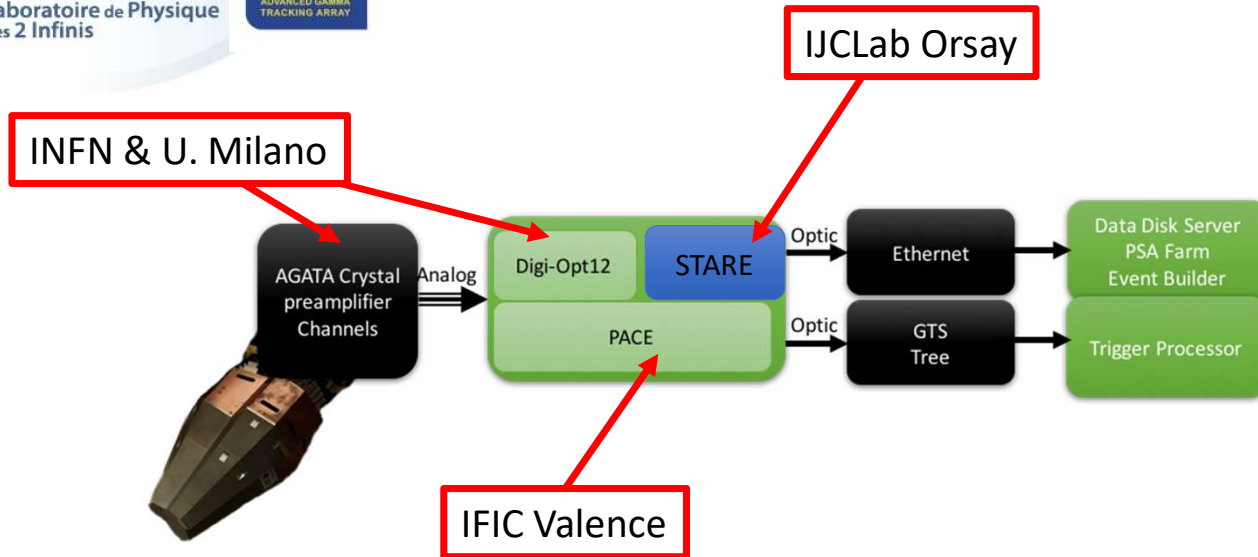


STARE

(Serial Transfer And Readout over Ethernet)

AGATA Project

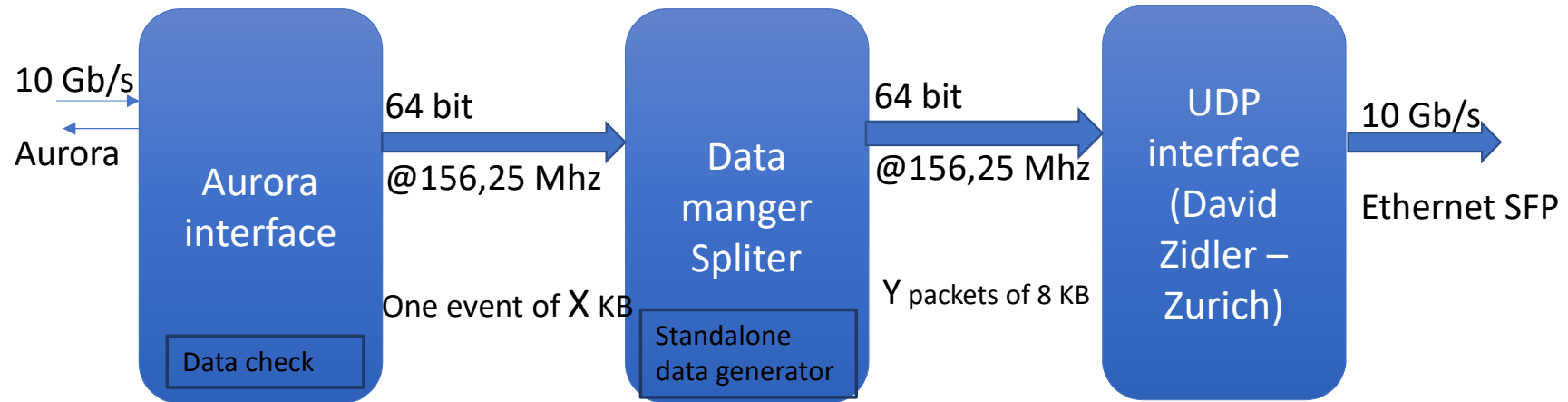
- ✓ STARE for AGATA
- ✓ STARE Firmware
- ✓ STARE Production
- ✓ AGATA simulator bay using STARE



**Input data rate from pre-processing : 4 x 10 Gbps serial (AURORA)
Network Bandwidth up to 4 x 10 Gbp (UDP)**

FMC vita 57.2
Spare LVDS I/O with the pre-processing
Full clock management inside the SOM and the FMC carrier.

1 Gbps IPBus for slow control (use 1*10Gbps network link)



- _ Slow control
- _ EEPROM
- _ Clock manager
- _ Spare LVDS link

Generators available (compute by Ipbus, independant, rate ajustable, random trigger) :

- _ byteANDpackage_counter : data can be checked by SQM ; size of event 8 Bytes -> 256 MBytes
- _ 2 Rams of 8KB : can be fill by Ipbus

- Manufacturer : STAE (Savigny-sur-Orges)
- 140 Stare produced (10 Pre-production)
 - 64 (+10 Pre-production) delivered at Orsay (+1 not_OK)
 - 61 ready to be delivered (+ 4 not_OK)
- testbench and test procedure developped at IJCLab :
board is validated by the manufacturer before delivery



_ shortcut test

_ STARE-interface board

power supply (LED indicator)

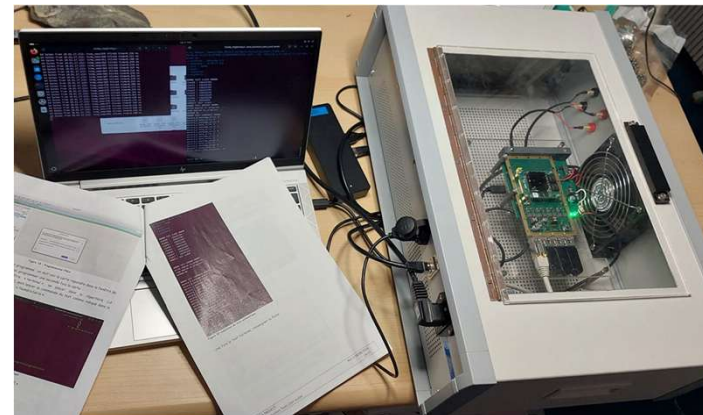
power consumption measurement

loopback FMC link

_ optical loopback (SFP)

_ dedicated computer, control by Ipbus, log file

_ configure MAC address

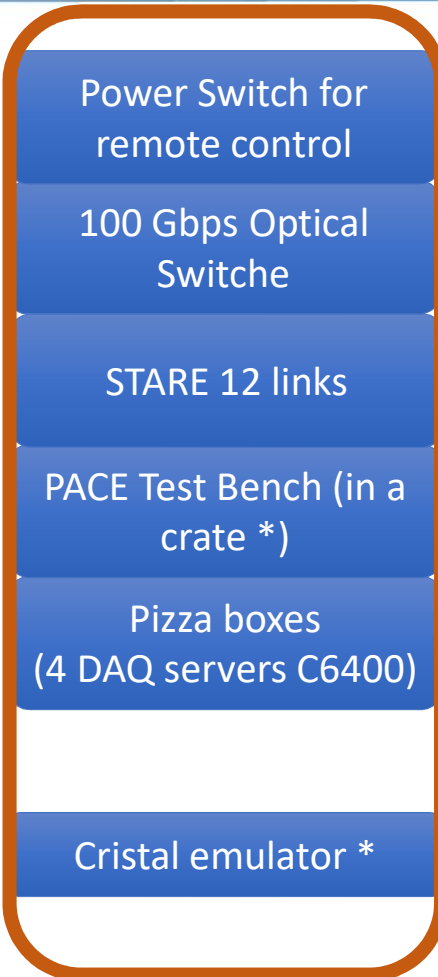


```
le ~/home/STARE_TB/test_prod_fth
03-10-24 10:35:55.252580 [131309]
> protocol : ipbusdp-2.0
> hostname : 10.81.17.212
> port : 50001
> path :
> extension :
> arguments :

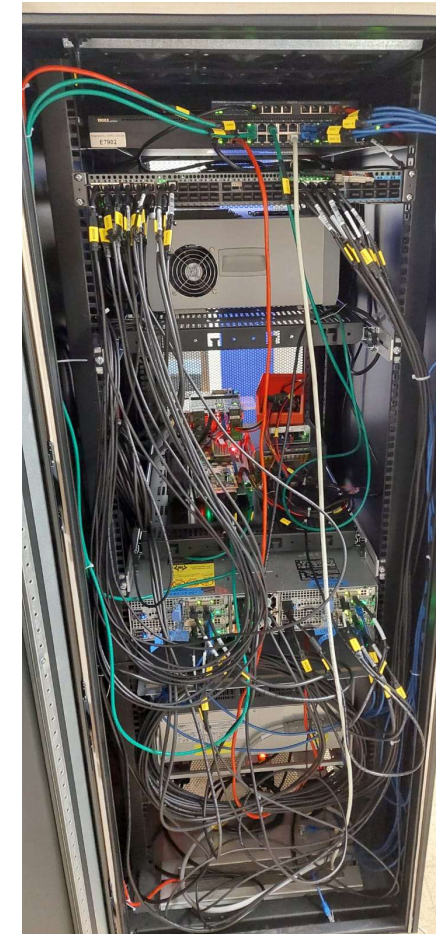
##### TEST CLOCK #####
clock0 : 156252599
clock1 : 156252600
clock2 : 156252599
clock3 : 156252599
clock4 : 156252454
clock5 : 156252454
clock6 : 156252454
clock8 : 99999999
CORRECT TEST CLOCK
##### TEST EEPROM #####
write eeprom in progress ...
read eeprom in progress ...
EEPROM OK
##### TEST LOOPBACK #####
aurora_0 package_error 0
aurora_0 byte_error 0
aurora_1 package_error 0
aurora_1 byte_error 0
aurora_2 package_error 0
aurora_2 byte_error 0
aurora_3 package_error 0
aurora_3 byte_error 0
aurora_4 package_error 0
aurora_4 byte_error 0
aurora_5 package_error 0
aurora_5 byte_error 0
aurora_6 package_error 0
aurora_6 byte_error 0
error_count_slow_loopback: 0

TESTS ARE OK
STARE_TB@11-lefav1:~$
```

- A new Bay to be designed to house all the STARE facilities
- New PACE crate with cooling, Fans, PS mechanics to fix the backplane and up to 38 channels. Plus 3 Stare links
- 12 links Stare bench
- 100 Gbps switches
- Power switch
- 4 DAQ servers up to 8 STARE emulators
- Cristal emulator (pulser + fanin/fanout + single_diff)
- Total of 23 links @ 10 Gbps each (230 Gbps).
- 100 Gbps fibre between 104 and 206 (200 Gbps as an upgrade)



* Missing some parts



Commande :
3*9,5 Gbit/s
3*7,5 Gbit/s
9*4 Gbit/s
1*5 Gbit/s
Total = 80 Gbit/s

SQM :
3*1187 Mo/s
3*937 Mo/s
9*500 Mo/s
1*625 Mo/s
9997 Mo/s (=79,98 Gbit/s)

Après 24h aucune loss, aucune corrupted
À Vérifier : les empty (missing) sont causés par l'encombrement du réseau ?

MERCI