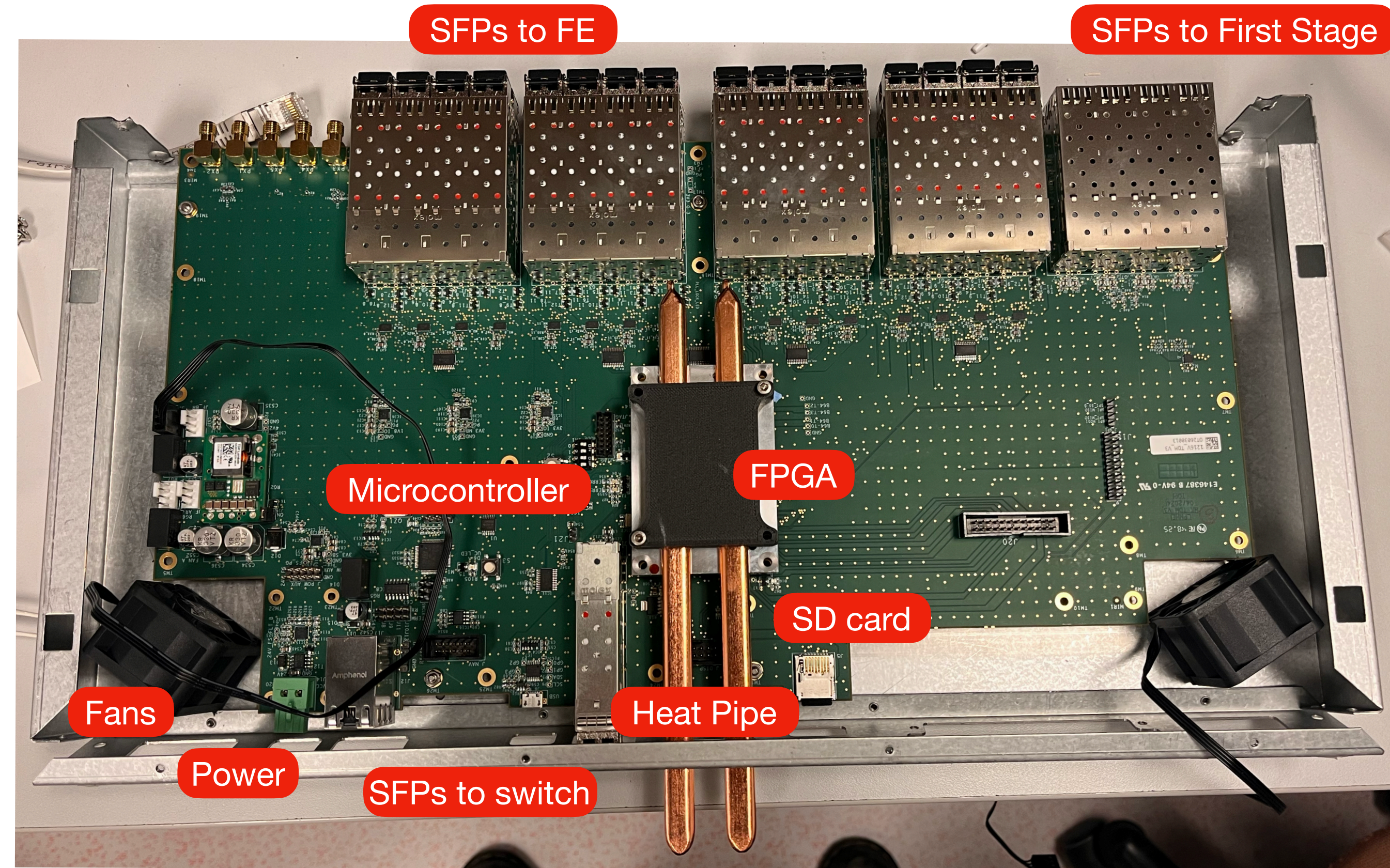


# Time Distribution Module Setup at LPNHE

Maria Adriana Sabia - CNRS, LPNHE

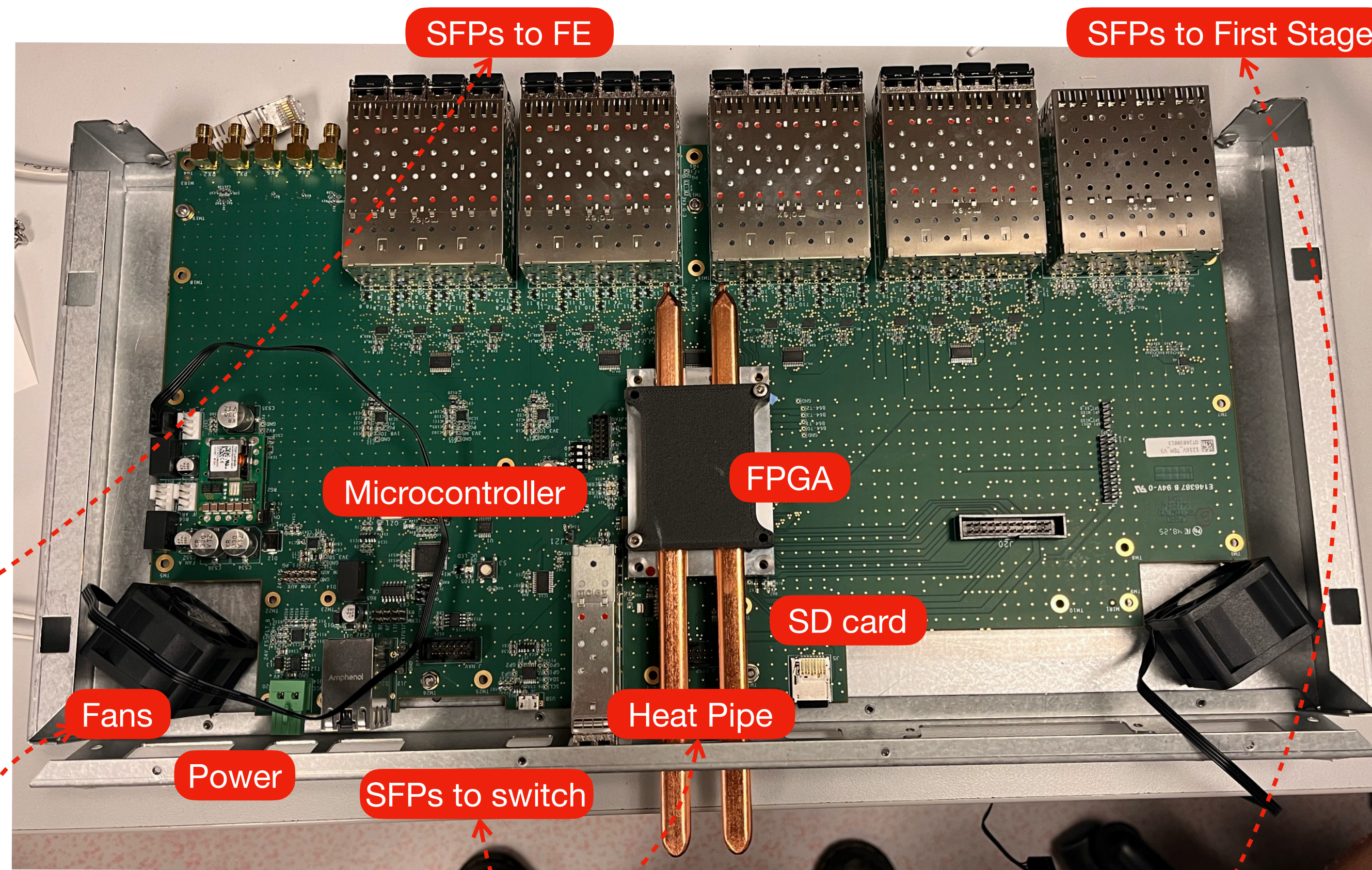
- The TDM board is designed to:
  - Receive master clock and distribute it with jitter at the endpoint  $<$  requirement
  - Guarantee a constant channel to channel phase difference over each reset and power up compensating the differences introduced by different cable lengths
  - Guarantee a bidirectional data bandwidth  $>$  100 Mbps
  - Communicate to the DAQ system to exchange slow control data.
  - Redundant optical fiber link to each FE to be activated by a software command



- Main element : a Xilinx XCZU9EG Zynq ultrascale+ SoC FPGA
  - FPGA comes pre-assembled on a electronics board hosting main power supply section, a double data rate (DDR) memory for the processor etc... no complex routing on the board
  - Link between the TDM and the system-on-module with 4 high-speed connectors with 160 pins each

- Receives:
  - Reference clock
  - TDC reset
  - Global coarse counter
  - PPS
  - Synchronous commands from the first stage

SFP cages: bi-directional, synchronous and phase deterministic link over optical fiber pair used also to exchange slow control information between the DAQ system and the front-ends

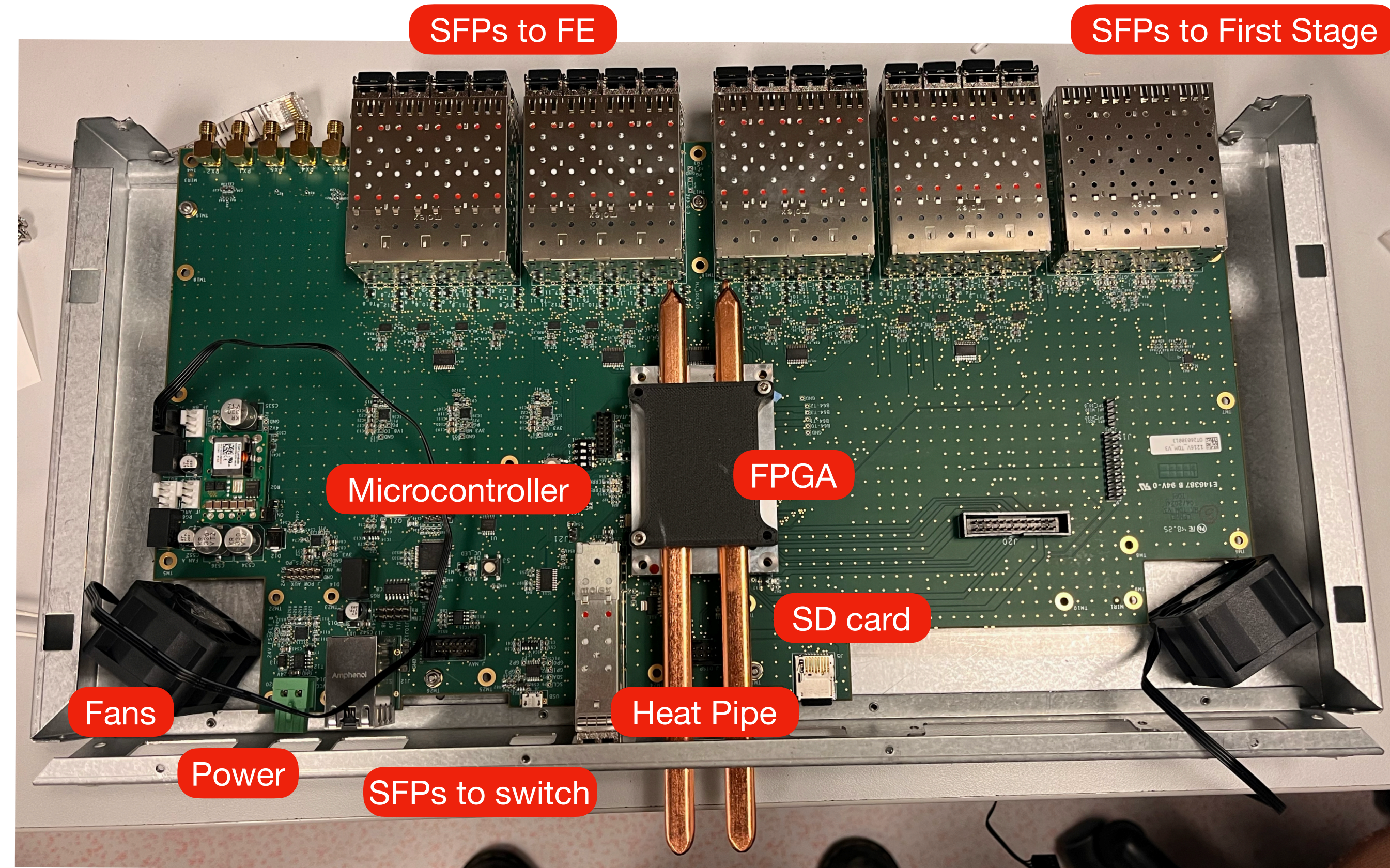


Heat pipe and 2 fans to provide cooling to the FPGA and SFPs

1 Gb/s Ethernet x2 to DAQ for slow control

SFP cage connection to First Stage Distribution

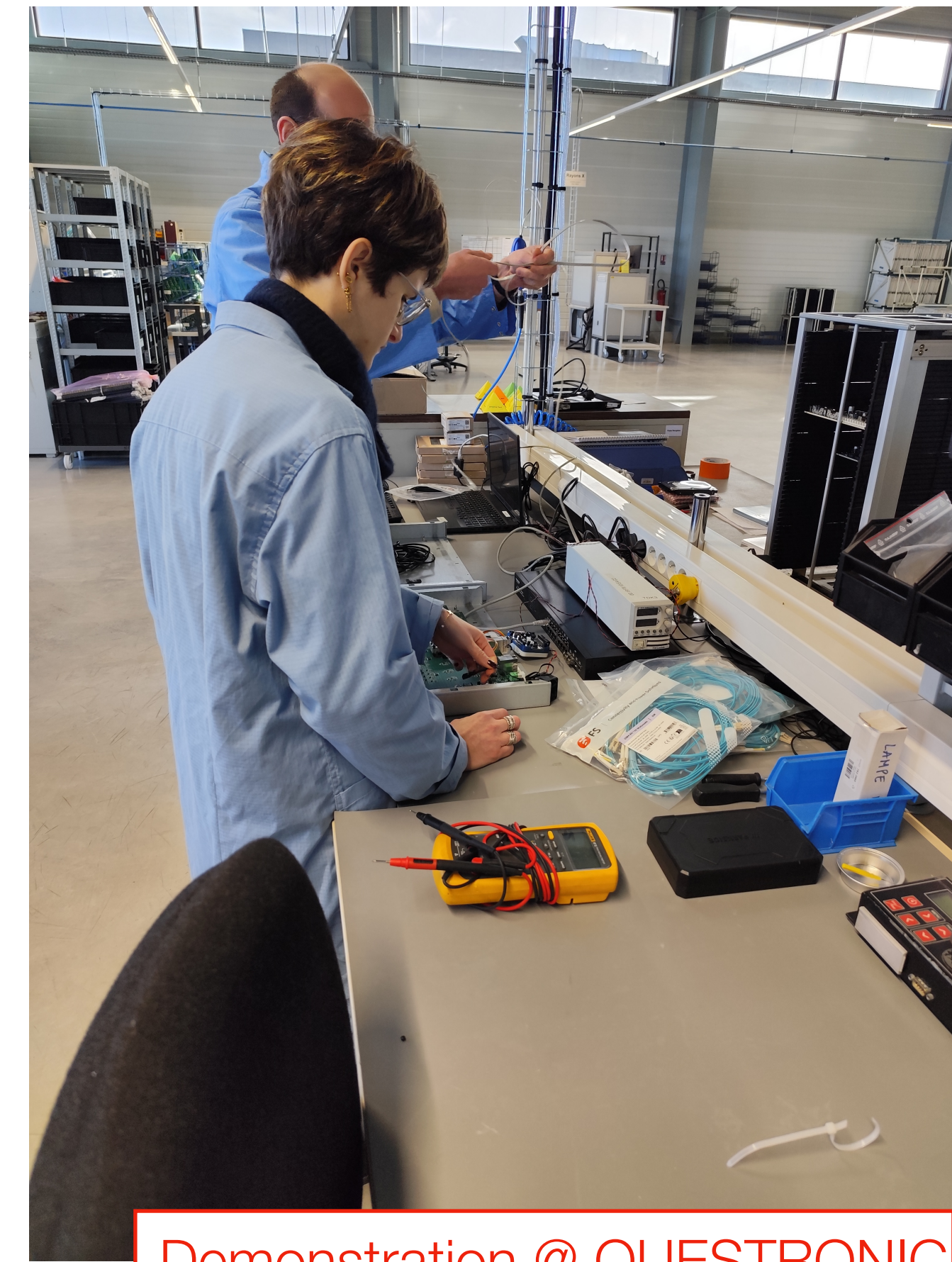
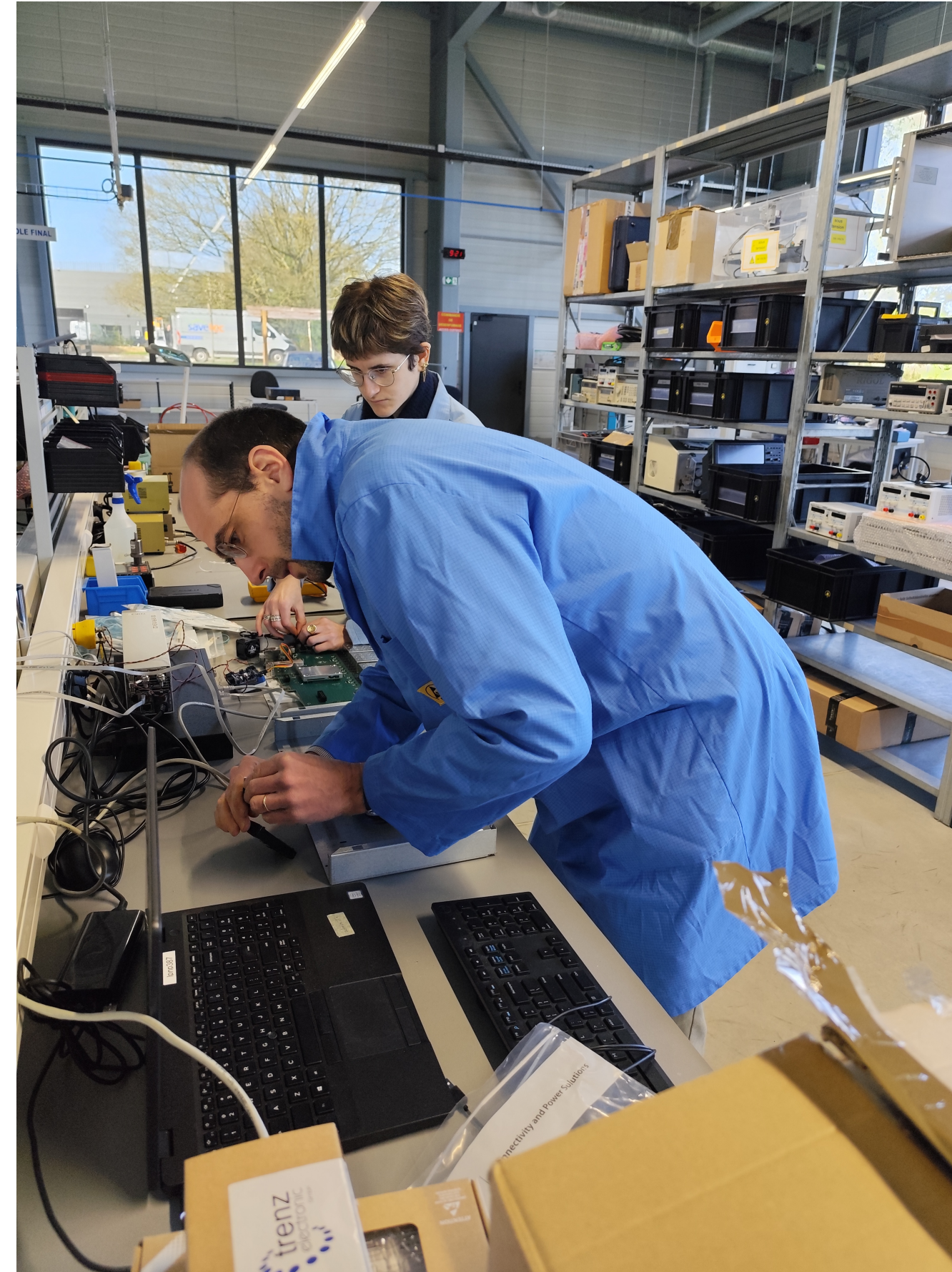
- Assembly and testing procedure ready to be handled to external company (OUESTRONIC)
  - Goal: screening of faulty components and bad solderings
  - Procedure:
    - Physical installation: populated board fixed on a dedicated support, external components are mounted (mezzanine module, SFPs, SD card and cables)
    - Automatic tests: board switched on, ID info collected and network configured. Board parameters checked (voltages, current, temperature). Bit error rate measurement is done on all links.
    - Physical disassembly: the operator checks that data is collected and removes the SD card.



- At the end of the tests, the TDM is either ready to be used or declared faulty
- A report is posted on the github page of the tests.

# Integration: assembly procedure

- Assembly and testing procedure ready to be handled to external company (OUESTRONIC)
  - Goal: screening of faulty components and bad solderings
  - Procedure:
    - Physical installation: populated board fixed on a dedicated support, external components are mounted (mezzanine module, SFPs, SD card and cables)
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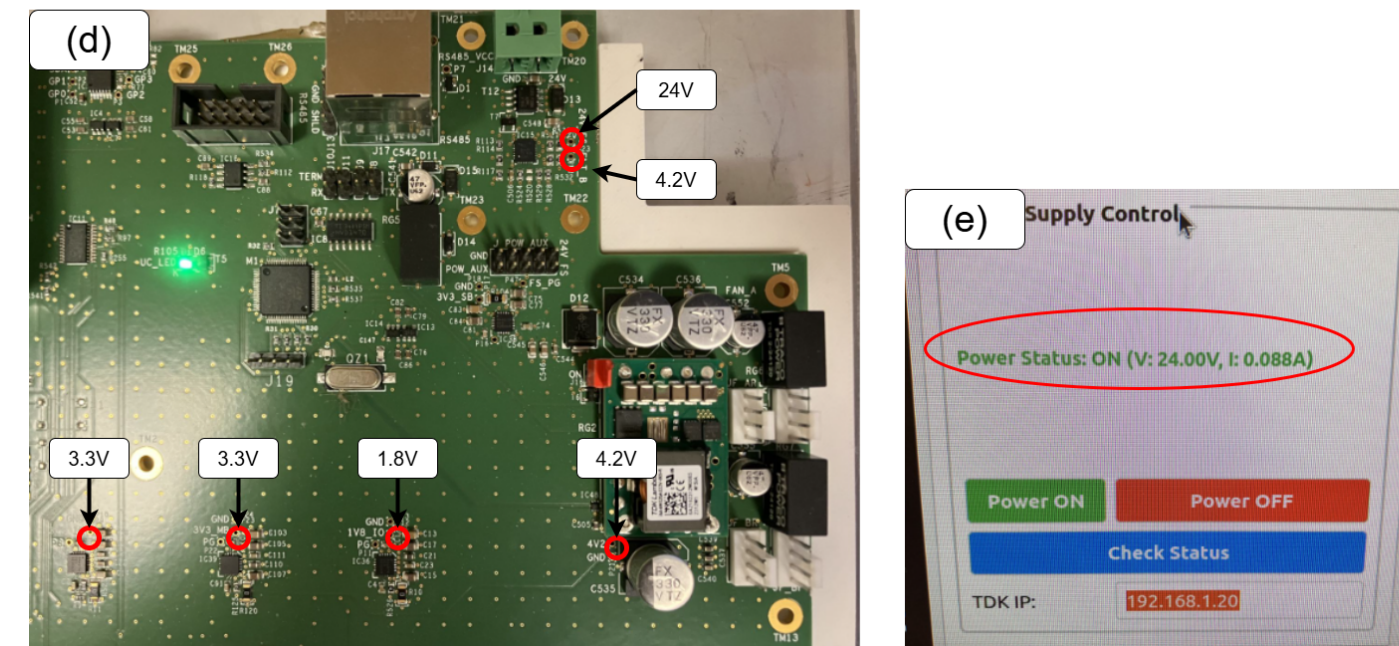
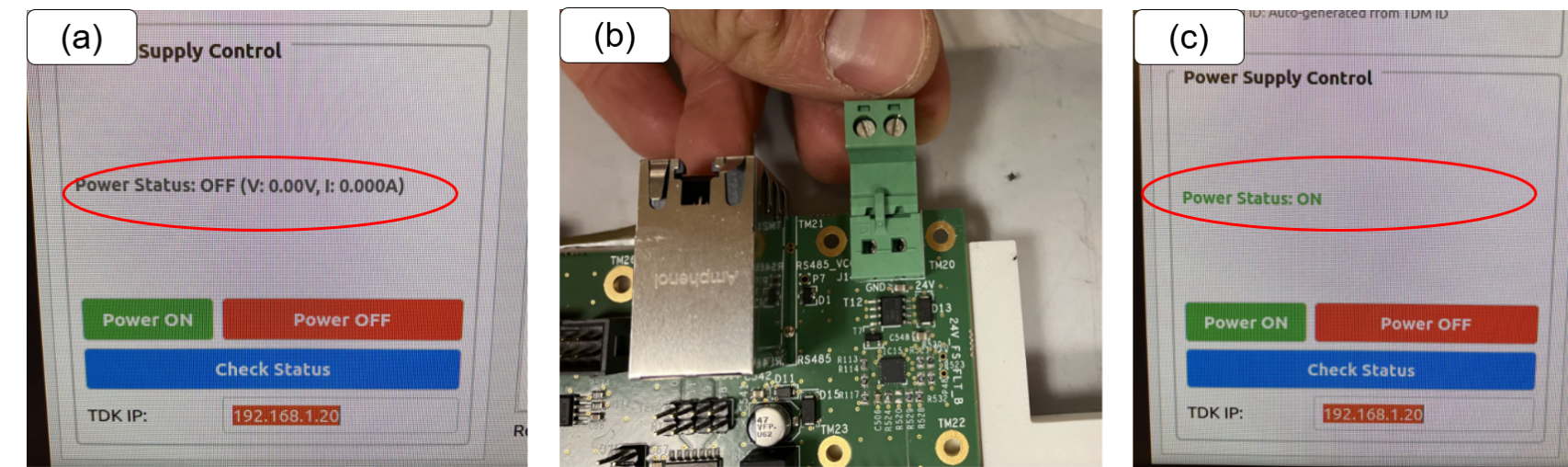
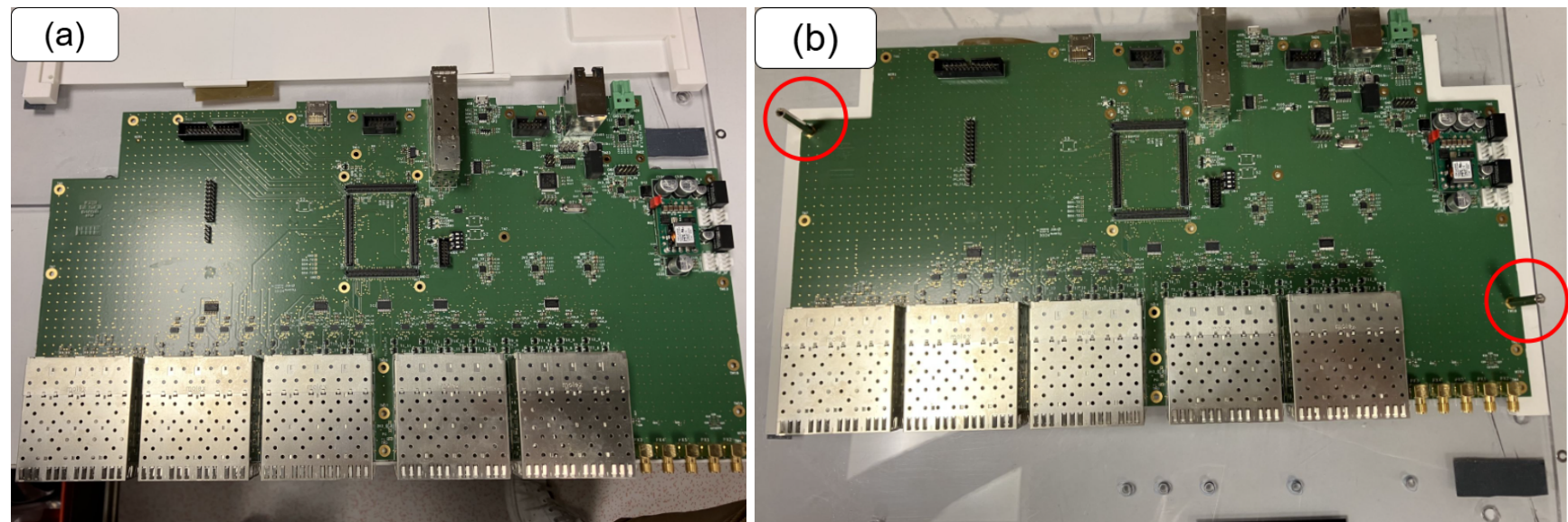


Demonstration @ OUESTRONIC

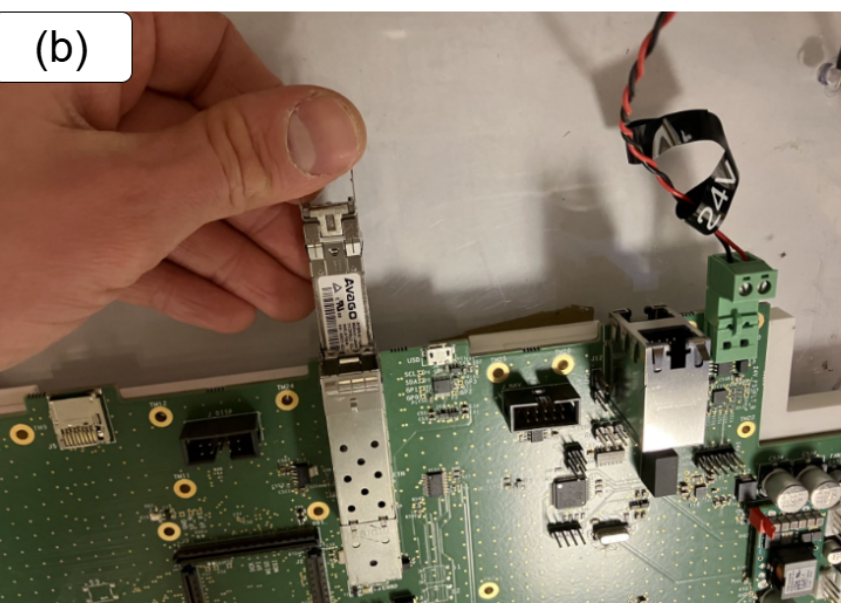
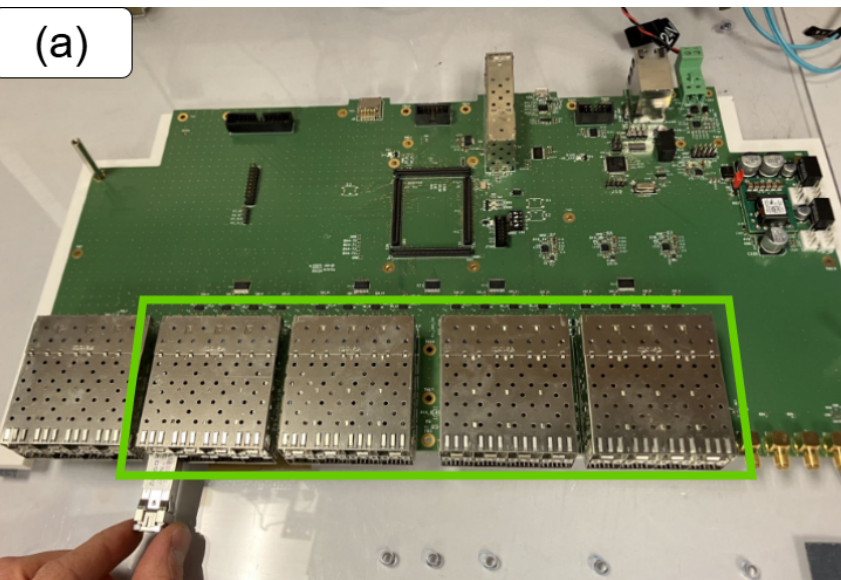
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# Hyper-K Assembly

## 1 Support mounting

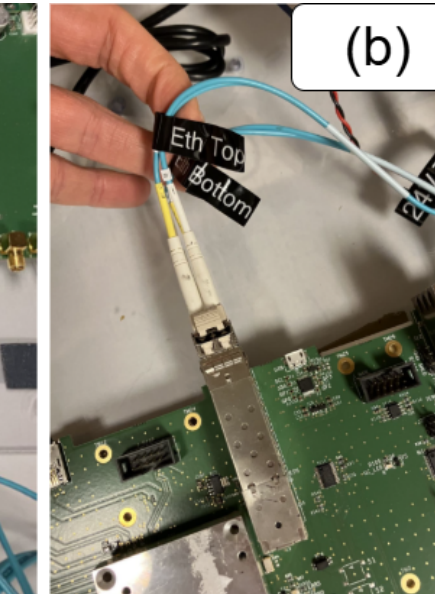
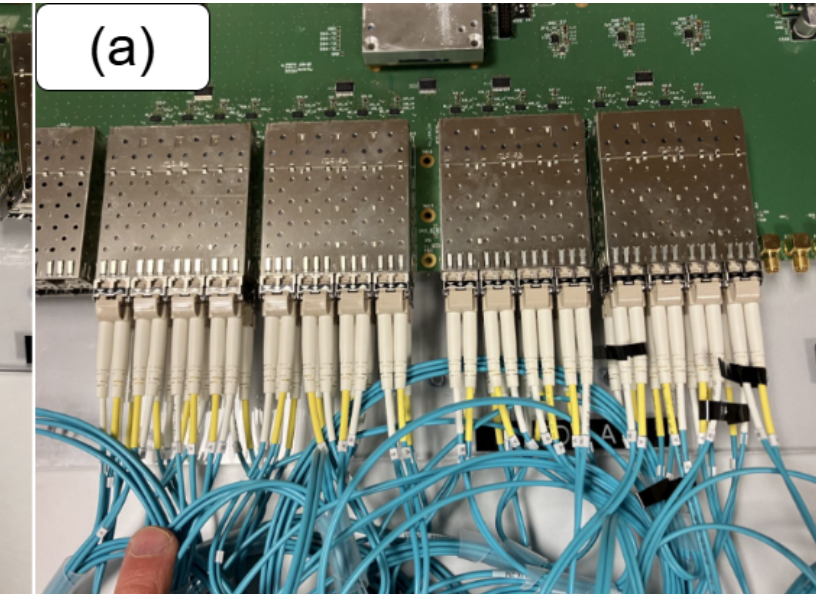
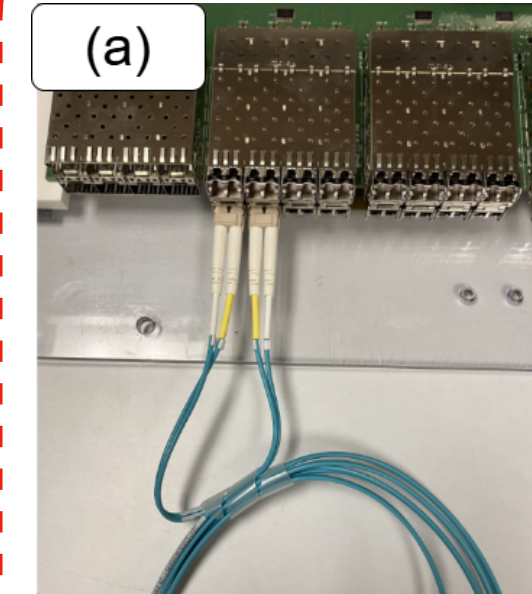
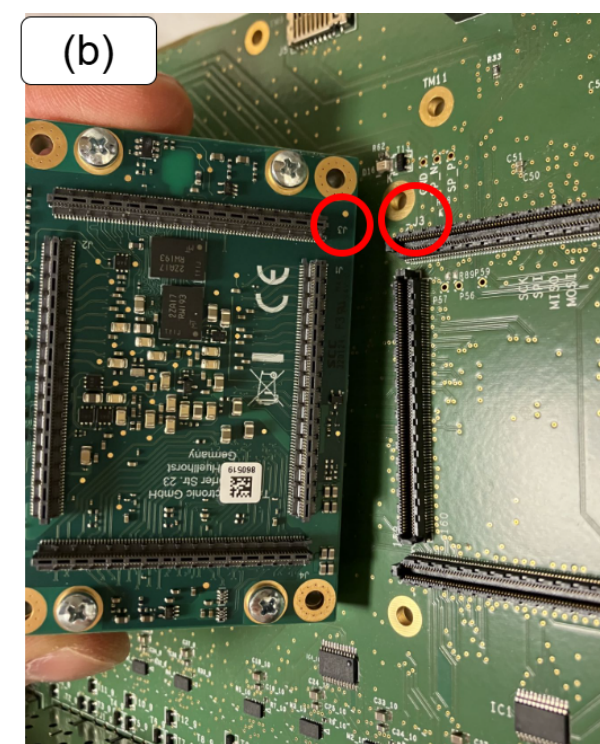
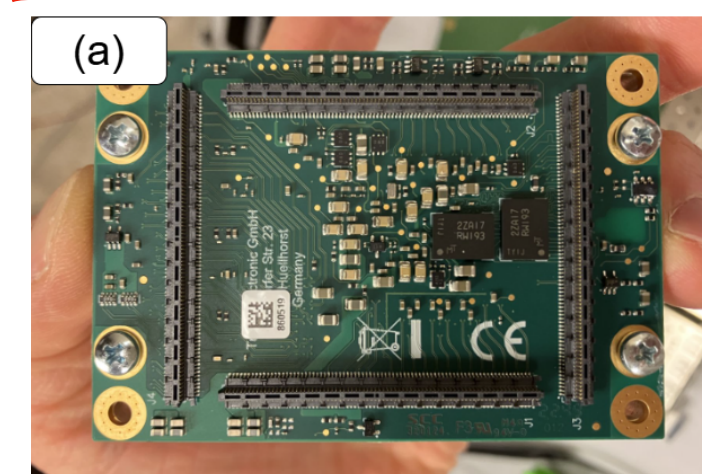


- Power supply connection
- Board switch on
- Voltages measurement

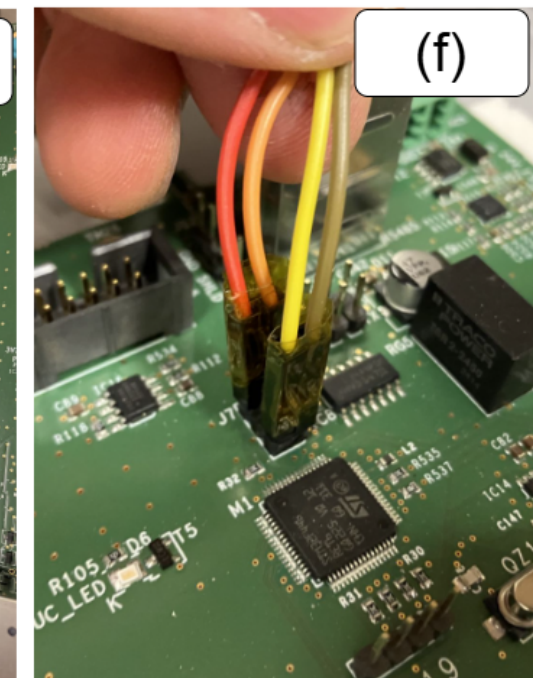
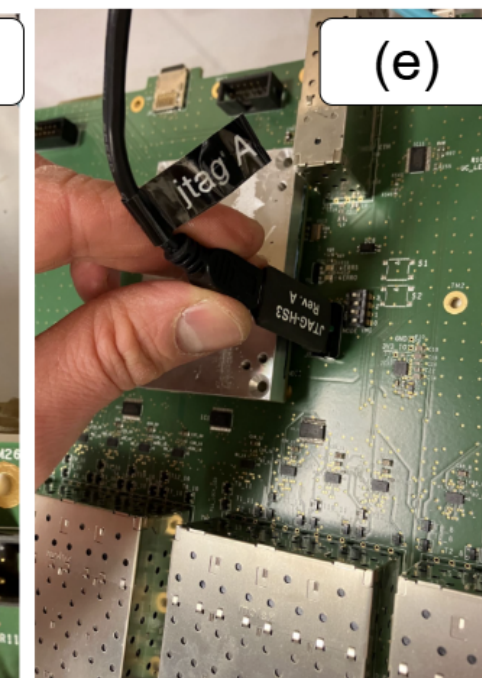
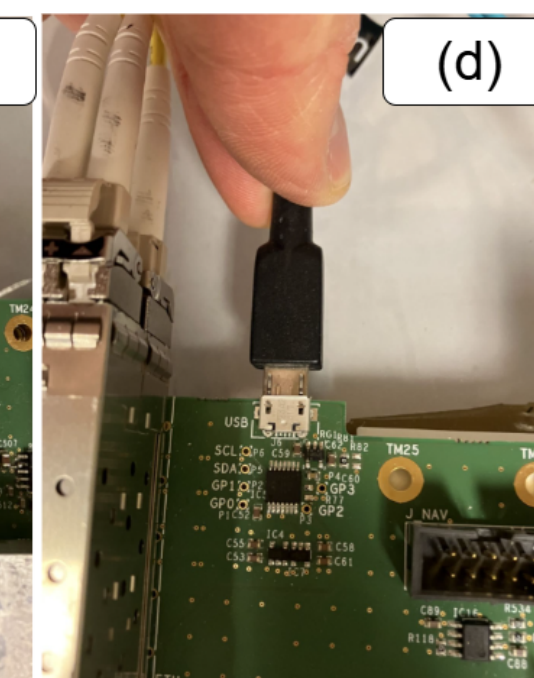
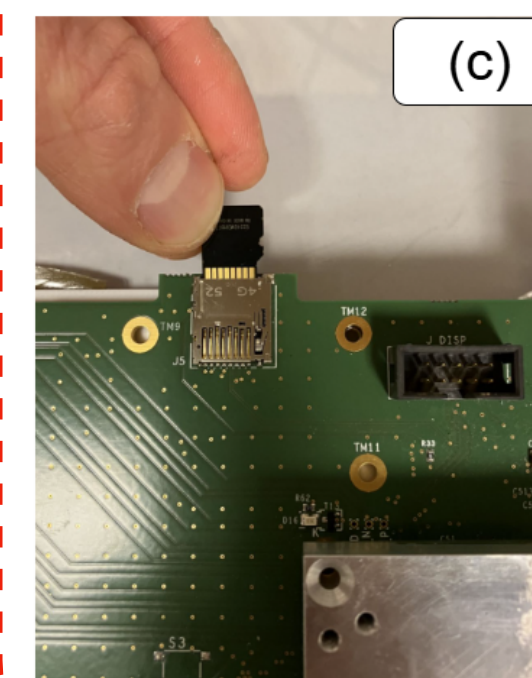


## 3 SFP mounting

## 4 FPGA installation

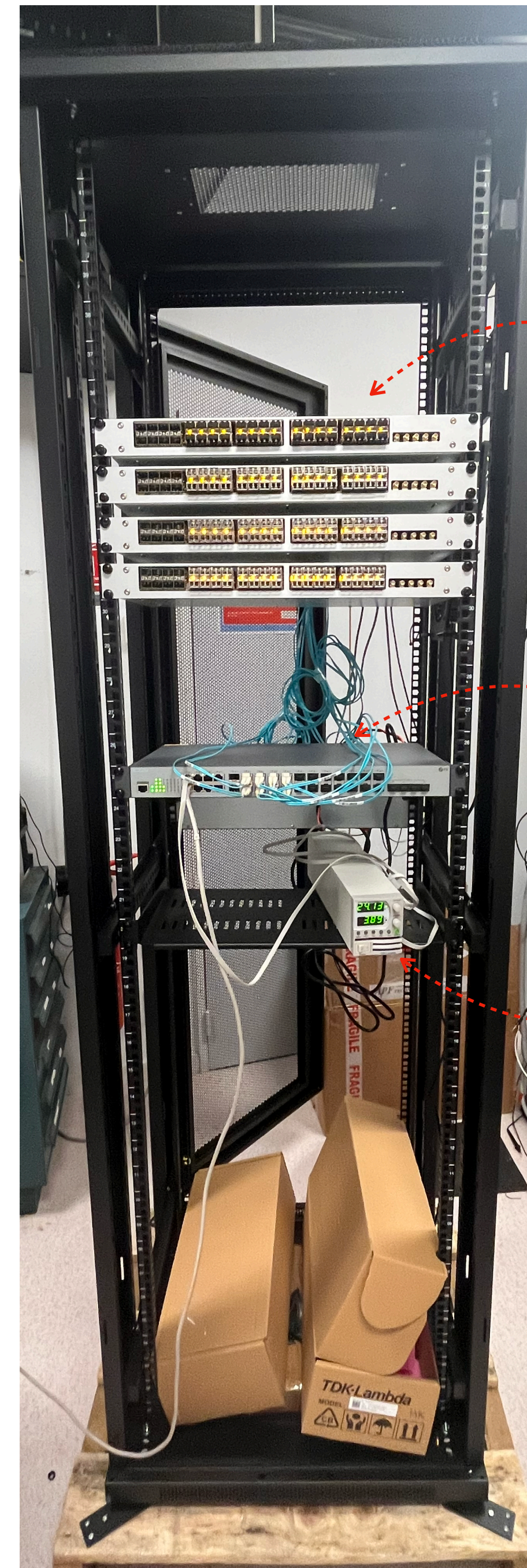
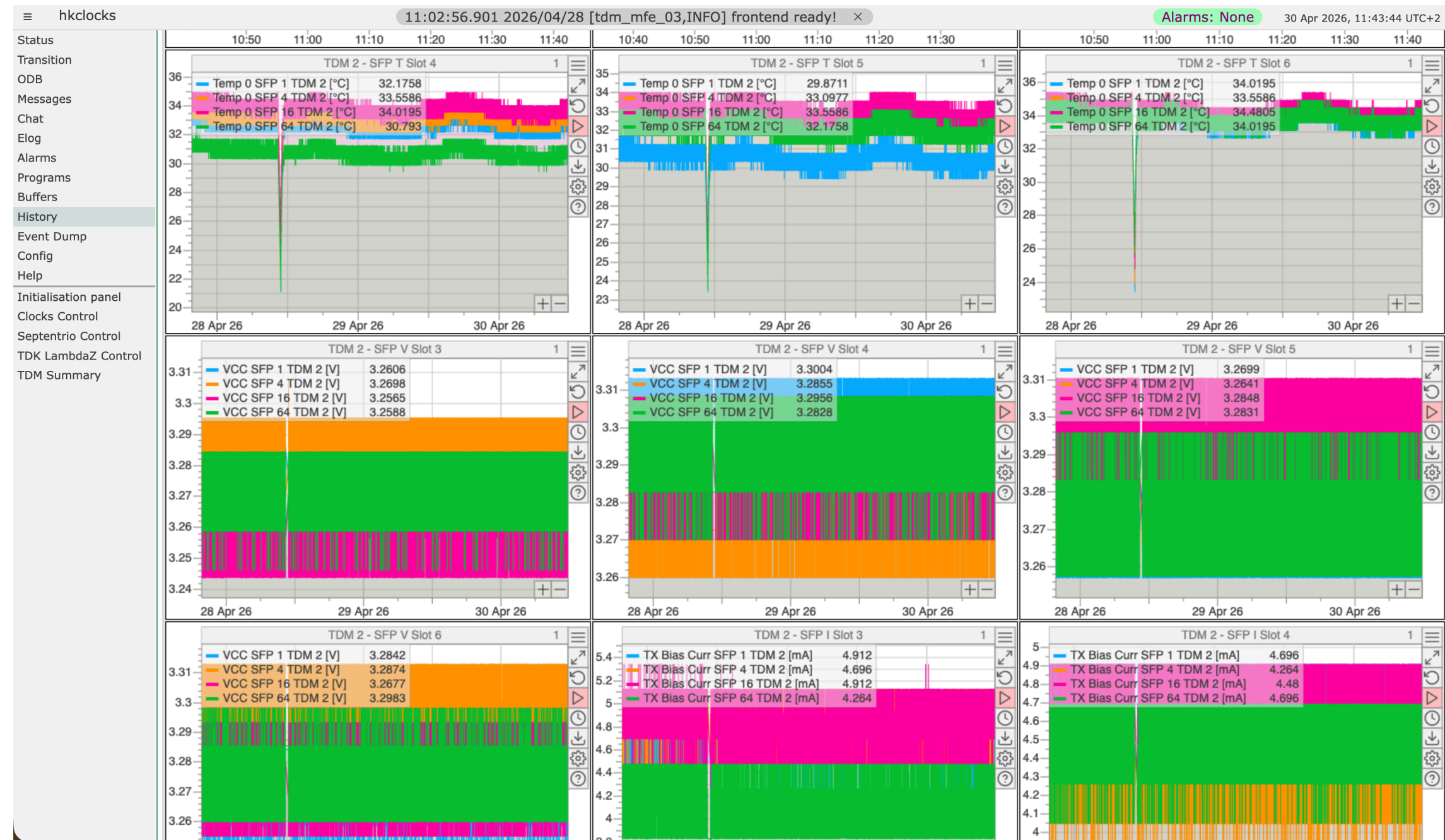


## 5 Interfaces connections



# Integration

- Fully equipped rack to mimic the configuration at Hyper-K
- 4 latest version TDMs up and running
- One TDK Lambda power supply
- One switch
- External fans for additional ventilation (exploits the heat pipe)
- Slow control via MIDAS to monitor temperature, voltages etc.



Time Distribution Modules

Switch

Power Supply TDK Lambda

Voltage Splitter

