

# Partage d'outils Opensource

## PeakRDL

<https://peakrdl-regblock-vhdl.readthedocs.io/en/latest/>

**Amaury HERVO**

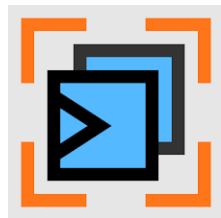
**01/06/2026**

## Fonctionnalités principales:

- Générer du code RTL
  - VHDL/System Verilog
  - Registres de contrôles et de status
  - Synthétisable
  - Compatibilité protocole d'interfaçage : AXI4, Avalon,...

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  - Registres de contrôles et de status
  - Synthétisable
  - Compatibilité protocole AXI4, Avallon,...
- Outil Python
  - open-source
  - SystemRDL (*Register Description Language*)



SystemRDL



PeakRDL



## Exemple :

### Description RDL

```
addrmap top_regmap {  
    default regwidth = 32;  
    default accesswidth = 32;  
  
    reg {  
        name = "LED managment";  
        field {  
            sw = rw;  
            hw = r;  
            desc = "enable/disable front-end LED";  
        } led [4] = 4'h0;  
    } led_reg @0x10;  
};
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$ peakrdl regblock-vhdl top_regmap.rdl --cpuif avalon-mm-flat -o . --addr-width 32
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SystemRDL



PeakRDL

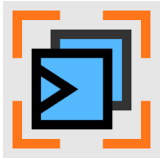
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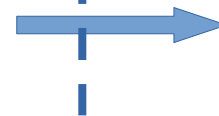
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SystemRDL



PeakRDL



```
-- Generated by PeakRDL-regblock-vhdl - A free and open-source VHDL generator
-- https://github.com/SystemRDL/PeakRDL-regblock-vhdl
entity top_regmap is
  port (
    clk : in std_logic;
    rst : in std_logic;

    avalon_read : in std_logic;
    avalon_write : in std_logic;
    avalon_waitrequest : out std_logic;
    avalon_address : in std_logic_vector(29 downto 0);
    avalon_writedata : in std_logic_vector(31 downto 0);
    avalon_byteenable : in std_logic_vector(3 downto 0);
    avalon_readdatavalid : out std_logic;
    avalon_writeresponsevalid : out std_logic;
    avalon_readdata : out std_logic_vector(31 downto 0);
    avalon_response : out std_logic_vector(1 downto 0));
    hwif_out : out top_regmap_out_t
  );
end entity top_regmap;

architecture rtl of top_regmap is*
  process(clk) begin
    if false then -- async reset
      field_storage.led_reg.led.value <= 4x"0";
    elsif rising_edge(clk) then
      if rst then -- sync reset
        field_storage.led_reg.led.value <= 4x"0";
      else
        if field_combo.led_reg.led.load_next then
          field_storage.led_reg.led.value <= field_combo.led_reg.led.next_q;
        end if;
      end if;
    end if;
  end process;
  hwif_out.led_reg.led.value = field_storage.led_reg.led.value;
end architecture rtl;
```

## Evolution de pratique:

### AVANT

Use	Connections	Name	Description	Ex...	Clock	Base
<input checked="" type="checkbox"/>		ipbus_avalon_mast...	ipbus_avalon_master			
		▶ m0	Avalon Memory Mapped Master	Dou	[clock]	
		▶ irq0	Interrupt Receiver	Dou		IRQ 0
		▶ ipb	Conduit	m...		
		▶ Mode_system	Conduit	m...		
		▶ clock	Clock Input	Dou	clock_in...	
		▶ reset	Reset Input	Dou	[clock]	
		▶ Cmde_stat	Conduit	c...	[clock]	
<input checked="" type="checkbox"/>		getibg_add1	PIO (Parallel I/O) Intel FPGA IP			
		▶ clk	Clock Input	Dou	clock_in...	
		▶ reset	Reset Input	Dou	[clk]	
		▶ s1	Avalon Memory Mapped Slave	Dou	[clk]	# 0x0000_1040
		▶ external_connection	Conduit	g...		
<input checked="" type="checkbox"/>		getibg_add0	PIO (Parallel I/O) Intel FPGA IP			
		▶ clk	Clock Input	Dou	clock_in...	
		▶ reset	Reset Input	Dou	[clk]	
		▶ s1	Avalon Memory Mapped Slave	Dou	[clk]	# 0x0000_1030
		▶ external_connection	Conduit	g...		

Pour chaque nouveaux registres :  
→ Ajout de PIO sur le bus avalon

Inconvénients :  
→ Maintenance  
→ Cartographie de registres

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### AVANT

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<input checked="" type="checkbox"/>		[-] ipbus_avalon_mast...	<b>ipbus_avalon_master</b>				
		[-] m0	Avalon Memory Mapped Master			[clock]	
		[-] irq0	Interrupt Receiver				IRQ 0
		[-] ipb	Conduit				
		[-] Mode_system	Conduit				
		[-] clock	Clock Input			clock_in...	
		[-] reset	Reset Input			[clock]	
		[-] Cmde_stat	Conduit			[clock]	
<input checked="" type="checkbox"/>		[-] getibg_add1	<b>PIO (Parallel I/O) Intel FPGA IP</b>				
		[-] clk	Clock Input			clock_in...	
		[-] reset	Reset Input			[clk]	
		[-] s1	Avalon Memory Mapped Slave			[clk]	# 0x0000_1040
		[-] external_connection	Conduit				
<input checked="" type="checkbox"/>		[-] getibg_add0	<b>PIO (Parallel I/O) Intel FPGA IP</b>				
		[-] clk	Clock Input			clock_in...	
	[-] reset	Reset Input			[clk]		
	[-] s1	Avalon Memory Mapped Slave			[clk]	# 0x0000_1030	
	[-] external_connection	Conduit					



### APRES

<input checked="" type="checkbox"/>		[-] ipbus_avalon_master	<b>ipbus_avalon_master</b>				
		[-] avm_m0	Avalon Memory Mapped Master				
		[-] clock	Clock Input		Double-click to	[clock]	
		[-] reset	Reset Input		Double-click to	clock_in...	
		[-] ipbus_read	Conduit		Double-click to	[clock]	
		[-] ipbus_write	Conduit		Double-click to	ipbus_read	
					Double-click to	[clock]	
					Double-click to	ipbus_write	
					Double-click to	[clock]	
					Double-click to	[clock]	
<input checked="" type="checkbox"/>	[-] top_regmap	<b>Avalon-MM Pipeline Bridge Intel ...</b>					
	[-] clk	Clock Input		Double-click to	clock_in...		
	[-] reset	Reset Input		Double-click to	[clk]		
	[-] s0	Avalon Memory Mapped Slave		Double-click to	[clk]	# 0x0008_0100	
	[-] m0	Avalon Memory Mapped Master		Double-click to	top_regmap		

Pour chaque nouveaux registres :  
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Pour chaque nouveaux registres :  
→ Ajout dans le fichier RDL

Avantages :  
→ Transparent dans le développement  
→ Suivi des registres centralisées

## Conclusions :

- Gain de temps de développement (toolchain automatique)
- Standardisation de description de registres
- Facilite la maintenance et le travail collaboratif
- Autres capacités : Export Doc (HTML), export ip-xact (XML)