Brief on Hdlmake

Workshop: Partage autour des logiciels Open-source et La gestion de conception

HDLMake

« Python framework for generating multi-purpose Makefiles for various FPGA projects and vendors. »

Open source tool from CERN for:

- Synthesis Makefile generation
- Simulation Makefile generation
- HDL parser and dependency solver
- GIT/SVN Support
- Multiple HDL Languages
- Multiple Tools (Xilinx, Altera, Microsemi, ...)
- Multiple Operating Systems

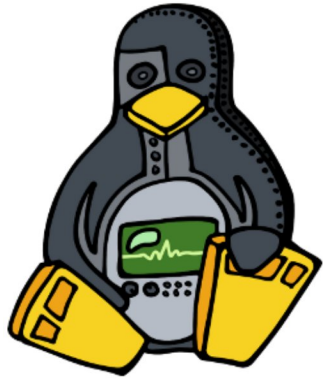
Python files tree structure to describe :

- Project properties
- Target FPGA
- Project files

In practice :

- Generate project and compile it in two commands hdlmake makefile && make
- Parse files to include only required files
- Manage sources from different vendors / targets in the same project
- Easy to include a sub-module library

https://gitlab.com/ohwr/project/hdl-make

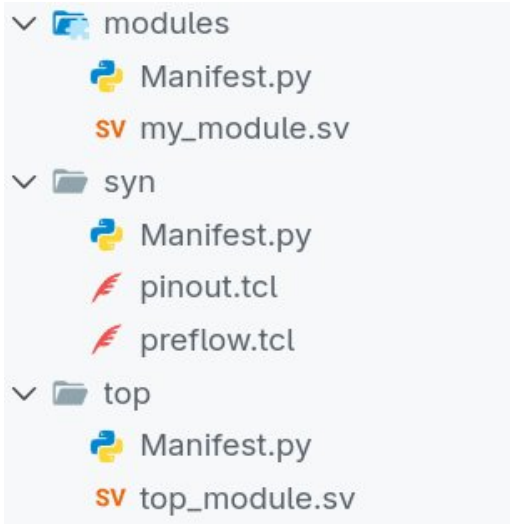


HDLMake

Basic example for Arria10 project synthesis

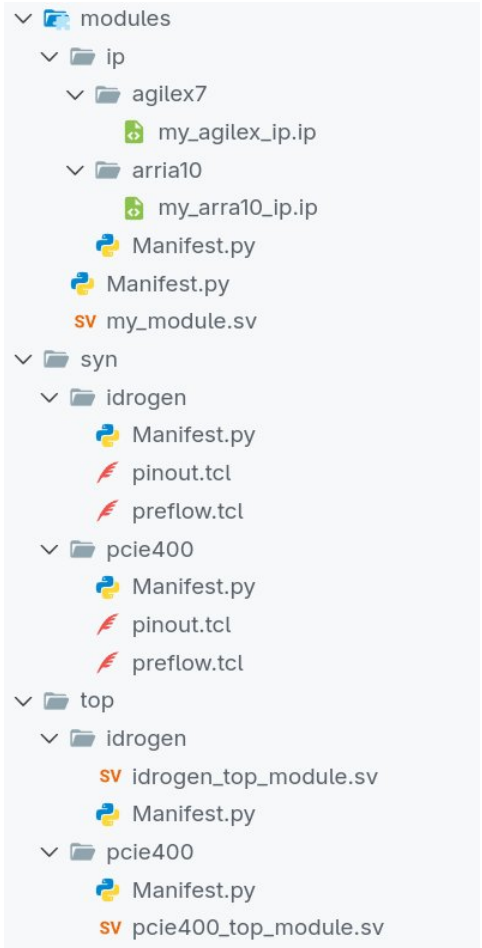
syn/Manifest.py

```
1  target = "altera"
2  action = "synthesis"
3
4  syn_tool = "quartus"
5  syn_family = "Arria 10"
6  syn_device = "10AX027H3"
7  syn_package = "F34"
8  syn_grade = "E2SG"
9
10 syn_top = "top_module"
11 syn_project = "project"
12
13 quartus_preflow = "preflow.tcl"
14
15 modules = {
16         "local": ["../top"]
17 }
```



Manage Project for multiple devices or vendor

```
1 if target=="altera":
2         modules = {"local" : "altera"}
3 elif target=="xilinx":
4         modules = {"local" : "xilinx"}
5
6 if syn_device[:3].upper() == "10A":
7         dirs.extend(["arria10"])
8 elif syn_device[:3].upper() == "AGM":
9         dirs.extend(["agilex"])
```



Register Description

Generate memory-map (registers, memory, sub-block, ...) code from text files.

Cheby

- Made at CERN (https://github.com/tgingold-cern/cheby)
- Use .cheby file format (based on YAML)
- Generate HDL code (VHDL or Verilog), C headers, documentation (HTML, Markdown, Latex, …)
- Multiple compatible bus : Wishbone, Avalon, AXI, APB bus

SystemRDL (PeakRDL)

- Standard defined by Accellera Systems Initiative (UVM, SystemC, IP-XACT): Intel, AMD, Cadence, ARM, … (https://github.com/SystemRDL/PeakRDL)
- Use .rdl file format
- Generate HDL code (SystemVerilog or VHDL(plugin)), C headers, documentation, UVM model, IP-XACT XML
- Can be extended with your own Importer/Exporter

More tools and libraries

FPGA Developers' Forum (FDF) held at CERN (27 – 29 May 2026)

FDF propose a list of tools for FPGA development (https://fpga.web.cern.ch/fdf-tools-and-libraries/)

- RgGen (Code generation tool for control/status registers) ;
- FWK (Creation and build processes for FPGA) ;
- Cheby (Code generator from a register map description) ;
- Veryl (Hardware description language) ;
- OpenLogic (FPGA Standard Library, vendor Independent) ;
- Surfer (Waveform viewer) ;
- ...