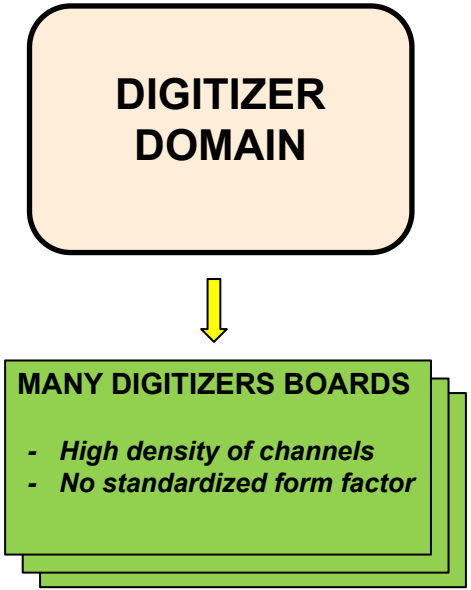
FASTER3 Hardware

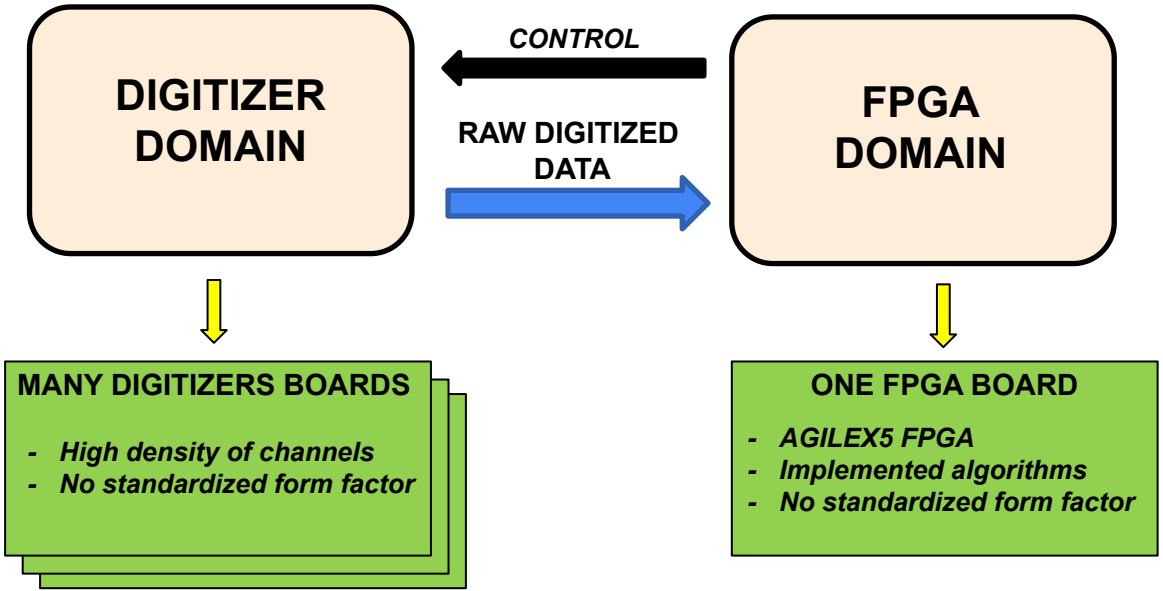
- Overall view
- Main characteristics of the Digitizers
- Focus on the FPGA board
- Interactions with the CPU board and possibilites

OVERALL HARDWARE ARCHITECTURE

Base overview :

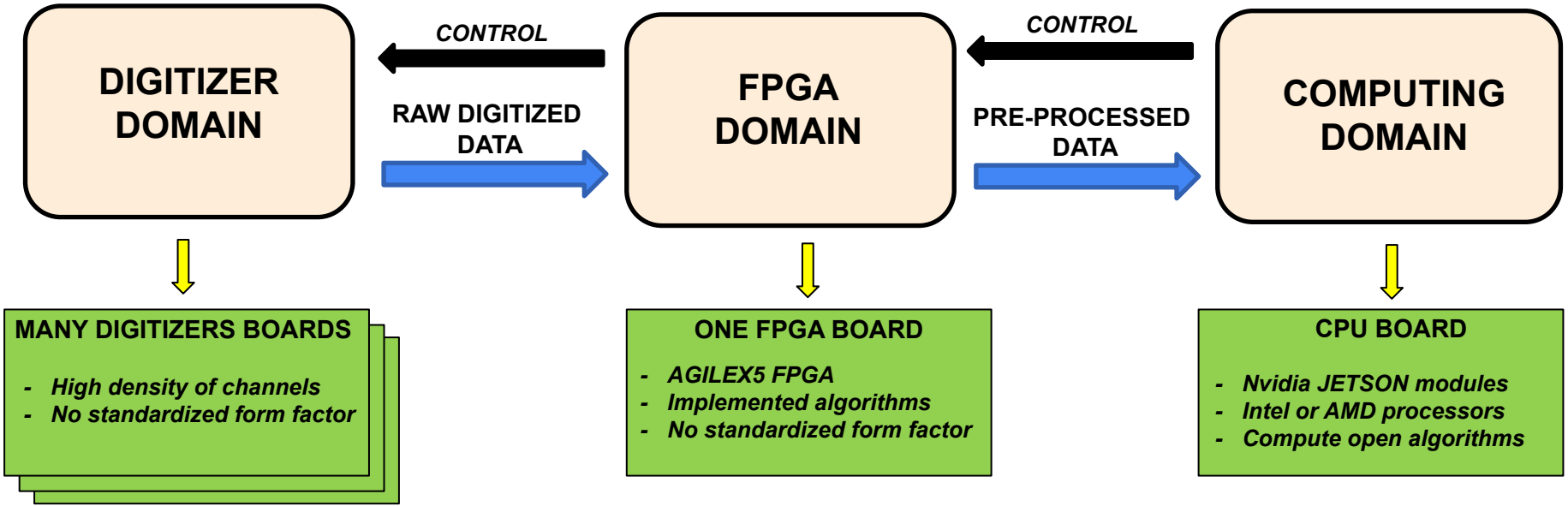


Base overview :



OVERALL HARDWARE ARCHITECTURE

Base overview :



Electronic parameters by digitizer board :

FASTER2 → FASTER3

	RESOLUTION	
	MOSHAR	HYDRA
Channels	4	24 (8 for prototype)
Sampling rate	14bits@125MSps	16bits@125MSps
ENOB target	12	12,5
Bandwidth	25MHz	25MHz

Electronic parameters by digitizer board :

FASTER2 → FASTER3

	TIMING		
	CARAS	PEGASUS	VIRGO
Channels	2	16 (4 for prototype)	8 (4 for prototype)
Sampling rate	12bits@500MSps	16bits@1,5GSps	12bits@4GSps
ENOB target	10,6	11	9
Bandwidth	100MHz	300MHz	300MHz

Mechanical outlines :

FASTER2 > FASTER3

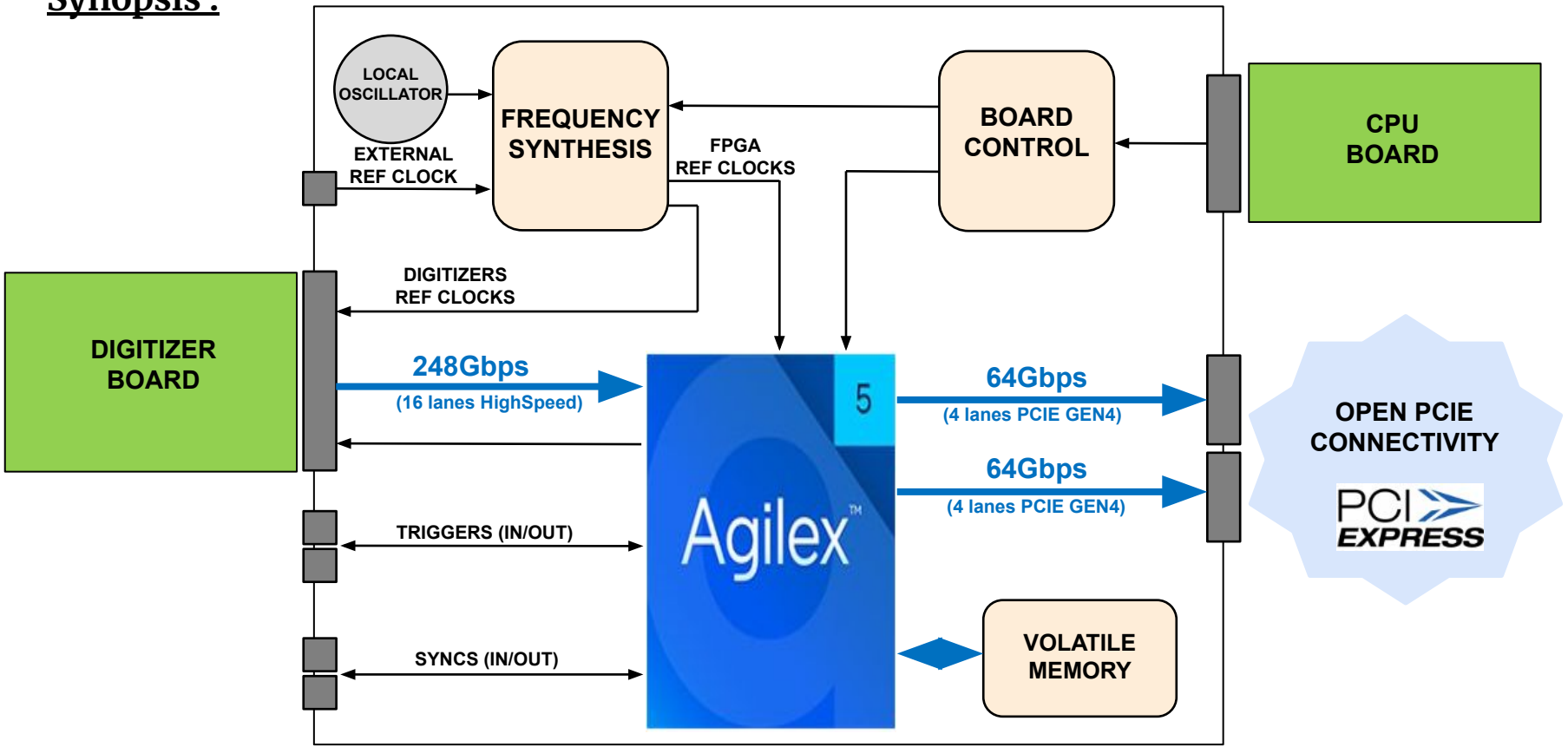
MicroTCA standard

- CARAS
- MOSHAR

Open standard

- HYDRA
- PEGASUS
- VIRGO

Synopsis :


LOCAL OSCILLATOR
EXTERNAL REF CLOCK
FREQUENCY SYNTHESIS
FPGA REF CLOCKS
BOARD CONTROL
CPU BOARD
DIGITIZERS REF CLOCKS
DIGITIZER BOARD
248Gbps
(16 lanes HighSpeed)
5
Agilex™
64Gbps
(4 lanes PCIE GEN4)
64Gbps
(4 lanes PCIE GEN4)
OPEN PCIE CONNECTIVITY
PCI EXPRESS
TRIGGERS (IN/OUT)
SYNCS (IN/OUT)
VOLATILE MEMORY

Capabilities :

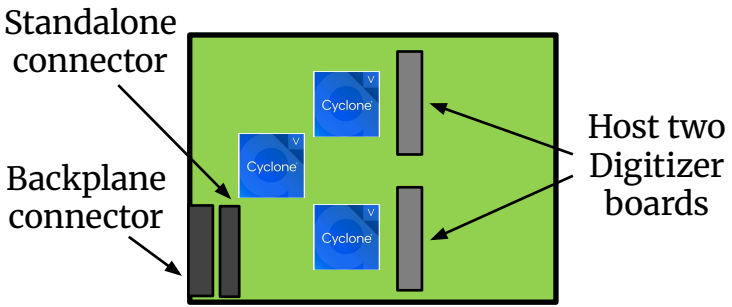
	FASTER2	FASTER3
Digitizer bitrate	6Gbps	248Gbps
Output bitrate	1Gbps	128Gbps
Volatile memory (capacity @ bitrate)	1Gb @ 12,8Gbps	128Gb @ 477Gbps
Synchronization	10 Mhz clock + T0	WR or SMART protocol

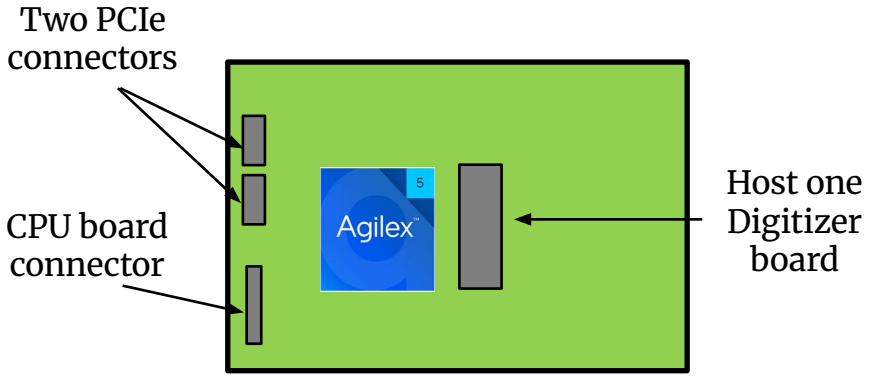
Mechanical outlines :

FASTER2 → FASTER3

MicroTCA standard

Open standard





JETSON DEVKIT INTERFACES :

FPGA BOARD

CONTROL
(SPI, I2C, GPIOs)

NX ORIN MODULE

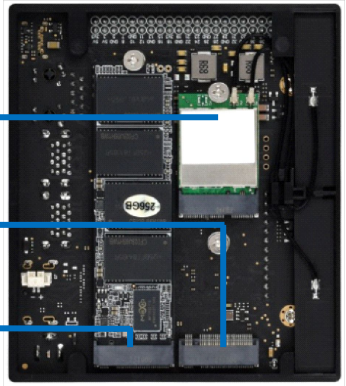
TOP VIEW

1Gbps

ETHERNET CONTROL

EXTERNAL PERIPHERALS
(USB, DP/HDMI)

BOT VIEW



OPEN PCIE CONNECTIVITY

PCI EXPRESS

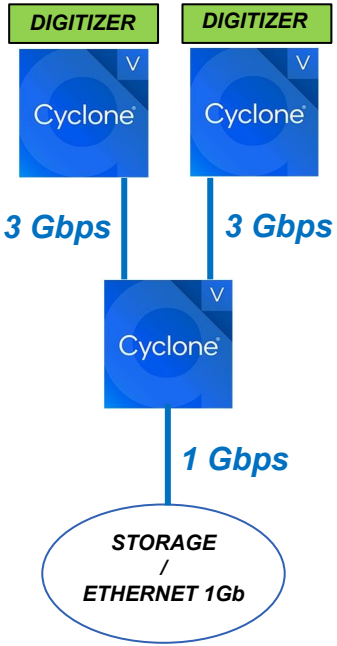
32Gbps
(2 lanes PCIE GEN4)

16Gbps
(1 lane PCIE GEN4)

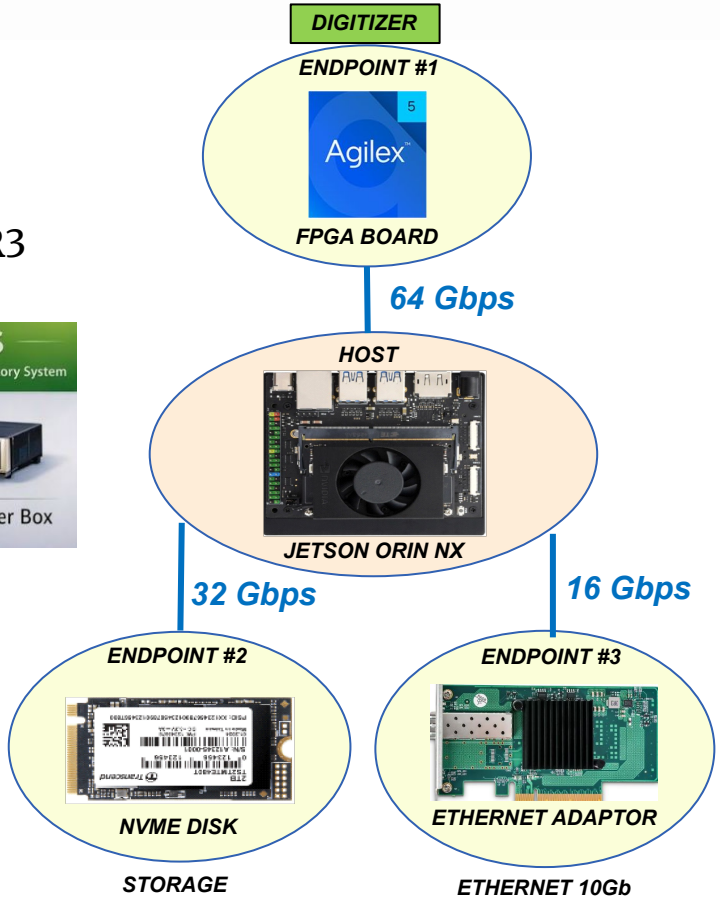
64Gbps
(4 lanes PCIE GEN4)

OPEN PCIE CONNECTIVITY

BASIC TOPOLOGY :



FASTER2 › FASTER3



ADVANCED PCIE TOPOLOGY :

HOST

JETSON ORIN NX

64 Gbps

PCIE SWITCH

128 Gbps

ENDPOINT #1

Agilex

FPGA BOARD

DIGITIZER

64 Gbps

ENDPOINT #2

NVME DISK

STORAGE

128 Gbps

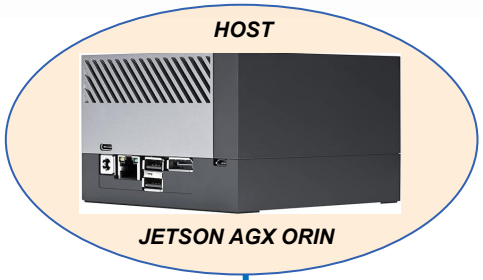
ENDPOINT #3

ETHERNET ADAPTOR

ETHERNET 100Gb

OPEN PCIE CONNECTIVITY

FUTURE UPGRADE :



256 Gbps

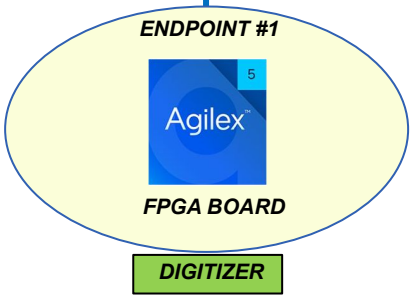
PCIE SWITCH

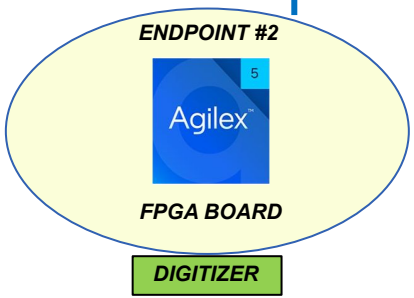
128 Gbps

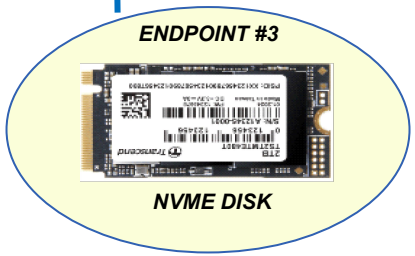
128 Gbps

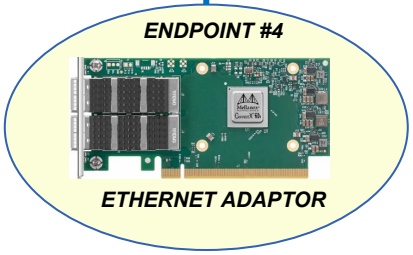
64 Gbps

256 Gbps

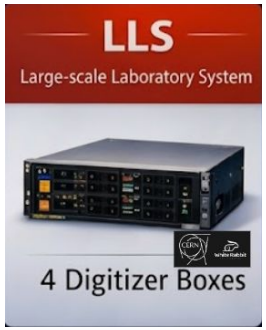








FUTURE UPGRADE :



Massive Throughput: From 12 to 86 cores (24 to 172) threads.
Extreme I/O: 80 PCIe 5.0 lanes for maximum high-speed connectivity.

2 x

2 x — 128 Gbps — ENDPOINT #1 — FPGA BOARD — DIGITIZER

2 x — 128 Gbps — ENDPOINT #2 — FPGA BOARD — DIGITIZER

128 Gbps — ENDPOINT #3 — NVME DISK — STORAGE

n x

400 Gbps — ENDPOINT #4 — ETHERNET ADAPTOR — ETHERNET 400Gb

FASTER3 Hardware

- Number of channels increasement
- Higher data throughput
- Open algorithms possibilities
- Scalable configurations

THANKS FOR LISTENING

ANY QUESTIONS ?