FASTER DAY

EnsiCaen Site B@31 Mars 2026

Electronic Timestamp alignment

- What’s wrong?
- Technical solution
- Implementation and results
- Conclusion

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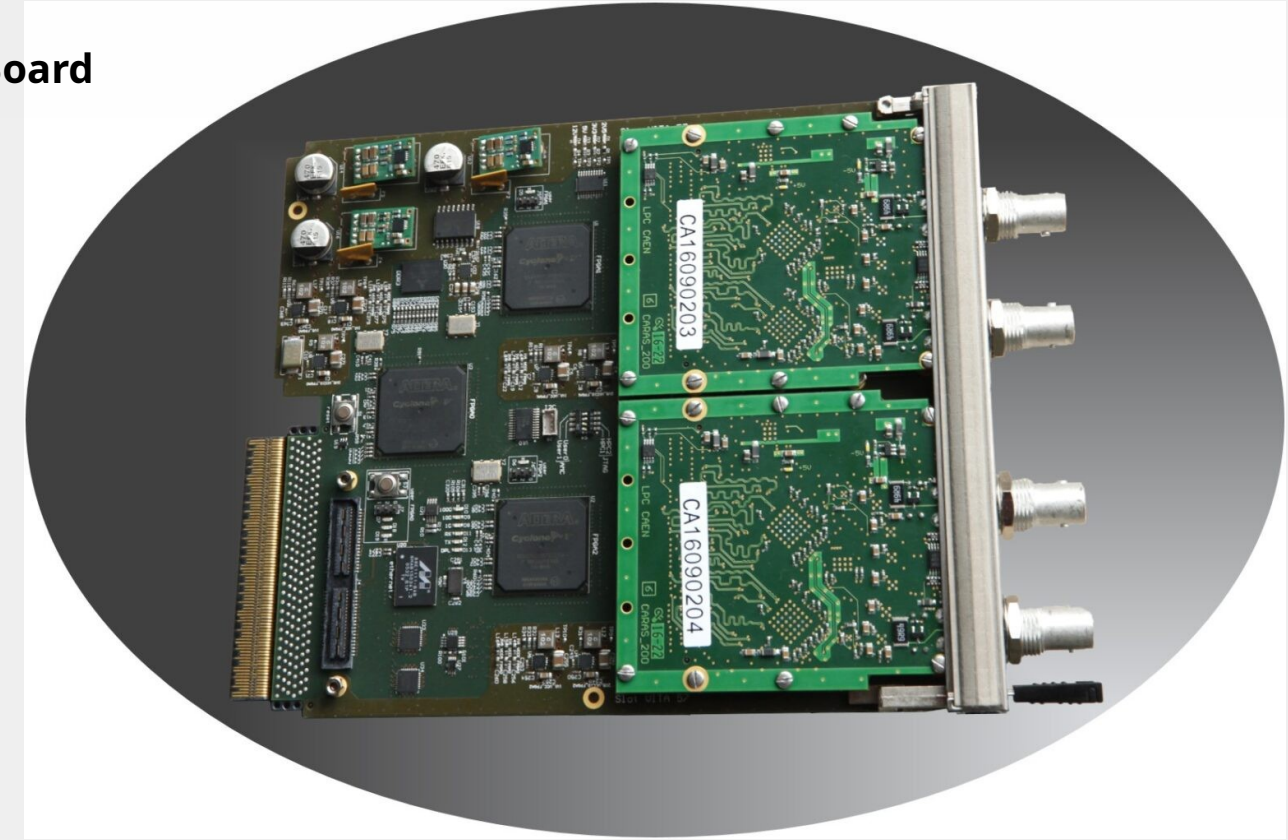
What's wrong?

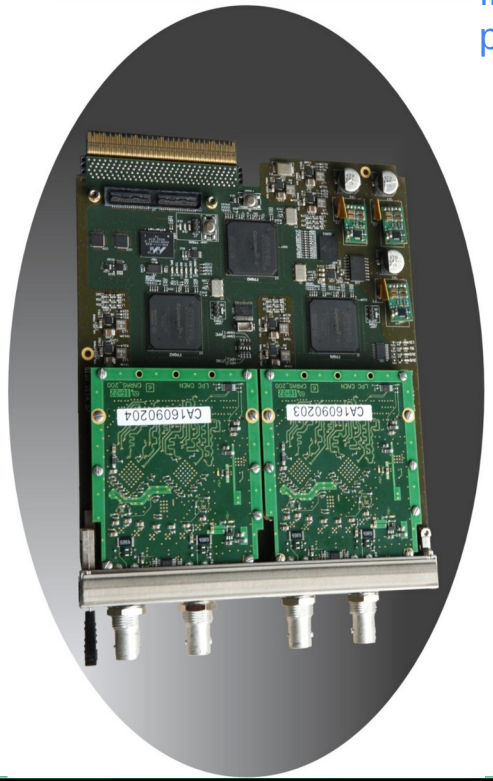
Current AMC mother Board

3 FPGA

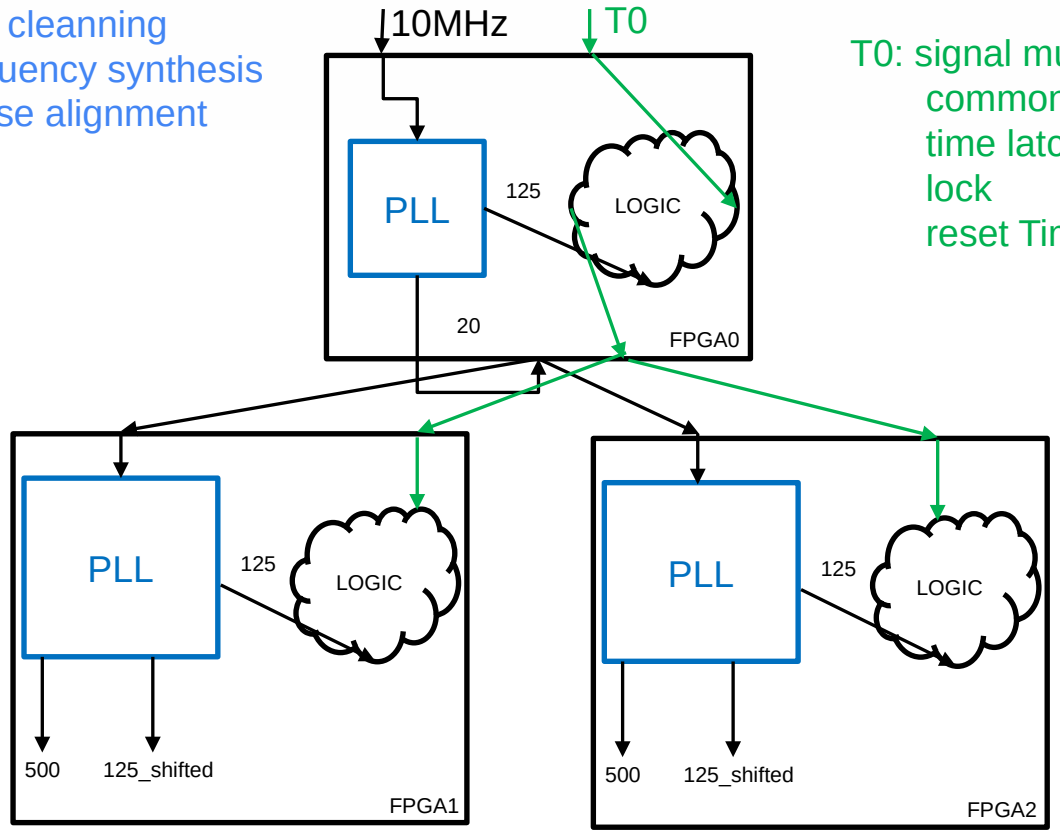


What's wrong?

Clock and T0 tree



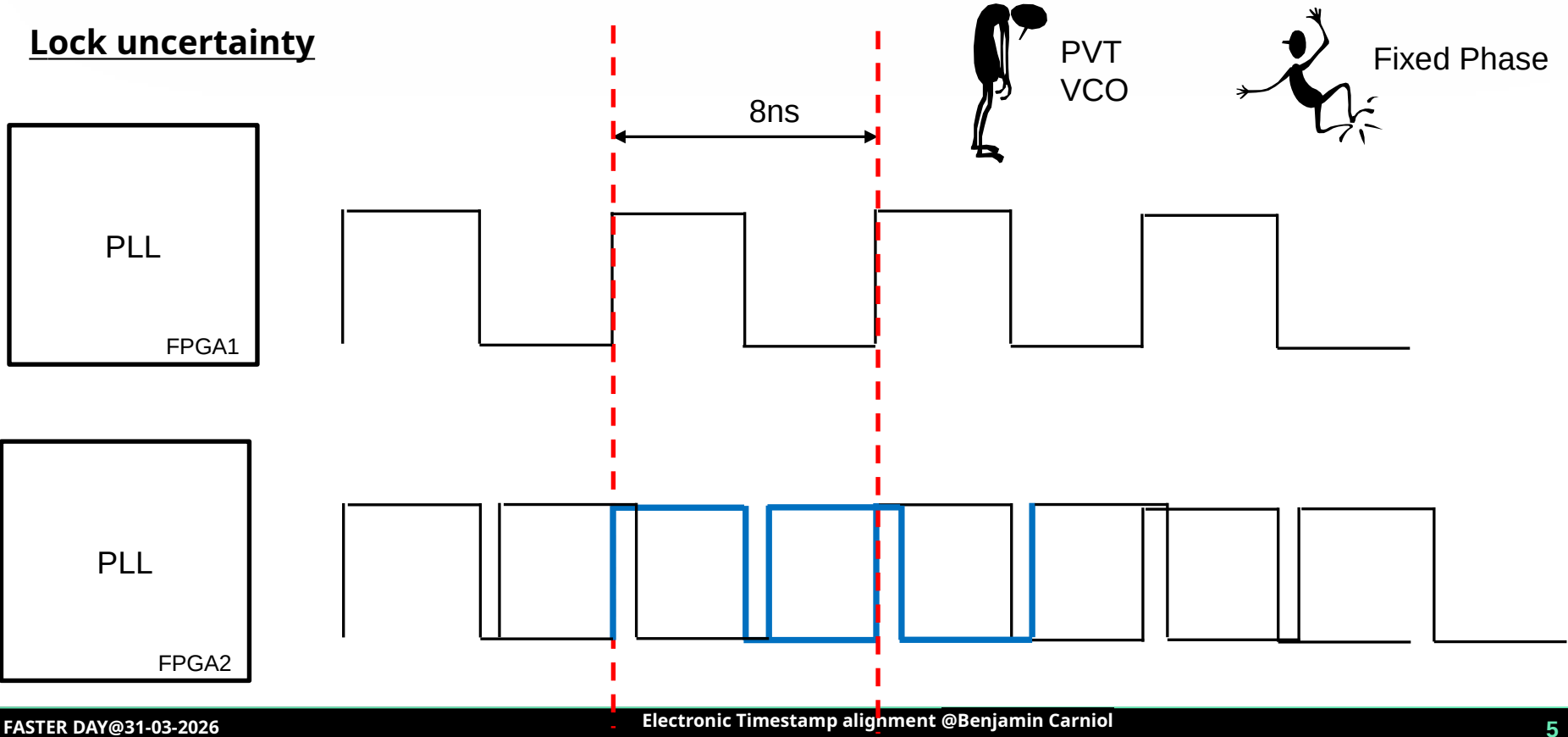
PLL: jitter cleanning
frequency synthesis
phase alignment



T0: signal multi function
common start
time latch
lock
reset TimeStamp

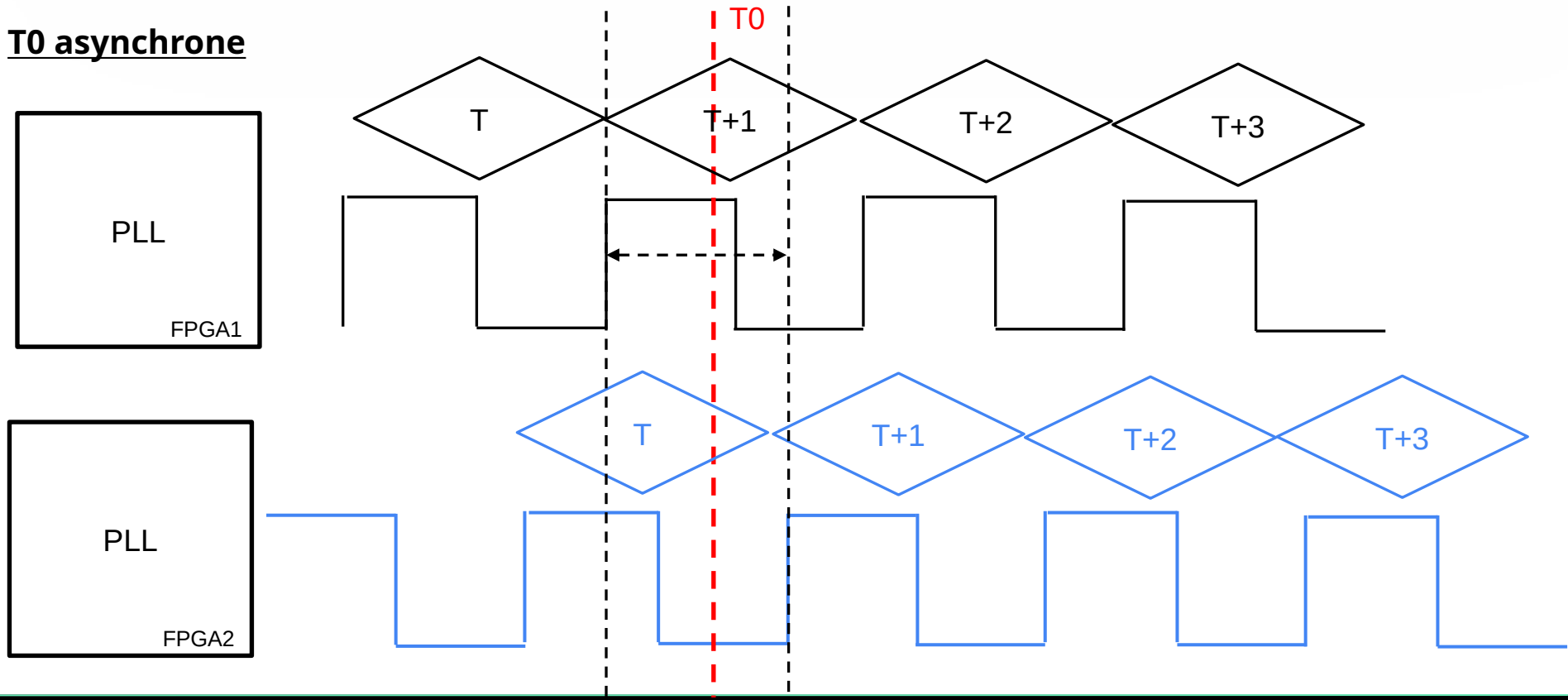
What's wrong?

Lock uncertainty



What's wrong?

T0 asynchrone



Least Common Multiple (T1,T2)= 200ns

T1=100ns
T2=8ns

Temporal Coincidence Point
Phase Alignment Window
Deterministic Start-up
Reference-Locked Trigger

The PPCM method shifts the problem from **Analog Uncertainty** (PLL Lock) to **Digital Determinism** (Mathematical Coincidence). We are not just resetting a counter; we are aligning a system to a universal time reference."

LCM (T1,T2)= 200ns

Tested Solution

Counter 500MHz
PLL phase alignment
Pulse stretcher

adopted Solution

Counter 500MHz
Ring counter architecture

Minimize propagation delay and bypass combinatorial logic bottleneck

Agnostic(works on any Flip-Flop)
Optimized for all families

Performance counter

ArriaGx : 533 MHz
Cyclone III : 512 MHz
Cyclone V : 650 MHz
Arria10 : 713MHz

Conclusion

Zero Drift Synchronization
Hardware Robustness
Scalability

TimeStamp offset : 260µs@8ns

Questions?