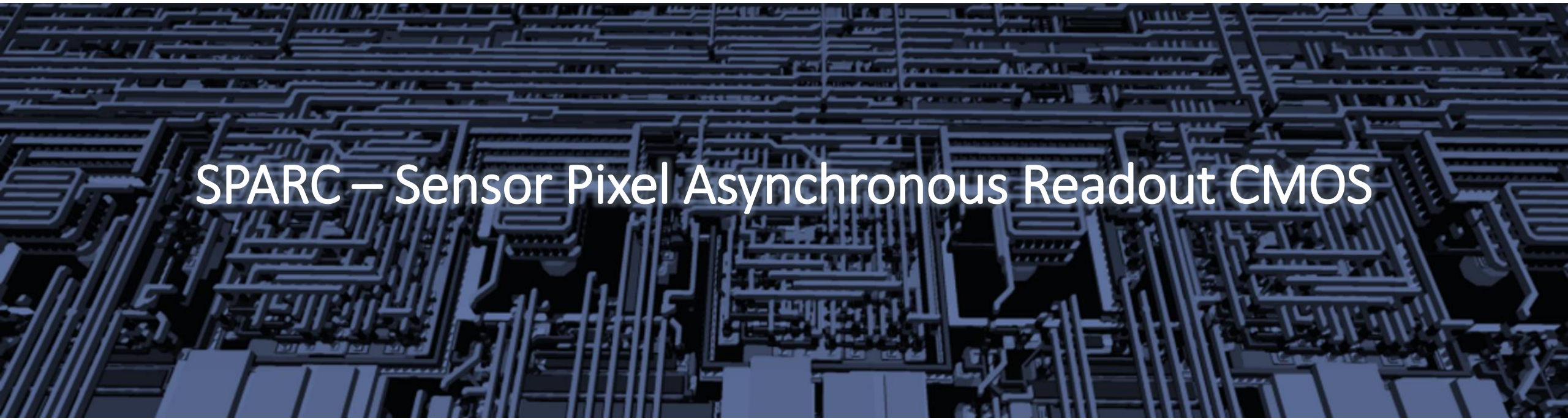


SPARC – Sensor Pixel Asynchronous Readout CMOS

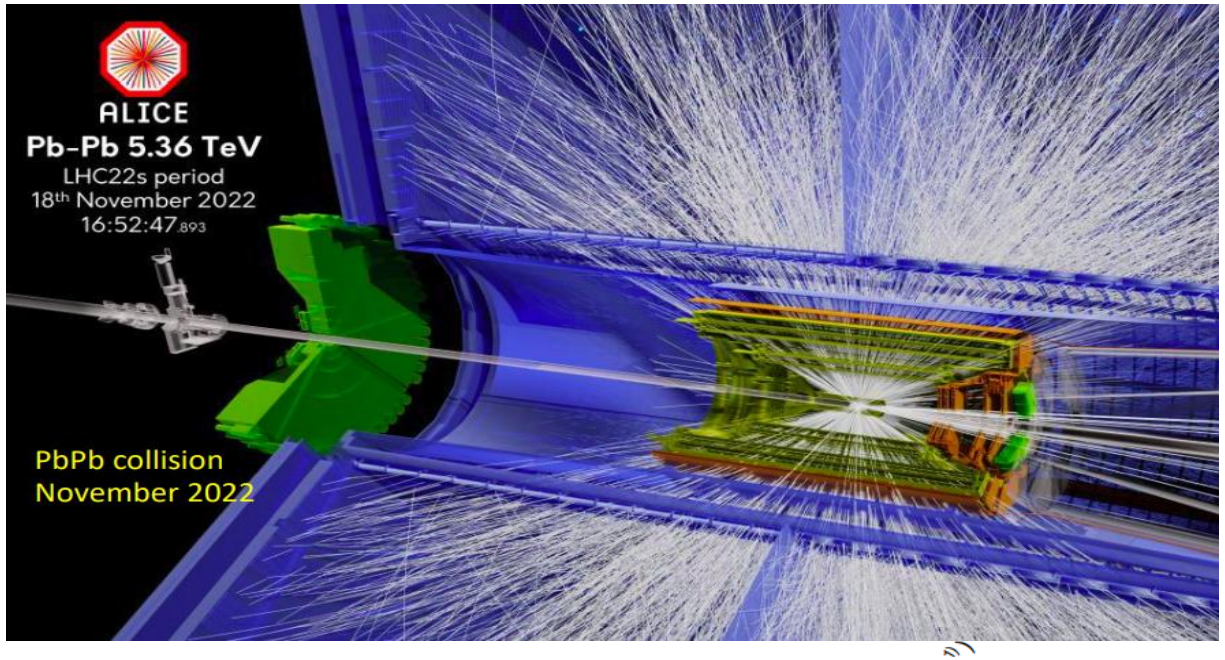
Camille Fournier *on the behalf of SPARC core team*

Phd student, Institut Pluridisciplinaire Hubert Curien (IPHC)

Subatomic Research Department, C4PI team

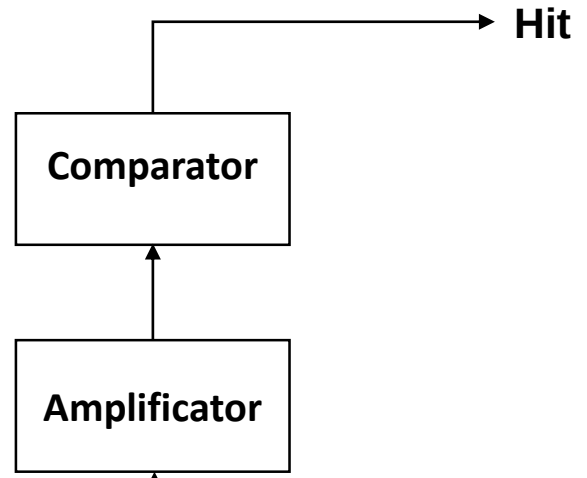
This work was supported by IdEx Unistra (ANR 10 IDEX 0002), and by SFRI STRAT'US project (ANR 20 SFRI 0012) and EUR QMAT ANR-17-EURE-0024.

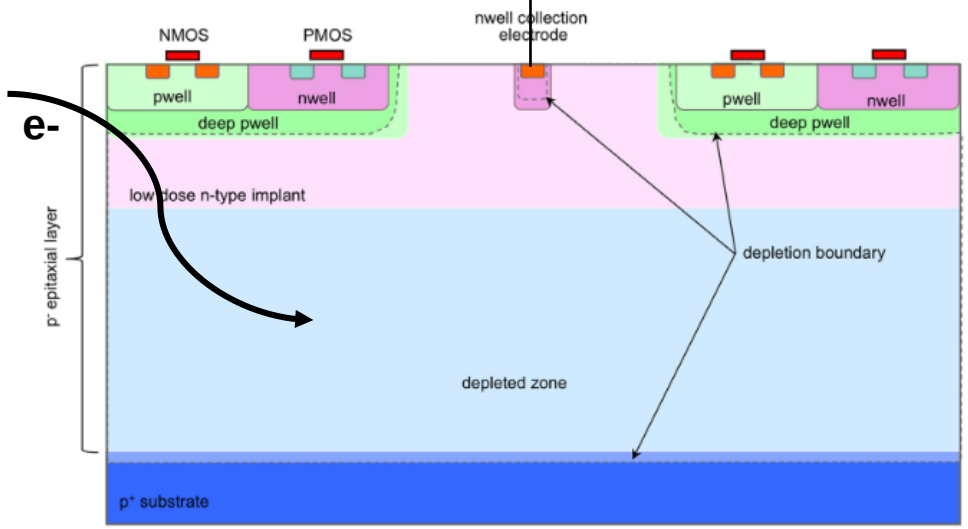
Context



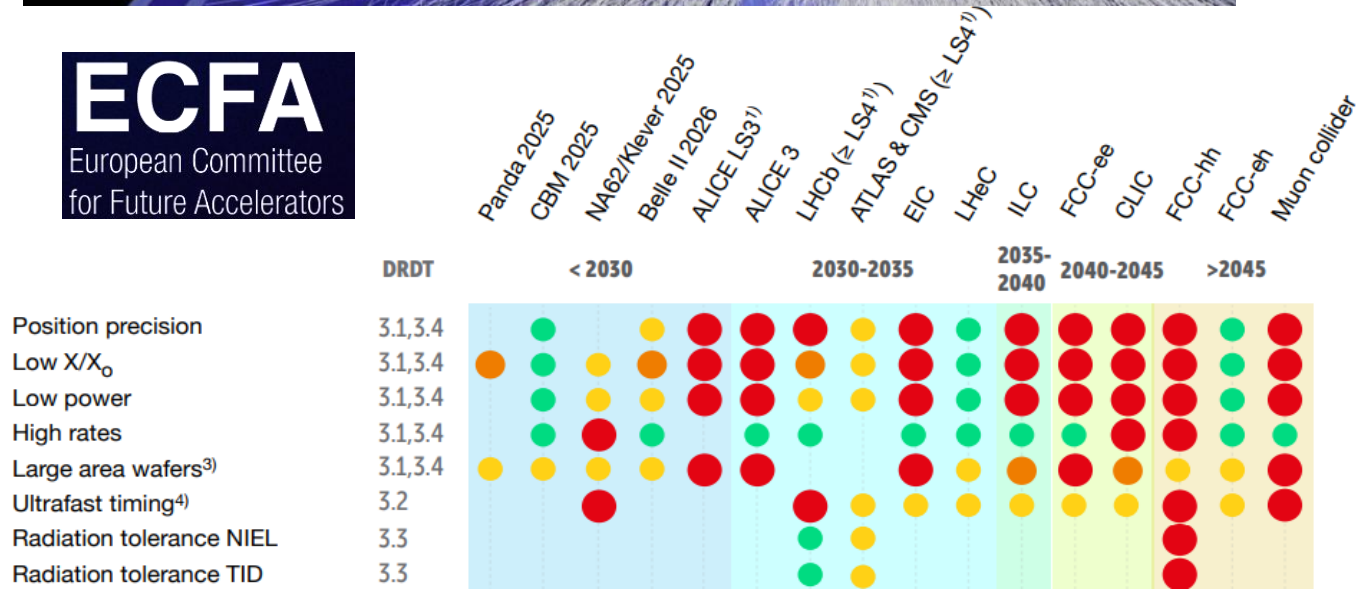
MAPS : Monolithic Active Pixel Sensors

- Detection and readout on the same chip
- retrieve the exact hit coordinates within the pixel matrix
- Established in the CERN ALICE ITS2 experiment since 2021 (ALPIDE sensors)





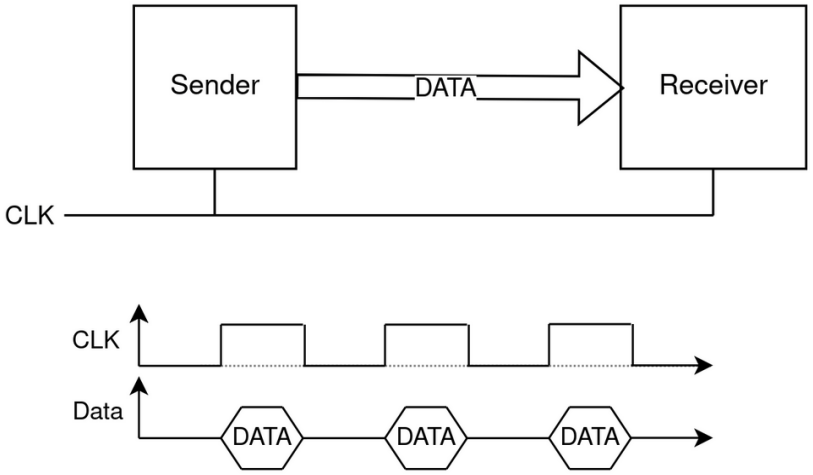
ECFA
European Committee for Future Accelerators



Asynchronous readout reminders

Synchronous

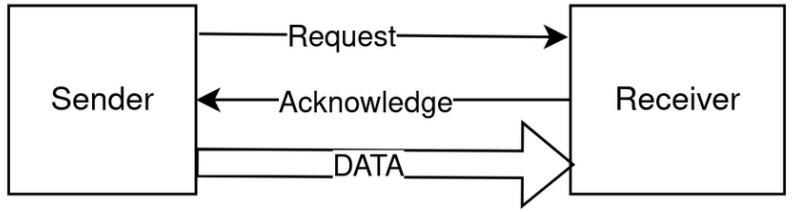
Data are read at regular intervals, synchronized to a common clock running at a specific frequency

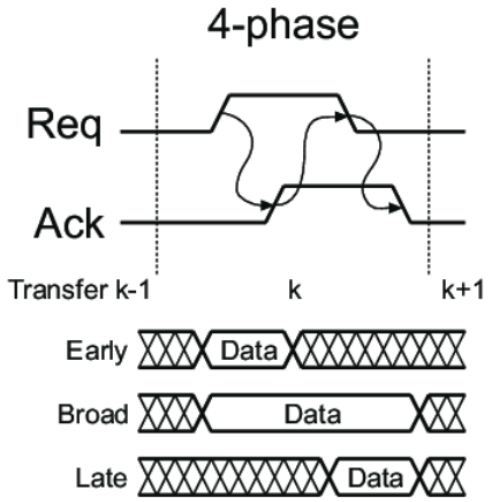


(-) Continuous readout (Wastes bandwidth)
(-) Sensitive to synchronization issues
(-) Complex clock distribution (increases latency)

Asynchronous

Data are read immediately when they become available through a handshake protocol





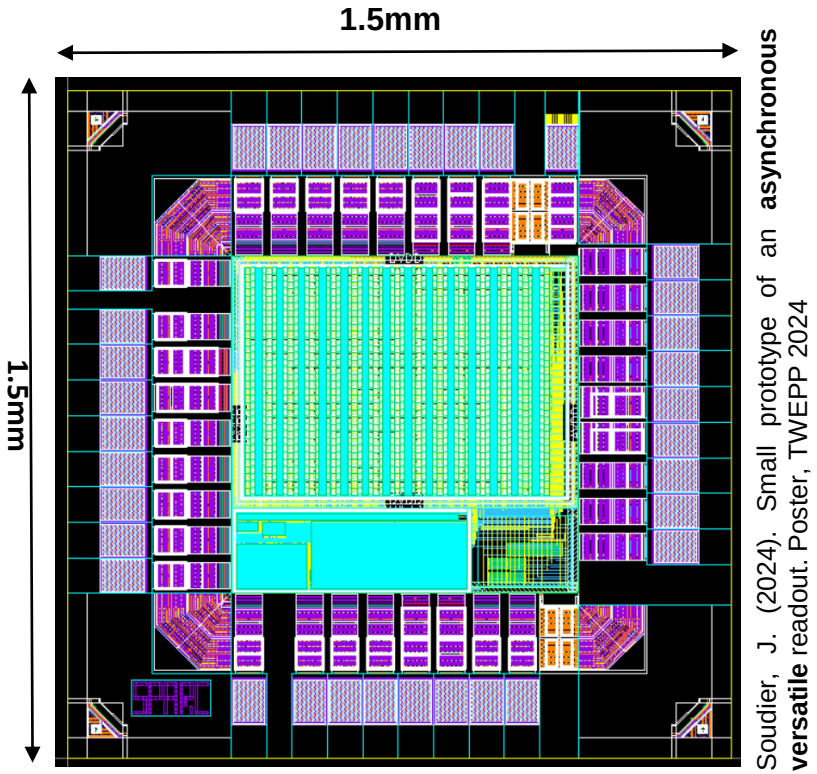
Carlsson, J., Palmkvist, K., & Wanhammar, L. (2003). An 8-by-8 point 2D DCT processor based on the GALS approach. In IEEE NorChip Conference

S = sender
R= receiver

1. **S issues data and sets Req high**
2. **R absorbs the data and sets ack high**
3. **S respond by taking Req low**
4. **R put Ack low**

(+) Data-driven readout

SPARC – Sensor Pixel Asynchronous Readout CMOS



Soudier, J. (2024). Small prototype of an **asynchronous** **versatile** readout. Poster, TWEPP 2024

Layout of SPARC *1.5x1.5 mm*
build in a TPSCo 65nm

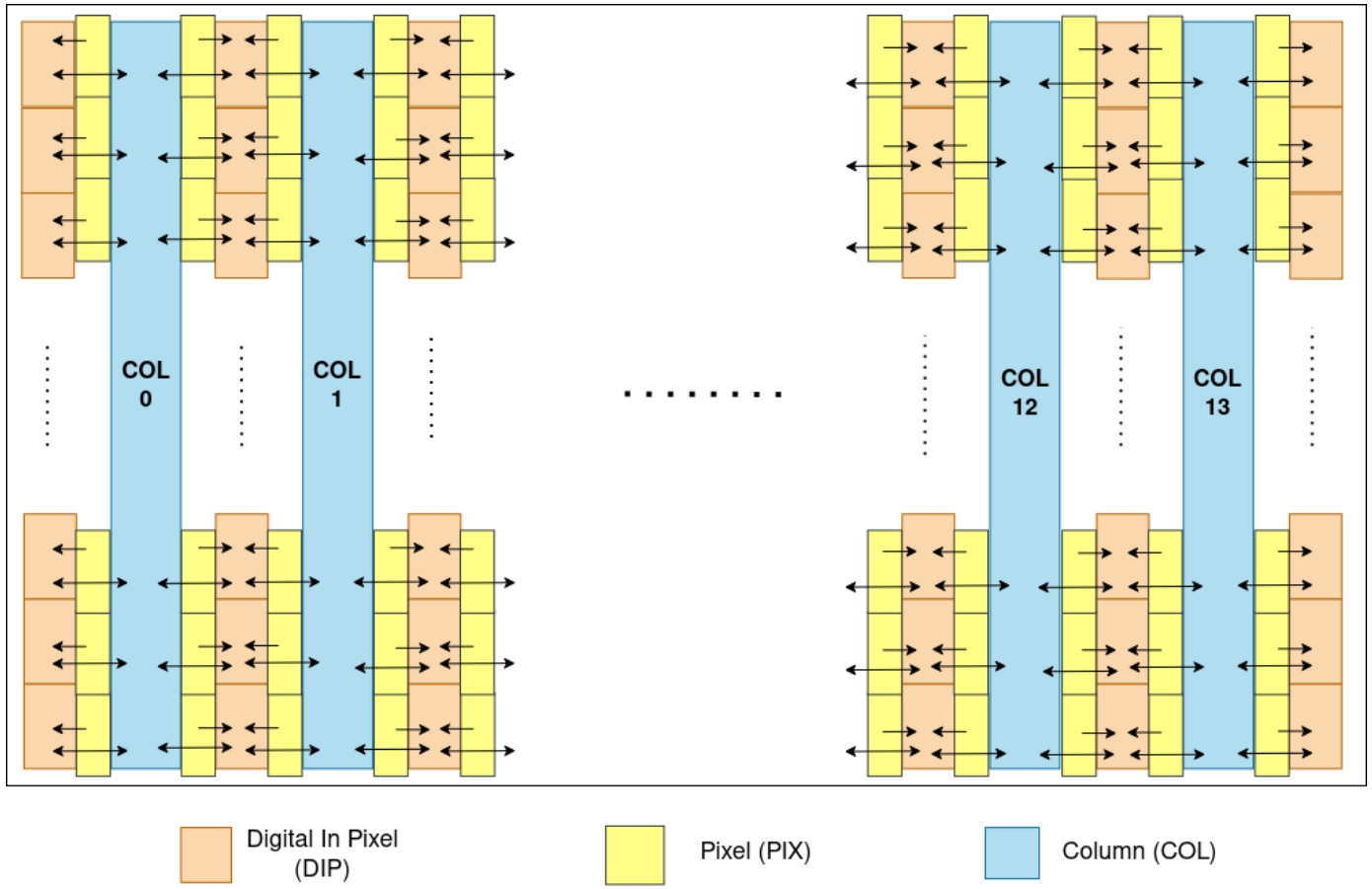
32x28 pixel matrix with a pixel pitch of **25x16** um²

The front-end is directly borrowed from CERN's DPTS

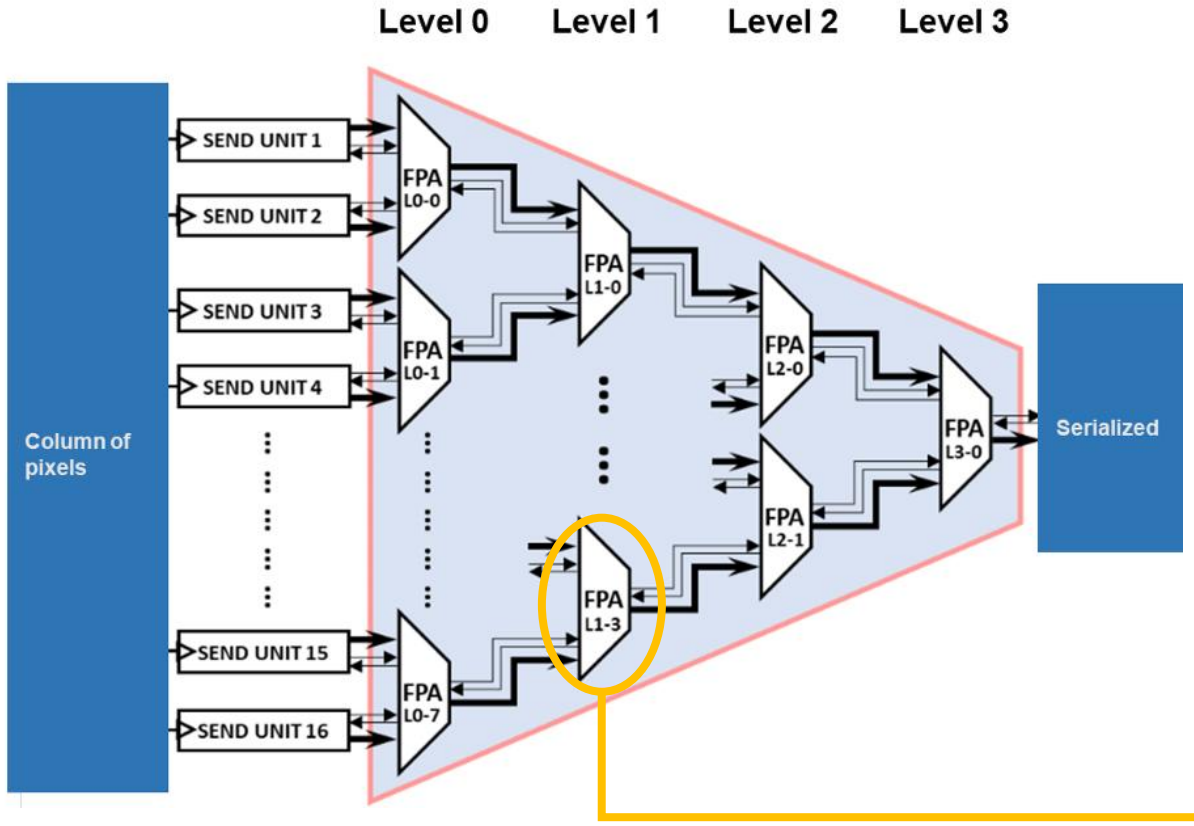
13 double columns of readout :

- 4 for 2-to-1
- 4 for 4-to-1
- 3 for 16-to-1 + 4-to-1
- 3 for 64-to-1

Enable a comparative evaluation of arbitration granularity and its impact on readout performance

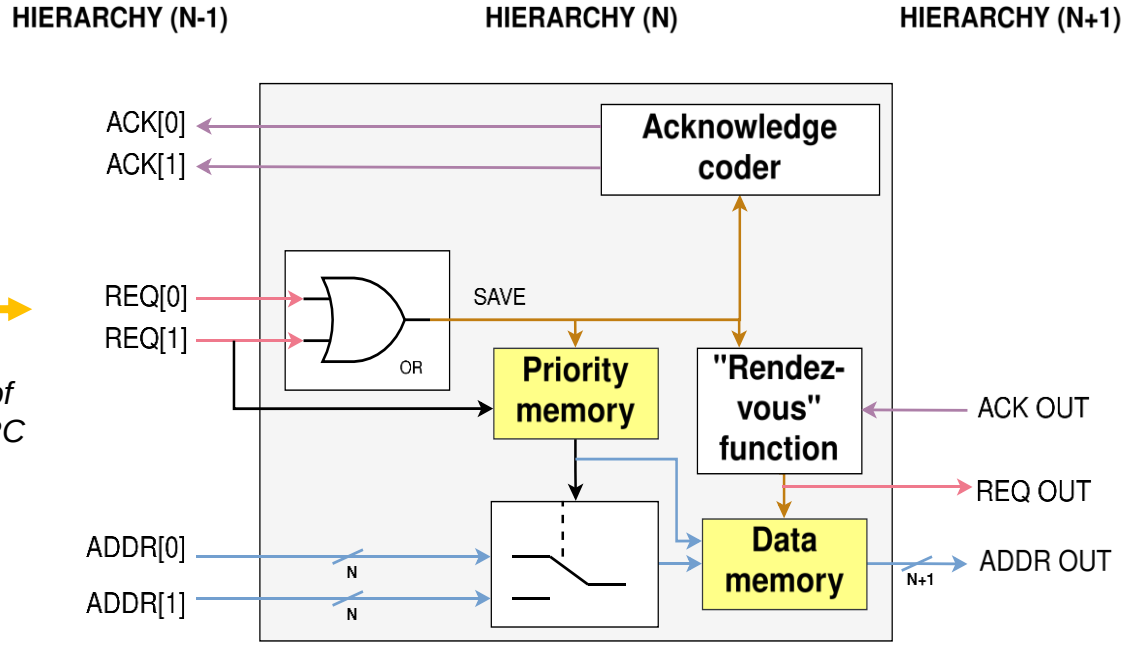


Working principle of the asynchronous readout



Architecture of the APA tree inside of readout columns in the matrix

- **Detection** : OR gate (SAVE signal)
- **Arbitration** : priority memory, selects the winner
- **Selection** : MUX who routes the winner's address
- **Handshake** : 4-phase rendezvous (REQ↑ ACK↑ REQ↓ ACK↓)
- **Acknowledgement** : ACK coder to releases the served master



APA architecture inside of readout columns of SPARC

Conflict-free, multi-speed compatible, event-driven

Sensor Architecture

FIFO + serializer

FIFO: buffers hit data (addr + timestamp) to absorb burst traffic
Serializer: formats and sends data out on the output bus
Output bus carries the complete hit word to the DAQ system

Fast OR selection	Timestamp (gray)	Address
1 bit	13 bits	10 bits

TABLE 5.1: Attribution of the 24 bits word in the FIFO.

Slow-control

Configuration interface (16 registers of 8 bits) for the whole chip
Controls : pixel masking, threshold tuning, TDC calibration, test injection

TDC + VCO

VCO : generates a fine time base
TDC : captures VCO phase at the moment of the hit
Produces a digital timestamp per event
Driven by Slow-Control for calibration
Feeds timestamp directly into the FIFO alongside the pixel address

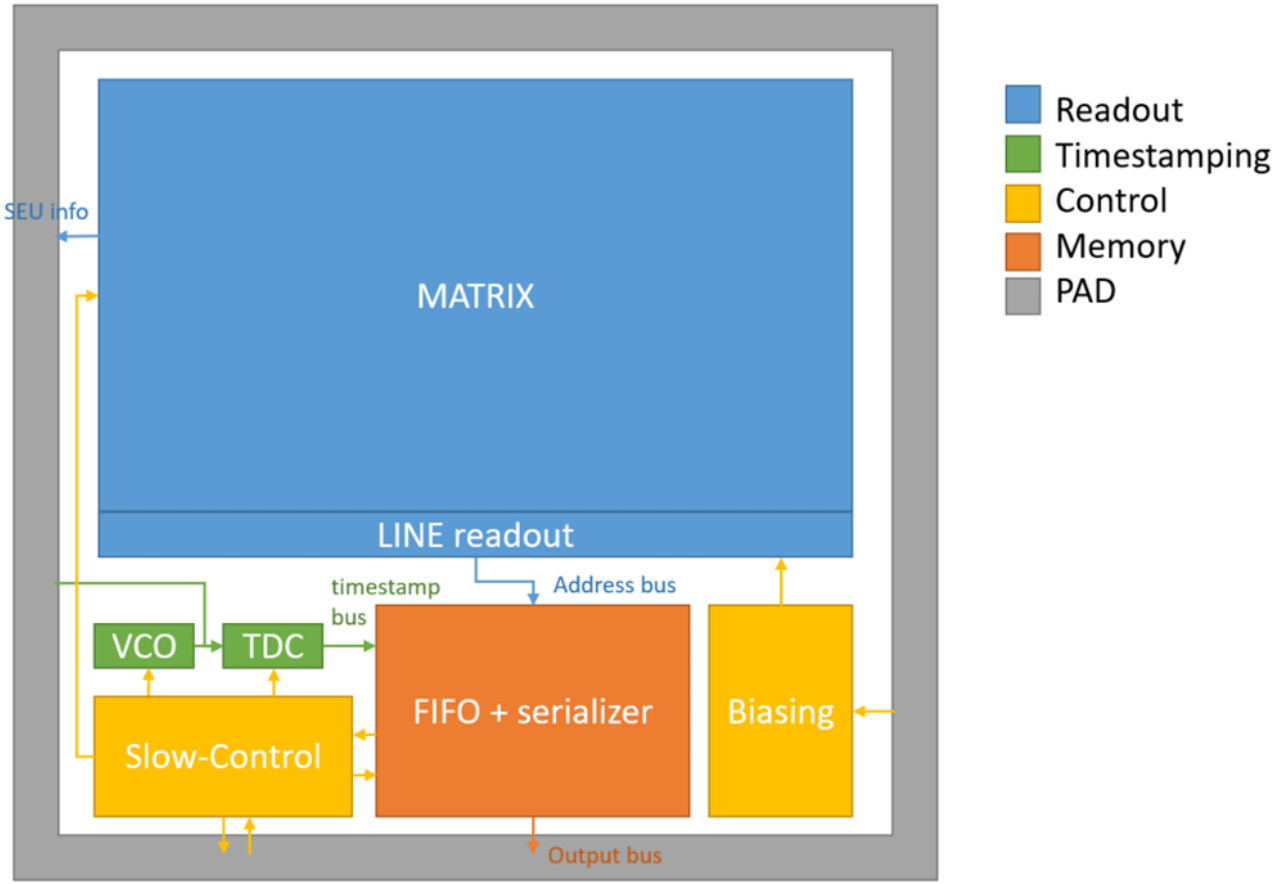


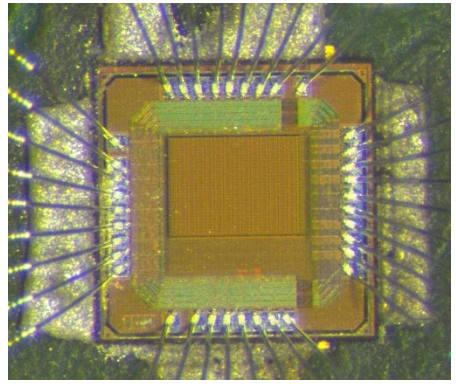
FIGURE 5.5: TOP view of the functional blocs of the SPARC sensor.

Biasing

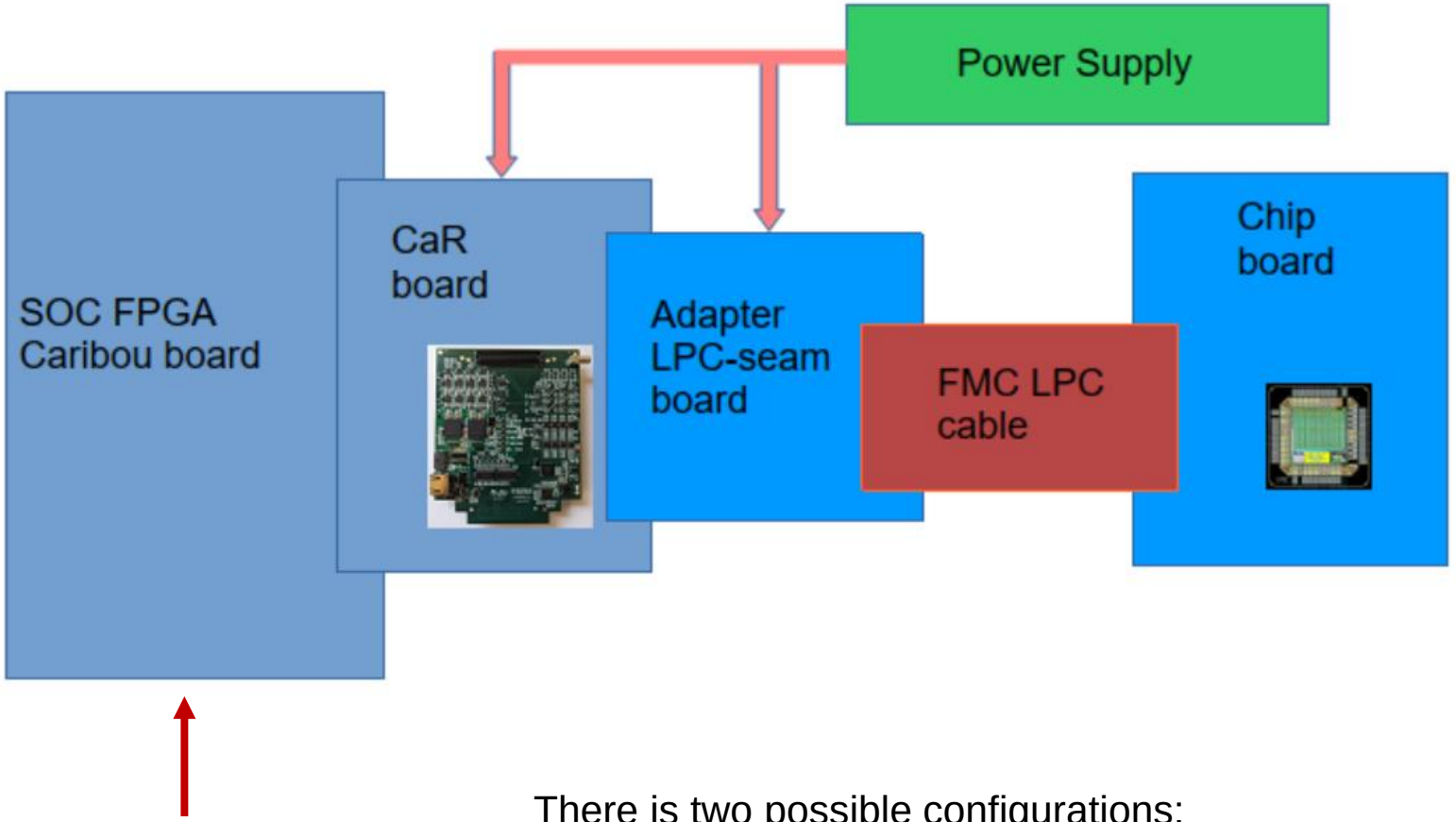
Generates analog bias voltages for the pixel front-ends
Configurable via Slow-Control registers

Test bench block diagram with FPGA-SOC as DAQ board

"***CARIBOU only" test bench*** : It is the collaboration test bench for SPARC which will be distributed



SPARC



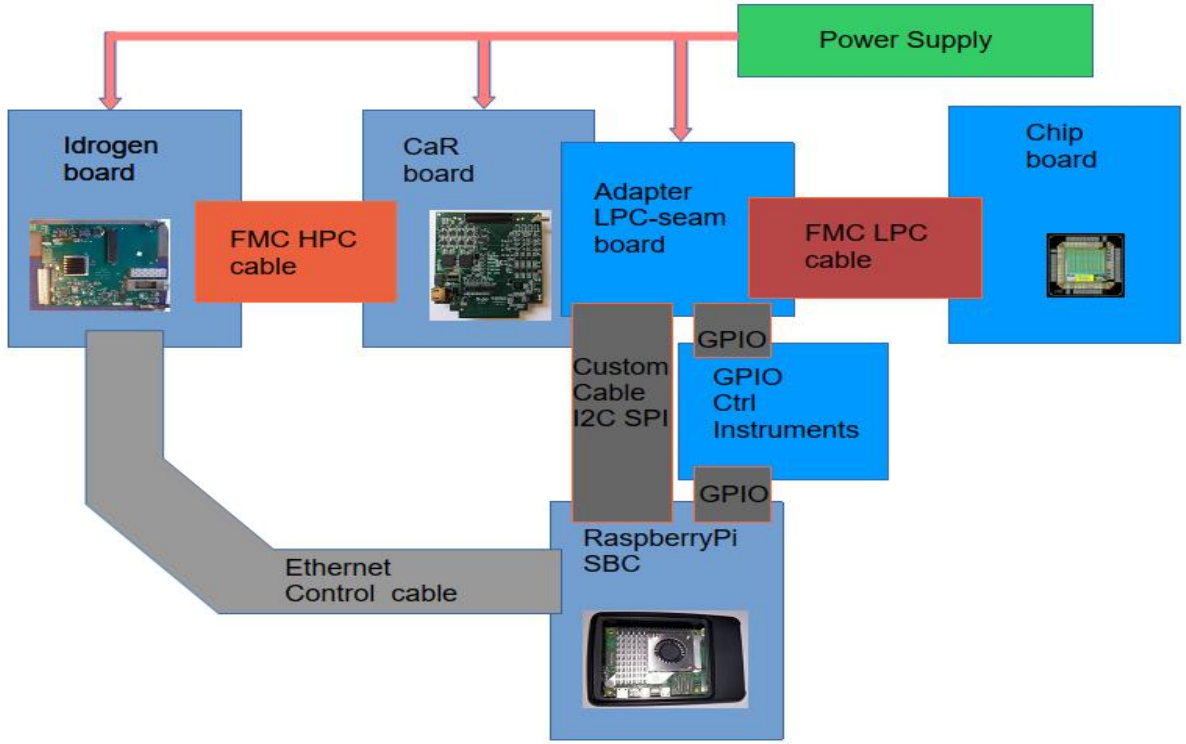
- Chip board / CaR board via FMC LPC cable
- Adapter board for LPC / seam 320 pins
- Caribou board
  - Slow control (I2C) config CaR
  - Slow control (SPI) config SPARC, Chip board
  - Acquiring data
- HW signal for SPARC testing (pulsing, etc) not presented on this slide

Not ready yet !

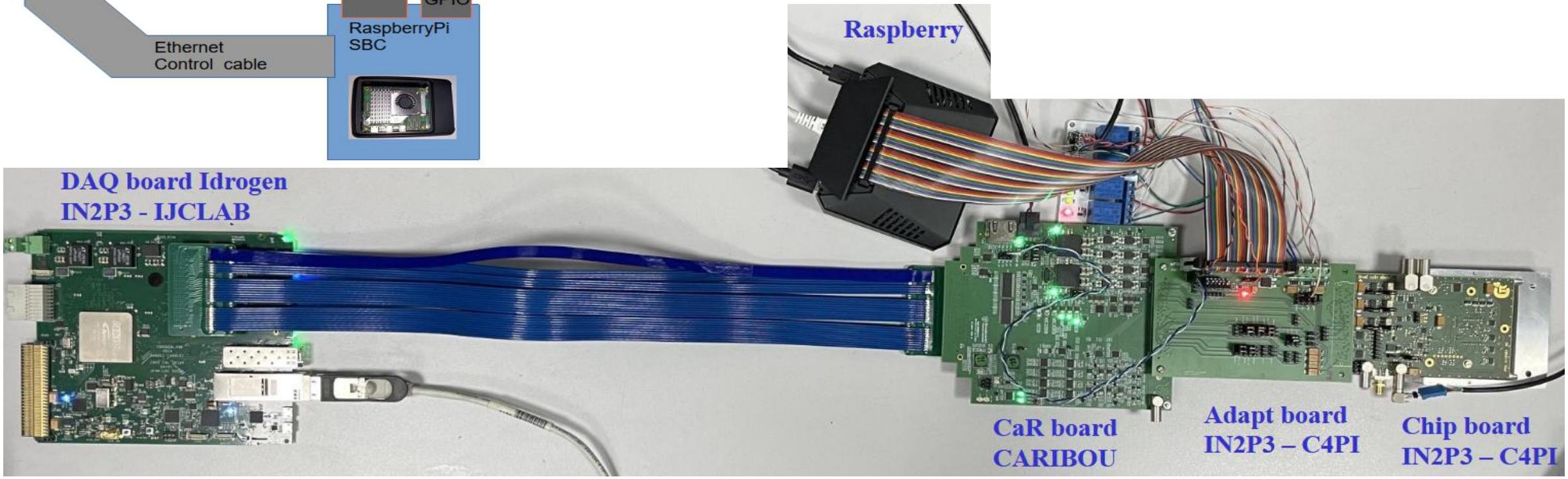
There is two possible configurations:

- ➢ Plug the Chip Board directly onto the CaR Board.
- ➢ Insert a flat ribbon cable between them for greater flexibility but the adapter board is required.

Test bench block diagram with Idrogen (IJCLab IN2P3) as DAQ board

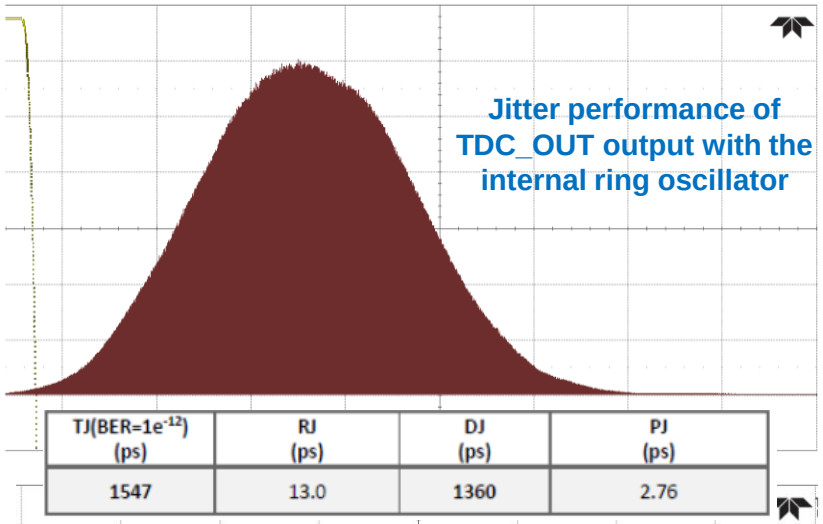


- Chip board / CaR board via FMC LPC cable
- Adapter board for LPC / seam 320 pins
- CaR to IDROGEN via FMC HPC cable
- DAQ Raspberry PI 5
  - Slow control (I2C) config CaR
  - Slow control (SPI) config SPARC, Chip board
  - Control IDROGEN (Ipbus ~ 20 MB/s)
- HW signal for SPARC testing (pulsing, etc) not presented on this slide

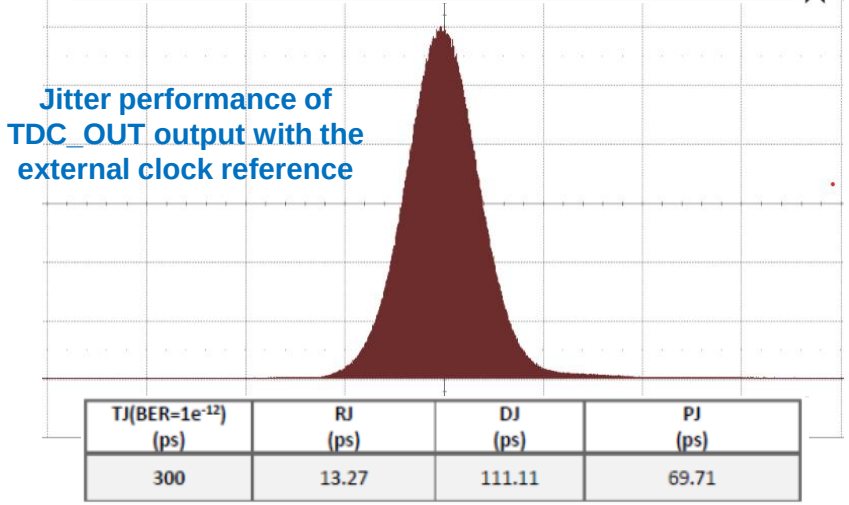


Preliminary Measurement : Ring Oscillator Clock Jitter

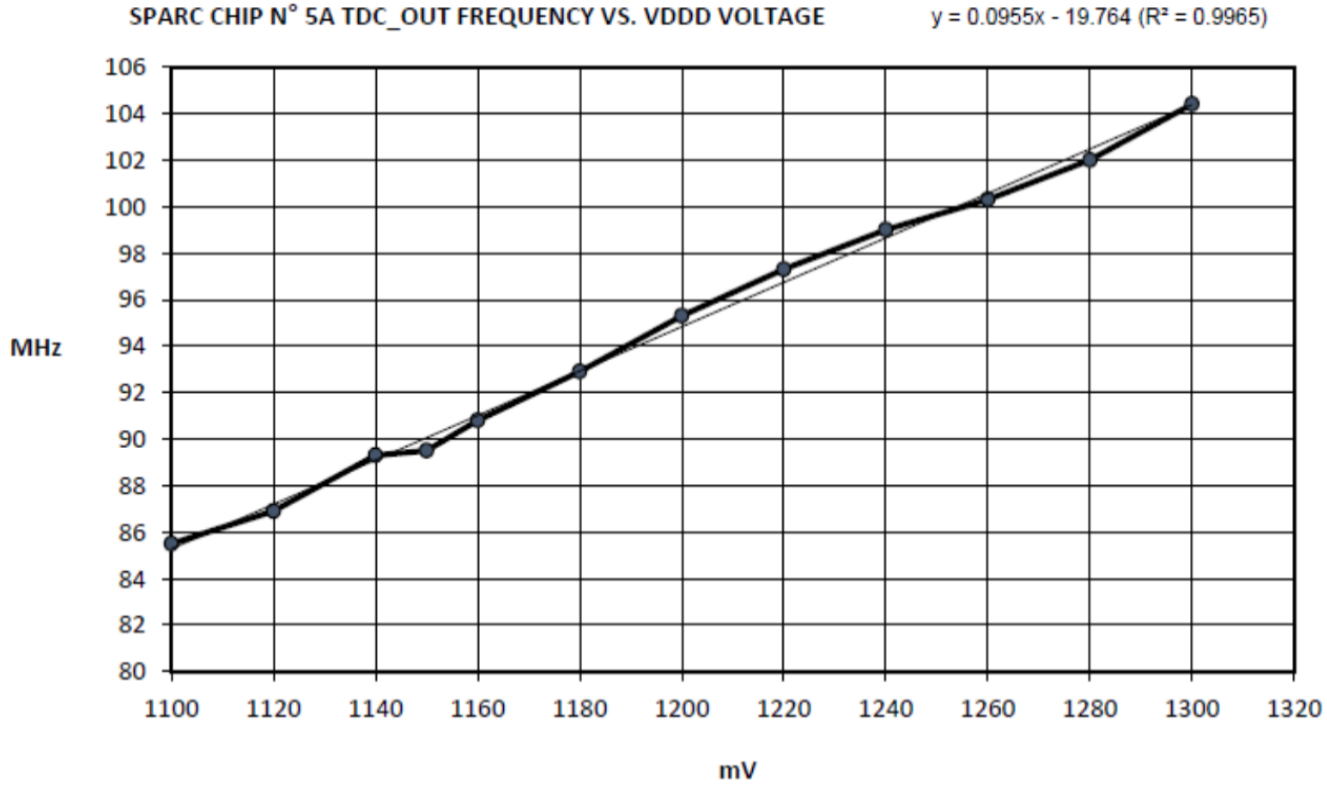
- Measured conversion gain of the TDC_OUT related to power supply DVDD voltage: 96 KHz/mV
- Conversion gain KVDDD-to-ring_osc of the RING_OSC related to DVDD voltage: 8 * 96 KHz/mV = 764 kHz/mV



TJ(BER=1e^{-12}) (ps)	RJ (ps)	DJ (ps)	PJ (ps)
1547	13.0	1360	2.76



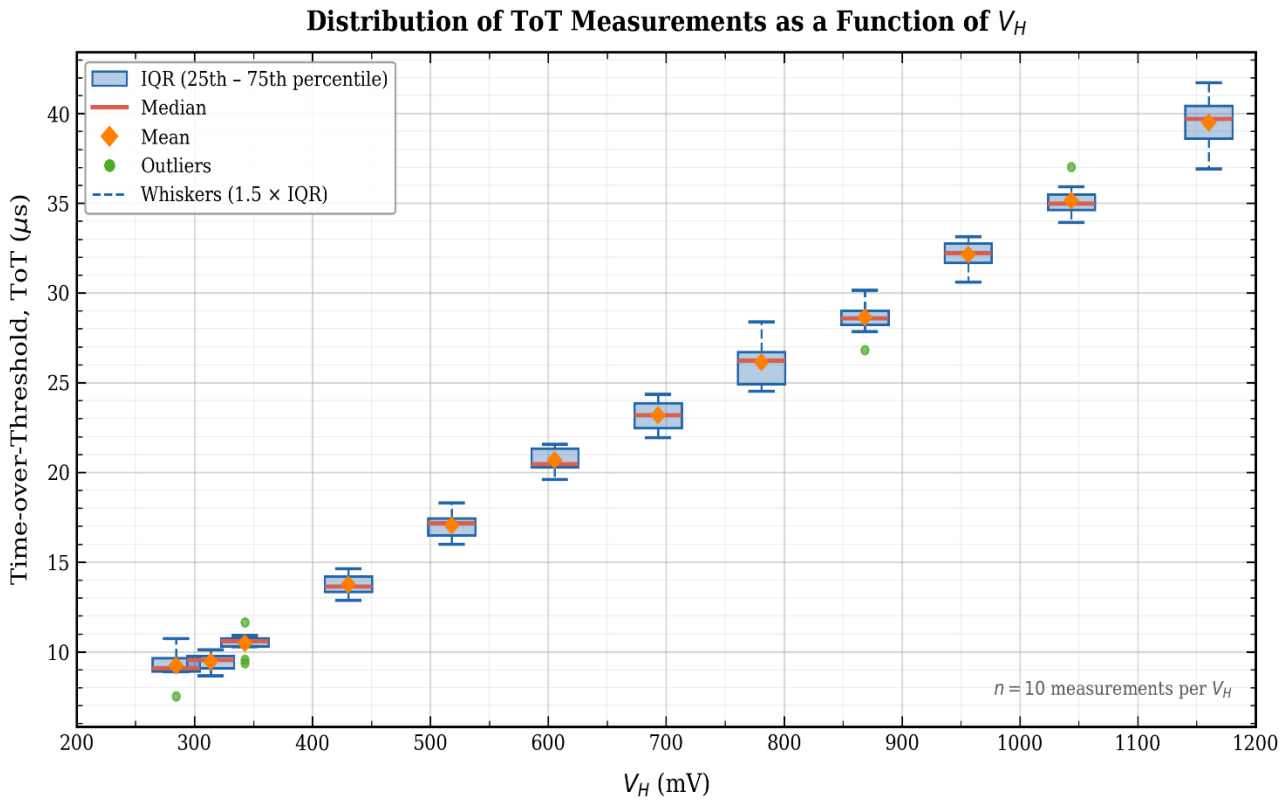
TJ(BER=1e^{-12}) (ps)	RJ (ps)	DJ (ps)	PJ (ps)
300	13.27	111.11	69.71

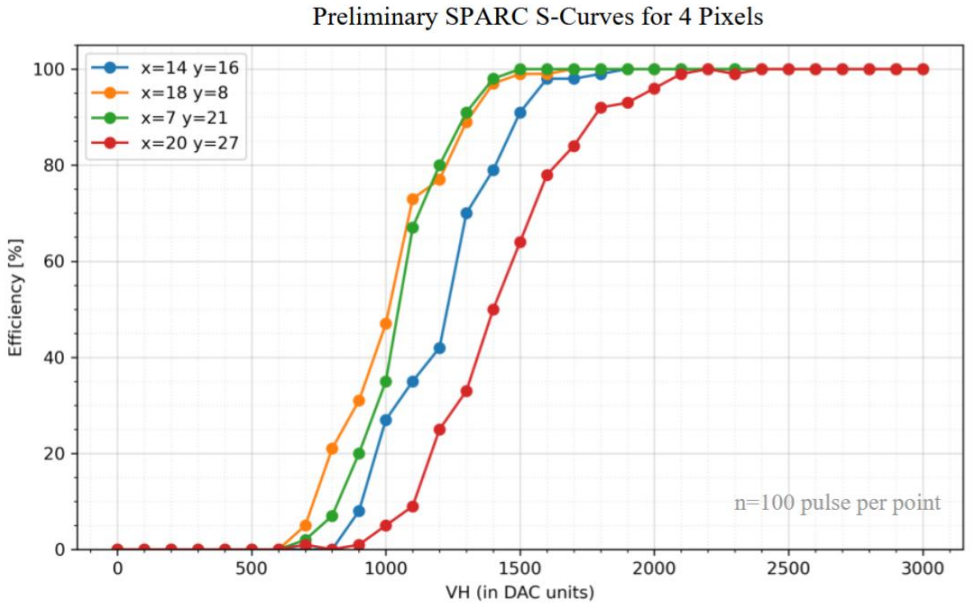


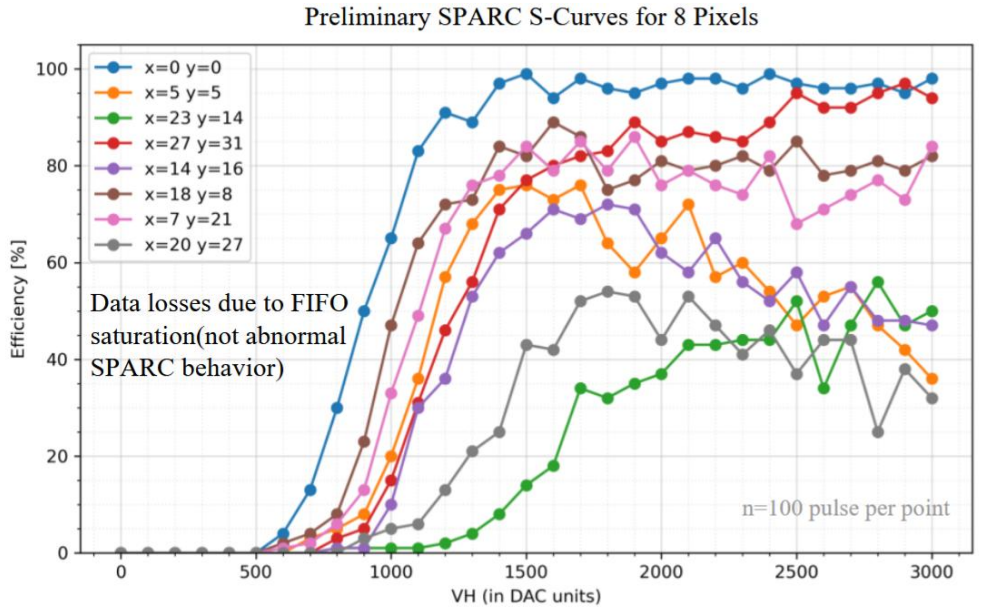
- Ring oscillator shows significantly larger jitter than external clock
- Internal oscillator is mainly intended for debug and tests, it is not designed to get a low jitter
- We will use external clock from Idrogen

Preliminary Measurement

First ToT measurements are consistent with simulations and confirm the functionality of the ToT mode.

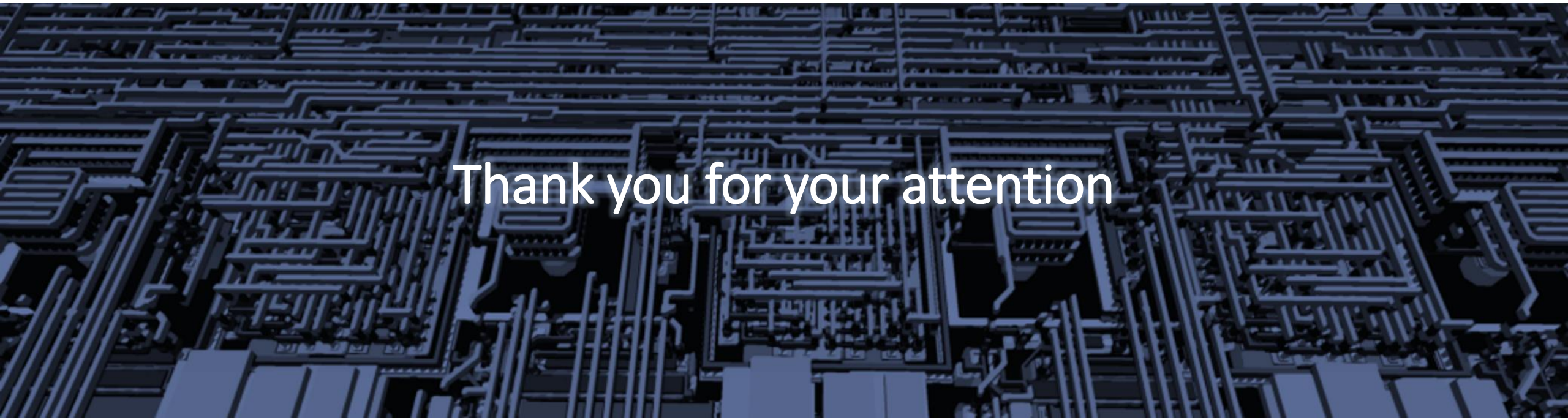






Simultaneous pulsing of 8 pixels ➔ SPARC FIFO saturation (FIFO depth = 32) and data losses.

An upgrade of the acquisition software is ongoing to perform the scan using smaller groups of pixels (less than 8), avoiding FIFO saturation.



Thank you for your attention

Camille Fournier *on the behalf of SPARC core team*

Phd student, Institut Pluridisciplinaire Hubert Curien (IPHC)

Subatomic Research Department, C4PI team

This work was supported by IdEx Unistra (ANR 10 IDEX 0002), and by SFRI STRAT'US project (ANR 20 SFRI 0012) and EUR QMAT ANR-17-EURE-0024.