Electronic Data Acquisition for the Ricochet Experiment

Cyrille Guérin - IP2I

RICOCHET
A Coherent Neutrino Scattering Program

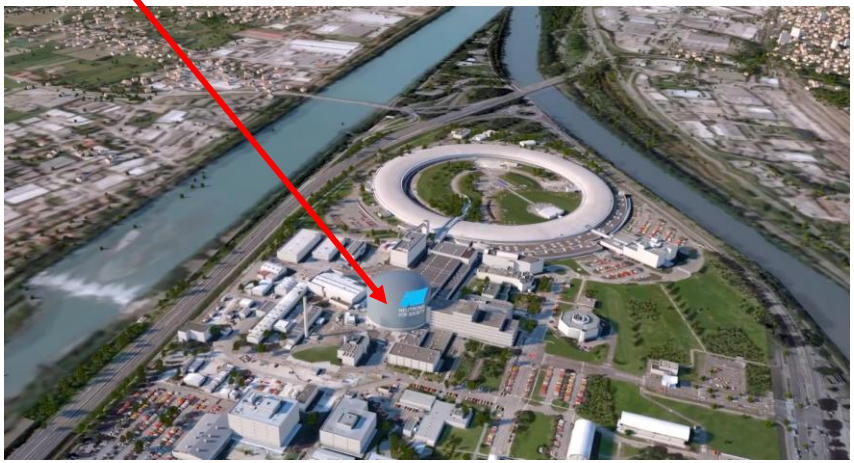
International collaboration :

- France (IP2I Lyon, LPSC, IJCLab, ILL, Néel, C2N)
- US (MIT, UMass, Northwestern, Lincoln, Argonne, Mines)
- Canada (Uni of Toronto)
- Russia (JINR)

- Context
- Electronics Architecture
- Readout System : « Bolo Box » & Digital Bolo Board
- Synchronization Board
- Testing
- Conclusion

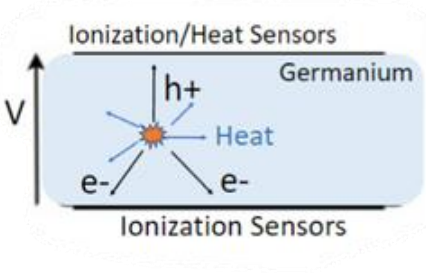
Outline

Ricochet installed at the Institut Laue-Langevin (ILL, Grenoble)



Main objective:

Study of coherent elastic neutrino-nucleus scattering (CEvNS)



Nuclear recoil : < 1 keVnr

Dual measurement

- Heat (< 1,2 keV)
- Ionization (< 160 eVee=> < 50 electron-hole paires)

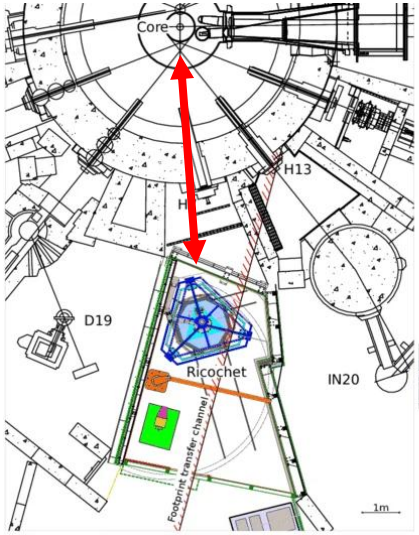
Key Numbers:

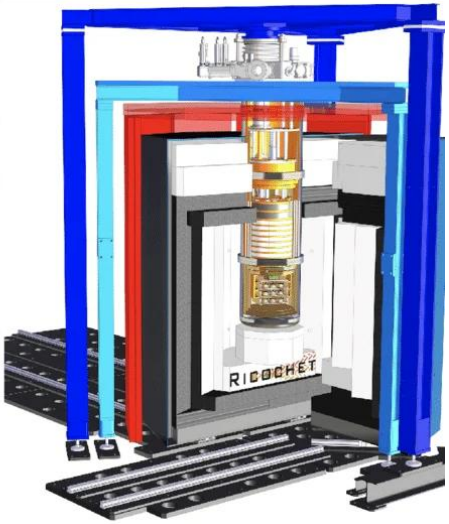
-Close to the research nuclear reactor @8.8m
- Intense low-energy neutrino flux
- Electron or gamma-ray background

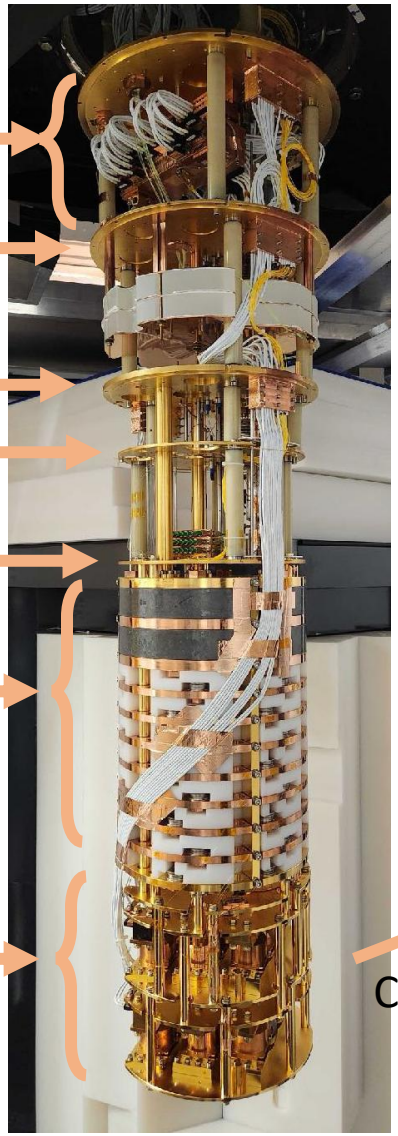
-20 ton cryostat shielding (Lead and polyethylene)

-External Veto Muons (17m²)

-42g Germanium detector at 10 mK







Specifications :

⇒ Resolutions : **20 eV heat** et **20 eVee ionization** (7 electron-hole pairs)

⇒ Threshold 100 eVnr

⇒ Discrimination between nuclear recoils (neutrinos) and electron recoils (gamma/electron background) starting around 400 eVnr.

⇒ Readout chain : require a resolution of approx. 50 nV on both heat and ionization channels.

Dynamic Range : Low-energy neutrino interactions **AND** Gamma background > MeV

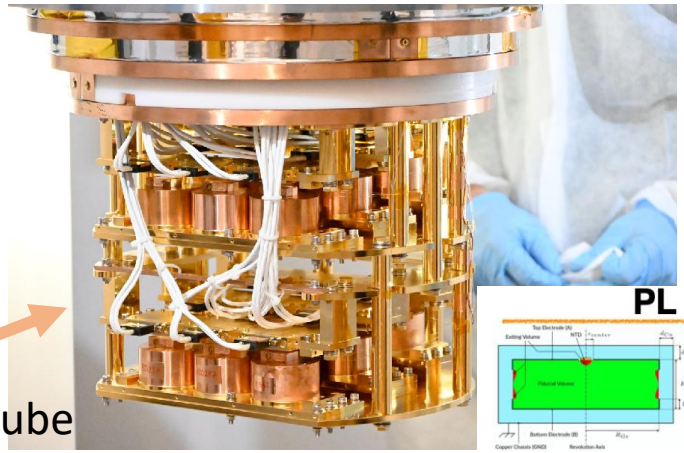
⇒ 10^5 dynamic range for the electronics (20 eV to 2 MeV)

⇒ Bipolar signals (positive and negative pulses)

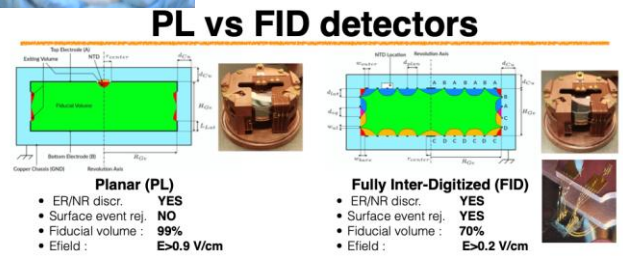
CryoCube :

- 18 Germanium detectors

⇒ **See Juliette's presentation at 10:50 AM for further details**



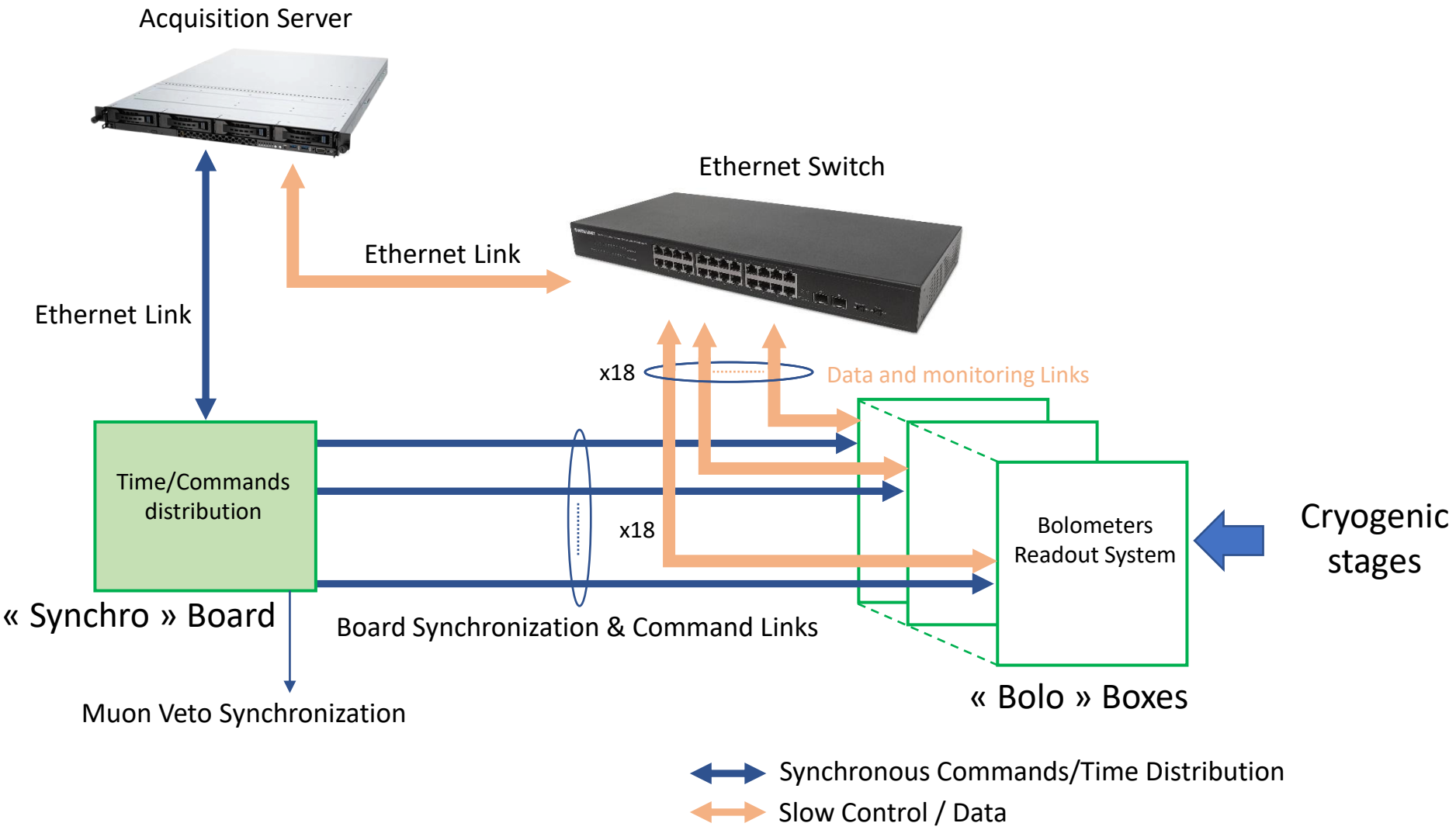
CryoCube



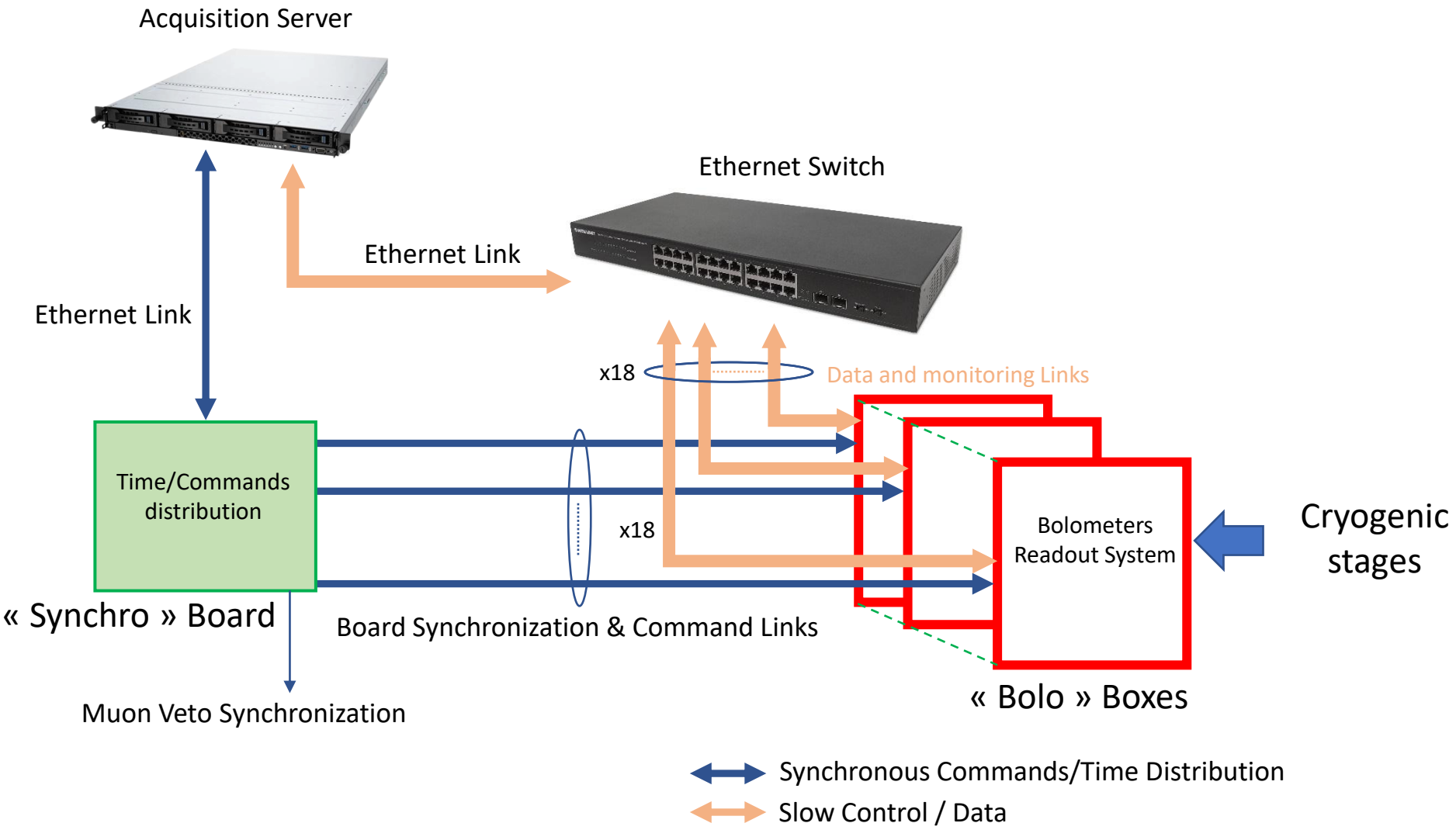
1 Heat
2 ionization

1 Heat
4 ionization

DAQ System Architecture

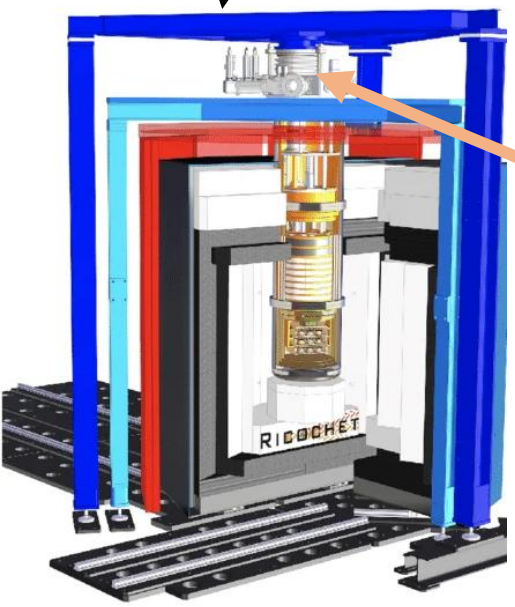


DAQ System Architecture

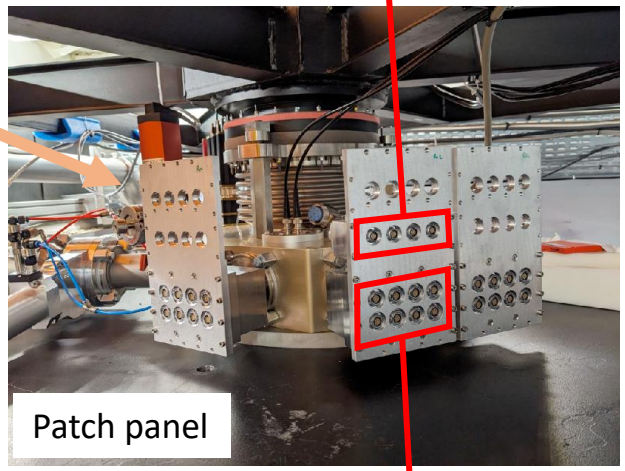


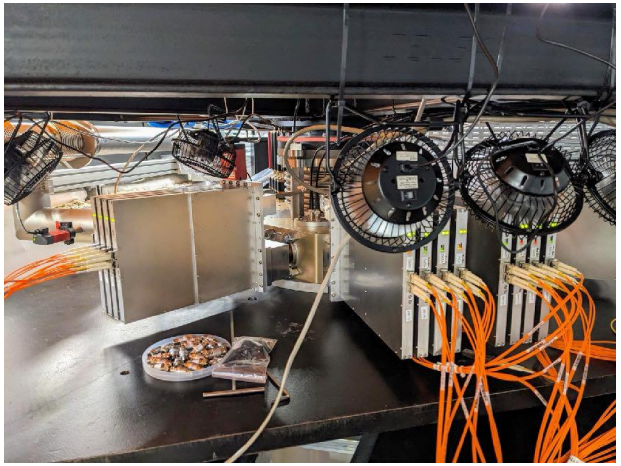
Mechanical Structure and Shielding

👉 Contribution of IP2I, LPSC, ILL



Power





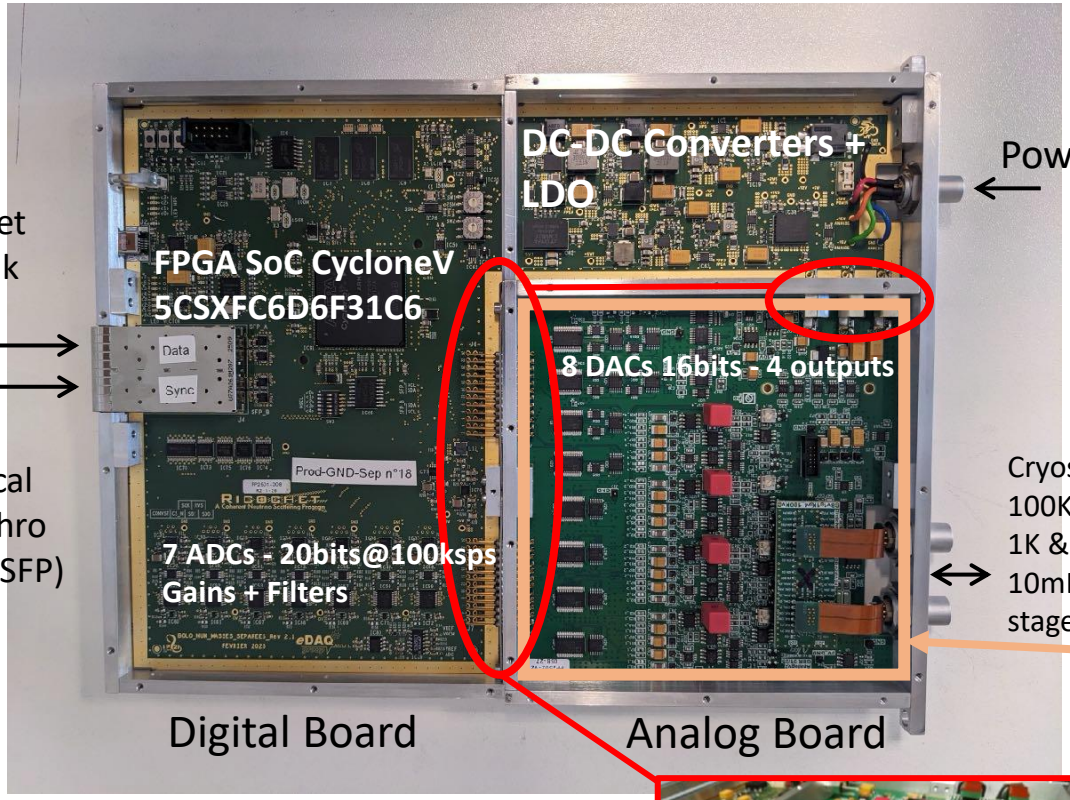
18 Bolo Box system

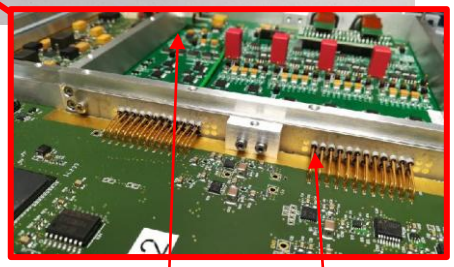
Biasing and signals

👉 Contribution of the IP2I Instrumentation department

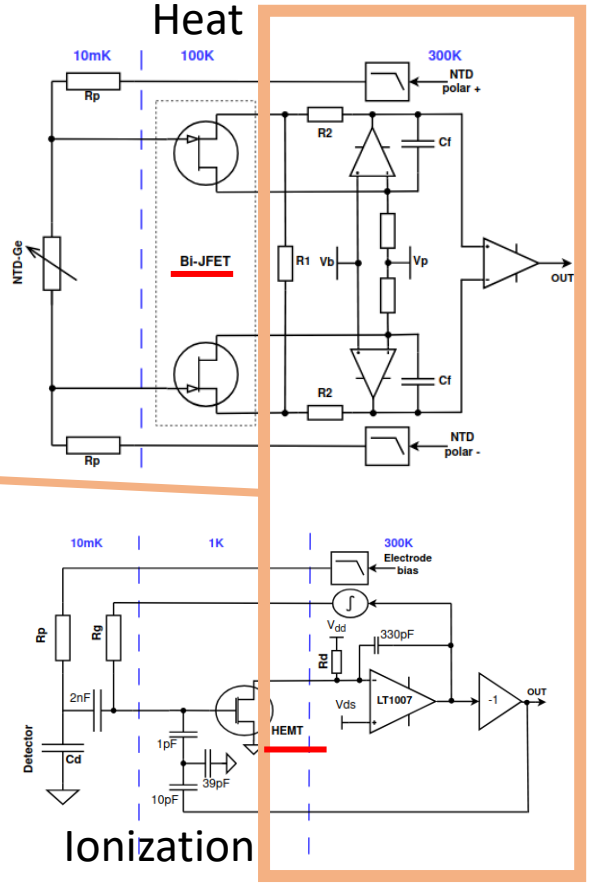
👉 Contribution of Néel Institut and IP2I for integration and testing

Dynamic range 20eV to 2MeV
Ionization channel: 40 kHz bandwidth





Feedthrough Filter
-Power
-Signals

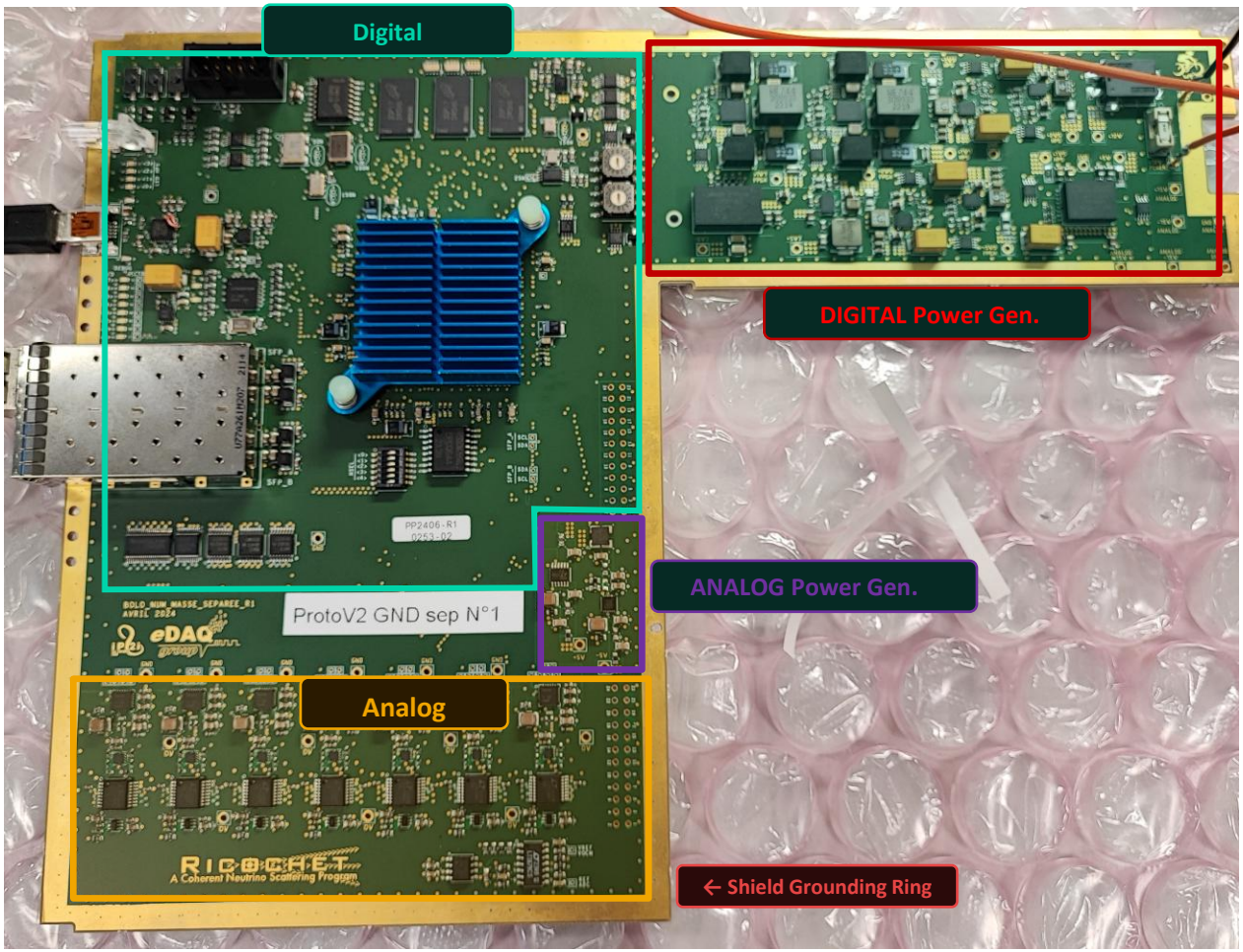


ADC 20 bits
-Effective dynamic range for bipolar signals
=> $2^{20}/2$ =524 288 codes
-For 20 eV resolution => 5 ADU

Gain 1,2,4,8,16 + Filter (10kHz, 20kHz, 40kHz)

👉 Guillaume Bres
Julien Minet

- CAO W. Tromeur, F. Doizon eDAQ/ IP2I - Rev 2.1 - 10/02/2025



PCB DETAILS

Specific Stack-up
16 layers · 7 cores + 2 Cu foils · 2.5 mm

Triple Independent Ground Planes
GND Num · GND Analog · GND shielding

FPGA SoC
Heatsink Cooling → Chassis cover

100 Ω differential
TOP · S1 · S2 · S3 · S4 · BOTTOM (balanced)

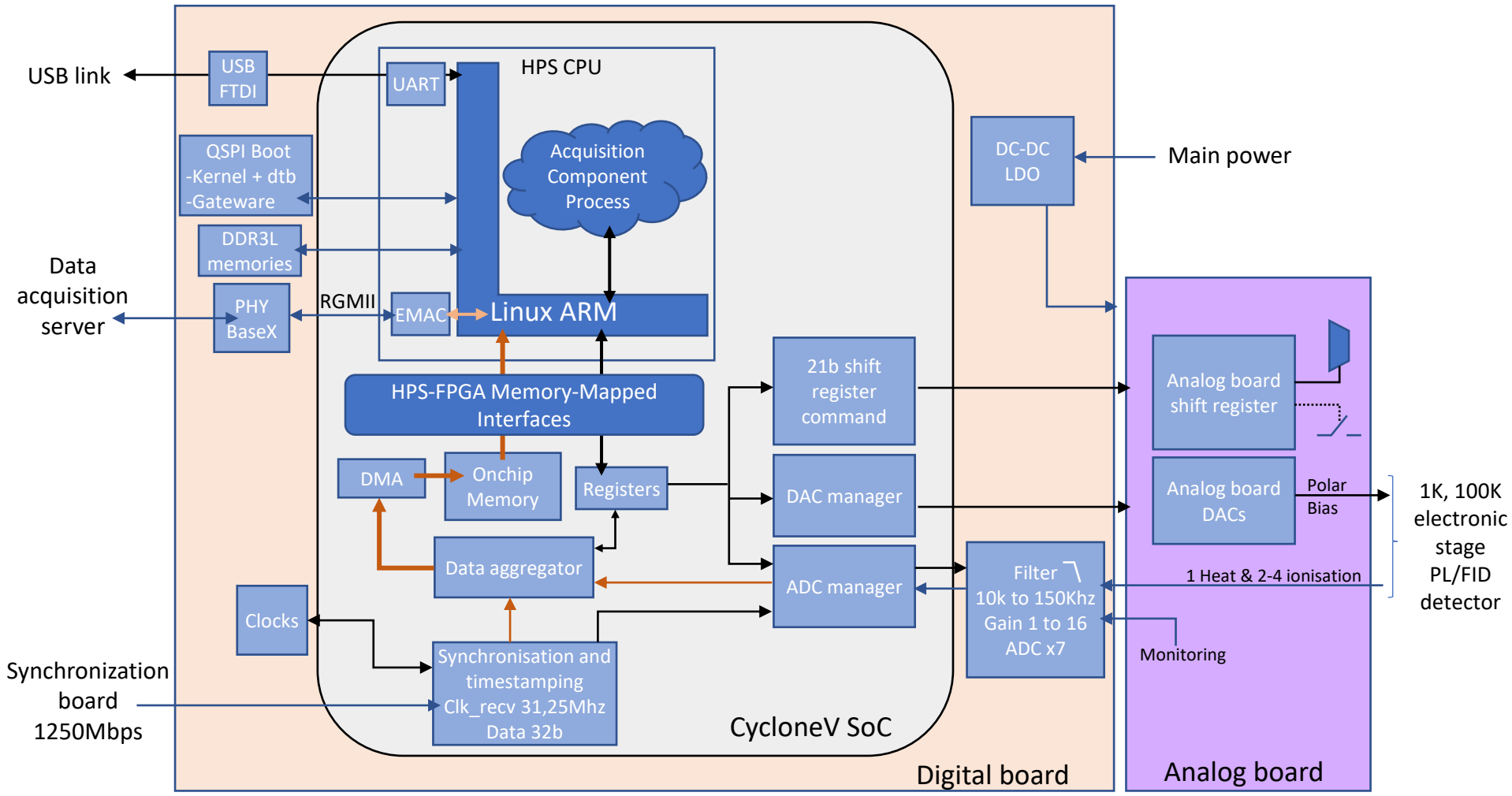
Etching
90 µm / 80 µm min. spacing · 200 µm finished via

εr dielectric
4.25 – 4.7 depending on the layer (Panasonic R-1551W / R-1566W)

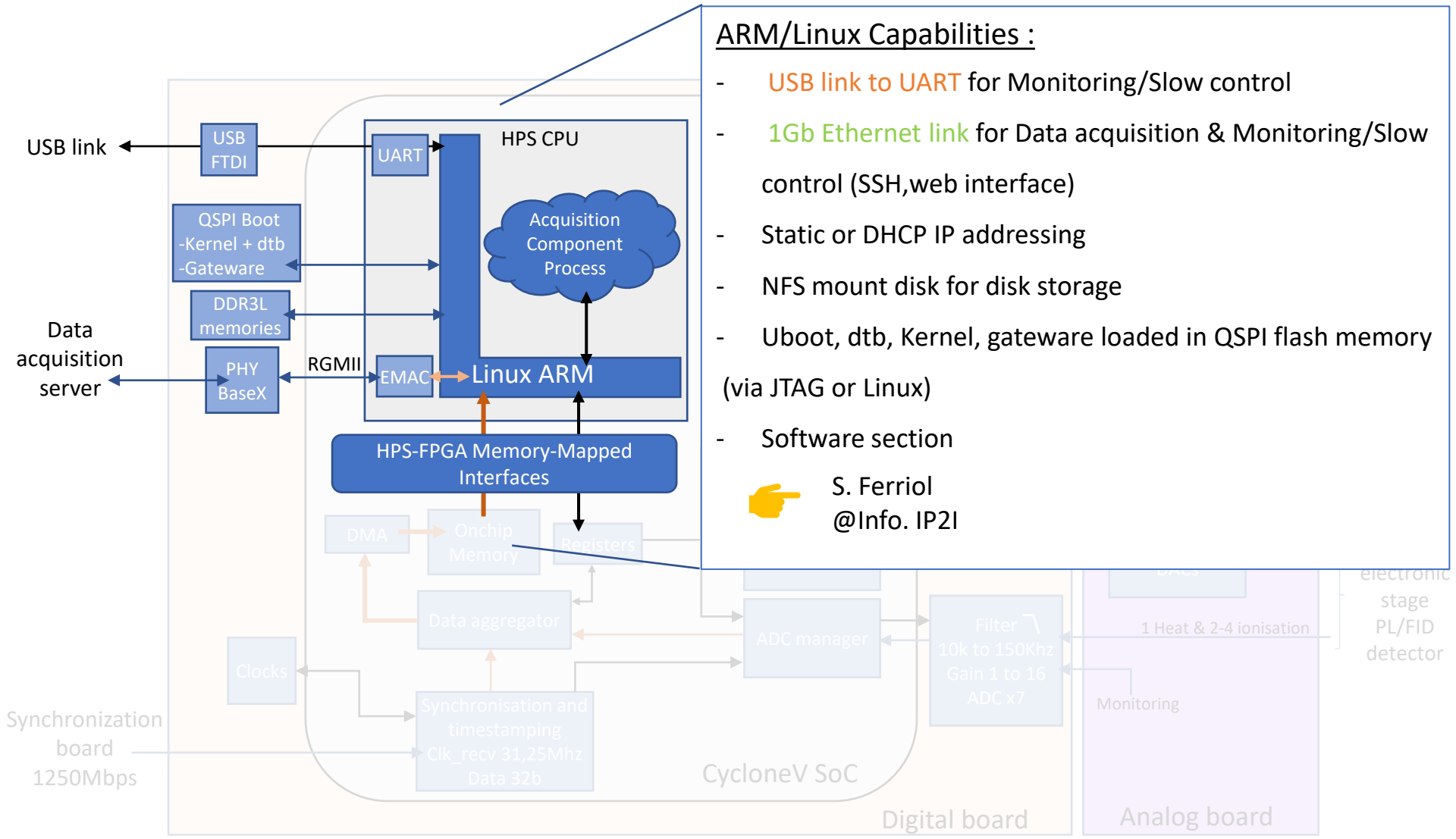
Dimensions
265.7 × 198.9 mm

Finition
Selective ENIG finish 15 µm · Soldermask 50 µm · Double-sided Silkscreen

Manufacturing
Würth Elektronik · 32 units produced



Overview Diagram



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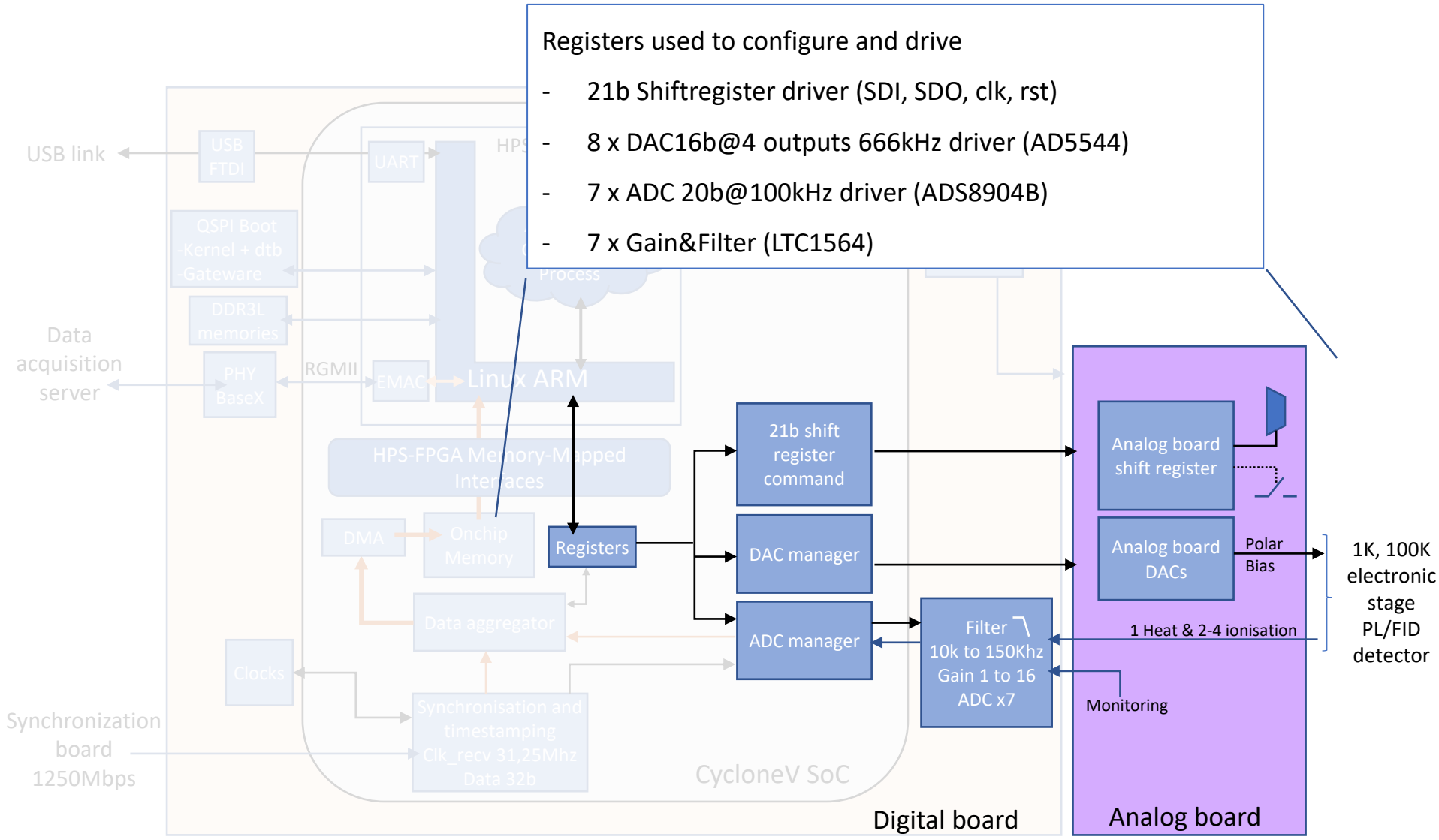

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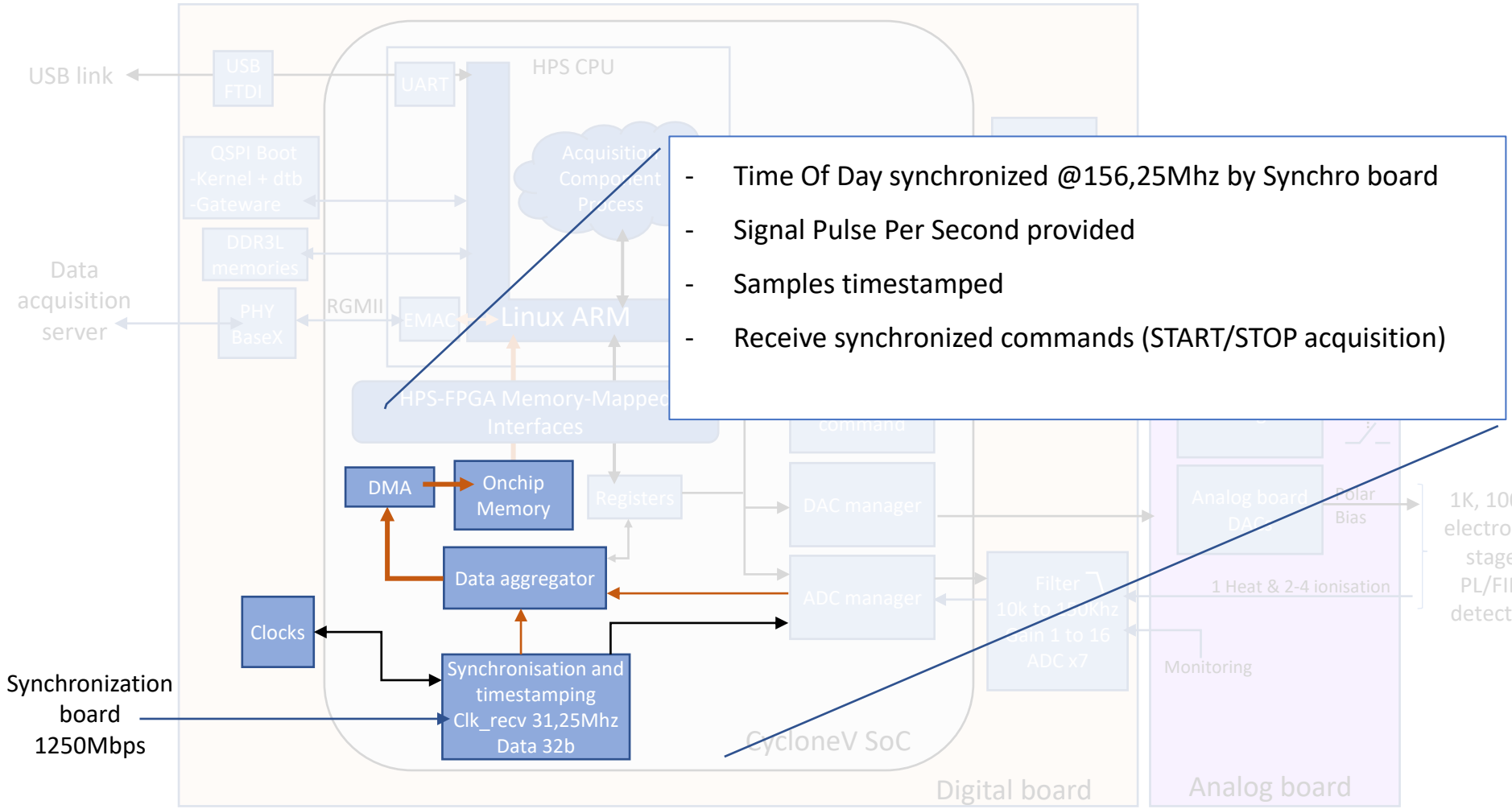
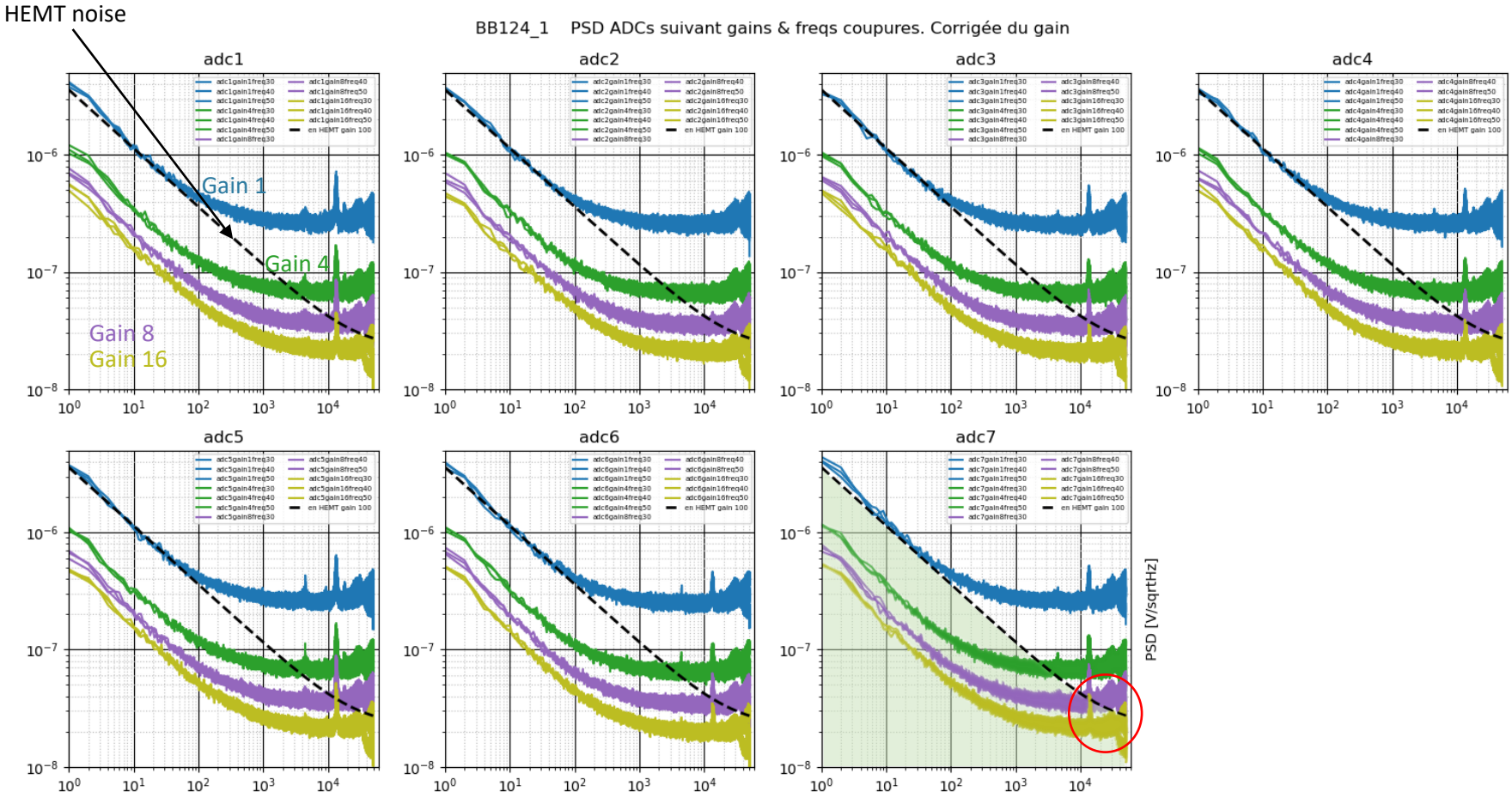


Overview Diagram

Input-referred PSD noise measurements of ADCs (variable gain 1-16 + fixed gain 100)

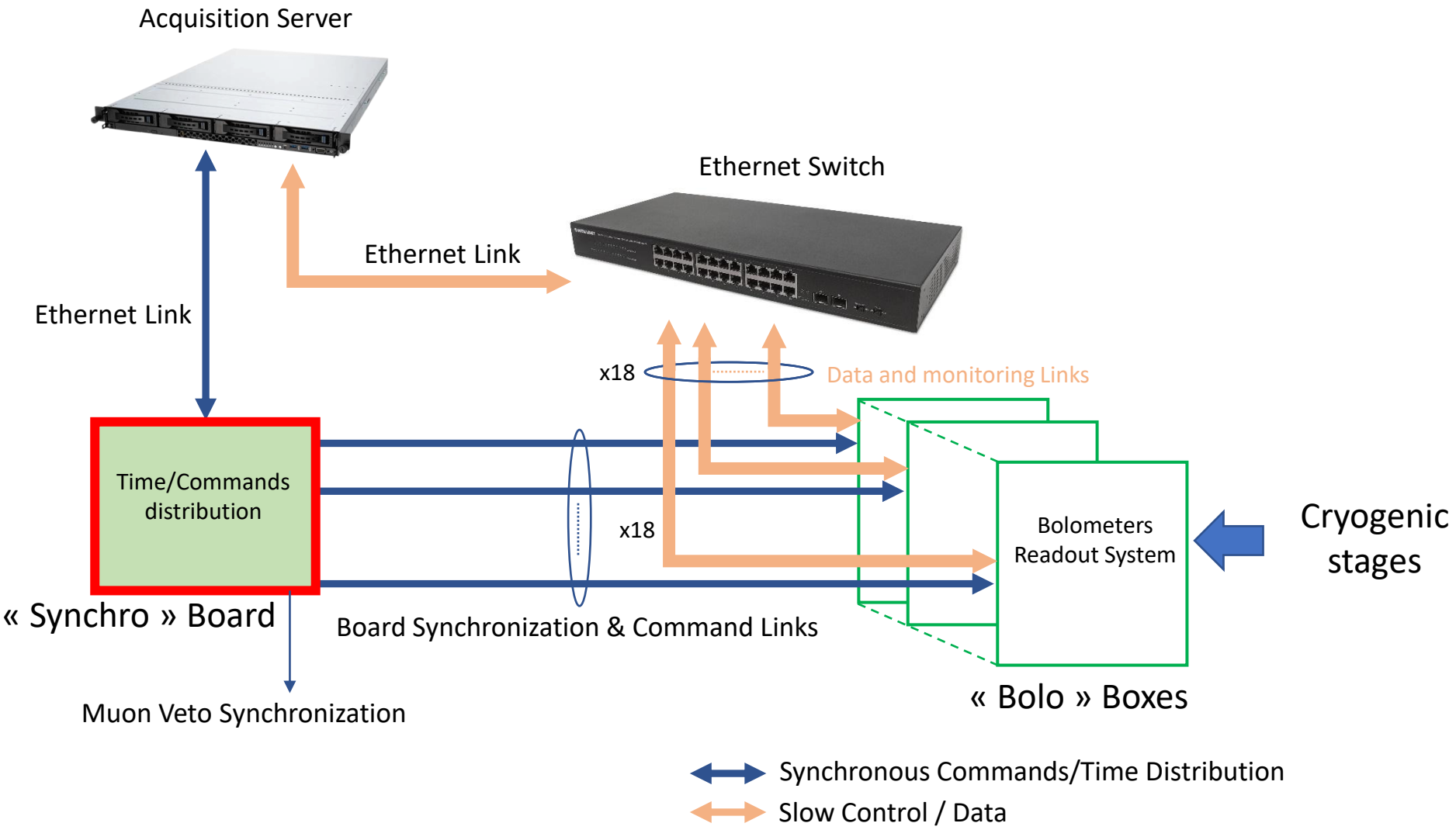


Noise contribution of the readout chain vs. gain

For gains 8 and 16, the electronics noise is lower than the HEMT noise across most frequencies.

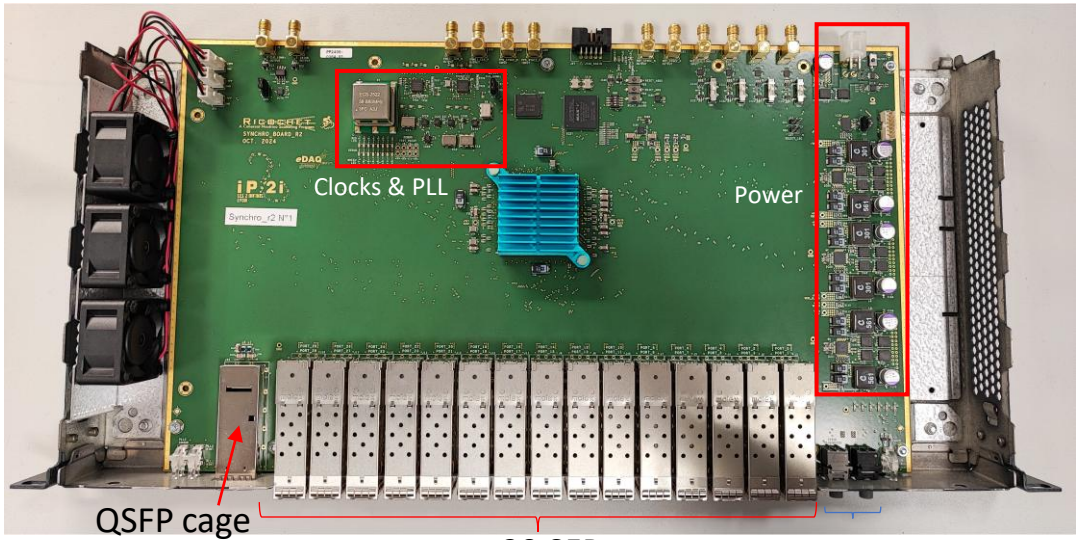
=> Using gain 8 to avoid saturating the Argon-41 peak (1.3 MeV)

DAQ System Architecture



Digital outputs (10Mhz, IRIGB)

Digital In/Out (Clocks, pps, IRIGB)



PCB DETAILS

Stack-up spécifique
16 layers · 7 cores + 2 Cu foils · 2.5 mm - *FR4.1 Panasonic*

Case 19" 1U
371.3 × 217.4 mm · Chassis Integration & Packaging

100 Ω différential
TOP · S1 · S2 · S3 · S4 · BOTTOM (balanced)

εr dielectric
4.25 – 4.7 depending on the layer (Panasonic R-1551W / R-1566W)

Dimensions
371.3 × 217.4 mm · Cutting ± 150 µm

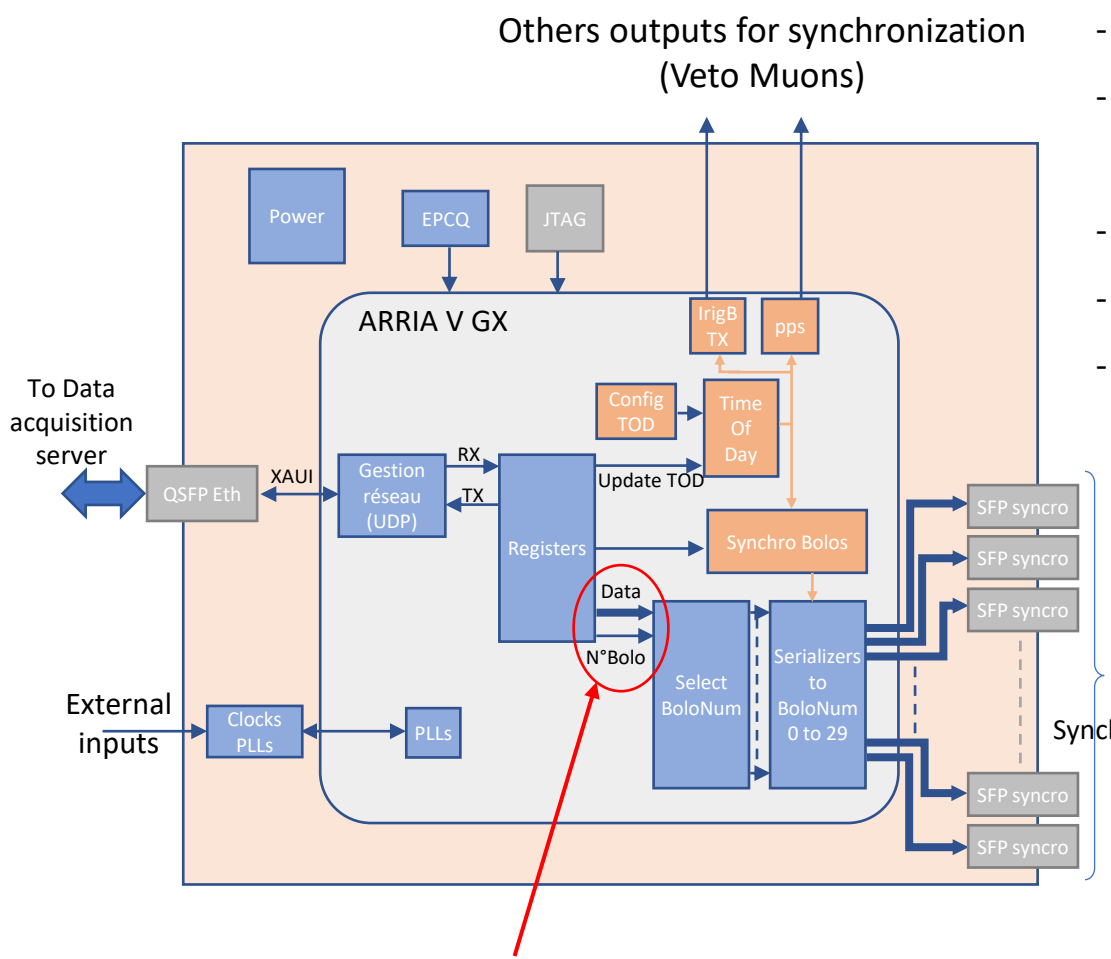
Finition
ENIG sélectif · Soldermask 50 µm · Via 250 µm
Würth Elektronik · 2 units produced

Timing Control
SFP TX / relative propagation delay 50 ps

10Gb Ethernet Link (UDP)
To server

1Gb Links
To Bolo Box

- Case D. Chaize Instrumentation/IP2I



Used to send Synchronized command START/STOP acquisition

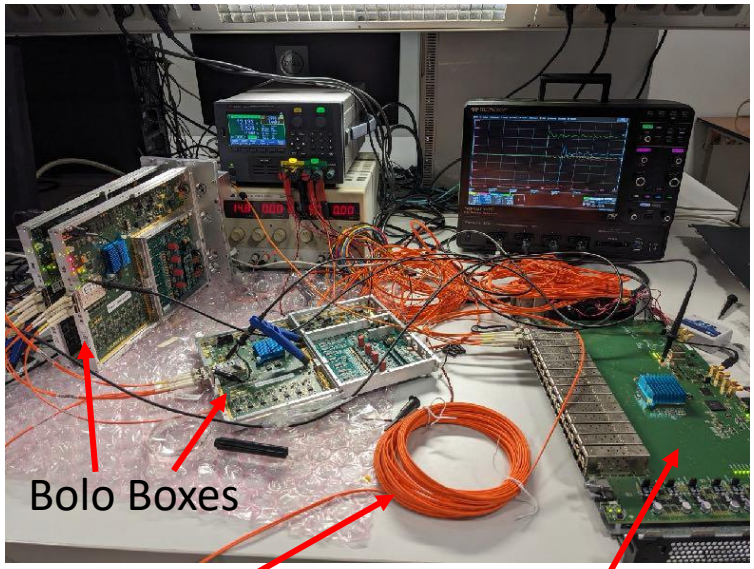
Overview Diagram

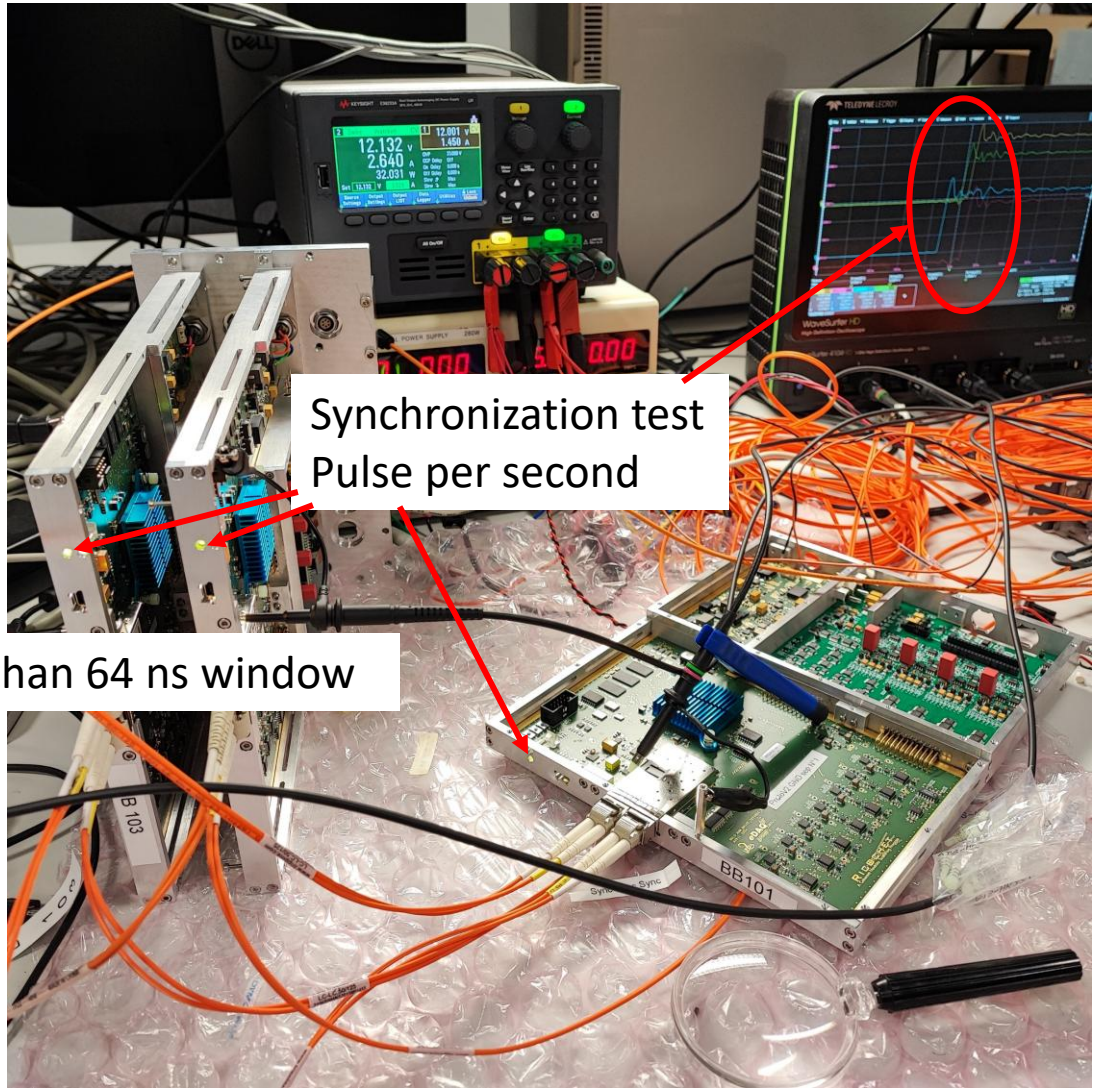
Capabilities for RICOCHET:

- Local Time Of Day @156,25Mhz (6,4ns)
- Up to 26 SFP cages (TX Only) for Synchro & START/STOP
- 10Gb Ethernet link (UDP) QSFP (4Tx/4Rx)
- Outputs to synchronized Veto Muons detector
- No processor

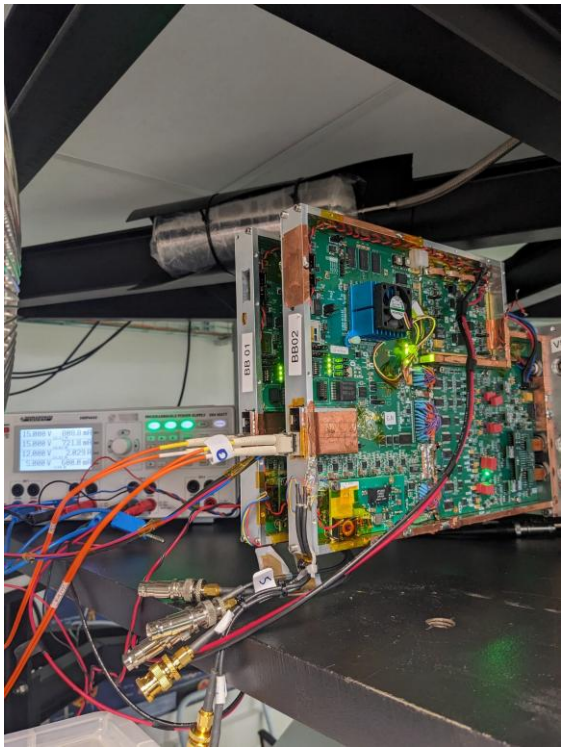
Other hardware capabilities:

- 30 SFP cages (Tx/Rx high-speed links)
- SyncE PLL and complex clock tree



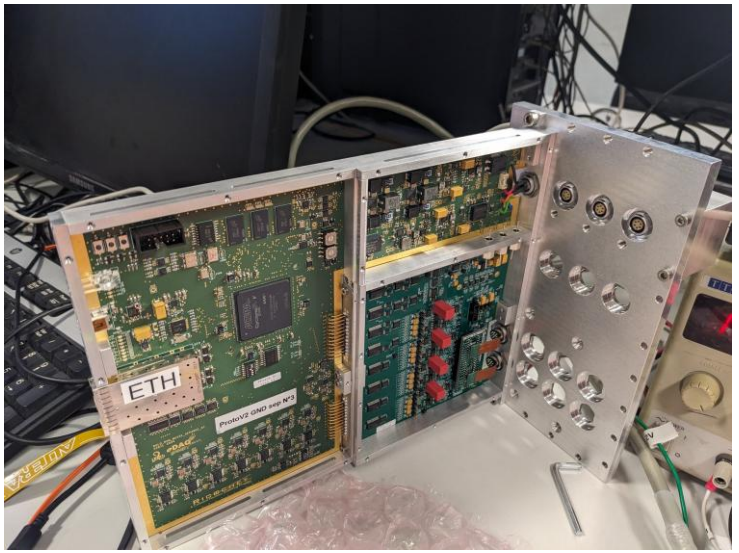


Synchronization Board

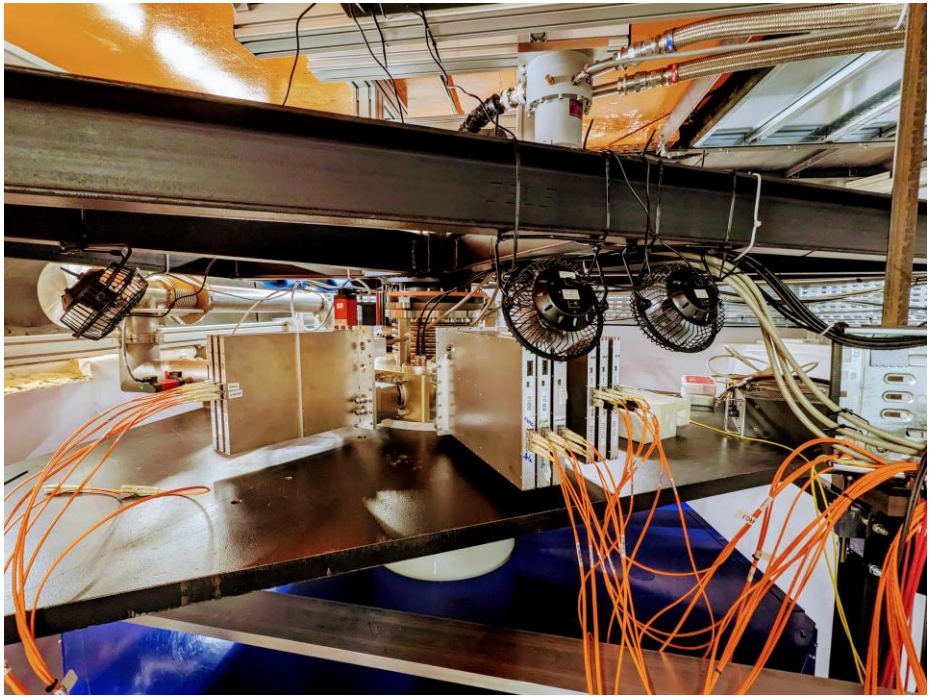


Test Proto BB01-02-03
cryo Ricochet @ IP2I
été 2023

Test présérie
BB101-102-103
eDAQ @ IP2I
été 2024



Opération @ ILL
9 BBs + carte synchro
3 protos + 6 préséries
Jan 2025



Conclusion :

⇒ Production and Deployment

- ❑ 30 + 6proto Bolo boxes & 2 + 2proto Synchro boards produced and tested
- ❑ 18 Bolo box and 1 Synchro board installed for RUN016 @ ILL - July 2025 (Plan for a 2-year science run)
- ❑ BB & Synchro board used at Lyon for R&D Ricochet and TESSERACT

⇒ Grounding Philosophy and Prototyping

- ❑ Architectural Trade-off: Extensive comparison between Split Grounds vs. Common Ground philosophies for Bolo Box boards and chassis.

⇒ Next Steps & Upgrades

Hardware development

- ❑ Expand Syncho Board capabilities (DHCP addressing, PTP core, remote firmware updates…)
- ❑ Deploy PTP synchronization on a SoC FPGA (ARM processor and external PHY)

For a potential Ricochet evolution…

- ❑ Architectural simplification by using PTP on the digital Bolo board
- ❑ Noise optimization of the readout electronics (Digital, analog, box, câbling, detectors…)
  - ⇒ Ionization resolution between 28eVee and 30eVee
  - ⇒ Heat resolution limited by JFET @ 25eV not by BB

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Merci!

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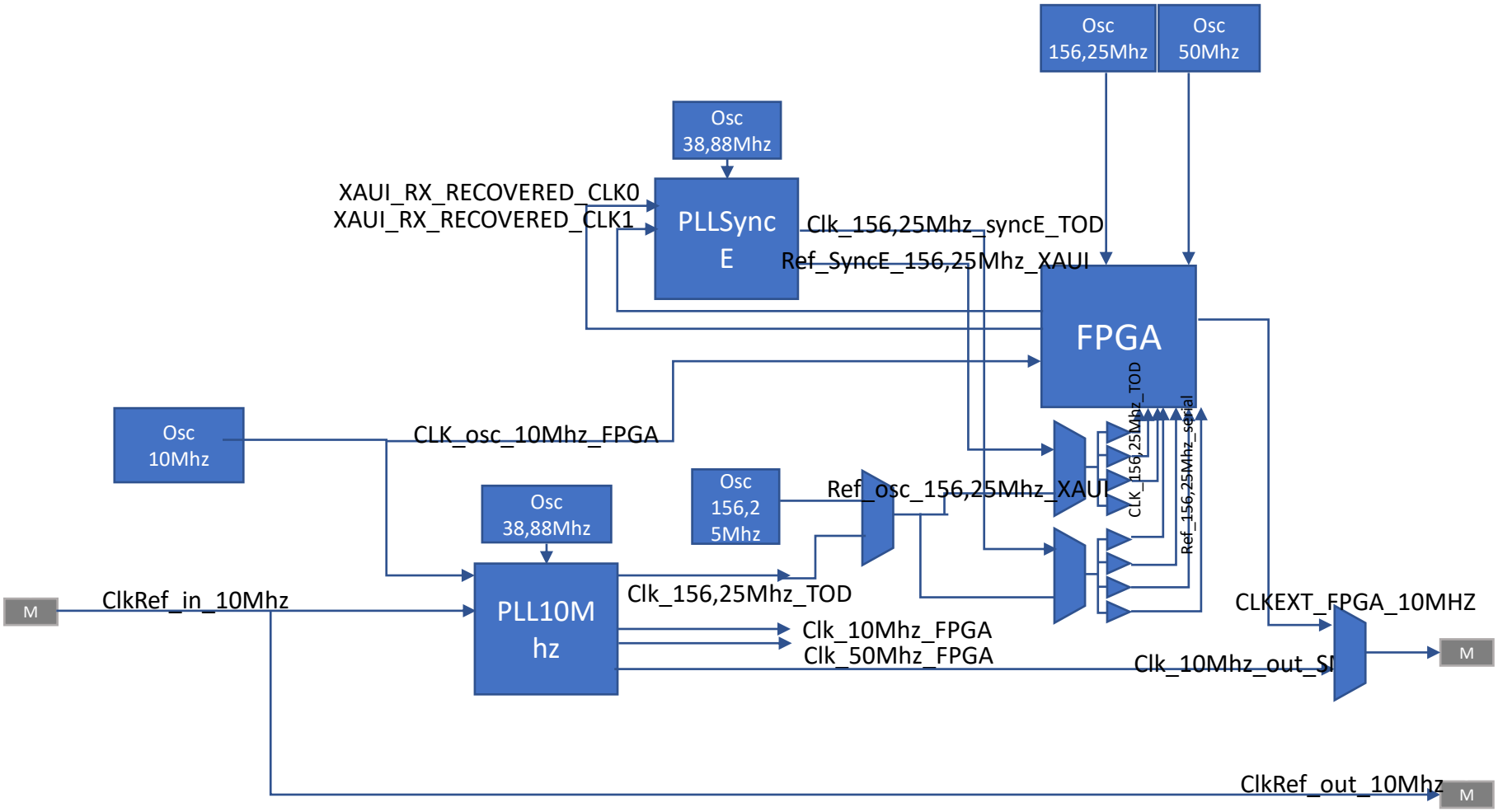
Osc
156,25Mhz
Osc
50Mhz
Osc
38,88Mhz
XAUI_RX_RECOVERED_CLK0
XAUI_RX_RECOVERED_CLK1
PLLSync
E
Clk_156,25Mhz_syncE_TOD
Ref_SyncE_156,25Mhz_XAUI
FPGA
CLK_156,25Mhz_TOD
Ref_156,25Mhz_serial
Osc
10Mhz
CLK_osc_10Mhz_FPGA
Osc
38,88Mhz
Osc
156,2
5Mhz
Ref_osc_156,25Mhz_XAUI
M
ClkRef_in_10Mhz
PLL10M
hz
Clk_156,25Mhz_TOD
Clk_10Mhz_FPGA
Clk_50Mhz_FPGA
CLKEXT_FPGA_10MHZ
Clk_10Mhz_out_S
M
ClkRef_out_10Mhz
M