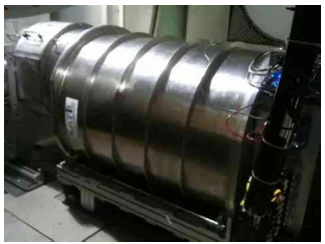
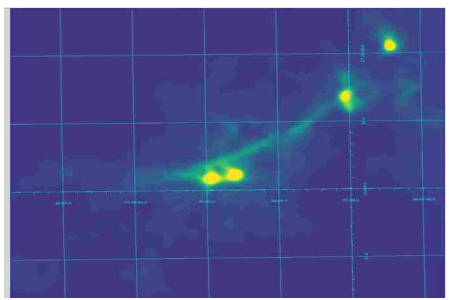
Détecteurs KIDs : Développements sur la chaîne d'acquisition

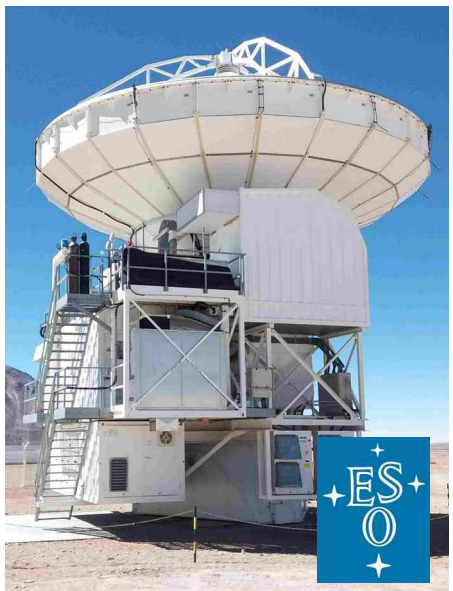
Julien BOUNMY

Kinetic Inductance Detector

- Astrophysics & Cosmology observations in millimeter wavelengths (100 to 300 GHz)
- NIKA2 (2015 - 30M (IRAM) at Pico de Veleta)
- KISS (2019-2021 – (IAC) 2.25M at Quijote)
- CONCERTO (2021-2023 – APEX (ESO) at Atacama)
- Nobeyama Radio Telescope (campaign in 2024, University of Tsukuba)
- Platforms at LPSC and Institut Néel

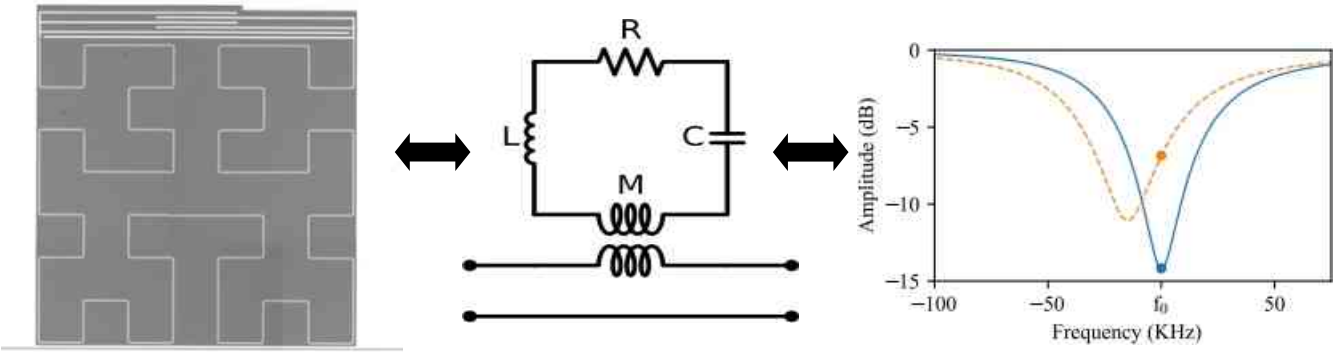






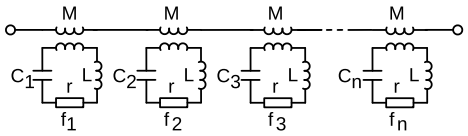
Kinetic Inductance Detector

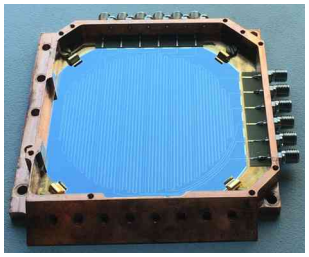
- **RF resonator**

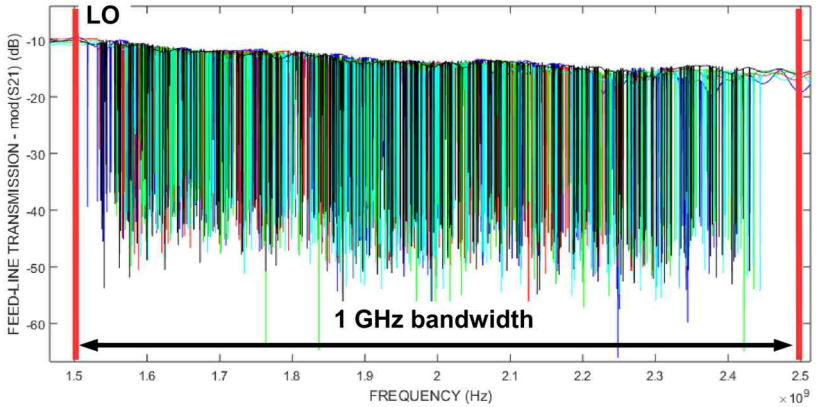


- ~ 100 mK
- ~ mm² ; $\nu \in [100, 300]$ GHz
- Q_{tot} ~ 10 000
- $f_0 \in [1, 3]$ GHz
- Δs_{21} ~ 15 dBm

- **Multiplexing**

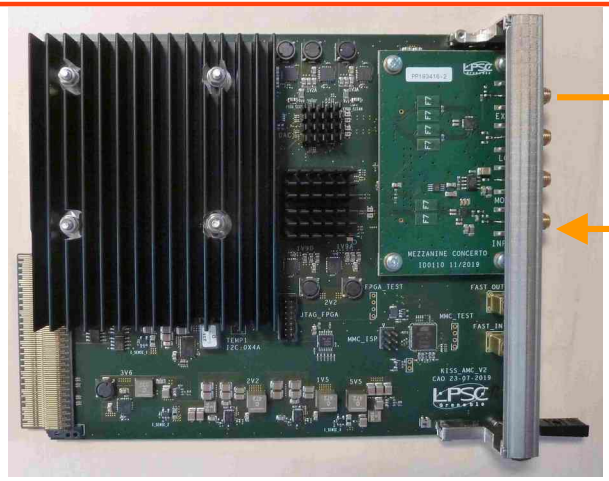


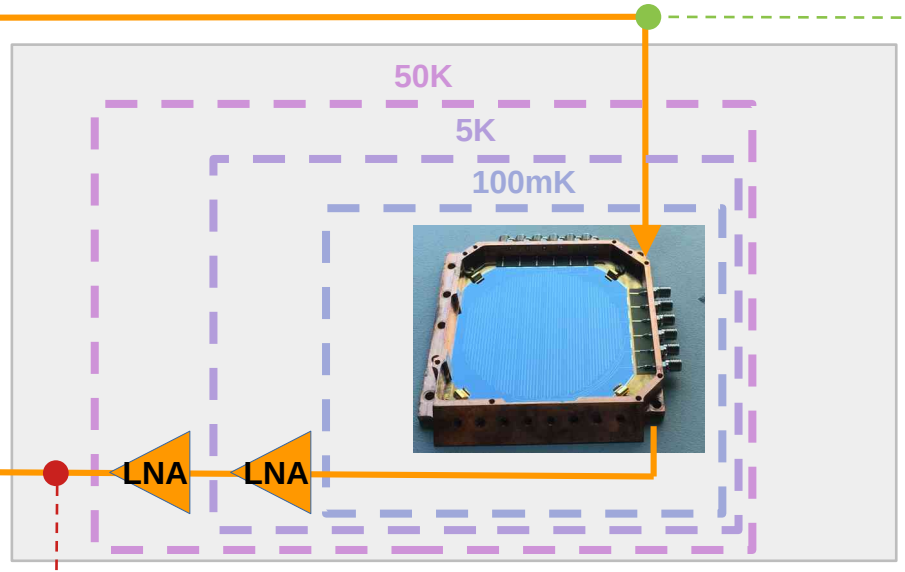




- **CONCERTO**
- 360 *tones* / RF line
- $f_0 \in [1,5 ; 2,5]$ GHz
- Δf ~ 150 kHz
- $f_j - f_i$ ~ 2,5 MHz
- ø ~ 120 mm
- Δs_{21} ~ 40 dBm

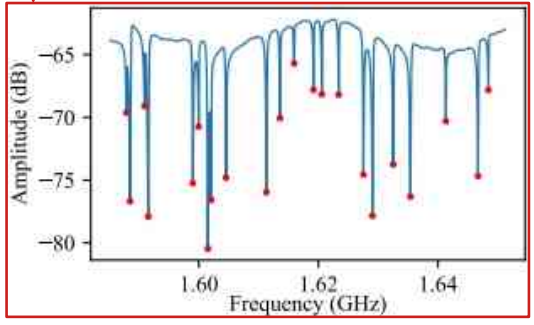
Kinetic Inductance Detector

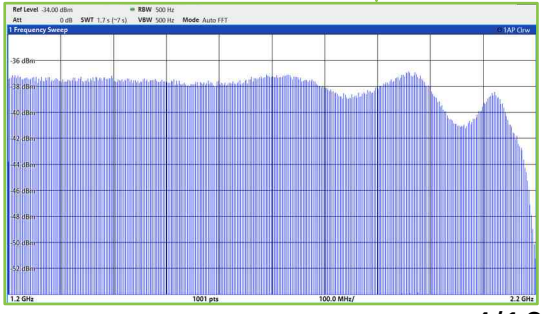




- **KISS_AMC_V2 Board**
- CONCERTO (2021)
- 400 Tones on 1GHz BW
- Modular RF mezzanine for comb frequency shift

- Xilinx XCKU60 FPGA
- AD9136 DAC : 16 bits dual 2GSps
- ADC12D1000 ADC : 12 bits single 2GSps





Kinetic Inductance Detector

Issues

- Need to update and standardize the aging platforms (Institut Néel, LPSC, IRAM...)
- New potential experiments
  - KAIROS : 30,000 KIDs (70 boards estimated)
  - CRESZENDO : 18,000 KIDs (20 boards estimated)
- Number of detectors increases significantly
  - CONCERTO (2021 : 4400 KIDs for 12 boards)
- Budgets restrains, Components costs increasing

→ Looking for ways to reduce costs & still increase the capabilities.

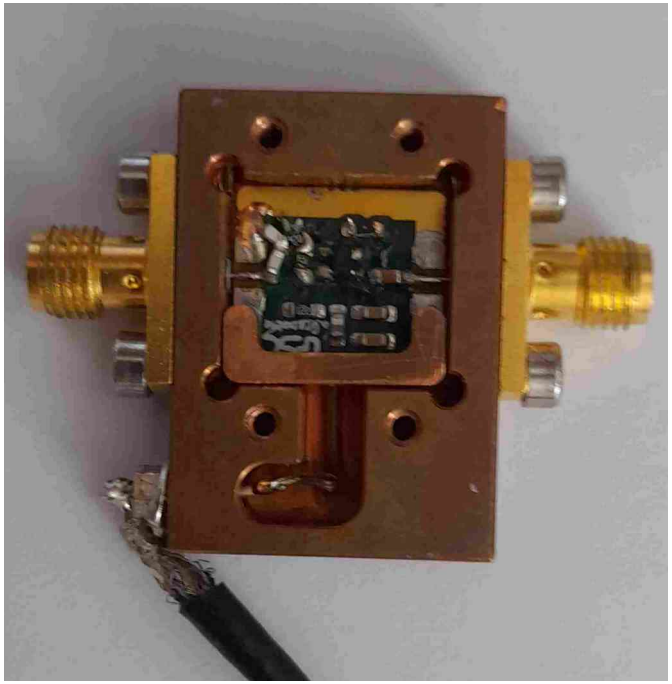
Developments & On-going designs

- Low Noise Amplifier in Cryostat
- Mezzanine with Embedded LO
- Optimized FPGA Signal Processing
- KID_READOUT_V3
- FOCUS_KID_READOUT

Low Noise Amplifier in Cryostat

- Used amplifiers are costly (~4000€ per channel) and take a lot of space
- Custom design solution based on Hetero-junction Bipolar Transistor BFP740.
- Plan is to produce boards to optimize cost and space (~900€ per channel estimated)
- Measurements in cold temperatures show significant BW transmission cuts.
- BFP740 production is at end of life.

→ Work is still in progress and important as cost and integration are major issues.

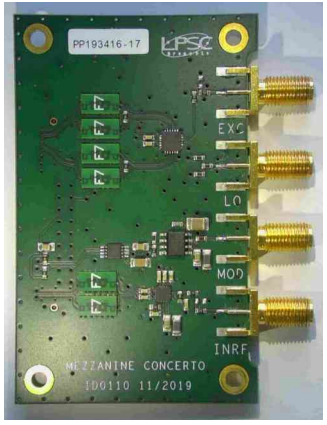


Design & CAO **: Christophe HOARAU**

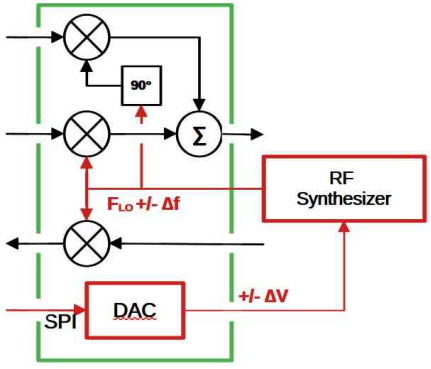
Mezzanine with embedded LO

- Mezzanine provides 2GHz frequency shift for excitation comb using an external RF synthesizer (**typical : HSM2001B ~6000€**).
- Calibration points produced with Synthesizer's modulation input (ΔV voltage adds Δf frequency on F_{LO}).
- Apprenticeship to explore solution with a ADF4350 chip (**up to 4,4GHz for 15€**).

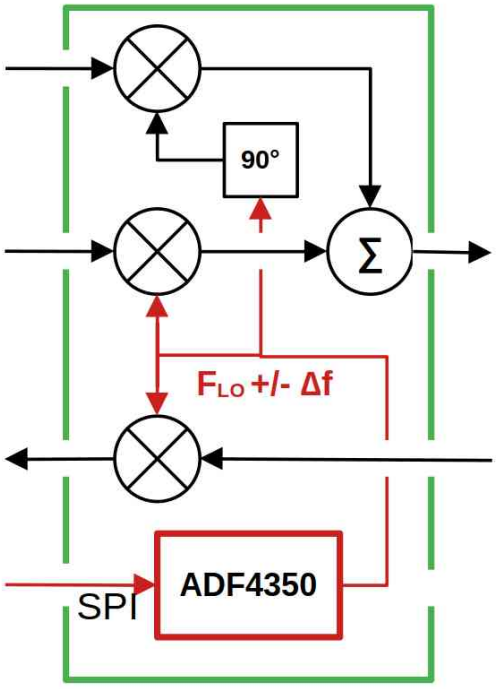
→ **Reduced number of I/Os, cables & dependency on singular expensive equipment.**



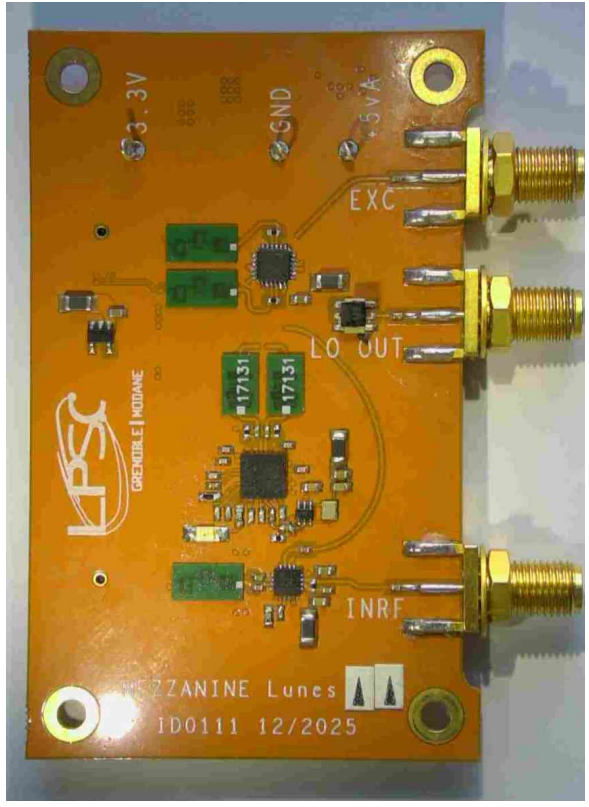
OLD



NEW

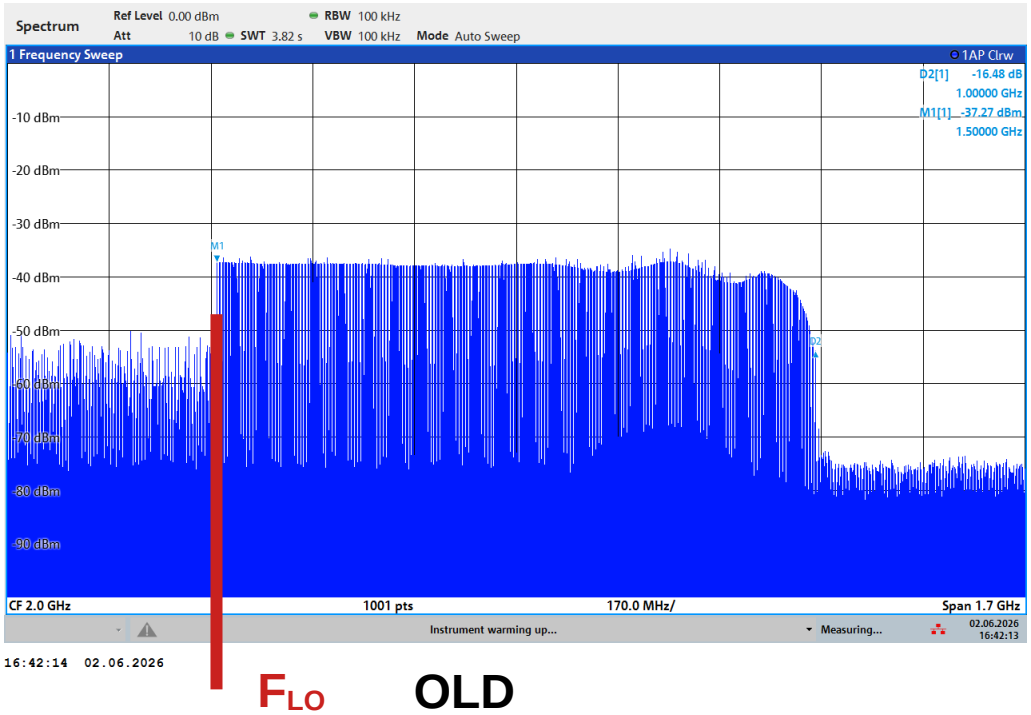


Câblage @LPC !

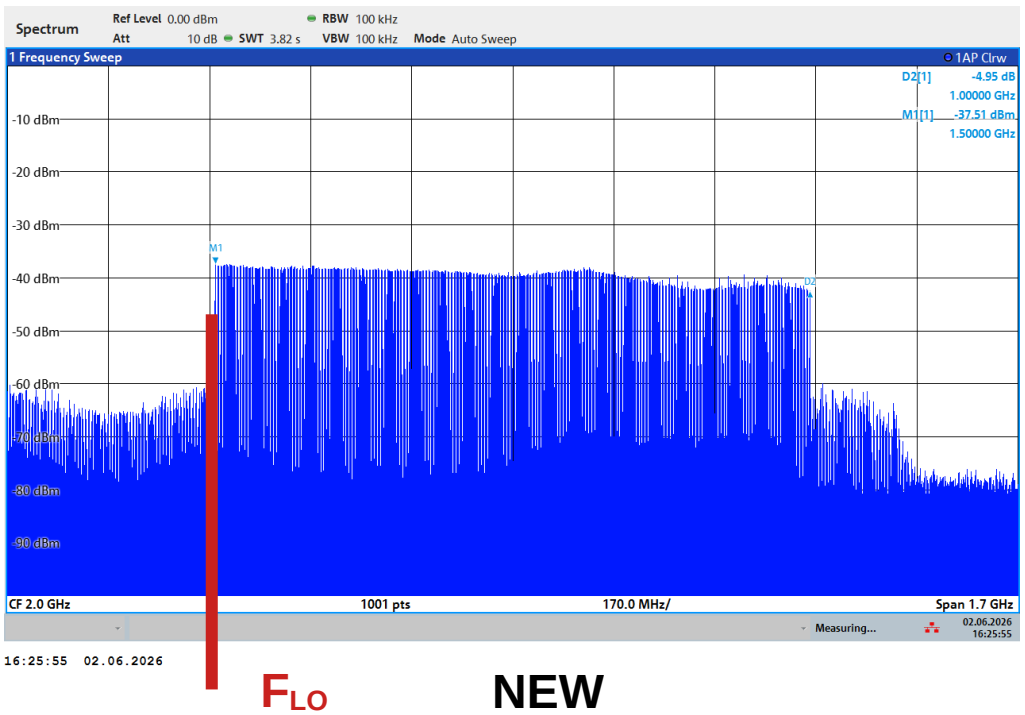


Design **: Lunes PELTIER**
CAO **: Jonathan WAQUET**

Mezzanine with embedded LO



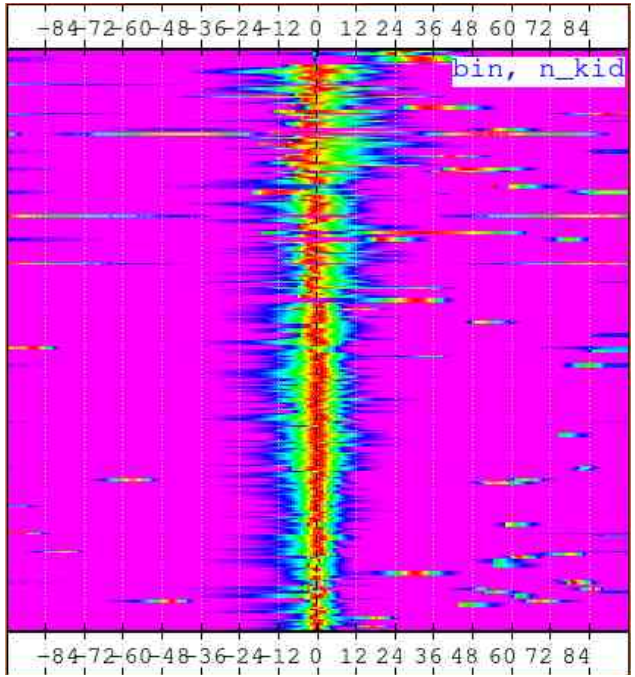
F_{LO} **OLD**

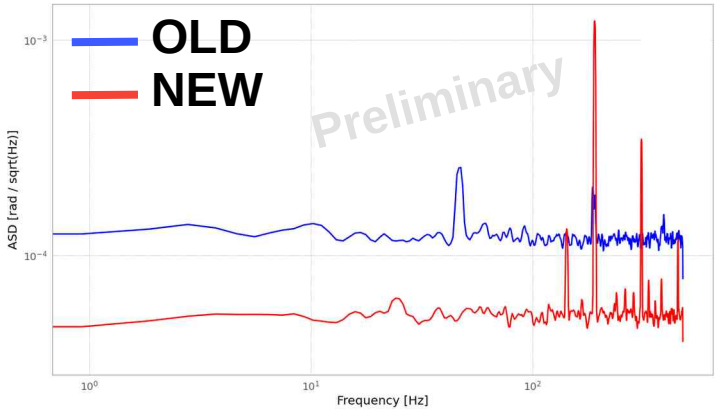


F_{LO} **NEW**

Mezzanine with embedded LO

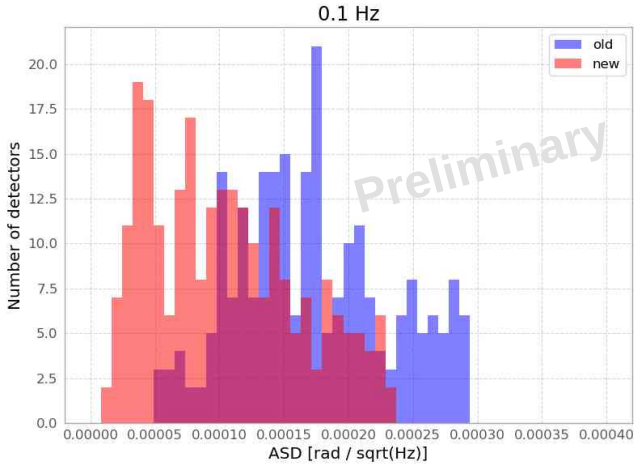
Data analysis **: Benedetta KALEMI**

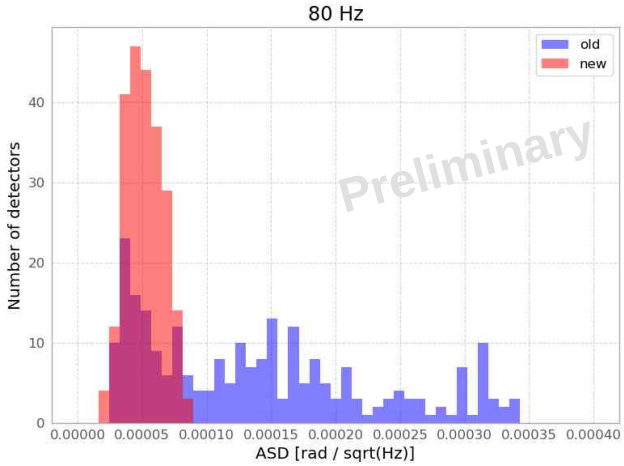




- Frequency sweep is functional & allows acquisition system to identify detectors.
- **Preliminary** noise measurements on detectors : Floor noise level is lower but spikes appear.

→ Work still in progress but the concept is interesting. Less noisy chip may be required.





Optimized FPGA Signal Processing

Thesis **: Mounir ABDKRIMI**

- Modeling of the readout chain and optimization of digital signal processing on FPGA for superconducting kinetic inductance detectors. Signal and Image processing.
  Université Grenoble Alpes [2020-..], 2025. English. ⟨NNT : 2025GRALT045⟩. ⟨tel-05447999⟩

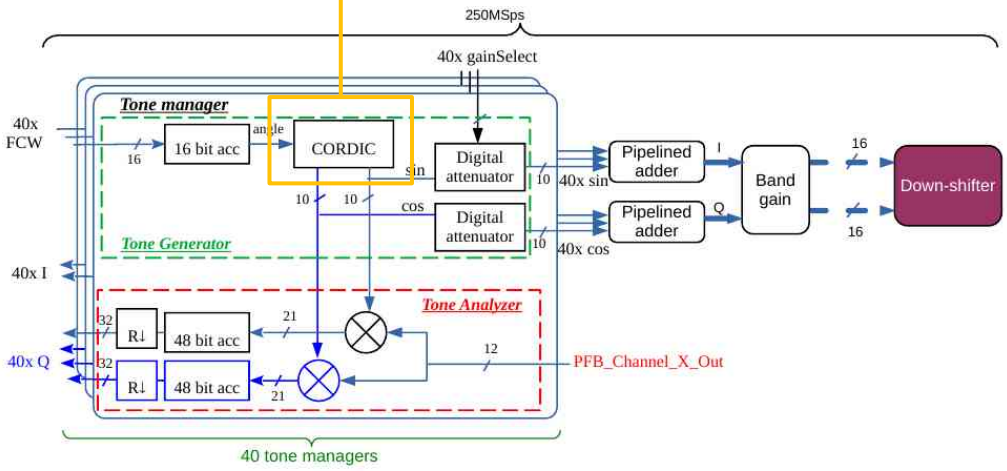


Figure 3.6: Band Manager architecture. It is composed of 40 parallel tones managers, each of them is composed of a tone generator and a tone analyzer.

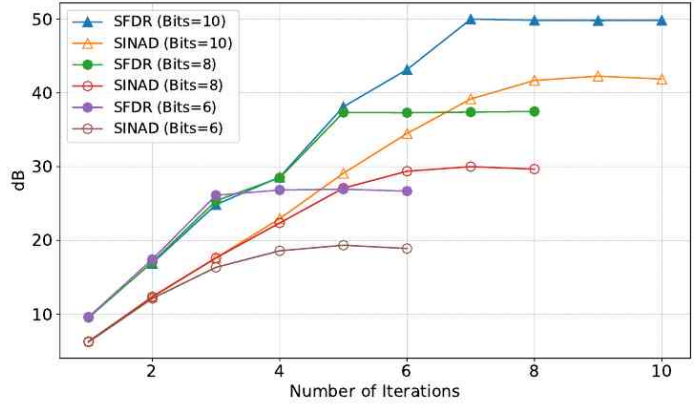
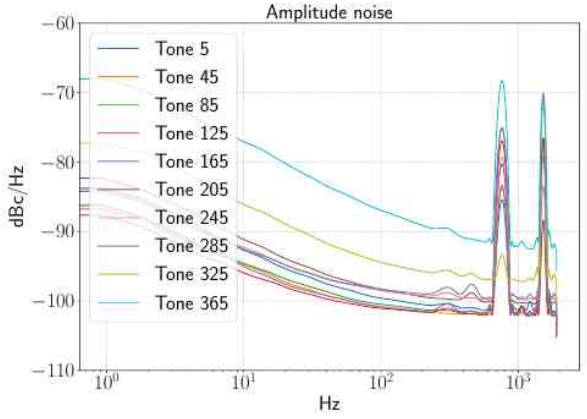


Figure 3.47: SINAD and SFDR as functions of number of iterations for different bit widths.

Optimized FPGA Signal Processing

OLD



-20dB

NEW

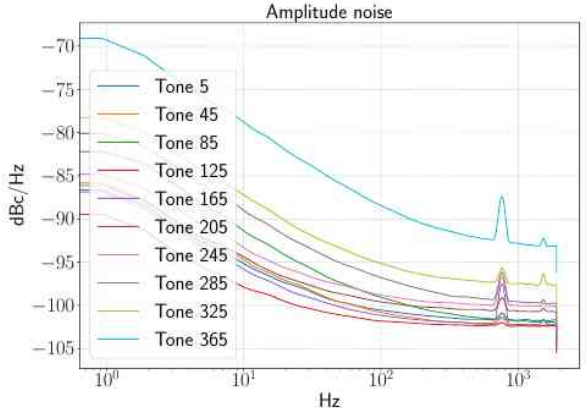


Table 4: FPGA resource utilization before and after optimization

Resource	Available	Original firmware	Optimized firmware	Savings
LUTs	331,680	215,228 (64.89%)	138,695 (41.82%)	−76,533 (-23.07%pt)
FFs	663,360	346,539 (52.27%)	214,993 (32.41%)	−131,546 (-19.86%pt)
DSPs	2,760	1,953 (70.76%)	1,153 (41.78%)	−800 (-28.98%pt)

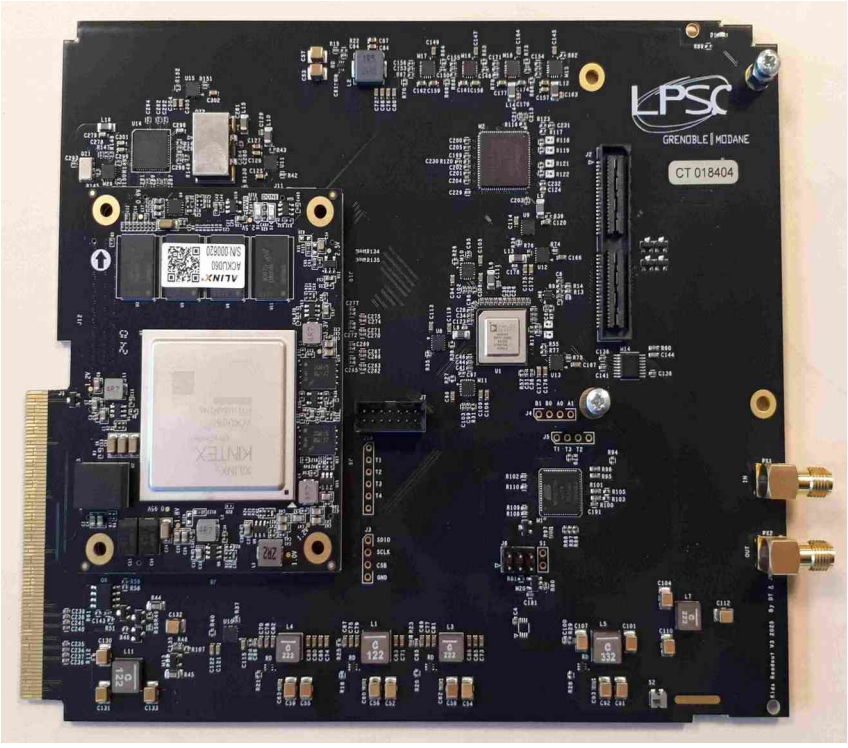
- Signal processing induced peaks are significantly reduced (-20dB).
- Depending on the optimization choice, firmware's capability increases from 400 tones up to 800 tones.
- Up to 600 tones without impacting signal noise is possible.

→ **Same hardware but more detectors readout is possible.**

→ **Parasitic noise also has been significantly reduced.**

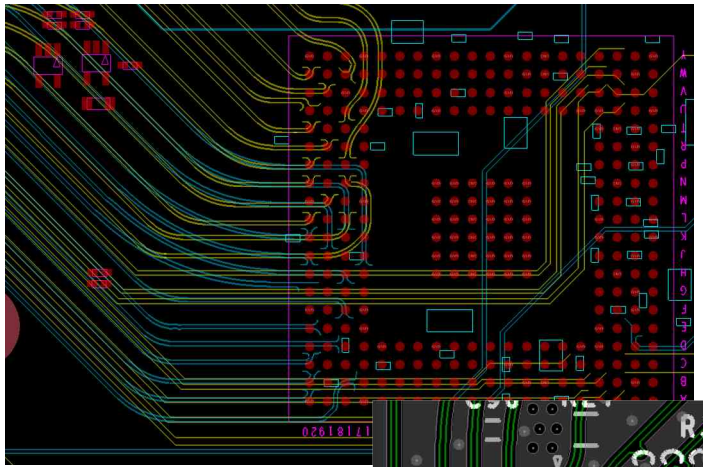
KID_READOUT_V3

Design **: Damien TOURRES**
CAO **: Jonathan WAQUET**
Firmware **: Olivier CHOULET**

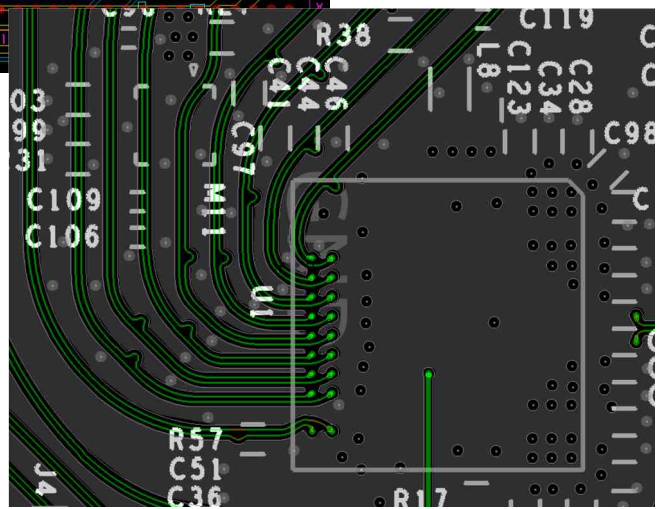


- **Low cost version of KISS_AMC_V2**
- **FPGA : ALINX's System On Module**
  - Xilinx XCKU60 FPGA
  - Single 12V power input
  - Cheaper than FPGA chip (~500€ vs ~3000€ per unit)
- **AD9136 DAC** : 16 bits dual 2GSps
- **AD9699 ADC** : 14 bits single 3GSps (used @ 2GSps)
  - Cheaper than previous ADC (~900€ vs 1300€)
- Same RF mezzanine format
- AMC back-end connector on board

KID_READOUT_V3



ADC12D1000

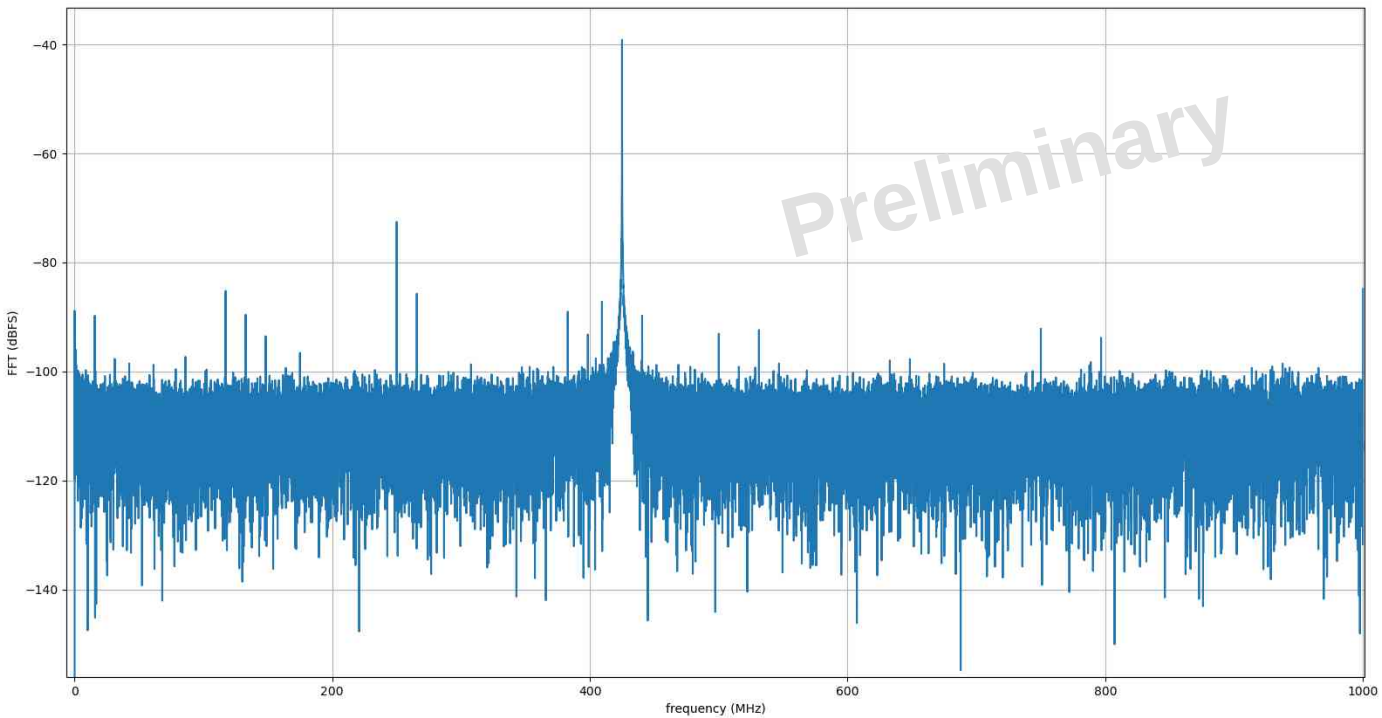


AD9699

- **AD12D1000 12-bits ADC (KISS_AMC)**
  - 2GSps Single input
  - 24 LVDS pairs (48 traces) @1Gbps
  - Parallel bus
  - 2 layers for high-speed signals
- **AD9699 14-bits ADC (KID_READOUT_V3)**
  - 3 GSps (Used @2GSps)
  - 8 MGBT pairs (16 traces) @5Gbps
  - JESD204B-fw (support added in Gitlab IN2P3)
  - 1 layer for high-speed signals
- New PCB board has 6 layers instead of 12
  - 1900€ vs 3300€ (unit cost)
- SOM provides all the power supplies for FPGA : Design needs less components

→ **Reduced costs & design time significantly.**

KID_READOUT_V3



→ **Work in progress but floor noise level is similar to manufacturer's specifications.**

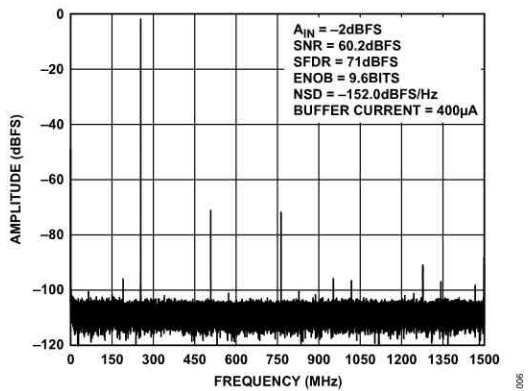
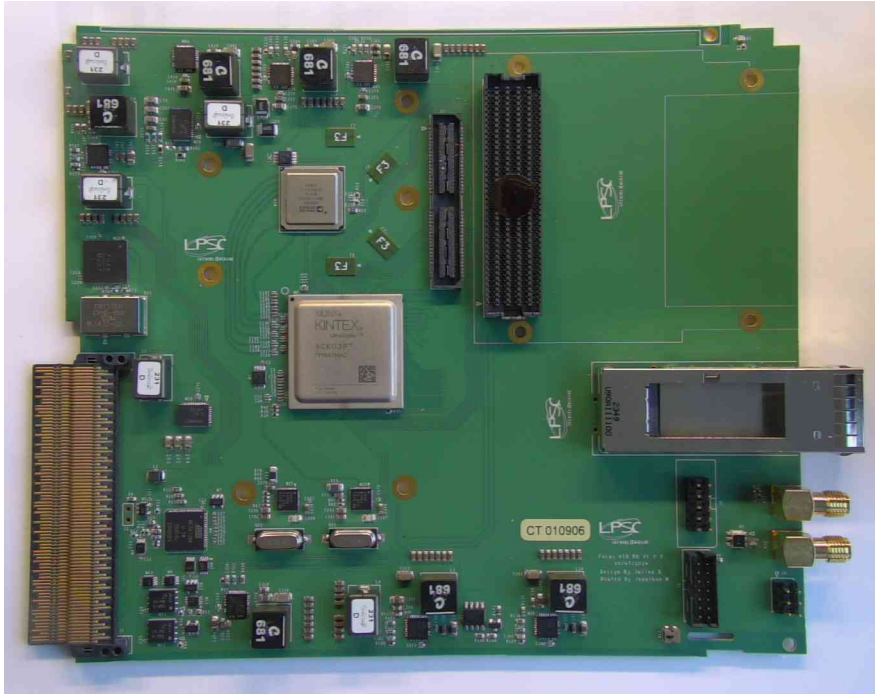


Figure 6. Single-Tone FFT at f_{IN} = 255 MHz (NSD Is Noise Spectral Density)

FOCUS_KID_READOUT

Design **: Julien BOUNMY**
CAO **: Jonathan WAQUET**



- **Wider Frequency Comb Prototype**
  - 2GHz capability, planning for 1.5GHz
- **FPGA :** Xilinx Kintex Ultrascale+ XCKUP05
- **AD9082 Mixed Signal Front-End**
  - Dual DAC outputs up to 12GSps
  - Dual ADC inputs up to 6GSps
  - ~2000€
  - JESD204B & JESD204C
- PCB : Megtron, 14 layers

→ On-going work to test the chip

→ Adding AD9082's support in JESD204B-fw

Thank you for your attention !