

# Microelectronics at CNRS Nucléaire & Particules

Frédéric Morel, on behalf of MI2I

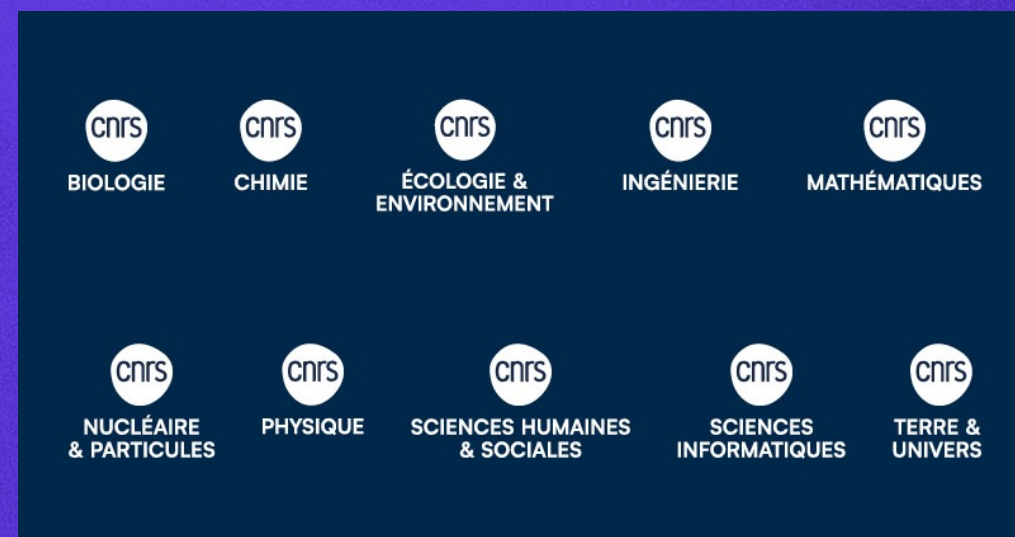
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# CNRS, IN2P3, and MI2I

# CNRS in brief

## National Centre for Scientific Research

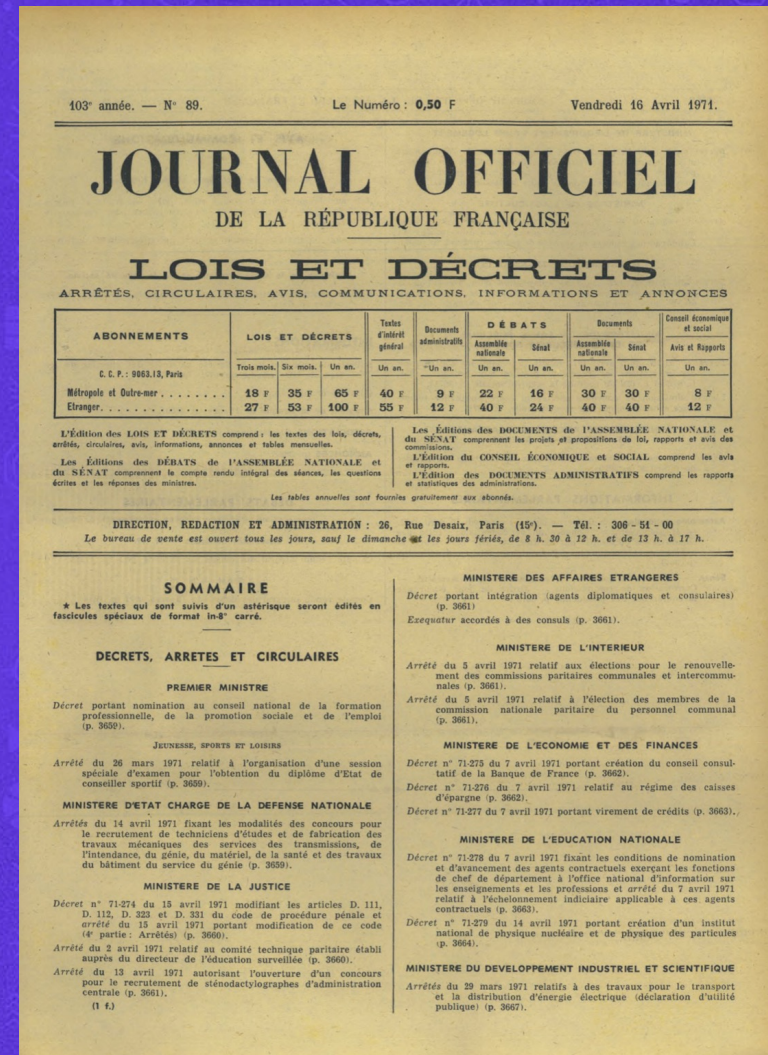
- **Founded in 1939**
- **Largest public research body in Europe and the second largest in the world**
- **CNRS is the only French organisation active in all scientific fields**



# CNRS Nucléaire & Particules

Originally known as IN2P3

- Founded in 1971
- Coordinates R&D in nuclear and particle physics
- Now also covers astroparticle physics



# CNRS Nucléaire & Particules

## A Unique CNRS National Institute

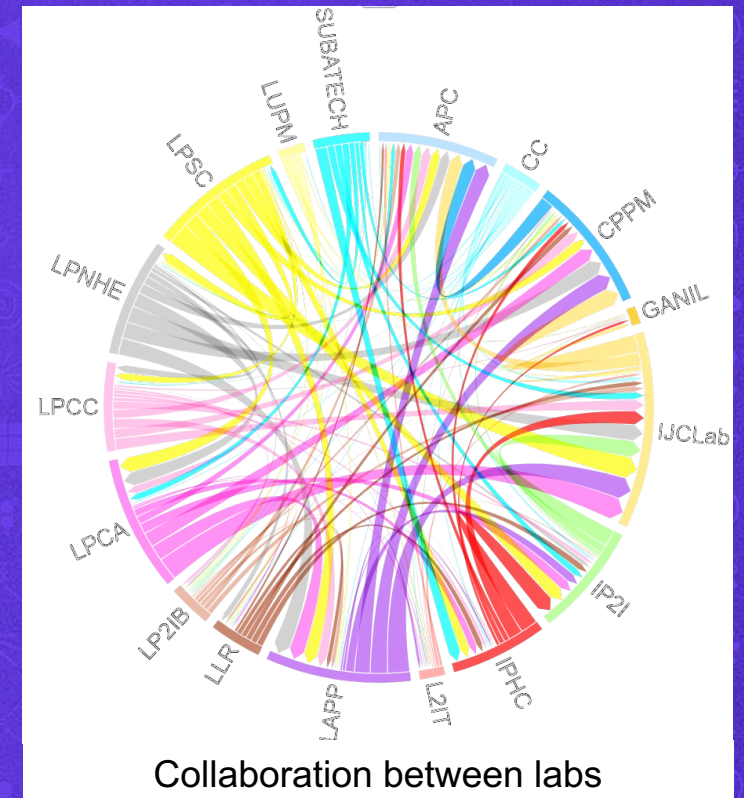
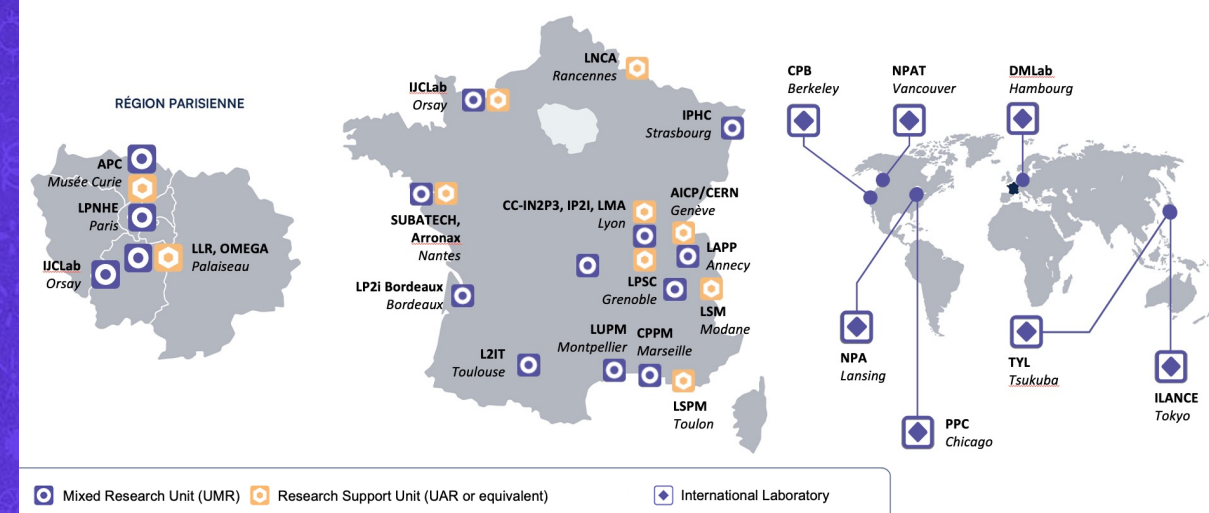
- A reduced number of labs
- A large proportion of engineers and technicians
  - 269 engineers with PhDs

<b>Staff</b> (perm. & Fixed-term)	<b>CNRS</b>	<b>IN2P3</b>	<b>Outside CNRS</b>
Total	34,700	2,340	1,120
Scientists	29,400	900	850
Engineers & Technicians	5,300	1,440	270
<b>Laboratories</b>	<b>CNRS</b>	<b>IN2P3</b>	
In France	1,100	24	
Aboard	85	7	

# CNRS Nucléaire & Particules

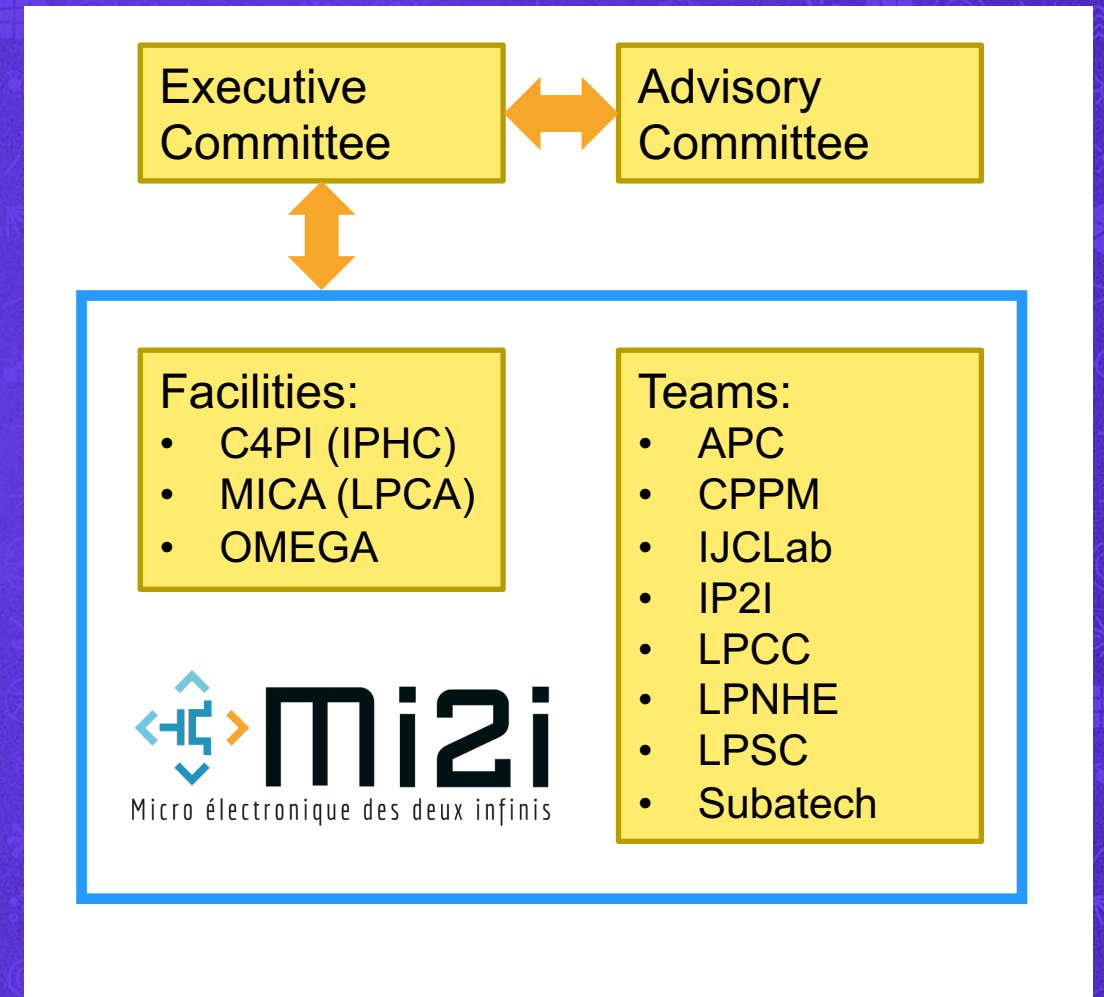
## A Collaborative Lab Network

- Laboratories are located close to major universities
  - Spread across the entire country
- Impossible to duplicate all expertise in every location
  - Need to work together



## Microelectronics for the Two Infinities

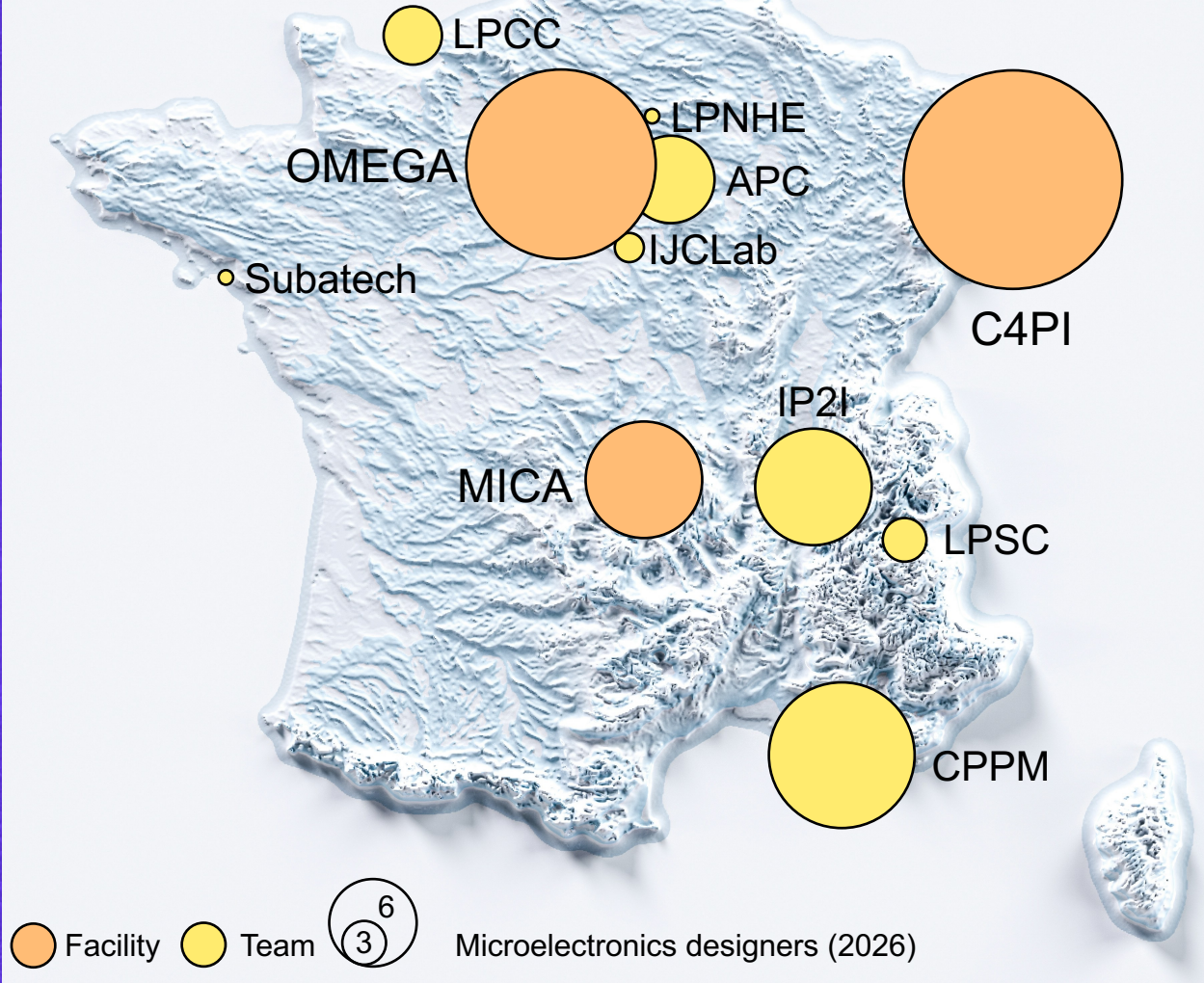
- **Federated Network**
  - Internal single point of contact
- **Network Actions**
  - Communication
  - MI2I Days
  - Specific working groups (e.g., timing)
- **Federation Actions**
  - CNRS Microelectronics School
  - CAD government contract support
  - CAD environment development



# MI2I

## Workforce

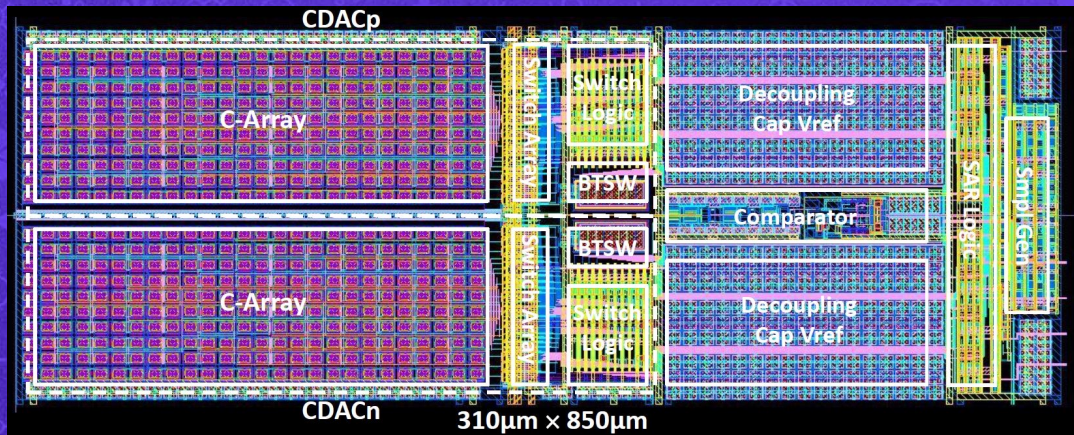
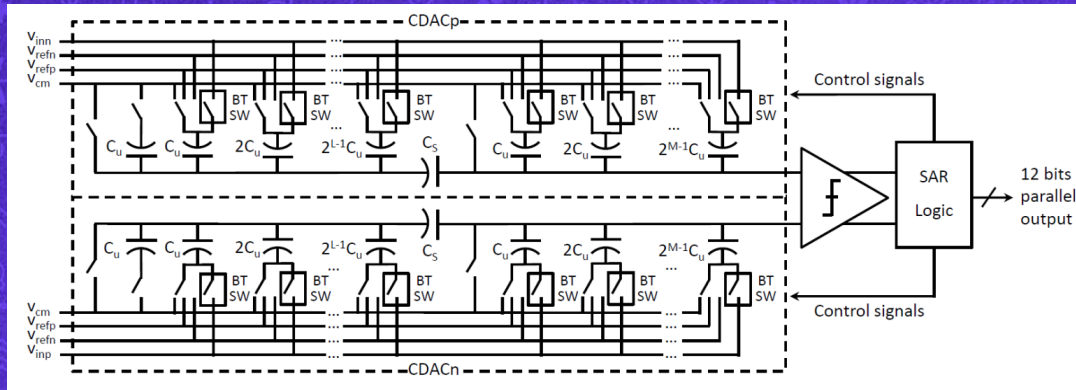
- 3 facilities
  - C4PI (IPHC), MICA (LPCA), OMEGA
- 8 teams
  - APC, CPPM, IJCLab, IP2I, LPCC, LPNHE, LPSC, Subatech
- Around 80 engineers
  - 60 in microelectronics



2

# Sampling: ADC, TDC, and Waveform sampler

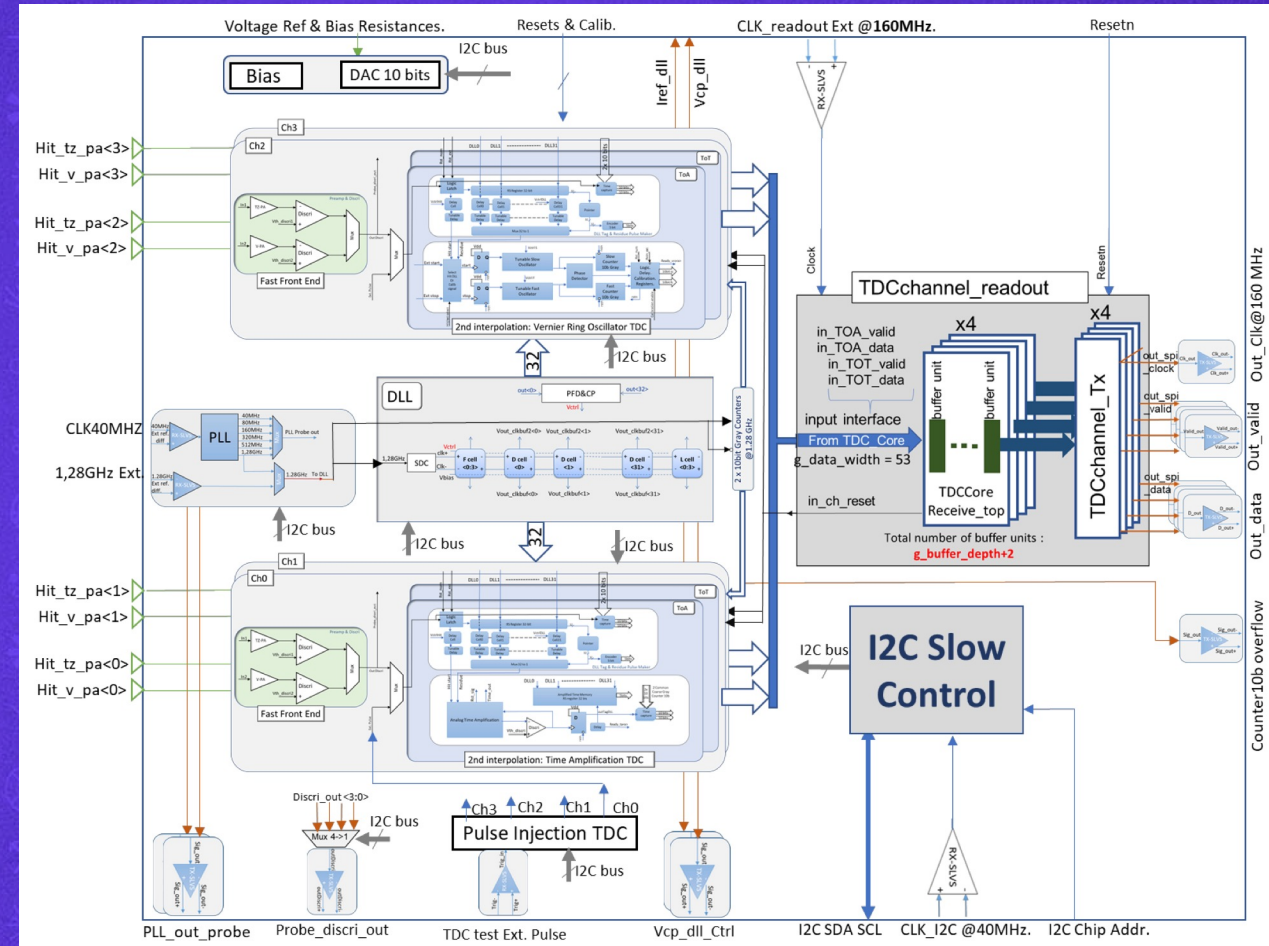
# 12bits 10MS/s ADC SAR



- Tower 180 nm
- IPHC<sup>1</sup>/LPSC<sup>2</sup>/APC<sup>3</sup> IN2P3 collaboration
  - 1M. Kachel / 1R. Sefri / 2F. Rarbi / <sup>3</sup>F. Voisin/ <sup>3</sup>S. Blin
- Identified as CERN DRD 7.6 activity
  - IP for MAPS
- Compatible with high-speed/high-resolution A/D converters requirements for IN2P3 projects
  - IPHC monolithic CMOS pixels
- First version submitted in 2025

# FastTime: A Multi-Channel ASIC for a Complete Fast and High-Resolution Time Measurement Chain

- TSMC 130 nm
- IN2P3 collaboration: IJCLab, IP2I, LP2IB, LPC, LPCA, OMEGA
- Targeted resolution:  $\sim 1$  ps
- Targeted input charge:  $\sim 1$  pC
- ToA and ToT measurements
- DLL @ 24 ps
- 1<sup>st</sup> stage interpolation:
  - Residue pulse maker
- 2<sup>nd</sup> stage interpolation:
  - Vernier ring oscillator TDC
  - Time amplification TDC
- Front-end:
  - Trans-Impedance preamplifier
  - Voltage Preamplifier



Counter10b overflow Out\_data Out\_valid Out\_Clk@160 MHz

# PLAS : PipeLined Asymmetric Switched Capacitor Array for GRIT experiment (Nuclear Physics)

- **PLAS\_v2** → Measured resolution 8 bits in TSI 180nm CMOS (no more available)
  - Designed by IFIC Valencia.
- **PLAS\_v3** → XFAB XH018 technology, submission in oct. 2026
  - Redesign by LPC Caen.
- Target resolution : 10 bits (noise expected below 340  $\mu$ Vrms with FS=1,2V)
- Sampling Features:
  - 32 inputs with independent trigger
  - Samples at 200 MHz (Write Clock=100MHz)
  - 224 samples captured per pulse
    - 32 before trigger (pre-trigger samples)
    - 192 after trigger (post-trigger samples)
  - No deadtime
- Reading Features:
  - 8 output queue slots
  - Single differential analog output
  - Serial readout at 50 MHz (Read Clock)
  - Needs external ADC
  - Designed for triggerless readout

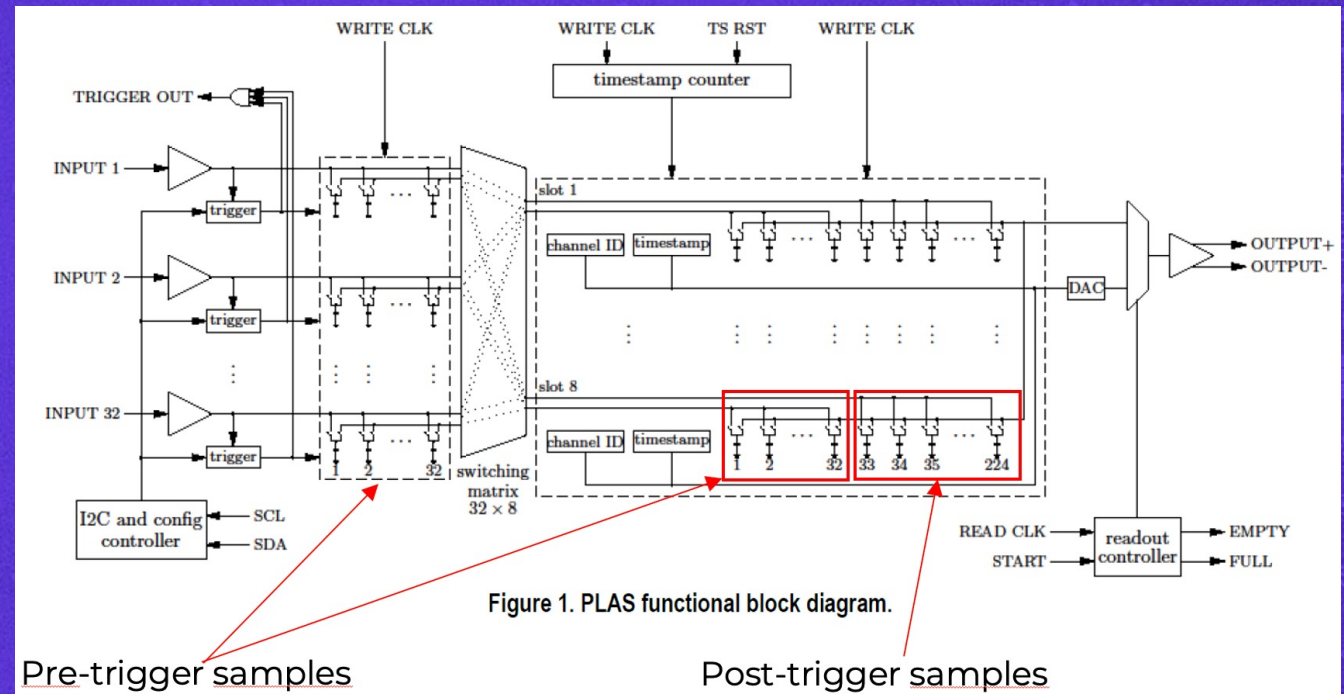


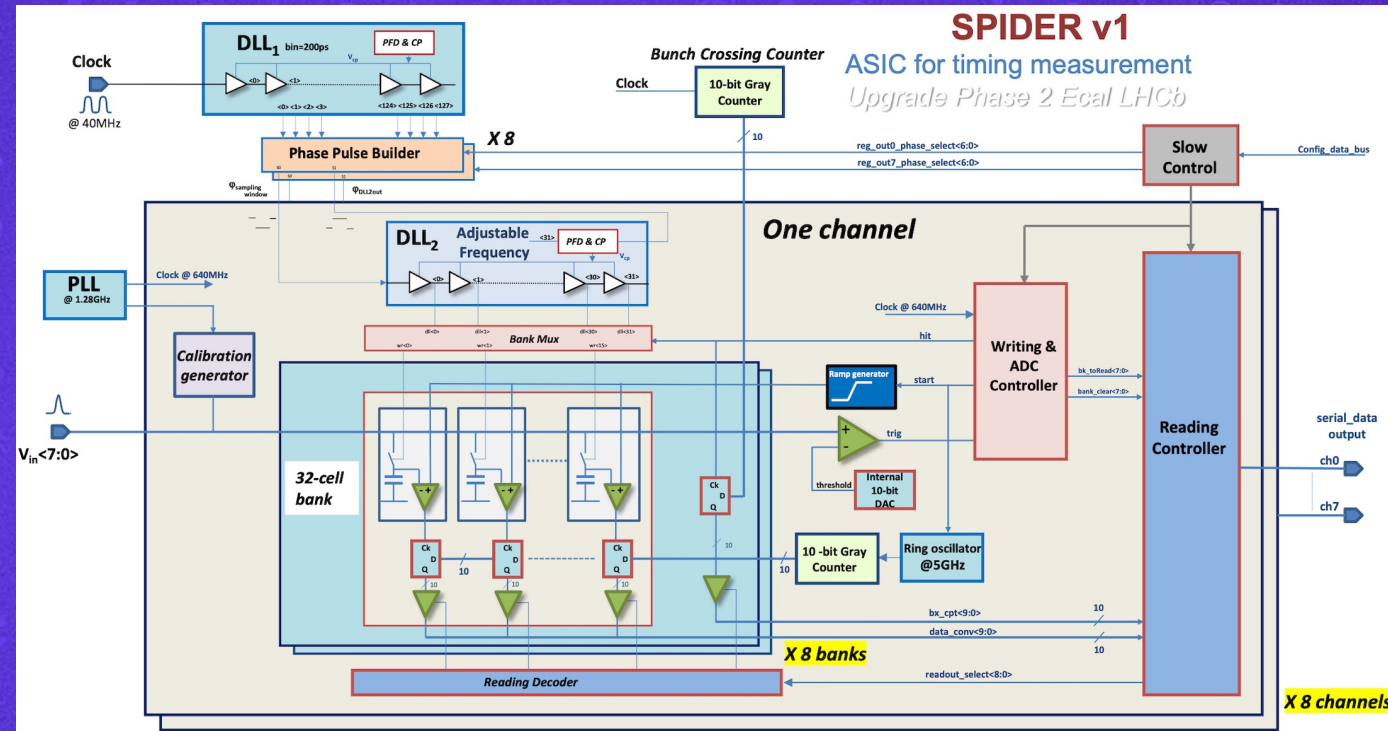
Figure 1. PLAS functional block diagram.

Pre-trigger samples

Post-trigger samples

# SPIDER: a Waveform Digitizer ASIC for picosecond timing in LHCb PicoCal

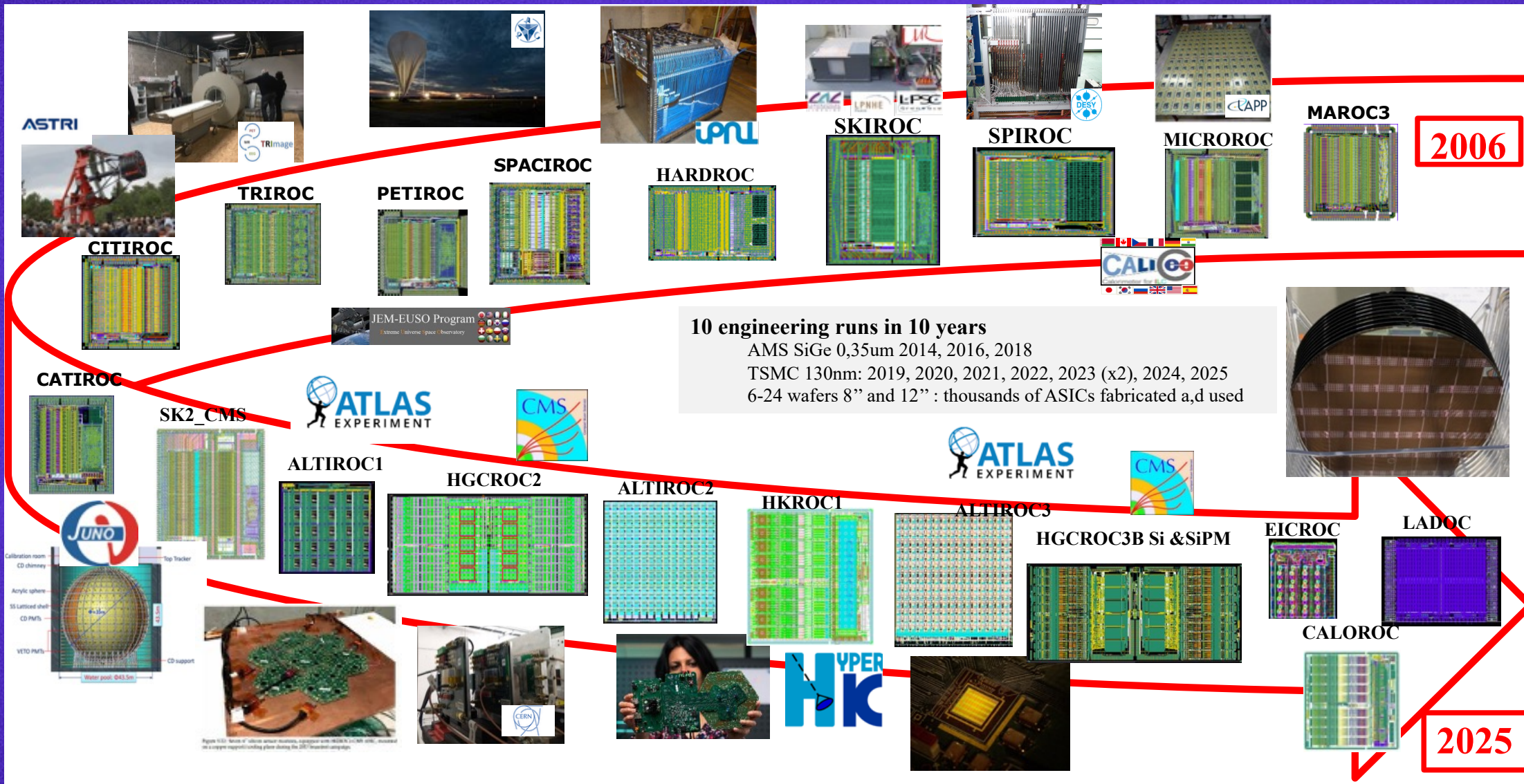
- TSMC 65 nm
- IN2P3 members: IJCLab, IP2I, LPC, LPCA
- 2 self-triggered channels (V0), targeting 8 on V1
- Sampling period 50ps to 600ps
- Adjustable sampling window w.r.t LHC clock
  - + trigger enable window
  - 32-sample waveform
- Analog bandwidth compatible with rise time ~250ps
- Noise < 0.5mV
- 10-bit conversion (range 0-800 mV)
- Max conversion time 200ns, optimized for positive pulses
- 8-bank derandomization buffer
  - Simultaneous writing, conversion (1 or several banks) and readout
  - Rotating FIFO
- Peak finder: allows to read a portion (e.g. 8 samples rising edge) => reduce extraction time



# 3

# Calorimetry

# OMEGA: ASICs fabricated and installed 2006-2025

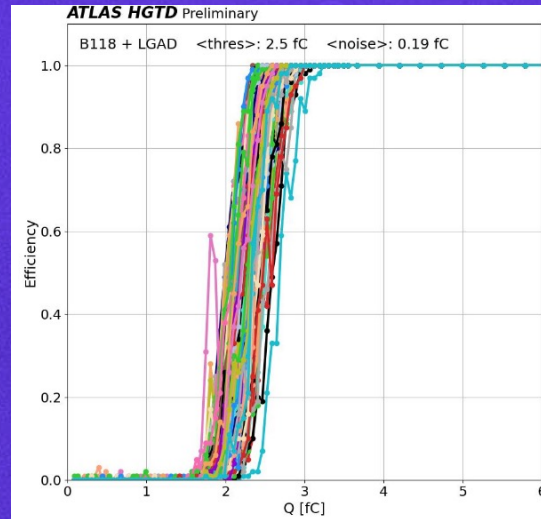
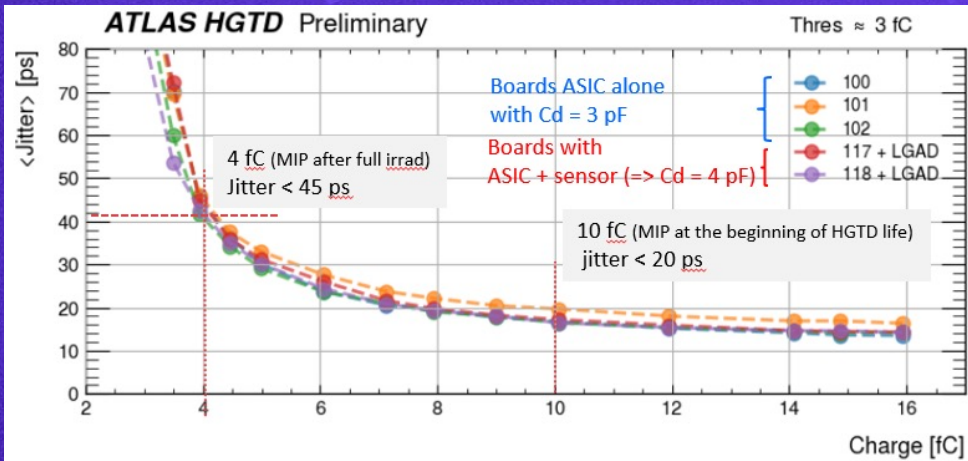
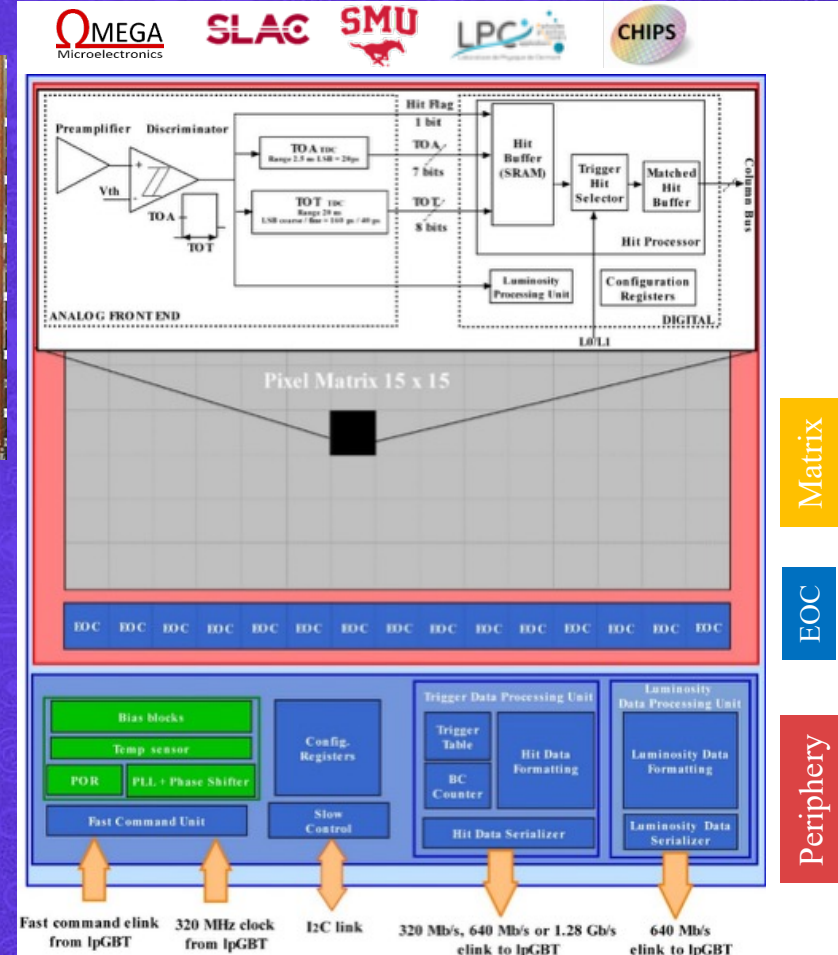
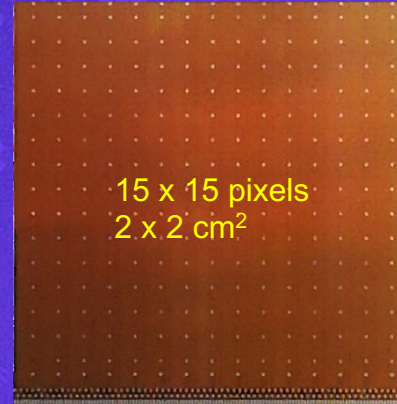


# ATLAS HGTD: ALTIROC



## • ALTIROC: Atlas Lgad Timing Integrated ReadOut Chip

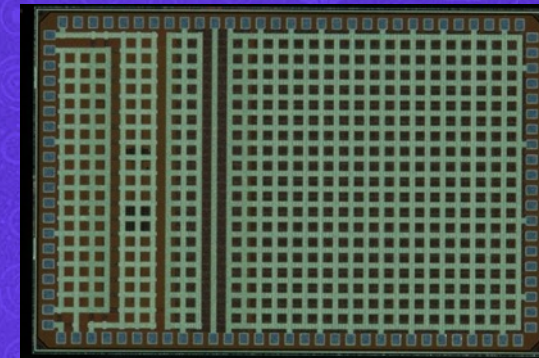
- 20 ps silicon timing detector for jet id and pileup rejection
- Active radius from 120 mm ( $\eta = 4$ ) to 640 mm ( $\eta = 2.4$ )
- ➔ 2.5 e15 neq/cm2 and 200 Mrad at the end of HL-LHC (4000/fb)
- Readout of 225 (1.3 mm)<sup>2</sup> LGAD sensors (Cd= 4 pF)
- 1 GHz preamp & discriminator + 20 ps TDC to measure ToA & ToT
- 225 wafers produced in 2025



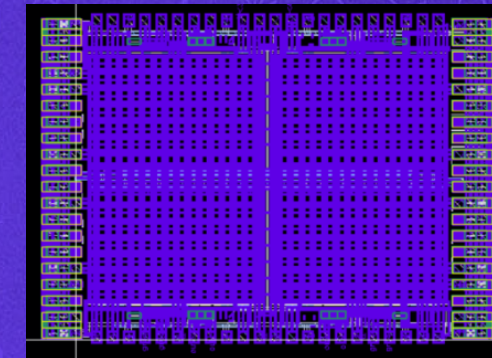
# ATLAS: LArg Calorimeter Upgrade



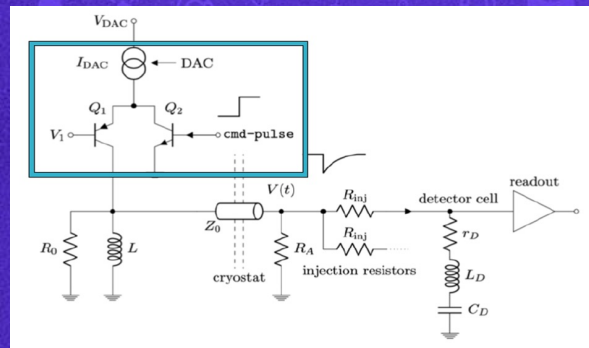
- **LADOC (Liquid Argon DAC Output Chip)**
  - Provides 0.1% accuracy current over 16 bits dynamic range for calibration of LAr Electromagnetic Calorimeter
  - Maximum current 320 mA
  - 6000 chips fabricated in 2025 in ATLAS/EIC combo run
- **CLAROC (Calibration Liquid Argon Output Chip)**
  - Provides a fast pulse similar to liquid argon signal up to - 7.5 V in 50  $\Omega$
  - Technology XFAB SOI 180nm, 6000 chips fabricated in 2024



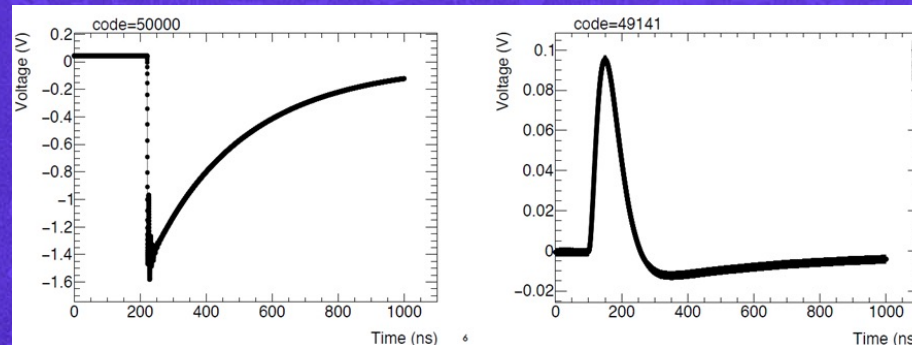
LADOC layout



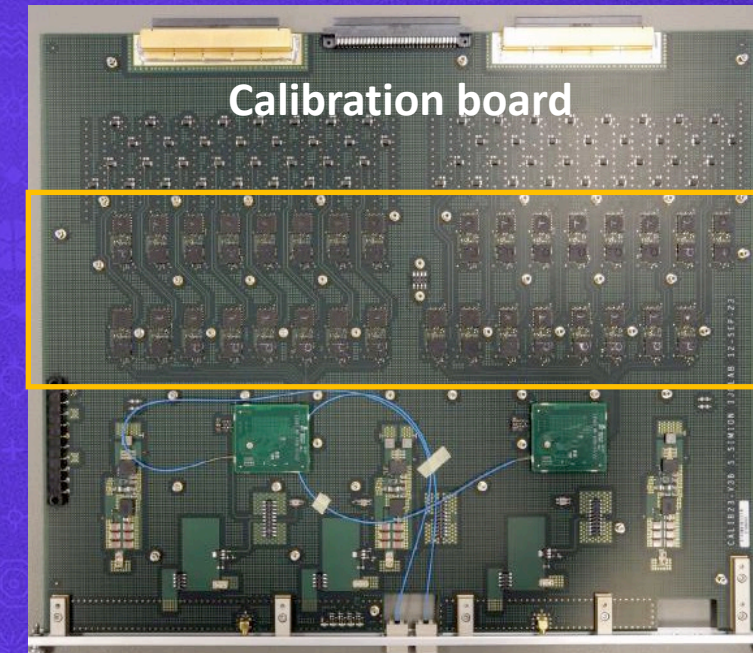
CLAROC layout



Calibration principle



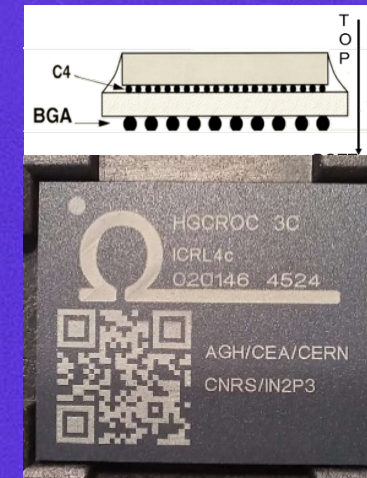
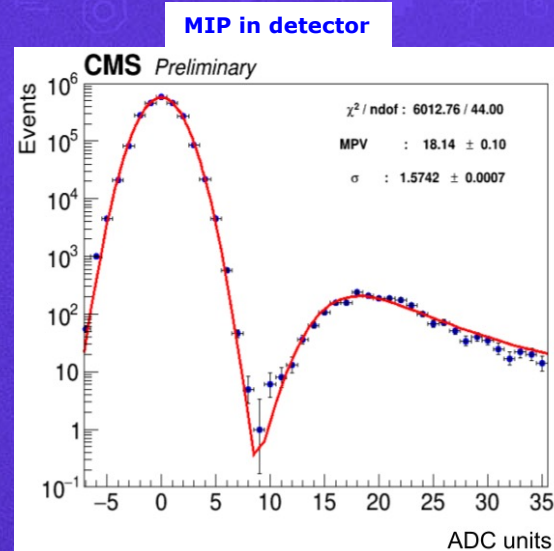
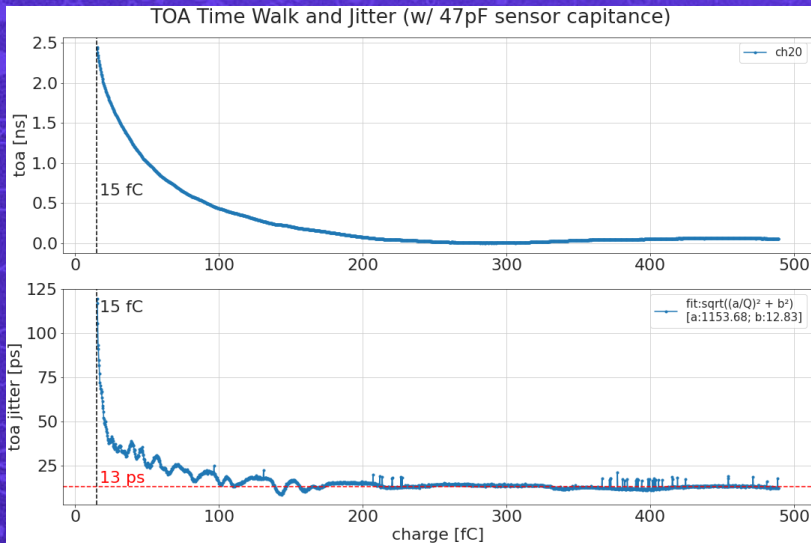
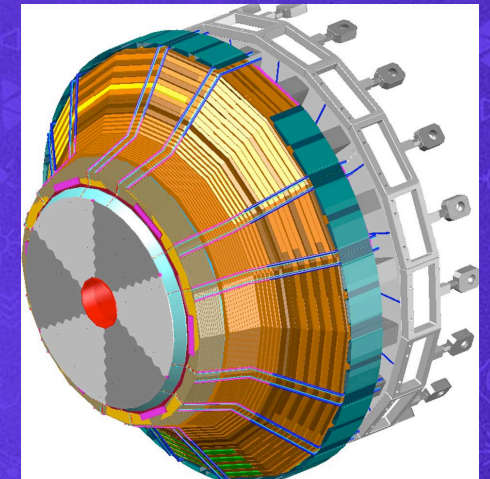
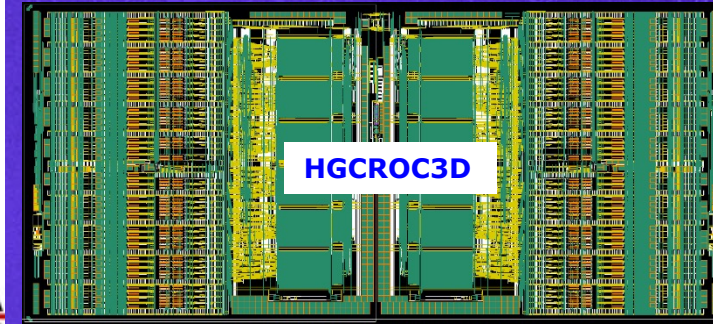
Pulse before and after shaping



# CMS: HGICAL



- **HGCROC (High Granularity Calorimeter ReadOut Chip)**
  - Calorimeter readout of PIN diodes and SiPMs of new HGICAL end cap calo
  - 0.1 MIP to 2000 MIPs digitization with 10bit ADC and ToT, 20 ns peaking time
  - 20 ps timing measurement with 3 ns time walk
  - 200 Mrad radiation hardness
  - 72 channels, 15 mW/channel, C4 bumping, BGA package
  - 120 000 chips produced in 2025

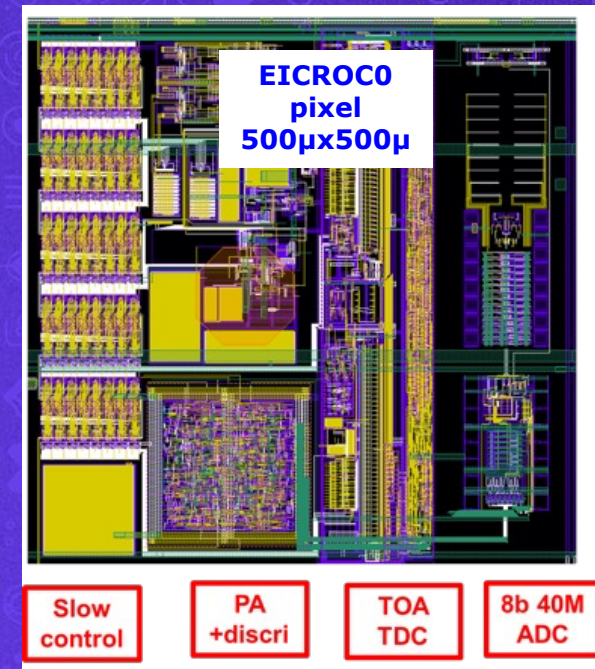


# EIC: EICROC AC-LGAD readout

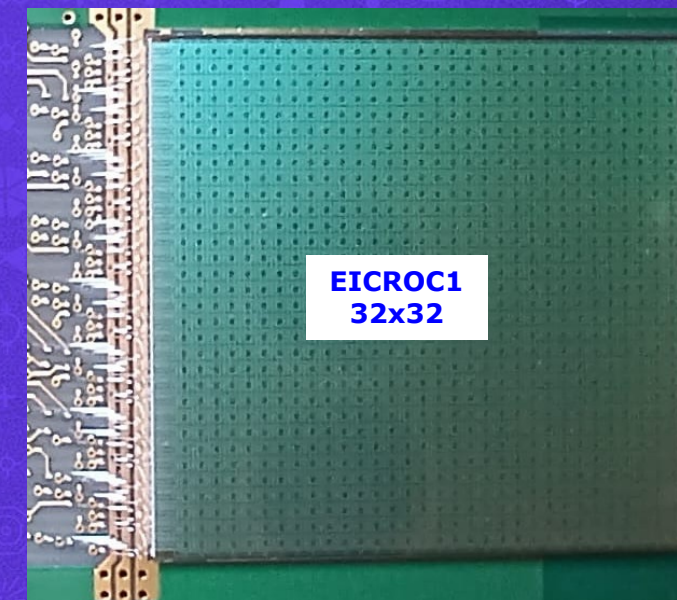
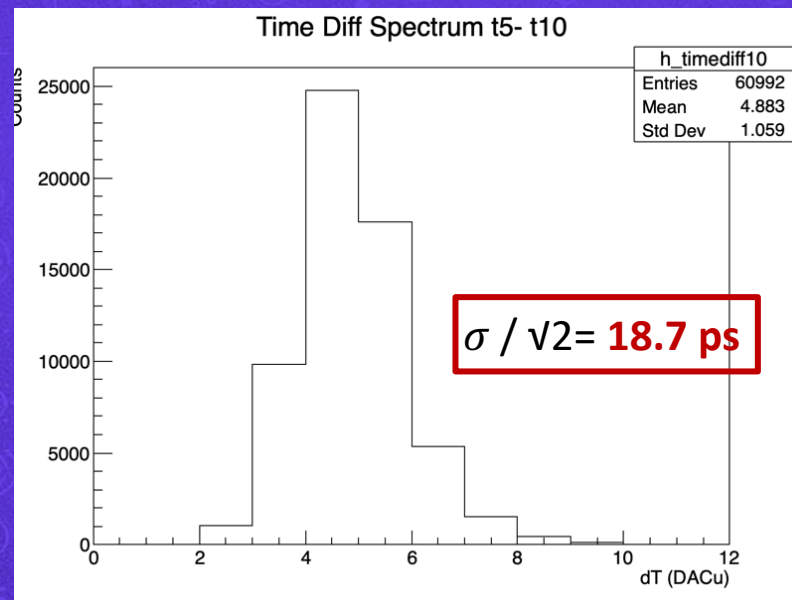
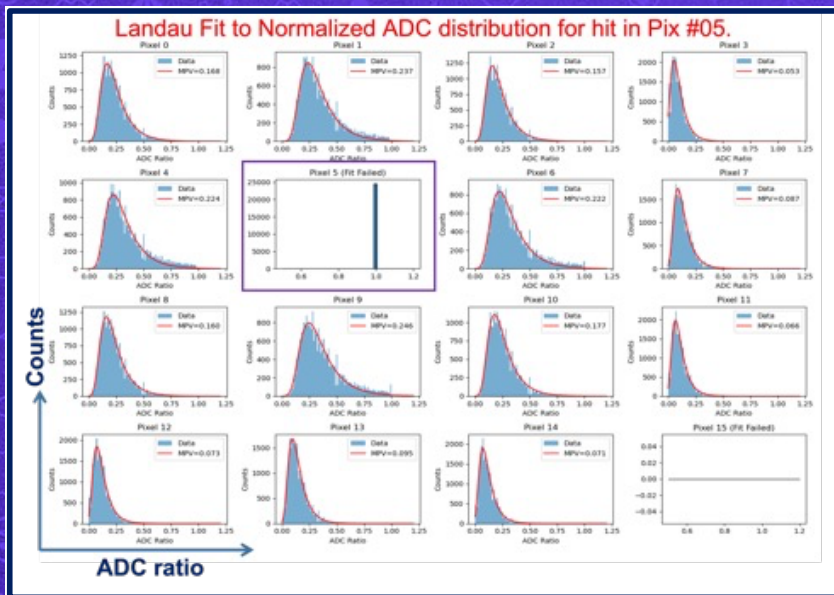


## • EICROC (EIC ReadOut Chip)

- Reads out 1024 pixels (500 μm<sup>2</sup>) of AC-LGAD for ToF detector (2 cm<sup>2</sup> sensors)
- 8-bit 40MHz ADC for position measurement down to 20 μm
- 20 ps TDC for timing measurement down to 20 ps
- 4x4 prototype in 2023, 32x32 in 2025, final chip DoT in 2027 (LPC Clermont-Ferrand)



Refer to OMEGA's talk



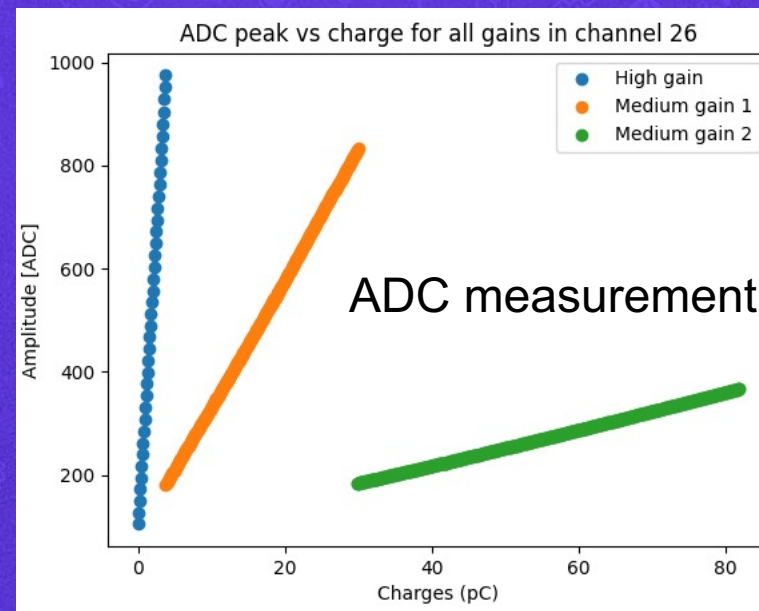
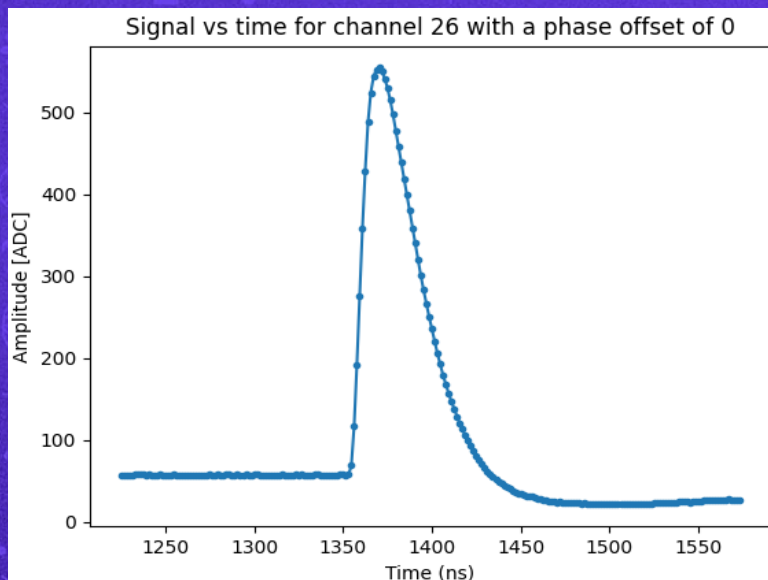
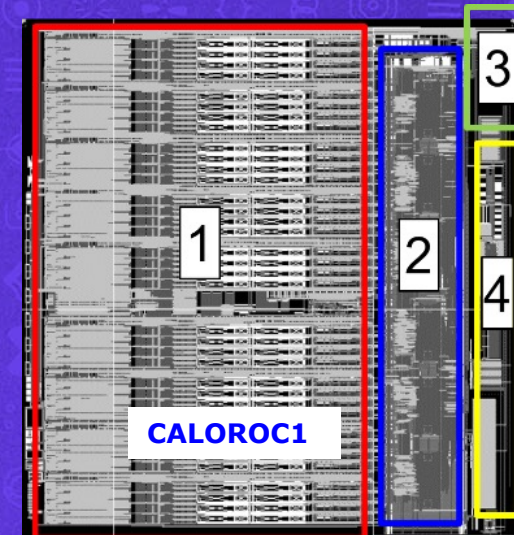
# EIC: CALOROC SiPM readout



- **CALOROC : SiPM readout for EIC calorimeter**

- 36 channels of charge and time measurement for SiPM up to 10 nF
- Streaming readout : auto-trigger and zero-suppress
- 4 gains
- 20 ps timing
- 12 mW/ch

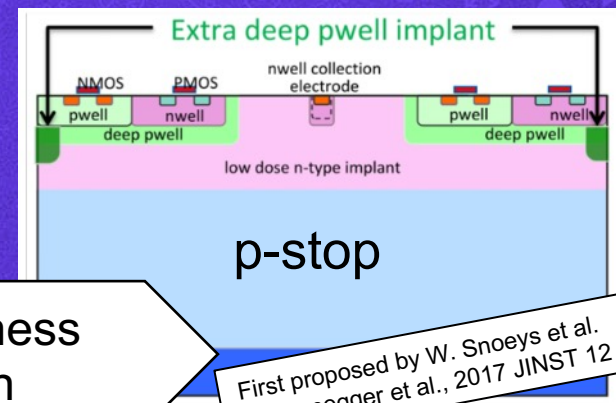
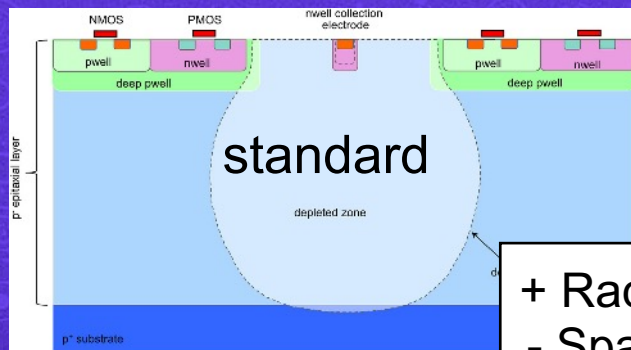
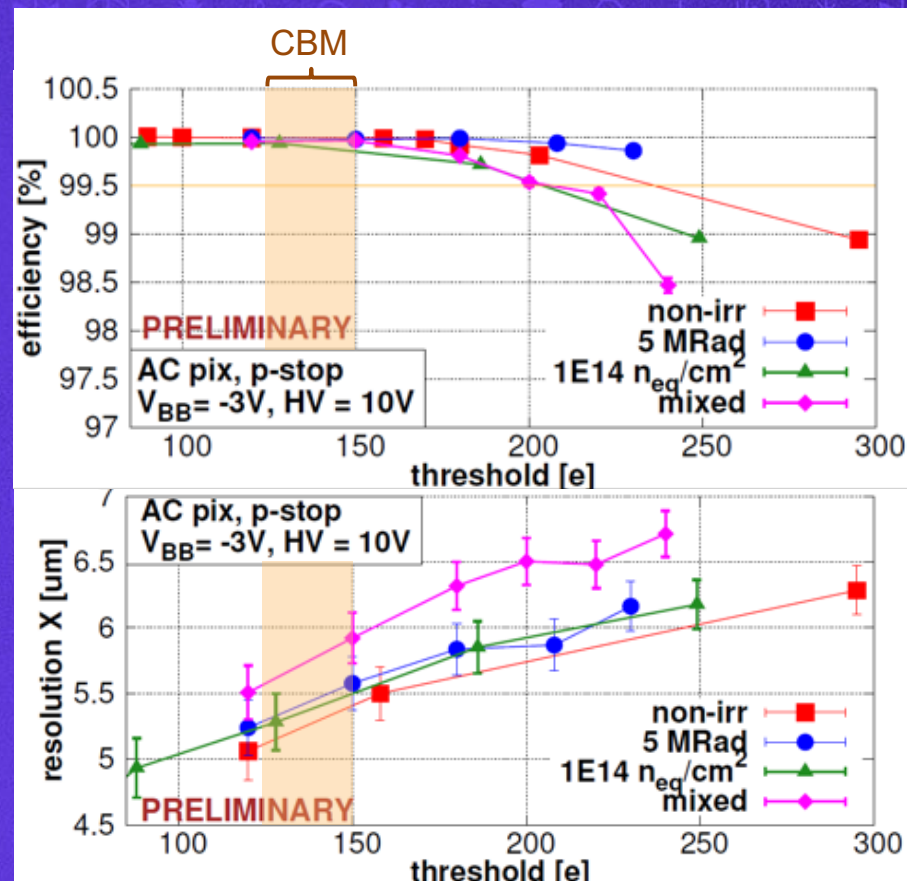
- **Variant for DRD6 and Allegro LAr calorimeter**



# 3 Vertexing & Tracking

# CBM-MVD: MIMOSIS

- Based on ALPIDE architecture
  - New readout to sustain space and time variations
  - Matrix dimension: 1024 col. X 504 row
  - Pixel dimension: 26.88  $\mu\text{m}$  (height) x 30.24  $\mu\text{m}$  (width)
  - 2 front-end variants AC and DC
  - Integration time: 5  $\mu\text{s}$
  - Tower 180 nm with modified process
  - Designed by IPHC
- MIMOSIS-3:
  - Production Readiness Review on 03/26
  - System Improvement in Progress

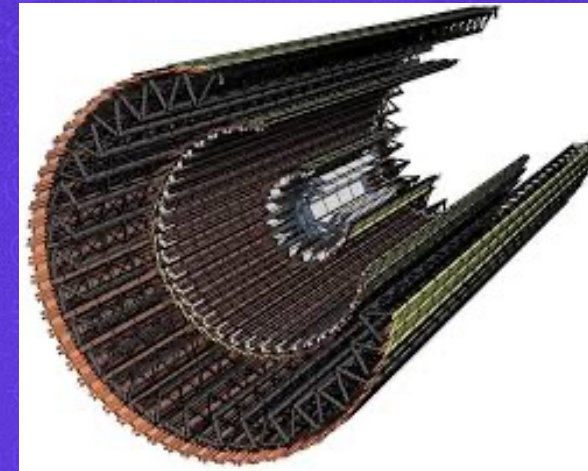


+ Radiation hardness  
- Spat. Resolution

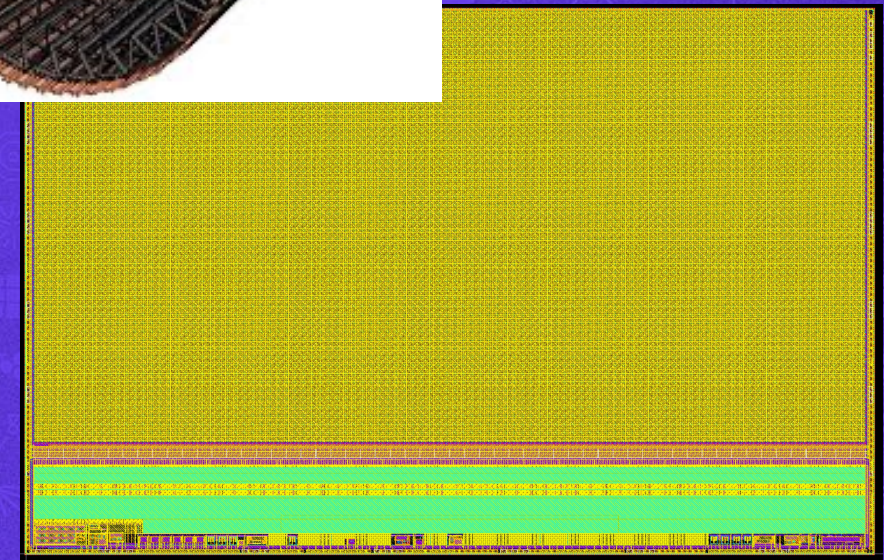
First proposed by W. Snoeys et al.  
H. Pernegger et al., 2017 JINST 12 P06008

# OBELIX: A Dedicated MAPS for Belle II experiment

- Tower 180 nm
- IN2P3 members: CPPM, IPHC
- Dedicated MAPS for Belle II vertex detector upgrade
- Based on TJ-Monopix2
- Digital-on-Top flow integration
- Matrix of 464x896 pixels ( $33.04 \times 33.04 \mu\text{m}^2$ )
  - Column-drain with data-driven readout
  - 21.1 MHz timestamping clock for ToA and ToT
- On-chip LDO regulation for all power domains
- New digital periphery to cope with Belle II trigger:
  - Two-level data buffering & trigger management
  - Trigger output for L1
  - High precision time stamping at low hit rate



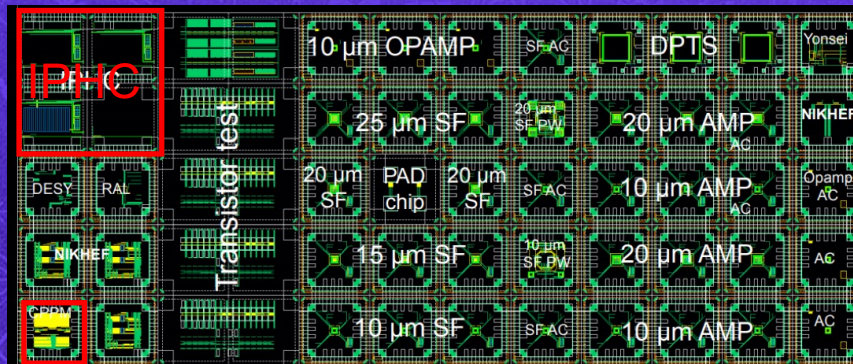
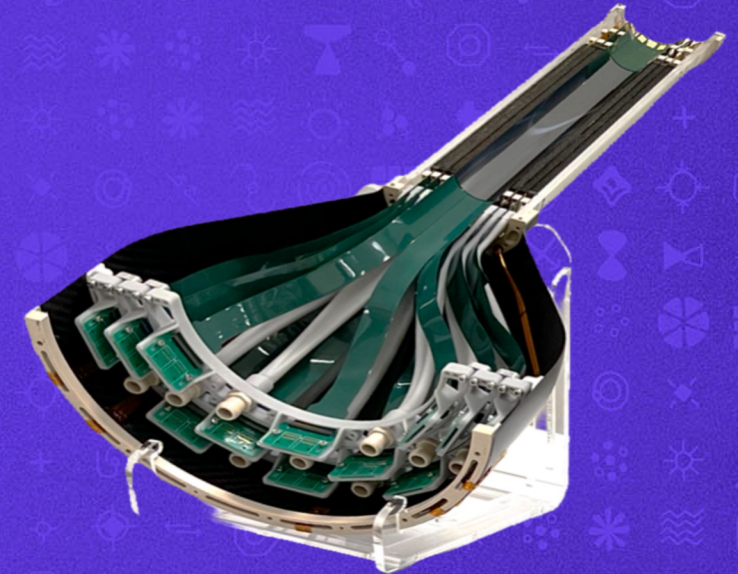
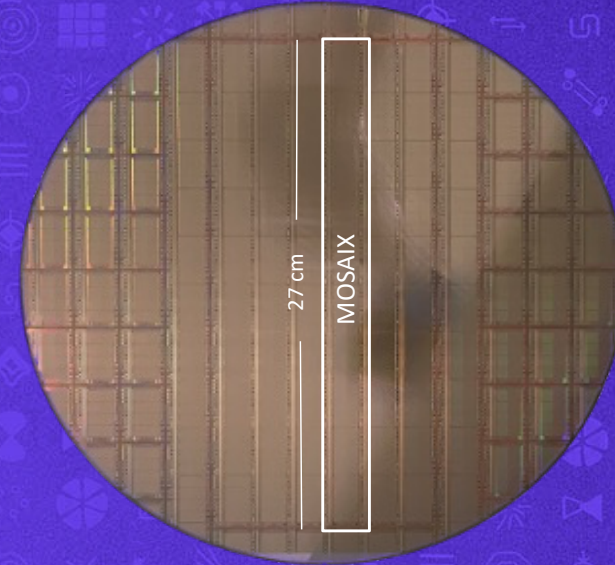
# ladders ~ 160  
# sensors ~ 2500



Refer to H. Pham's talk

# TPSCo 65nm: from baby steps to MOSAIX

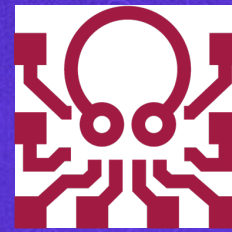
- **MLR1: 55 different chips to explore the technology**
  - IPHC: CE\_65v1 to explore charge collection
  - CPPM: Ring oscillator for radiation study on standard cells
- **ER1: stitching exploration focus on ALICE-ITS3 (MOSS/MOST)**
  - IPHC:
    - New version of CE\_65v2 (chiplet)
    - Matrix implementation and biasing for MOSS (large scale sensor)
- **ER2: first prototype of the final sensor for ALICE-ITS3 (MOSAIX)**
  - IPHC:
    - SPARC for asynchronous readout (see next slide)
    - Matrix implementation and biasing for MOSAIX
  - CPPM:
    - New version of ring oscillator (chiplet)



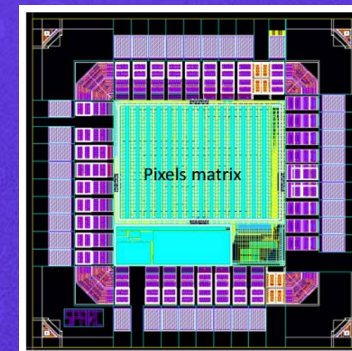
MLR1

ITS3 Qualification Model

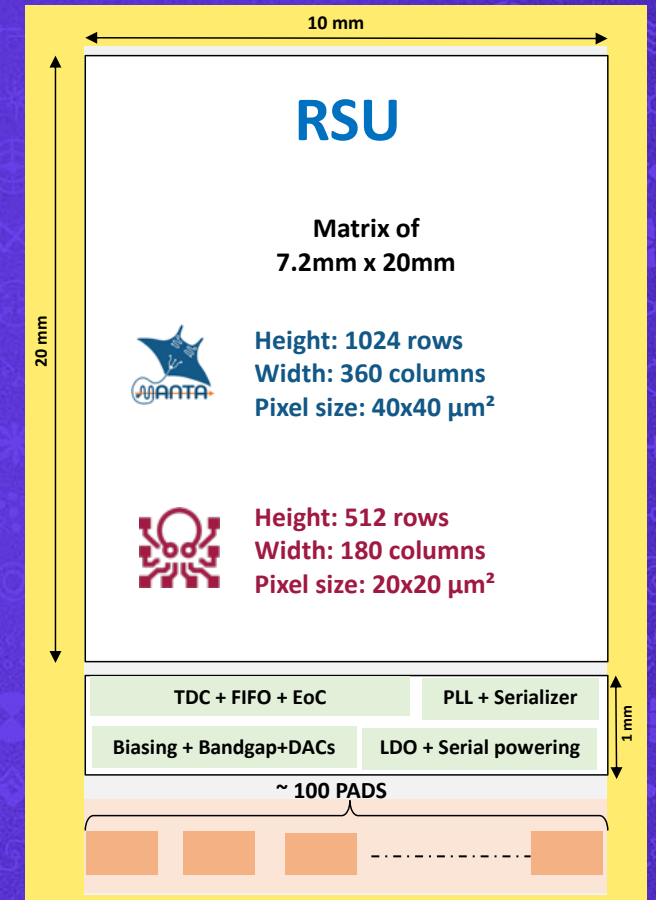
# DRD 3: MANTA & OCTOPUS



- **Technology:** TPSCo 65 nm
- **Asynchronous readout derived from SPARC**
  - IPHC, CEA-Irfu, ICube (University of Strasbourg & CNRS Ingénierie)
  - ToA and ToT on matrix periphery
  - Time resolution of few nanoseconds
  - First test seems promising
- **MANTA:**
  - For tracking applications
  - Diode pitch (20  $\mu\text{m}$ )  $\neq$  Pixel pitch (40  $\mu\text{m}$ )  $\rightarrow$  Pixel grouping Ana./Dig.
  - Fast OR and high-resolution time stamping:  $\sim 70$  ps
  - IN2P3 members: IP2I, IPHC, LPNHE, LPSC
- **OCTOPUS:**
  - For vertexing applications
  - Pixel pitch (20  $\mu\text{m}$ )
  - Increase spatial resolution with ToT measurement
  - IN2P3 members: APC, CPPM, IPHC



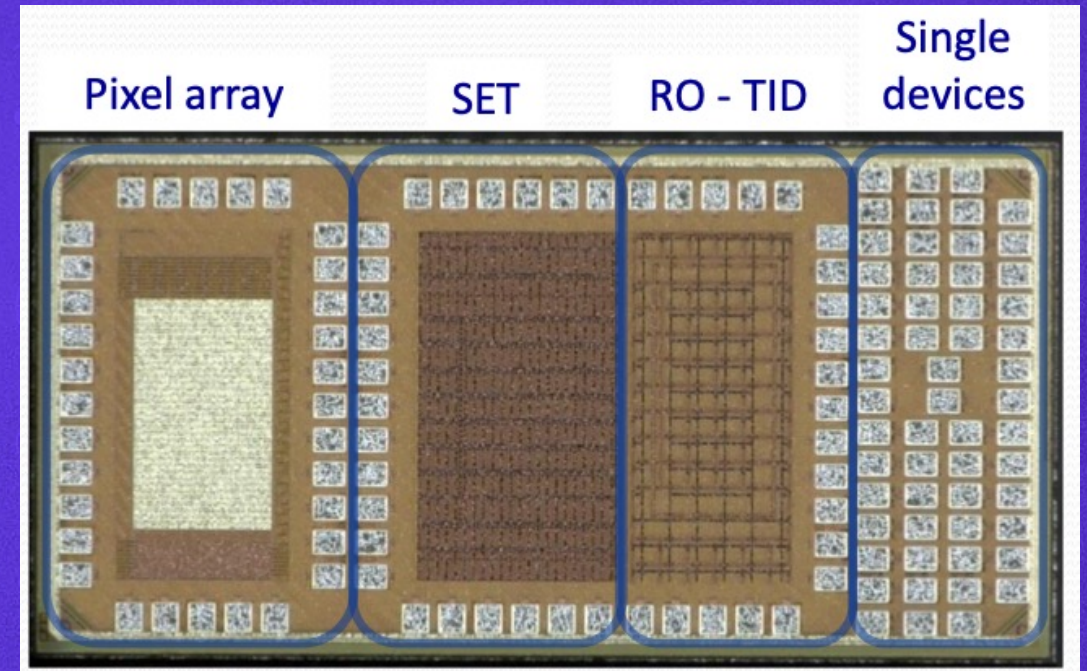
SPARC layout



MANTA1 & OCTOPUS1 schematic

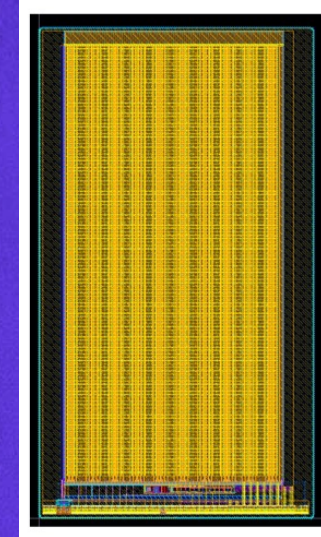
# 28 nm electronics developments for future pixel detectors

- TSMC 28 nm
- Exploring 4D tracking in future experiments using hybrid technologies
  - High spatial resolution
  - High time precision
  - Very high radiation tolerance
- Led by CPPM
- R&D activities on:
  - SEE/SET testing
  - Ring Oscillator Design
  - Analog FE pixel array



# MAPS spin-off in Tower 180 nm

- **IMPACT:**
  - Ion identification → proj. EU “Philm” in Hadron-2030
  - Need of ADC SAR 12bits 10MS/s: see previous slide
- **Spatial dosimetry:**
  - Developed inside LabCOM LAMAPS (IPHC and Weeroc)
  - Collaboration contract with CNES

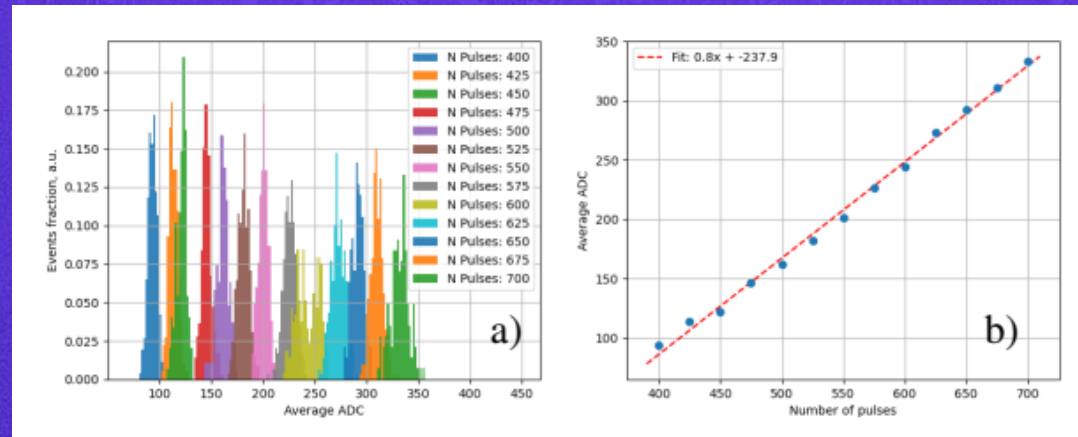


IMPACT layout

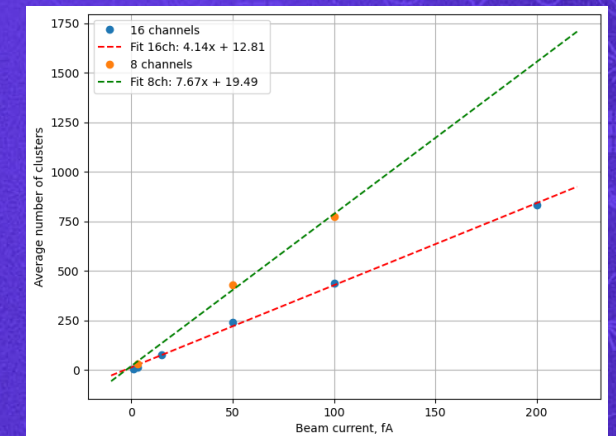
CNES DAQ – CubeSat format



Lab test with laser



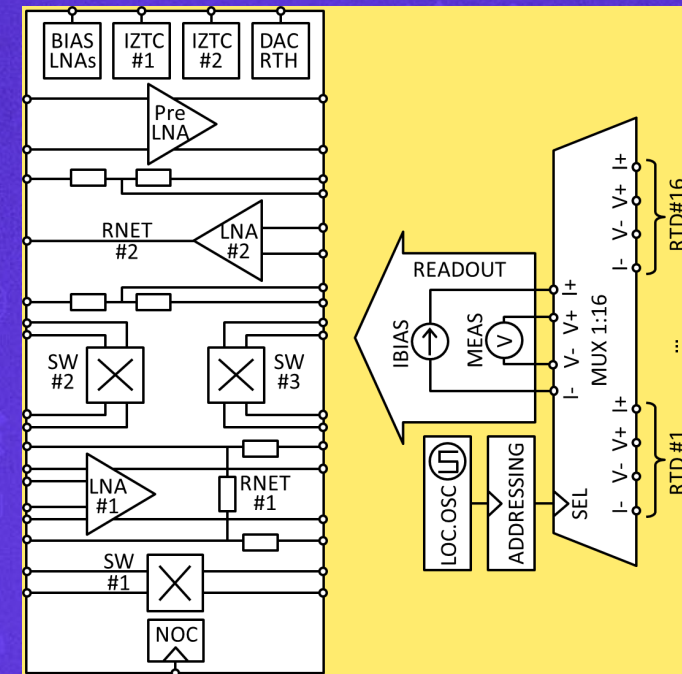
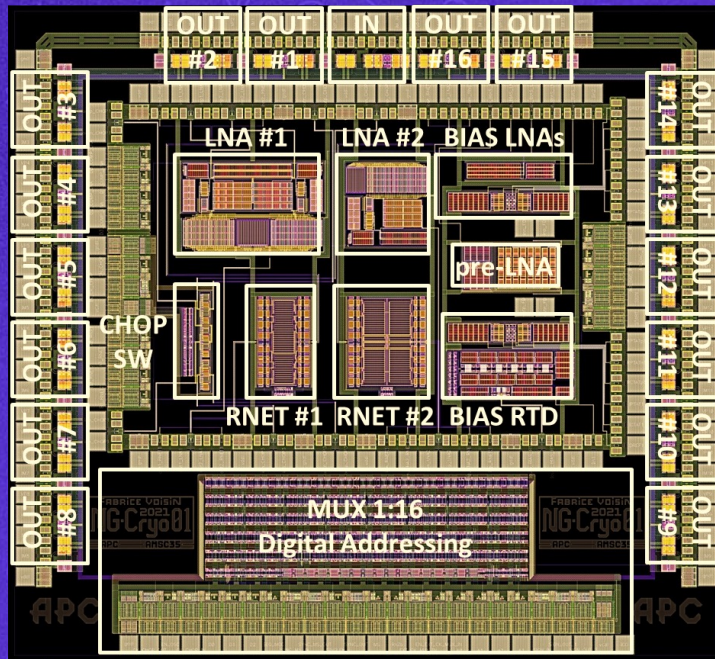
Proton beam — CYRCé



4

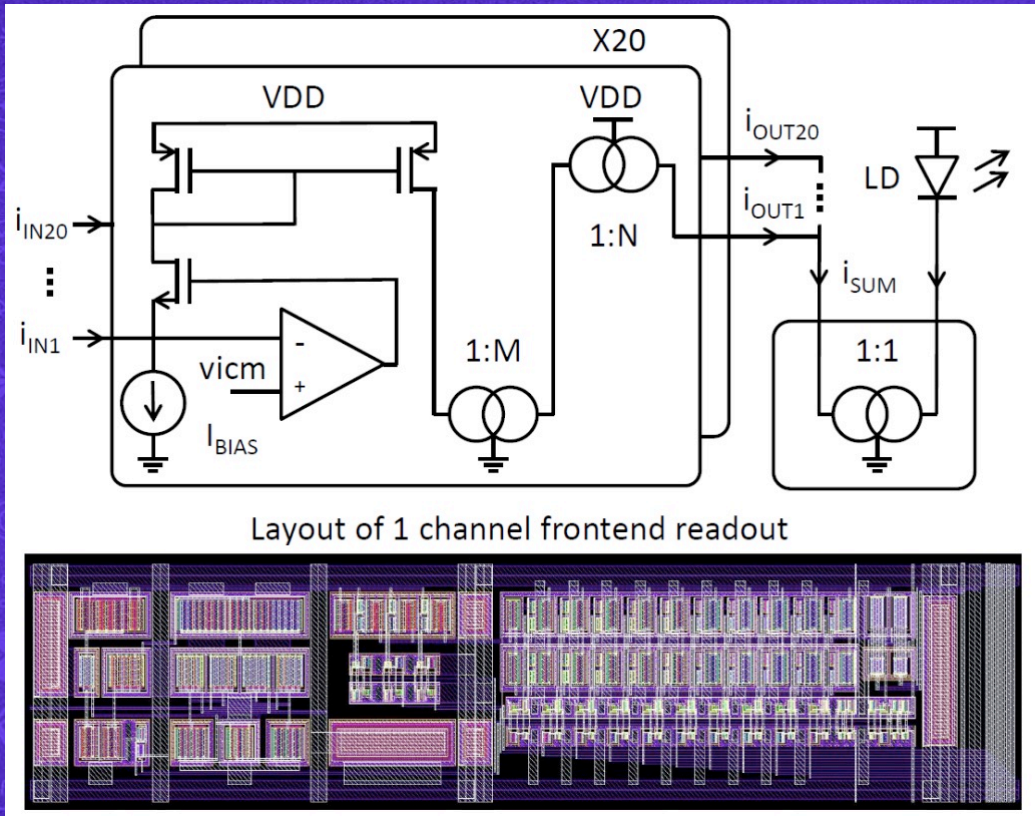
# Cryogenics & space applications

# R&T IN2P3 NGCryo



- Project larger than microelectronics
  - Designed at APC
- Simplify cryostat thermometry procedure in the sub-kelvin range
- Reduce the number of wires needed for in-situ thermometer measurements
- Cryogenic ASIC in AMS CMOS 350nm technology (2022), integrating multiplexing function and test architectures for the readout of thermometers operating at 300mK

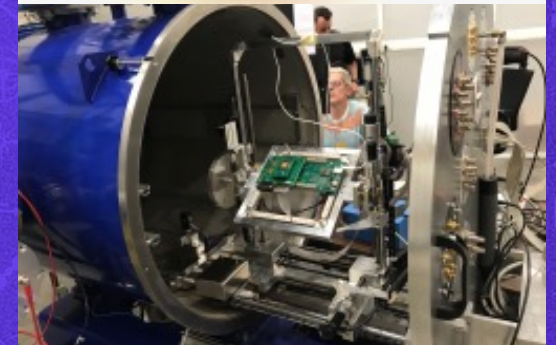
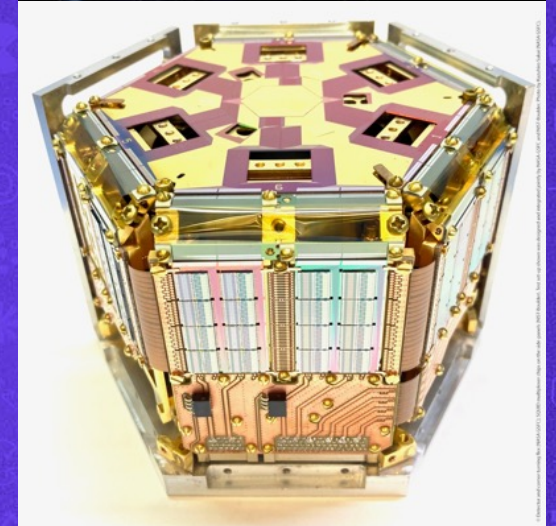
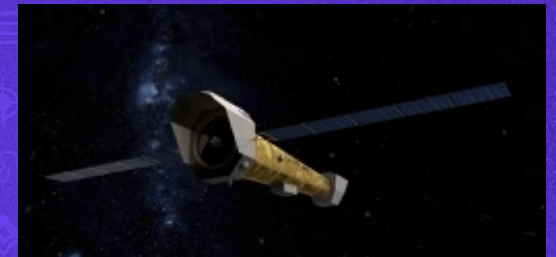
# ANR SOFIC



- Readout chain of the DUNE neutrino detection experiment photodetection system
- Multi-channel ASIC in AMS CMOS 350nm technology, operating at cryogenic liquid argon temperature (90K)
- Optical fiber readout and transmission of signals from SiPMs detectors (20x channels)
- Submission expected by the end of 2026
  - Designed at APC

# Low-Noise ASICs for Space Cryogenic Detector Readout

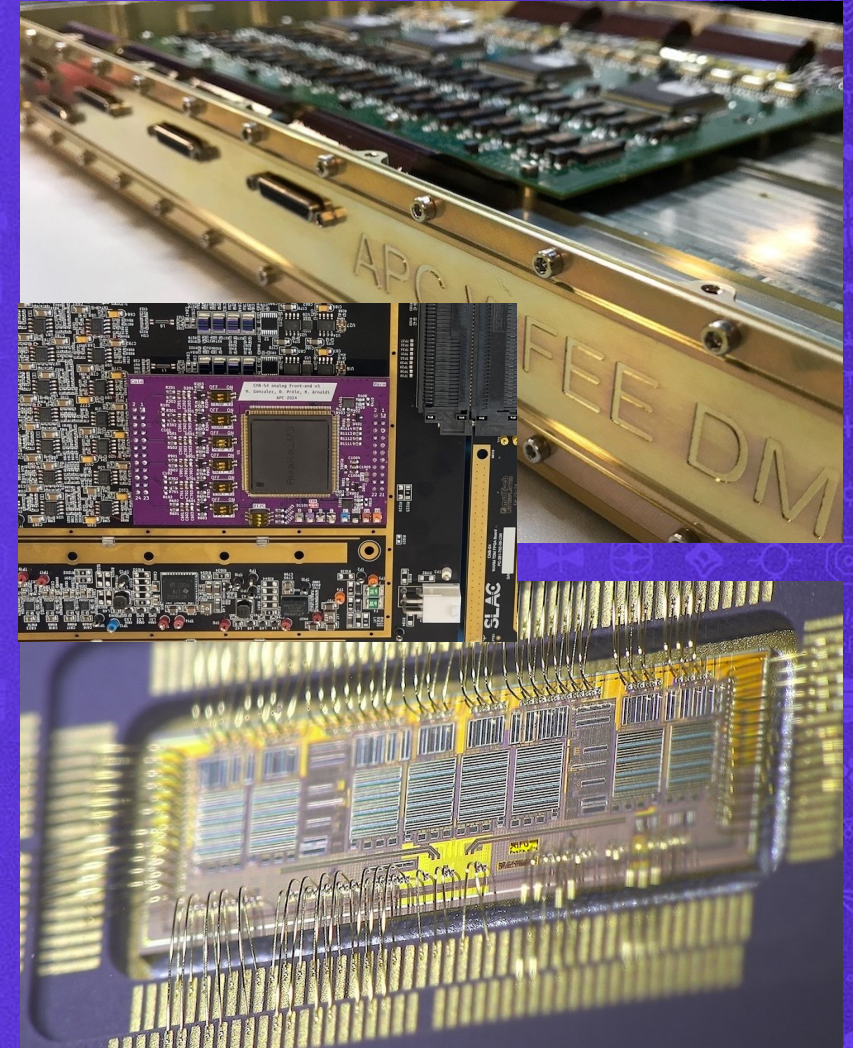
- **Mission context - ATHENA / X-IFU Warm Front-End Electronics (WFEE)**
  - ESA ATHENA mission, X-IFU instrument, 32 multiplexed readout channels, 1536 superconducting microcalorimeters @ 50 mK
  - Cryogenic readout : SQUID Time domain multiplexing
  - APC responsibility: warm (300 K) front end electronics WFEE
    - ➔ Target instrument: ~2.5 eV energy resolution @ 6 keV over 1536 detector : Xray spectro-imager
- **WFEE ASIC functions**
  - Differential low-noise LNAs
    - < 1 nV/√Hz input noise
    - Tens of MHz bandwidth
  - Low-noise programmable DACs for TES & SQUID biasing
    - Low 1/f noise
    - Thermal drift compensation
    - Radiation robustness up to 200 krad and 120 MeV/mg/cm<sup>2</sup>



# AwaXe ASIC Family Evolution

## Athena Warm ASIC for X-IFU Electronics

- 2020 — AwaXe\_v3 (AMS 350 nm BiCMOS SiGe)
  - Used in WFEE DM1 / DM2 (16 channels delivered to CNES & SRON):  
<https://x-ifu.irap.omp.eu/fr/announcement/successful-coupling-of-the-x-ifu-warm-front-end-electronics-demonstrator-at-sron>
  - Also deployed for CMB-S4 electronics at SLAC : see CMB-S4 SiGe ASIC-based daughter board for low-temperature detectors front-end analog readout L. H. Arnaldi, M. Gonzalez, D. Prêle, S. Chen, et al. [doi.org/10.1117/12.3020728](https://doi.org/10.1117/12.3020728)
  - See datasheet :  
[https://apc.u-paris.fr/~prele/datasheet\\_AwaXe\\_v3.pdf](https://apc.u-paris.fr/~prele/datasheet_AwaXe_v3.pdf)
- 2021–2025 — AwaXe\_vEM / v4 / v5 / v6 (ST 130 nm BiCMOS SiGe)
  - Engineering models back-up - Long-term technology sustainability (?)
- 2025–2027 — AwaXe\_TLH (last run AMS 350 nm BiCMOS SiGe)
  - Redundant AMS implementation
  - Modular architecture (LNA separated from DACs)
  - TMR on digital
  - Offset compensations



# 5

# Other Topics

# R&T BiCMOS Project

- **Applications:**

- cryogenic detectors, silicon detectors, TPCs and radio-frequency instrumentation

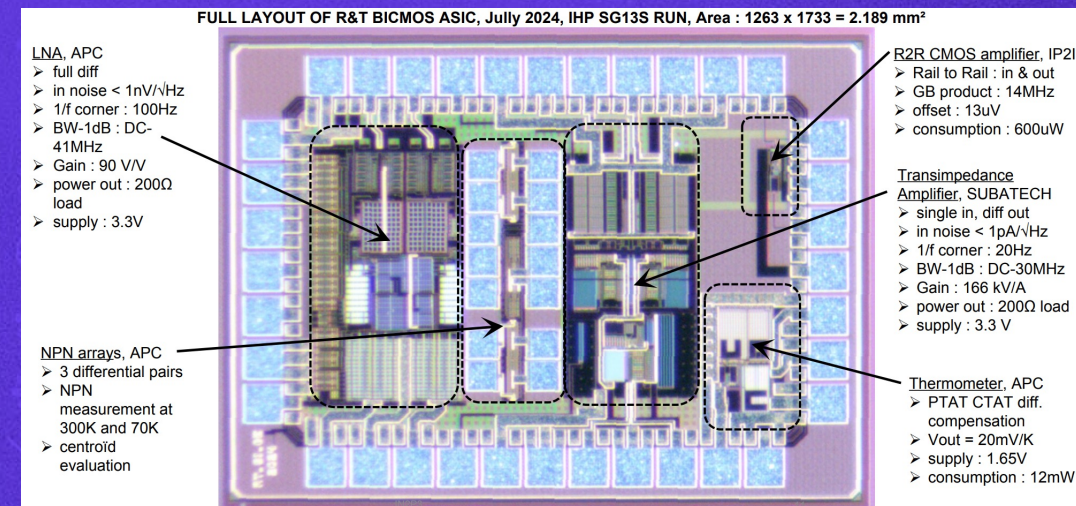
- **Designed at APC, IP2I, SUBATECH**

- **Project objectives:**

- Identify and characterize several alternative BiCMOS/CMOS technologies with a node size > 130 nm
- specific front-end applications requiring high dynamics, low flicker noise, high gain-bandwidth product, and performance at cryogenic temperatures
- Long-term MPW production availability and low-cost access are also required
- Perform cross-comparison of CMOS and BiCMOS technologies

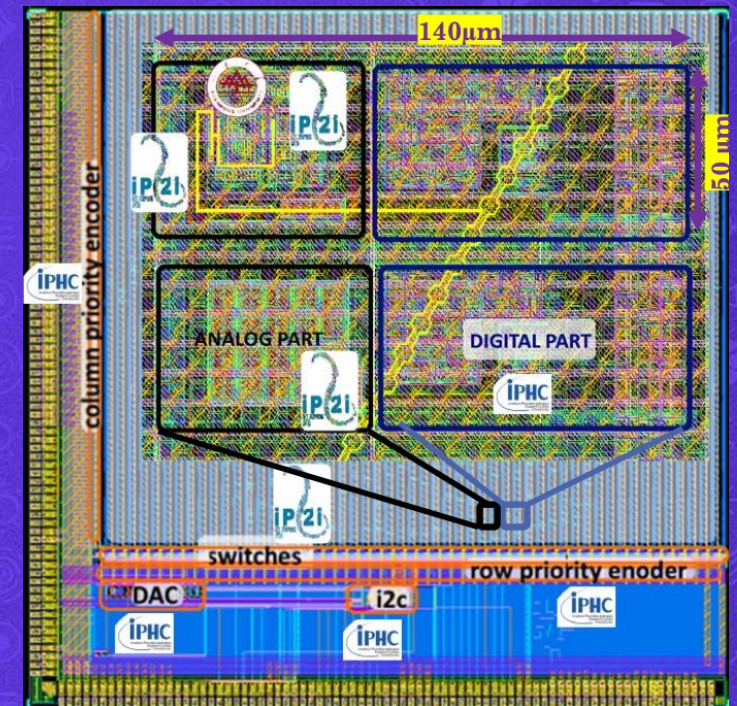
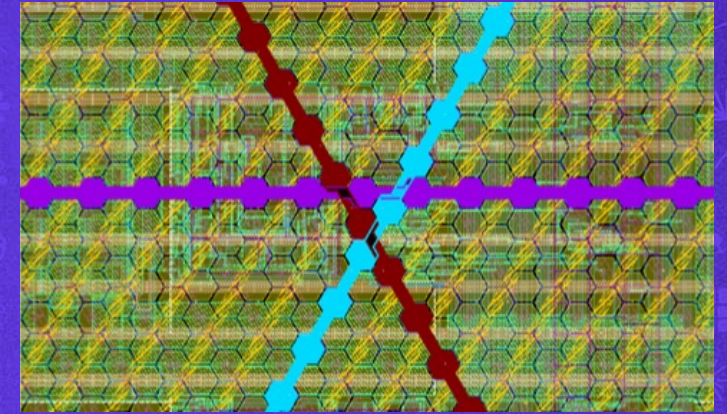
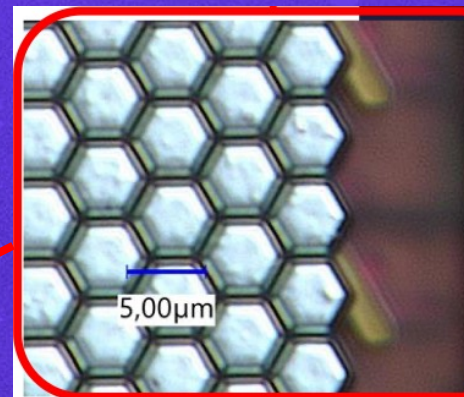
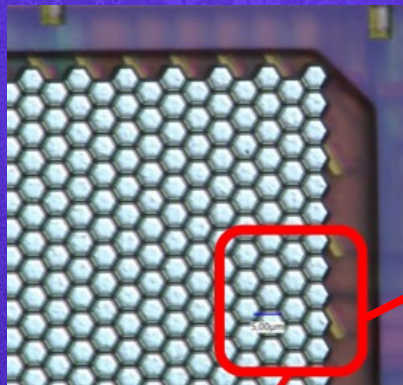
- **Main achievements:**

- IHP SiGe SG13S (130 nm) validated
- XFAB XH180 (180 nm) under validation
- Design and characterization of reusable analog building blocks
  - low-noise LNAs
  - Transimpedance amplifiers
  - Rail-to-rail CMOS amplifiers
  - Cryogenic thermometers
  - Current conveyor
  - Charge preamplifier



# PICMIC: Tri-axis 5 $\mu$ m hexagon pixel-strip matrix

- Tower 180 nm
- IN2P3 members: IP2I, IPHC (for first prototype)
- ASIC dedicated to direct readout of MCP or NCP
- Matrix for PICMIC-0
  - 53 rows by 128 columns
  - Active readout cell
    - Size: 140x50  $\mu$ m<sup>2</sup>
    - Channels: 2556
- Coincidence between a timing sensor and a position sensor
  - Time resolution: picoseconde
  - Spatial resolution: Micrometer
- 2<sup>nd</sup> prototype is submitted



# 6

# Summary

# Evolution of ASIC Design: Challenges and Collaboration

- **Context**

- Similar presentation by C. Colledani at TWEPP 2014 (Aix-en-Provence)

- **Key Challenges in Modern ASIC Design**

- **Increased Complexity:** ASICs are now more expensive, technically challenging, complex to design, and aggressive schedule
- **Shift in Design Ownership:** The era of a single analogue designer creating an ASIC is over

- **The Need for Multidisciplinary Teams:**

- Analogue designers
- Digital implementation designers
- RTL designers
- Verification designers
- Legal experts
- Customs experts
- Finance controller
- Tests and characterisation experts → This is a real bottleneck

} **World is more complex**

- **Collaboration is key to addressing these challenges**

- MI2I is one building block of the response for CNRS Nucléaire & Particules
- A broader response beyond CNRS Nucléaire & Particules is needed:  
Hub proposal by WG 7.7 of the DRD7 collaboration for example