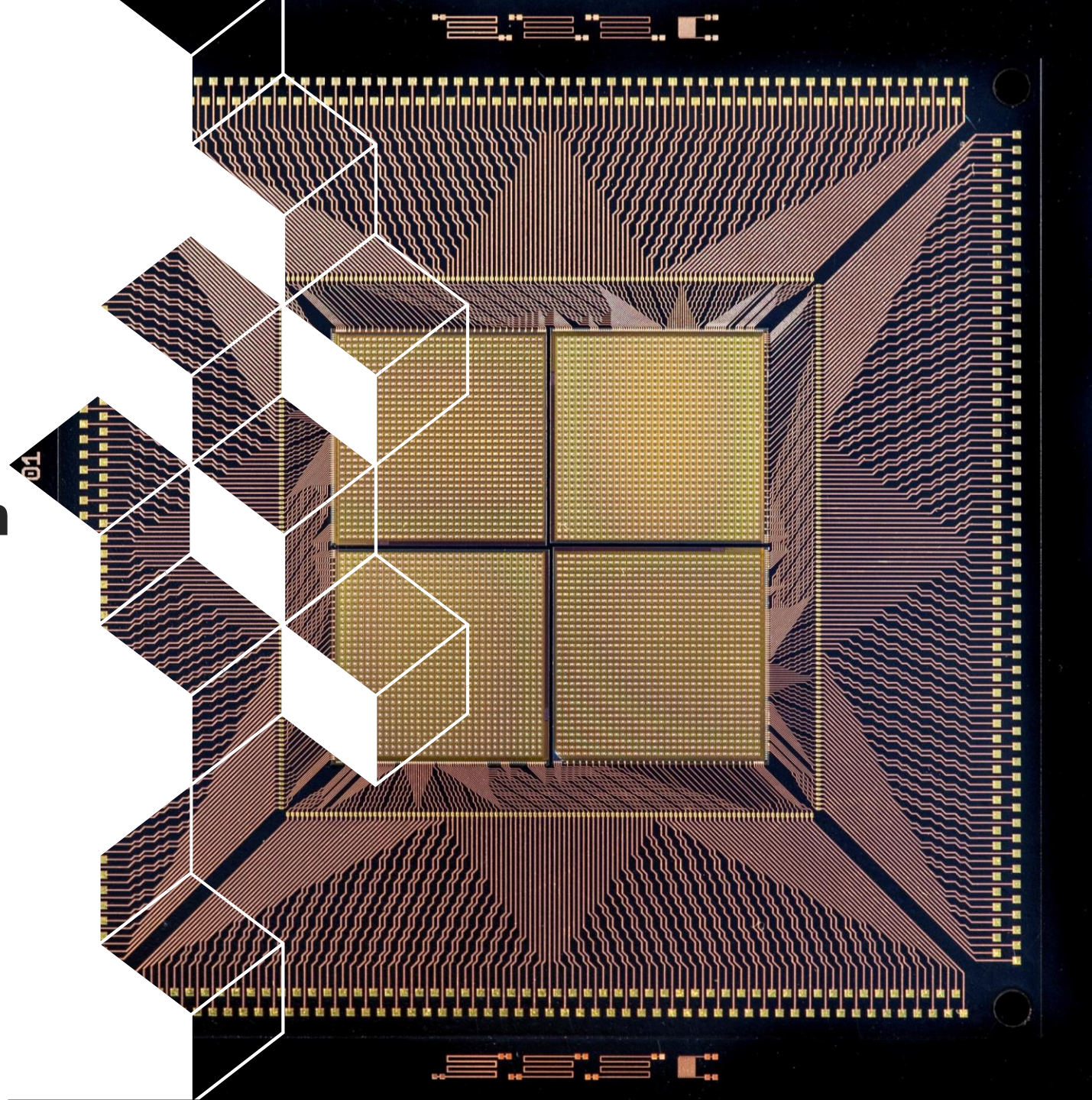
Front-end ASICs for high resolution imaging spectroscopy in space

David Baudin et.al.



Summary

1. **Astrophysic Context: Existing missions and future needs**
2. **Noise optimisation for high resolution**
   A. CMOS Amplifier
   B. Non Stationnary Noise Suppressor
3. **Matrix based optimisation**
   A. Double CR-RC stage
   B. AC link with low noise leakage current generation
4. **Packaging and interconnexion**
5. **Results and conclusion**

1. Astrophysic Context: Existing missions and future needs

Summary of astrophysic context: Solar physics

1. Science Case:

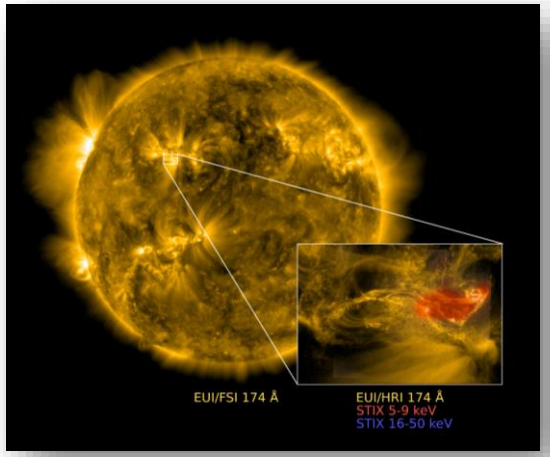


Fig1: Sum picture in UV and X-Ray taken by Solar Orbiter

- Study the electron acceleration in coronal emission (Solar Orbiter)
- Measure the electron distribution and polarisation
- Flux and transient phenomena measurements

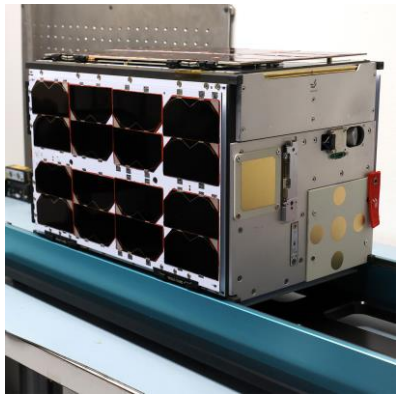


Fig 2: Padre nano satellite

- **Padre**:
  - Direct measurement
  - 4 modules – Caliste-SO
  - IDEF-X HD ASICs

2. Space missions (on-flight):

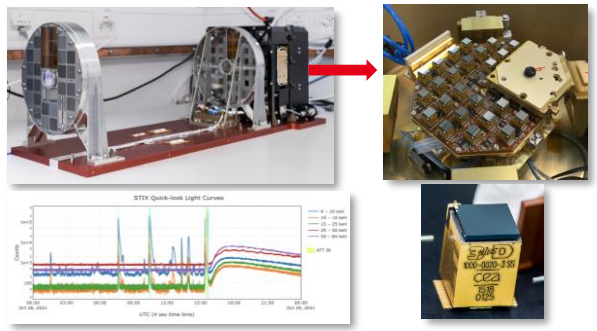


Fig 3: Solar orbiter imaging system, focal plane, flux variation with time, Caliste So module

- **Solar orbiter**:
  - Fourier-transform imaging
  - Stackup of CdTe – ASIC – Supplies

  12 Pixels per modules
  - 30 modules – Caliste-SO
  - IDEF-X HD ASICs (one per module)

3. Future Needs:

- Highly pixelated integrated circuit:
  - < 250 x 250 µm²
  - > 32 x 32 pixels
- Energy resolution < 2 keV @ 30 keV

  < 40 el.rms
- Flux: ~200 kHz/mm²

Summary of astrophysic context: Extra galactic [SNR, Gamma ray burst]

1. Science Case:

Fig 4: Cas-A picture (chandra-X)

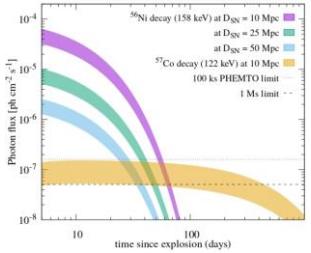


Fig 5: Simulated flux from SNR

- Study the metal generation on stellar generation
  - ^{56}Ni → ^{56}Co at 156 keV
  - ^{57}Co → ^{57}Fe at 122 keV
- Study polarization and energy distribution of Gamma ray bursts

2. Space missions (on-flight):

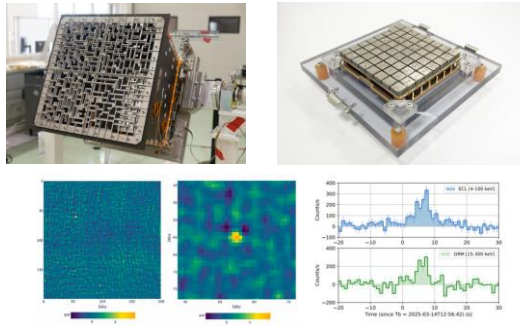


Fig 7: SVOM eclair coded mask aperture, focal plane, image of GRB

- **SVOM**:
  - Coded mask imaging
  - Stackup of CdTe – ASIC – Supplies

  32 Pixels per modules
  - 25 modules
  - IDEF-X Eclairs

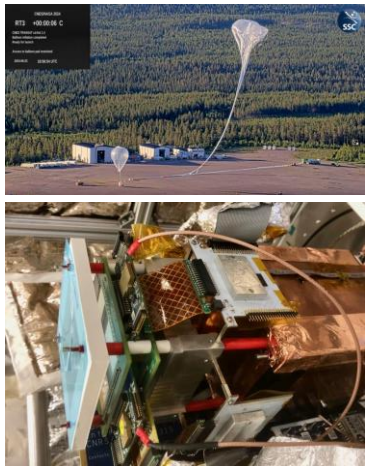


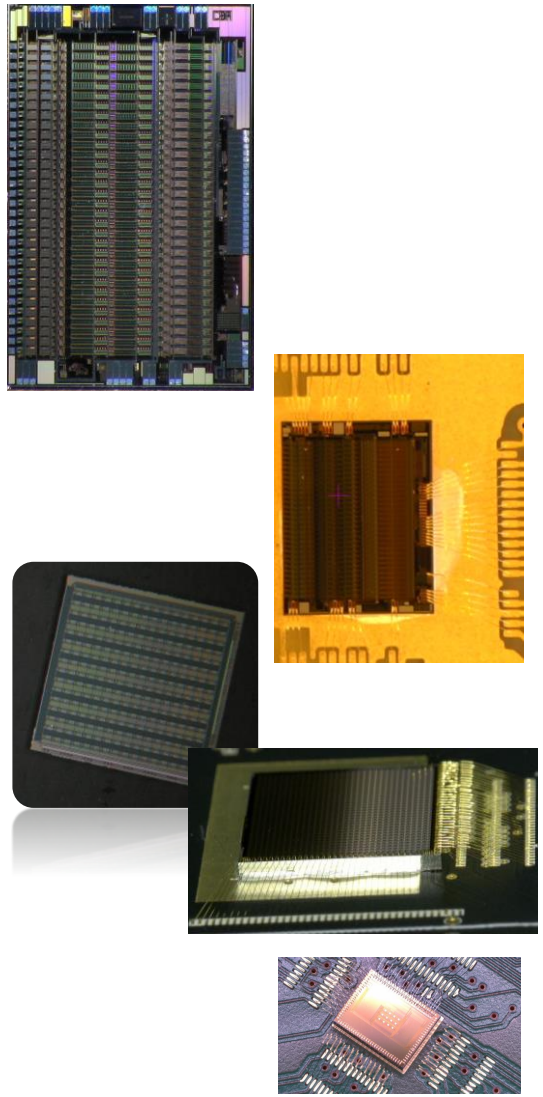
Fig 6: Comcube ballon launch and payload

- **Comcube**:
  - Coded mask imaging
  - SDD detector
  - Constellation of 27 nano-satelittes
  - 4 ASICs
  - IDEF-X HDBD

3. Future Needs:

- Highly pixelated integrated circuit (for polarisation):
  - < 250 x 250 µm²
  - > 32 x 32 pixels
- Energy resolution < 1 keV @ 30 keV
  < 20 el.rms

ASICs Developped at Saclay List and Specification



ASIC	Energy resolution eV @ 60 keV	Number of Pixels / channels	Size of pixels / channels (µm x µm)	Power density (mW/mm²) (mW/channel)	Options / Technology
IDeF-X HDBD	526 [17 el.rms]	32	150 x 2000	2,7 0,8	Bidirectionnal AMS 0.35 µm
IDeF-X S	474 [10 el.rms]	32	150 x 2500	2,2 0,8	Common mode rejection AMS 0.35 µm
D2R1	666 [29 el.rms]	16 x 16	300 x 300	2,7 0,25	CDS XFAB 0.18 µm
D2R2	910 [54 el.rms]	32 x 32	250 x 250	4,8 0,3	XFAB 0.18 µm
ANAQIN-X	NA [17 el.rms]	4 x 4	250 x 250	4,8 0,3	Prototype XFAB 0.18 µm

Fig 8: ASICs Developped at Saclay

General structure of our ASICs

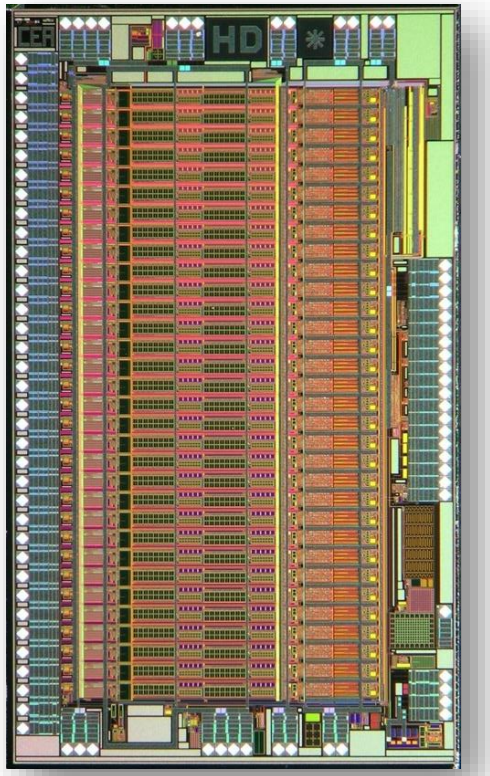


Fig 9: IDEFX-HD picture

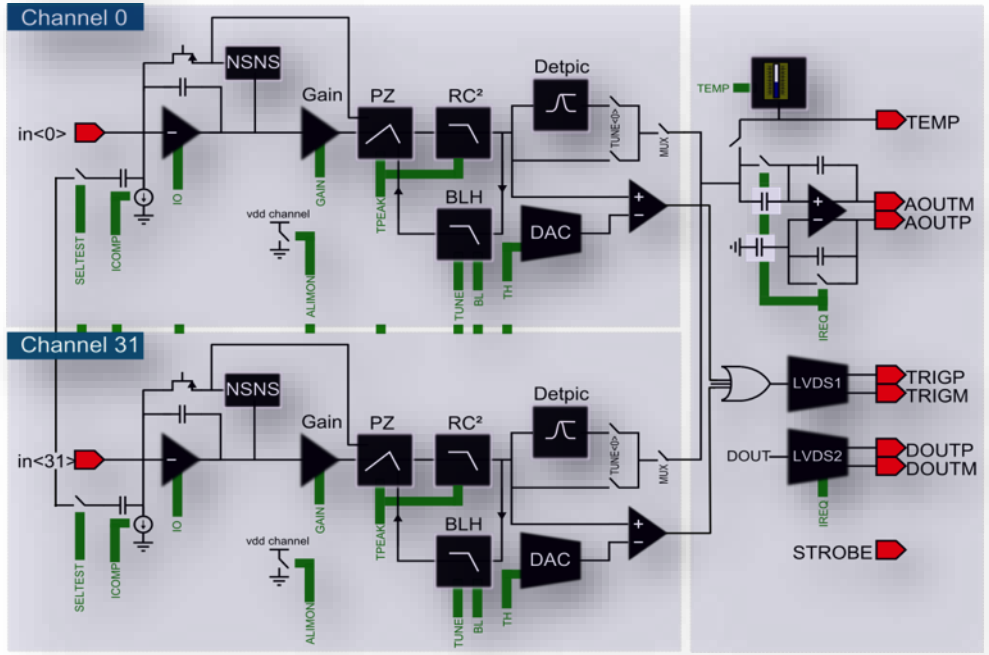


Fig 10: General spectroscopic instrumentation chain schematic

1. Amplification:
   - CSA with continuous reset
2. Filtering:
   - Analog CR-RC^n filter with transistors copy
3. Maximum detection:
   - Peak detector with or without pileup detection
4. Triggering:
   - Tunable threshold with baseline rejection

- Some options used in some designs:
  - Non stationnary noise suppressor
  - Multi-Stage CR-RC
  - CMOS amplifier

2. Noise optimisation for high resolution

A- CMOS architecture for Charge Sensitive Amplifier

Circuit:

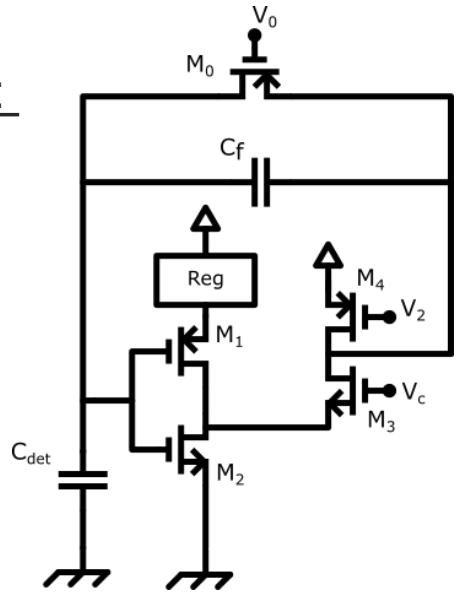


Fig 11: CMOS CSA

- Classical folded cascode architecture
- Both P and N mosfet are connected together
- A current regulation set the current state
  - In our case its a « mirror » version of the CSA that generate voltage reference for « current regulation »

Hypothesis: - Strong Inversion region
- $L_n = L_p = L_{min}$

Thermal Noise optimization

$$ENC_{th}^2 = \frac{\alpha''_{th}}{\beta_n\sqrt{\frac{W_n}{L_n}} + \beta_p\sqrt{\frac{W_p}{L_p}}} \times \left(C_{det} + \frac{2}{3}C_{ox}\left(W_nL_n + W_pL_p\right)\right)^2$$

$$With:\ \alpha''_{th} = \frac{8kTA_{th}}{3T_{peak}}$$

$$\beta_n = \sqrt{2k'_nI_d}$$

$$\beta_p = \sqrt{2k'_pI_d}$$

Optimum for:

$$C_{Csa} = \frac{C_{det}}{3}$$

Flicker Noise optimization

$$ENC_f^2 = \frac{A_fI_d^{AF}}{C_{ox}} \times \frac{\frac{K_{fn}}{L_n^2} + \frac{K_{fp}}{L_p^2}}{\left(\beta_n\sqrt{\frac{W_n}{L_n}} + \beta_p\sqrt{\frac{W_p}{L_p}}\right)^2} \times \left(C_{det} + \frac{2}{3}C_{ox}\left(W_nL_n + W_pL_p\right)\right)^2$$

Optimum for:

$$C_{Csa} = C_{det}$$

A- CMOS architecture for Charge Sensitive Amplifier

- We can fix some parameter to help us identify noise ratios

$$a = \frac{W_p}{W_n} \quad b = \frac{k'_p}{k'_n} \quad c = \frac{KF_p}{KF_n}$$

- Optimisation is found as:
  - a = b for both Flicker and Thermal
  - Then, depending on optimisation ($C_{Csa} = \frac{C_{det}}{3}$ or $C_{Csa} = C_{det}$) => W_p and W_n
- Noise ratio with respect to NMOS for thermal and Flicker for PMOS can be found as:

Noise Type	NMOS	PMOS	CMOS
Flicker	$\sqrt{\frac{b}{c}}$	1	$\left(\sqrt{\frac{c}{b}}\right)\left(\sqrt{\frac{1+cb}{1+b}}\right)$
Thermal	1	$\left(\frac{1}{b}\right)^{\frac{1}{4}}$	$\frac{1}{(1+b)^{\frac{1}{4}}}$

Technology	NMOS	PMOS	CMOS
Thermal AMS035	1	1,3	0,93
Thermal AMS018	1	0,5	0,95
Thermal XFAB018	1	1,5	0,95
Thermal TSMC0065	1	1,1	0,89

Noise Type	NMOS	PMOS	CMOS
Thermal AMS035	1	1,3	0,93
Flicker AMS035	1,1	1	0,95

A- CMOS architecture for Charge Sensitive Amplifier

- Several ASIC have been done with this circuit, one of the latest is:
  - IDEF-X HDBD:

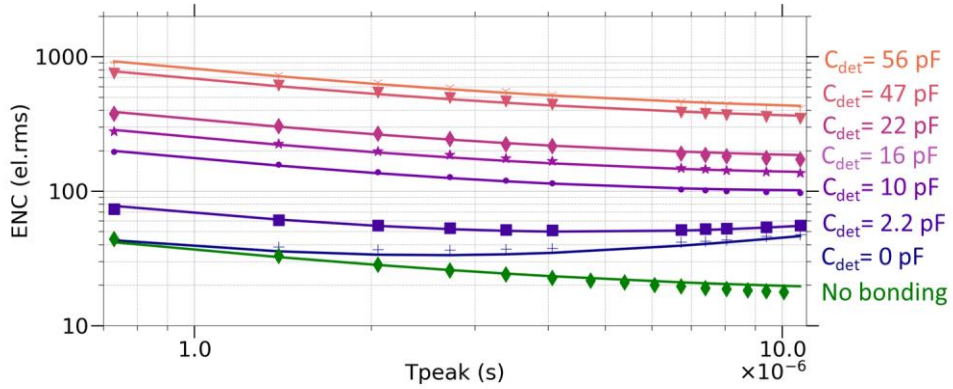


Fig 12: IDEF-X HDBD noise variation with peaking time and capacitance

- Coupled with a Silicon drift detector (C_{det} = 120 fF)
  - Resolution: 227 eV @ 5,9 keV
  - Threshold: 1,2 keV
  - Power: 26 mW
  - Channel: 32

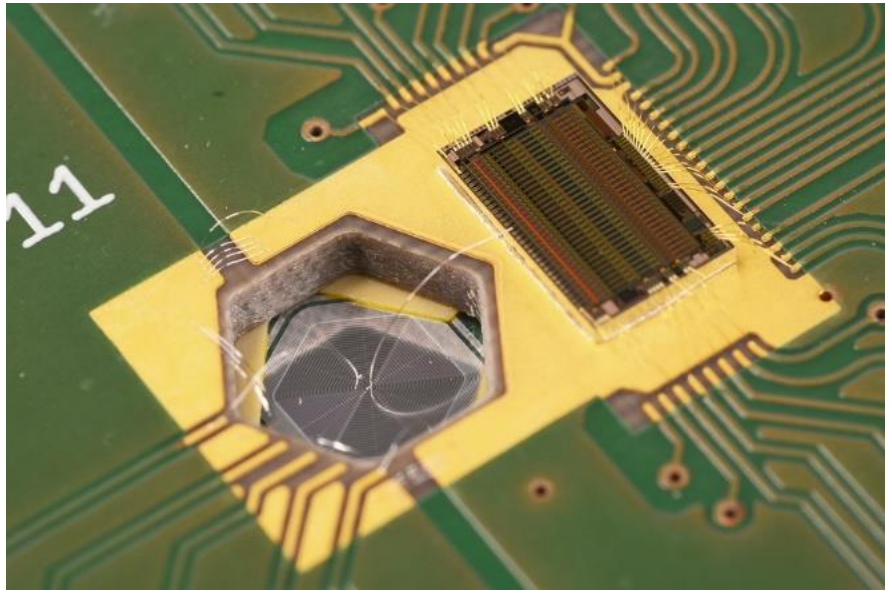


Fig 13: IDEF-X HDBD picture mounted with INAF-Triestre & Roma SDD

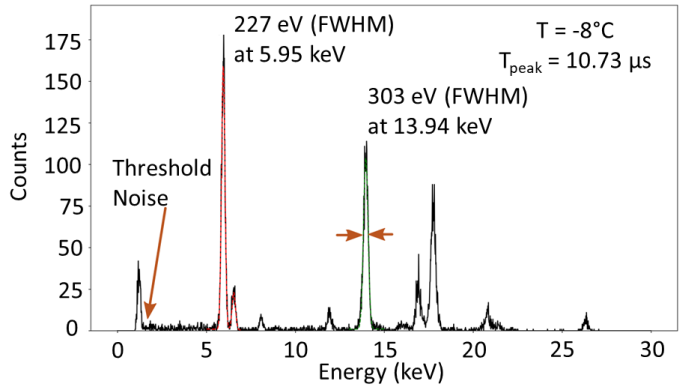


Fig 14: *Superposition of ^{55}Fe and ^{241}Am spectra with IDeF-X HDBD and SDD*

B- Non stationnary noise suppressor

- Our design are often base on a continuous reset done with a MOS transistor in subthreshold region.

[Geronimo et.al], "A CMOS fully compensated continuous reset system," IEEE Transactions on Nuclear Science, vol. 47, no. 4, pp. 1458–1462, Aug. 2000

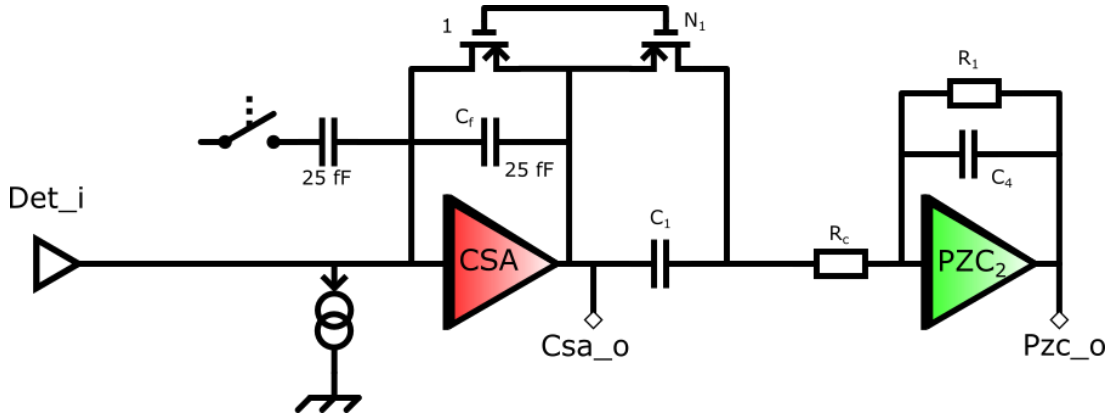


Fig 15: Single stage CR-RC in continuous reset

- When signal amplifies high value charges:
  - CSA output increases
  - Source voltage increase
  - Reset transistor is non longer in subthreshold region during that time
- **Consequences**:
  - Reset goes faster (could generates ballistic deficit)
  - Noise increase temporarily

- We implemented a special filter at CSA's output

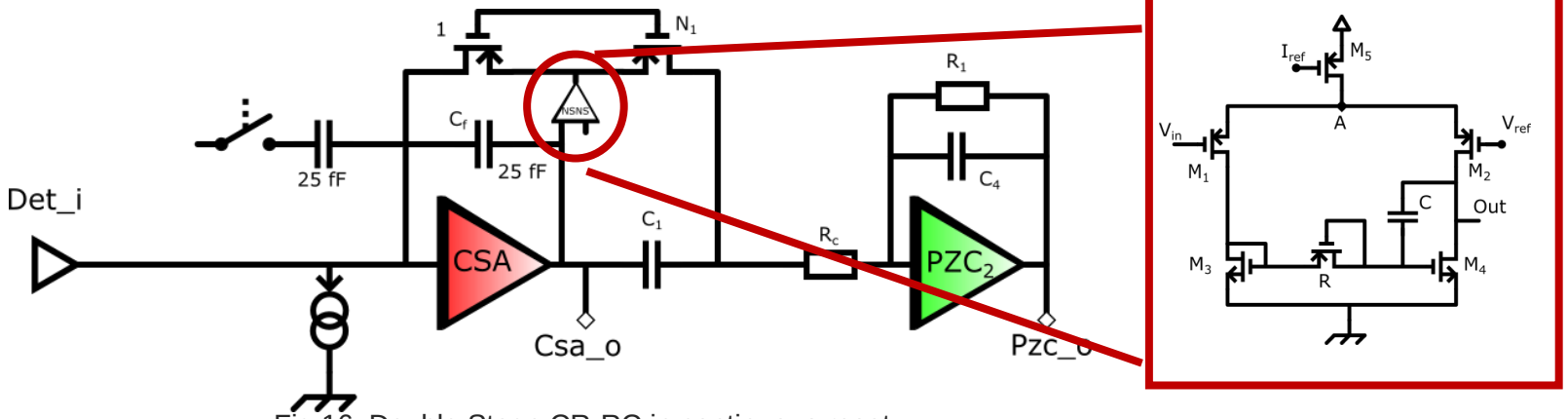


Fig 16: Double Stage CR-RC in continuous reset

- **Advantages**:
  - Supress gm variation with charges
- **Drawbacks**:
  - Increase Reset time
  - Generates oscillation when Ileak increases if low pass)

B- Non stationnary noise suppressor

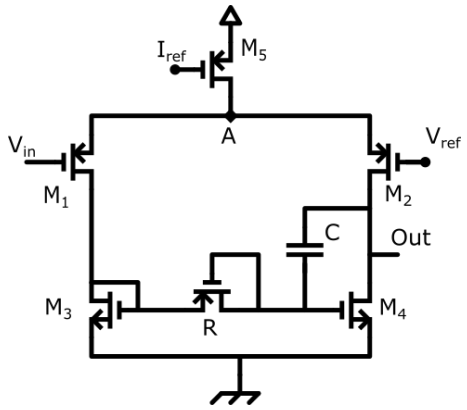


Fig 17: NSNS Structure

- Filter is based on a small differential pair with a zero and pole path done with « R » and « C ».
- R is based on an inverted diode with small potential accross in order to reach Tohms values
- Avoids having oscillation a high leakage, if design with a correct pole and zero, one can be always stable (if Ileak < 10 fA).
- One ASIC has implemented a version where we can turn on / off this features: D2R2

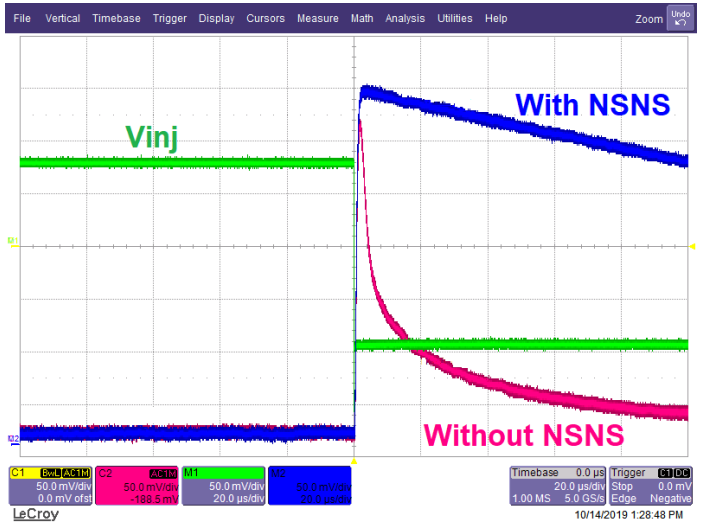


Fig 18: Oscilloscope output of a 27 kel equivalent pulse

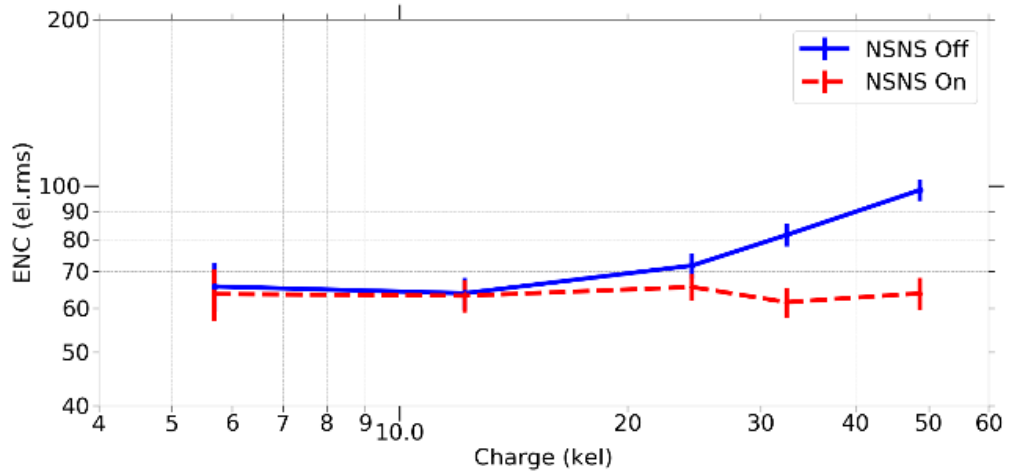
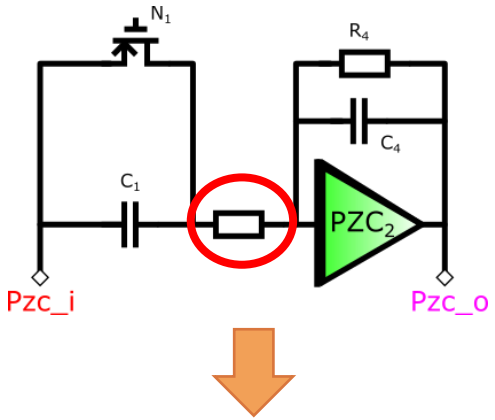


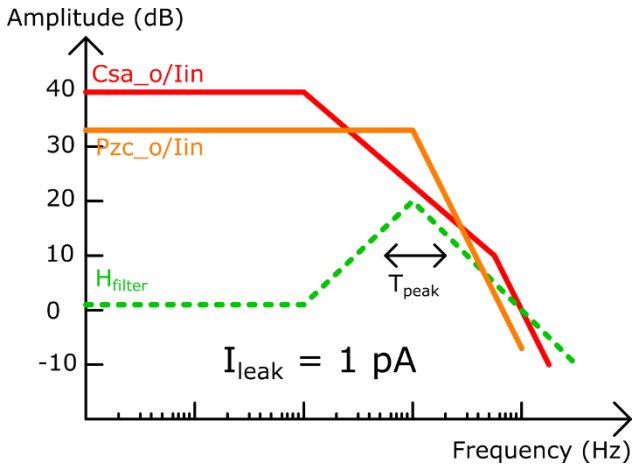
Fig 19: ENC variation with injected charge

3. Matrix based optimisation

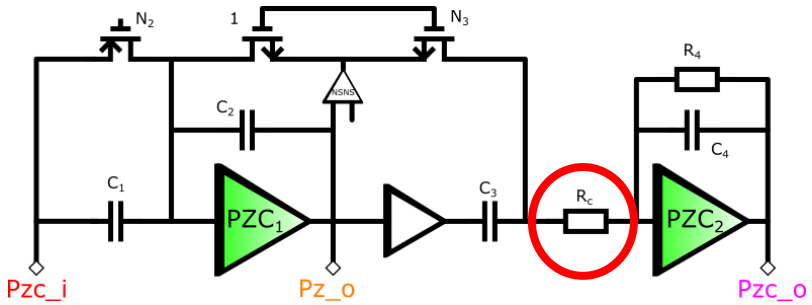
A- Double CR-RC stage

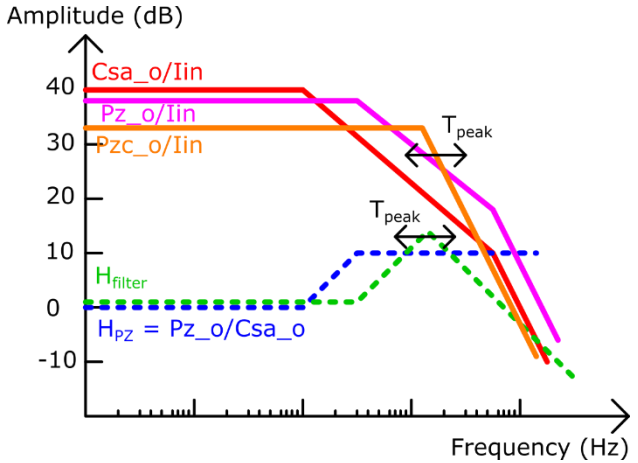
- One Stage CR-RC





- Double Stage CR-RC





- We add a resistor to add a « free pole »:

$$H_{tot}(s) = \frac{NR_4 s}{(1 + R_4 C_4 s)^2}$$

$$Hypothesis: \quad R_c \ll \frac{1}{N_1 g m_1}$$

- We can vary peaking time by varying R (N) or Cx
- Varying Cx allows to reduce amplifier throughput
- Noise:
  - One stage: $ENC_{PZC} \propto \frac{1}{N \times R_4}$
  - Double stage: $ENC_{PZC} \propto \frac{1}{N_1 \times N_2 \times R_4}$
- For low noise: $N = N_1 \times N_2$ should be high

Fig 20: Schematic of single stage and double stage continuous reset architecture (left) and resulting AC bode diagram (right)

A- Double CR-RC stage

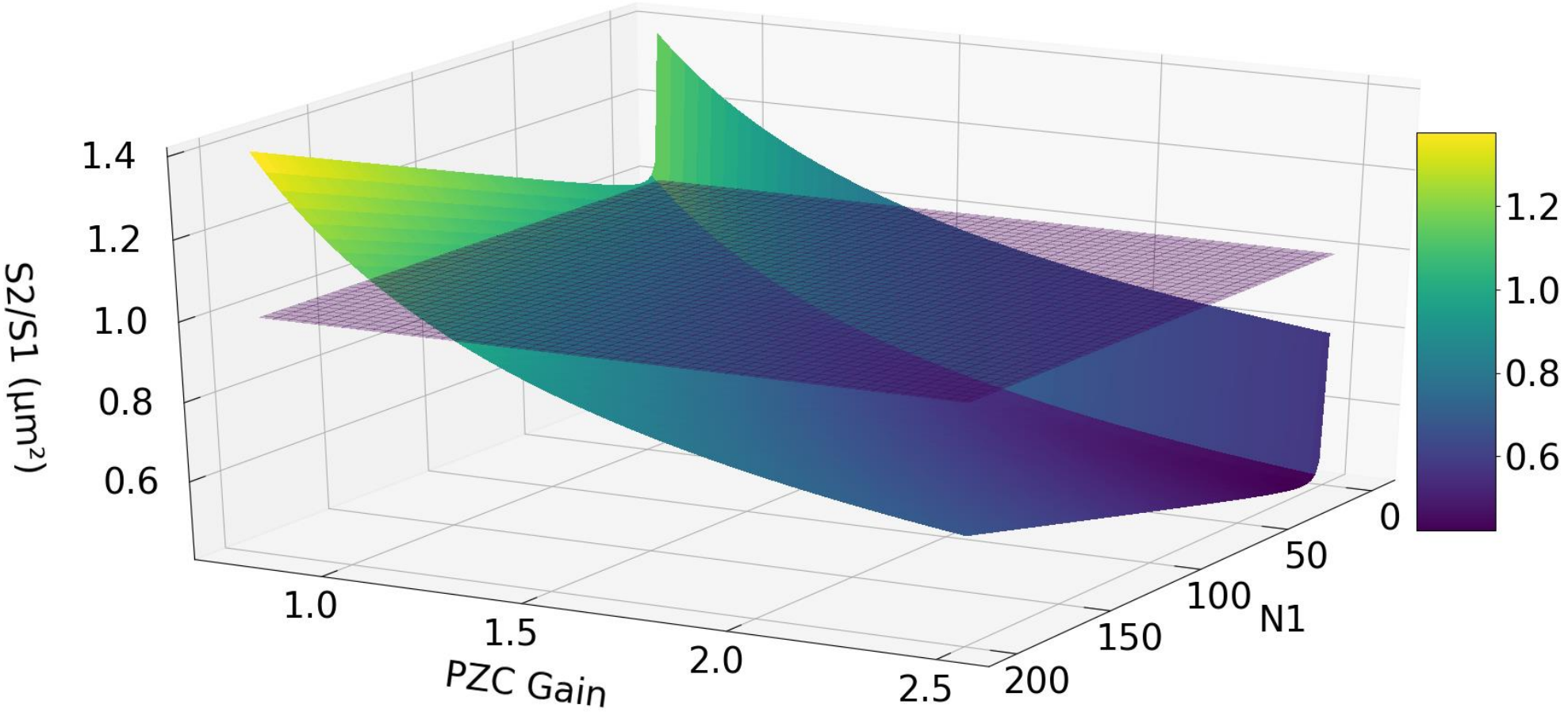


Fig 21: Plot of the mathematical representation of area ratio between two architecture, taking into acount transistors area together with capacitance area for $C_{density}$ = 2,35 fF/µm²

AC link with low noise leakage current generation

- With Continuous reset circuit:
  - If I_{leak} increases, noise will increase both due to schot noise in detector but also with thermal noise produced by the reset
- With radiation, detectors (Silicon) tends to have increasing leakage current
- We wanted to decouple inside the ASIC (for matrix connection) reset and detector bias => AC link

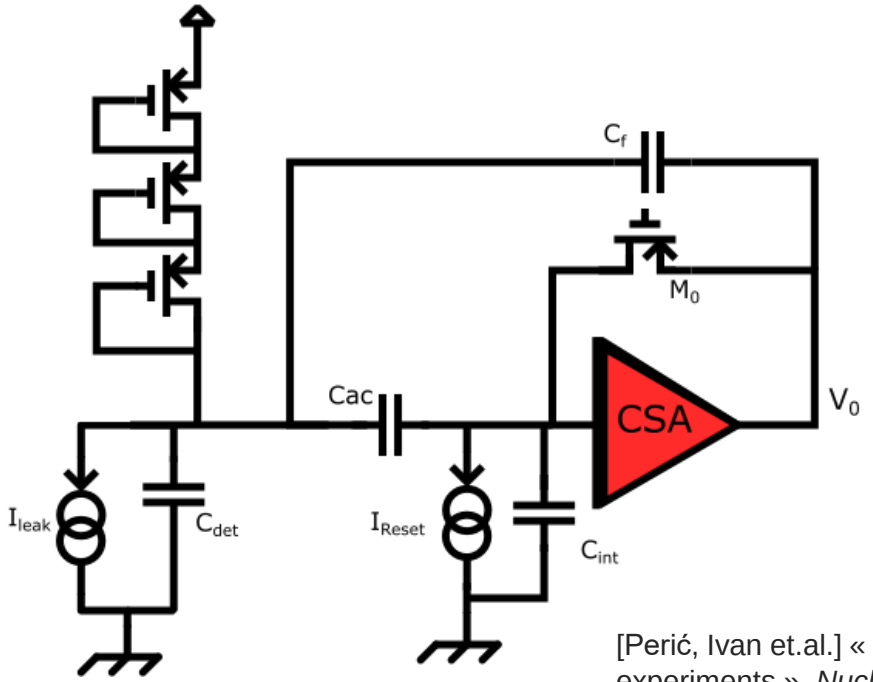


Fig 22: Semi-AC reset architecture.

- Feedback capacitance outside of AC link loops helps to provide

And amplification of Cac to be able to have 30 pF

with only 1 pF internal capacitance

- Reset can be done with N transistor in diode which allows:
  - $Noise_{reset} = \frac{Noise_{reset}(1\ Transistor)}{\sqrt{Nb_{diodes}}}$

[Perić, Ivan et.al.] « High-voltage pixel detectors in commercial CMOS technologies for ATLAS, CLIC and Mu3e experiments ». *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, PIXEL 2012, vol. 731 (décembre 2013): 131-36. https://doi.org/10.1016/j.nima.2013.05.006.

AC link with low noise leakage current generation

- We implemented this on two pixels of ANAQIN chip with possibility to change number of diodes

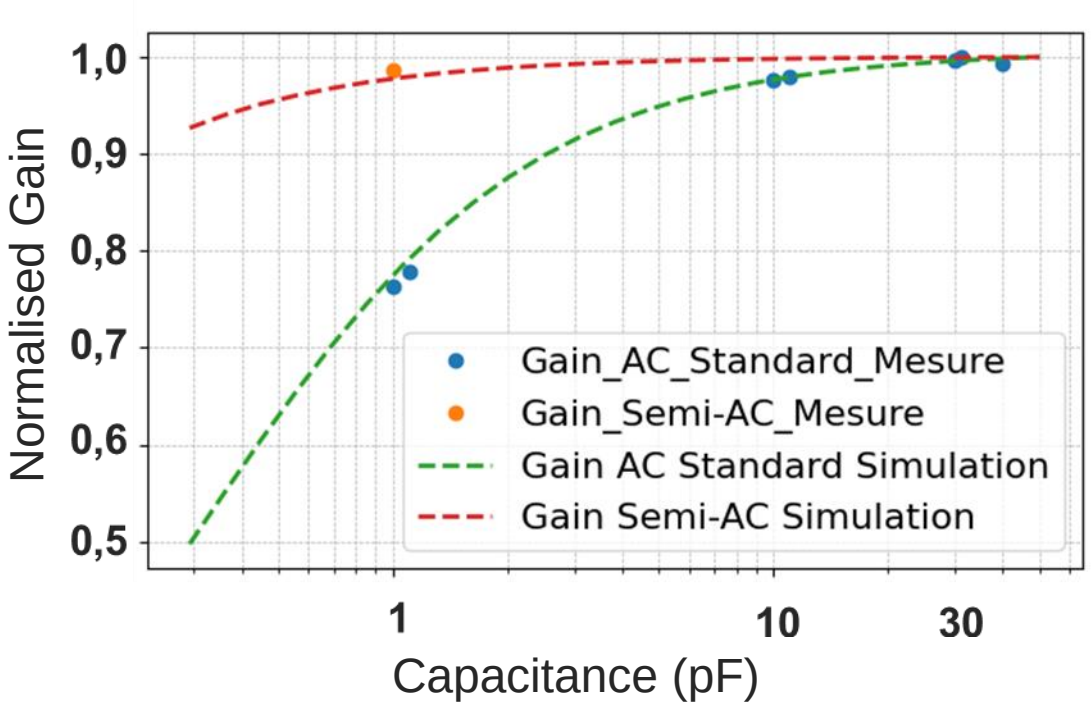


Fig 23: Gain measured with or without « semi - AC » architecture

- We reach with 1 pF and equivalent gain of 30 pF

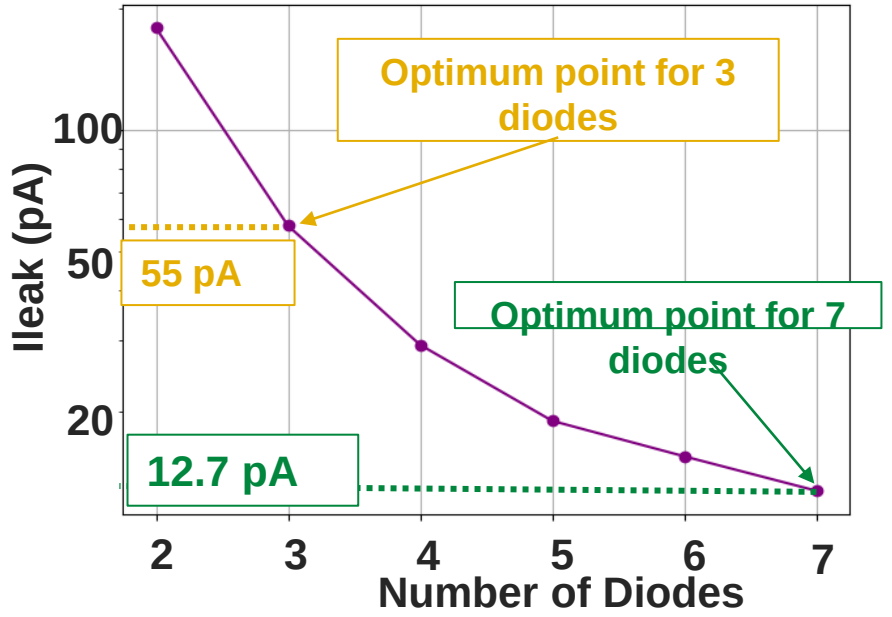


Fig 24: Simulated optimal point by variying both Tpeak and number of diode in series

- Leakage current is controlled with voltage reference
- We have seen an improvement with 1 – 2 transistors
- Larger number of transistors have shown issues in the leakage current generation

AC link with low noise leakage current generation

- We implemented this on two pixels of ANAQIN chip with possibility to change number of diodes

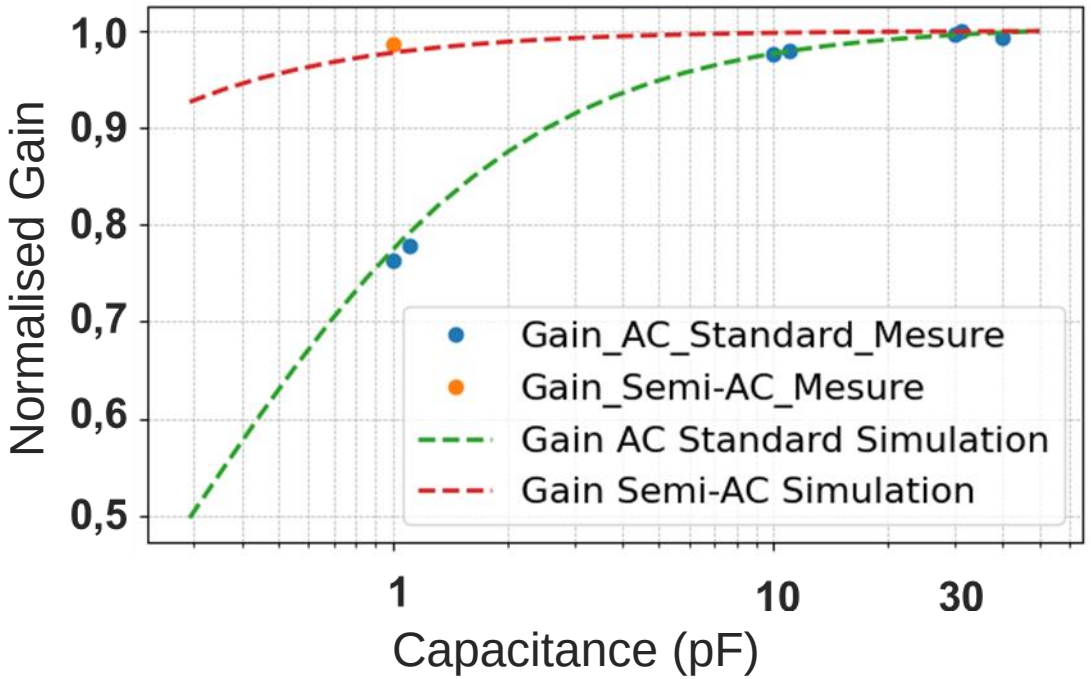


Fig 23: Gain measured with or without « semi - AC » architecture

- We reach with 1 pF and equivalent gain of 30 pF

$$ENC_{//}\ (semi - AC) \propto \sqrt{I_{leak}}.\sqrt{(N+1)/N}$$

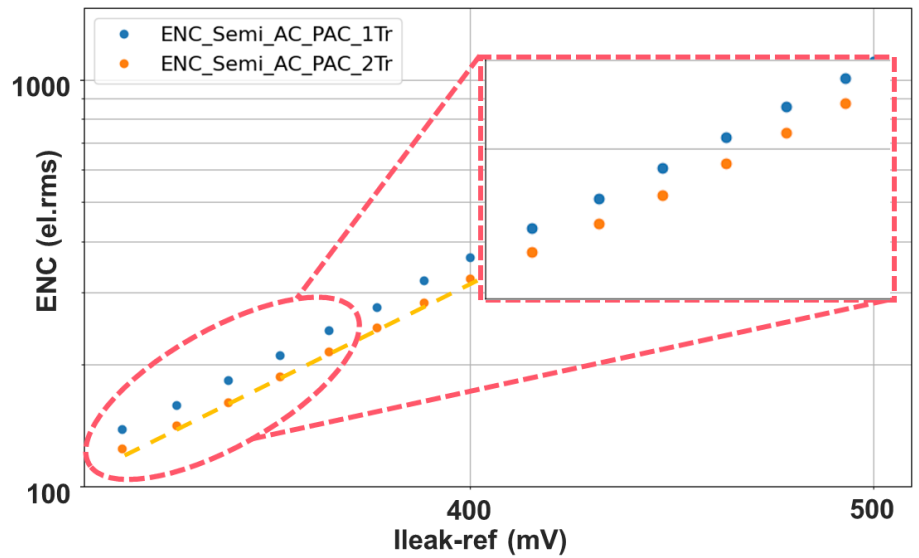


Fig 25: Measure of total noise with Varying Leakage current

- Leakage current is controlled with voltage reference
- We have seen an improvement with 1 – 2 transistors
- Larger number of transistors have shown issues in the leakage current generation

4. Packaging and interconnection

A- Packaging and interconnexion From 3D interconnection to 2D

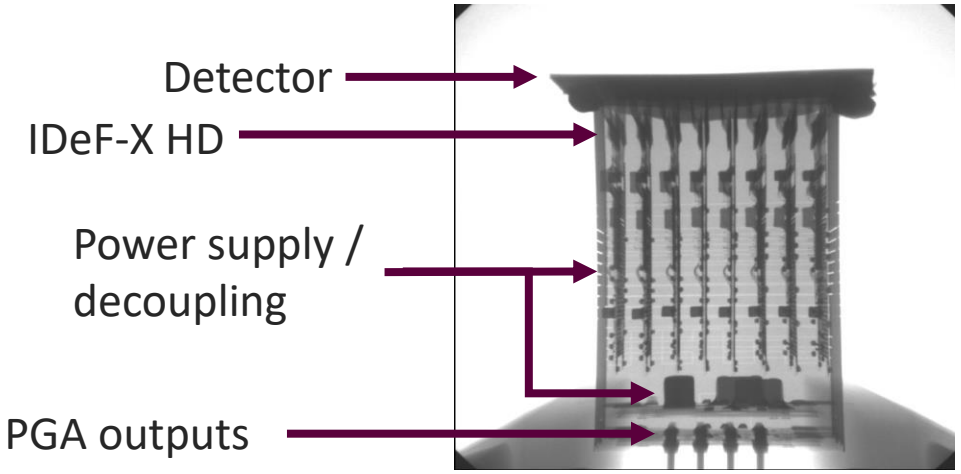
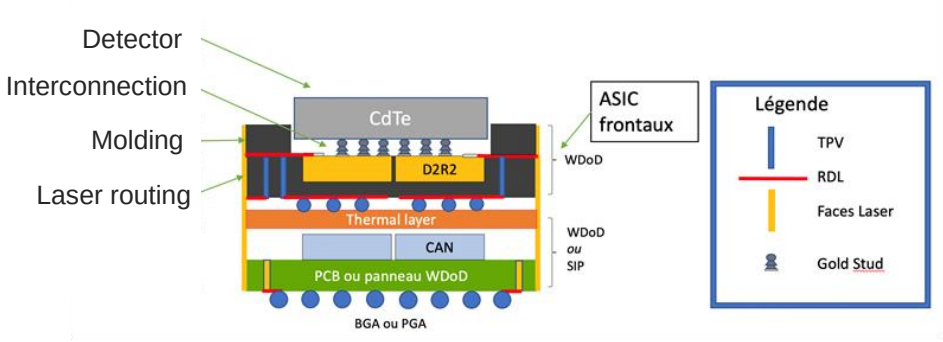
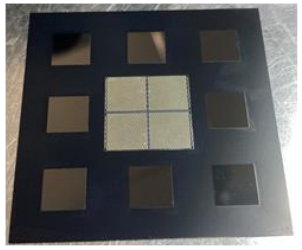
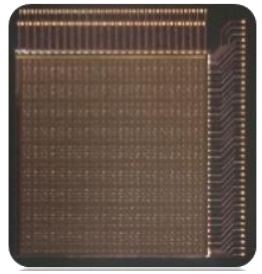


Fig 26: *X-Ray Photography of a Caliste - HD*

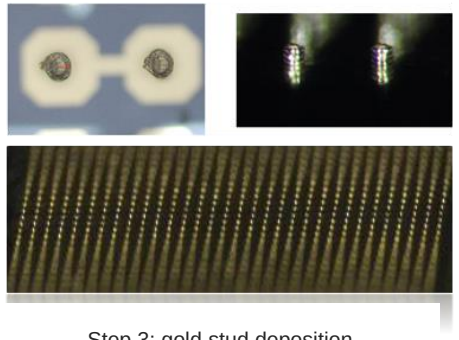




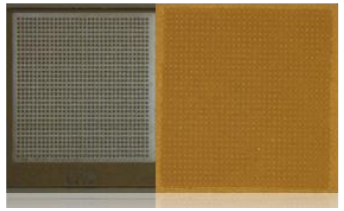
Step 1: chip molded in siliciced resin



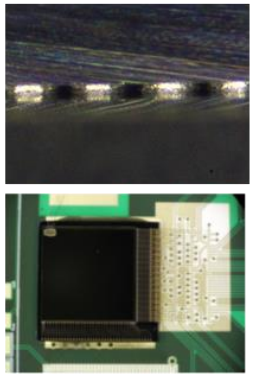
Step 2: copper deposition and lithography



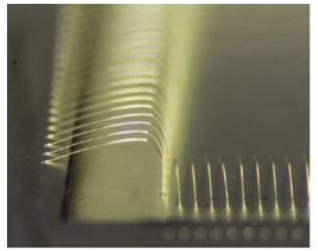
Step 3: gold stud deposition



Step 4: serigraphy with stencil and Ag epoxy



Step 5: detector deposition



Step 6: Gold wire insertion for « TPV »

Fig 27: *2D interconnection process steps*

5. Results and conclusion

A- D2R2 ASIC

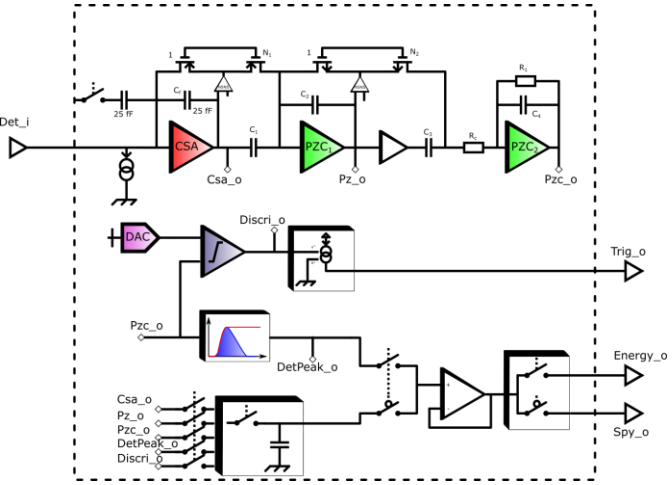


Fig 28: Schematic of one pixel

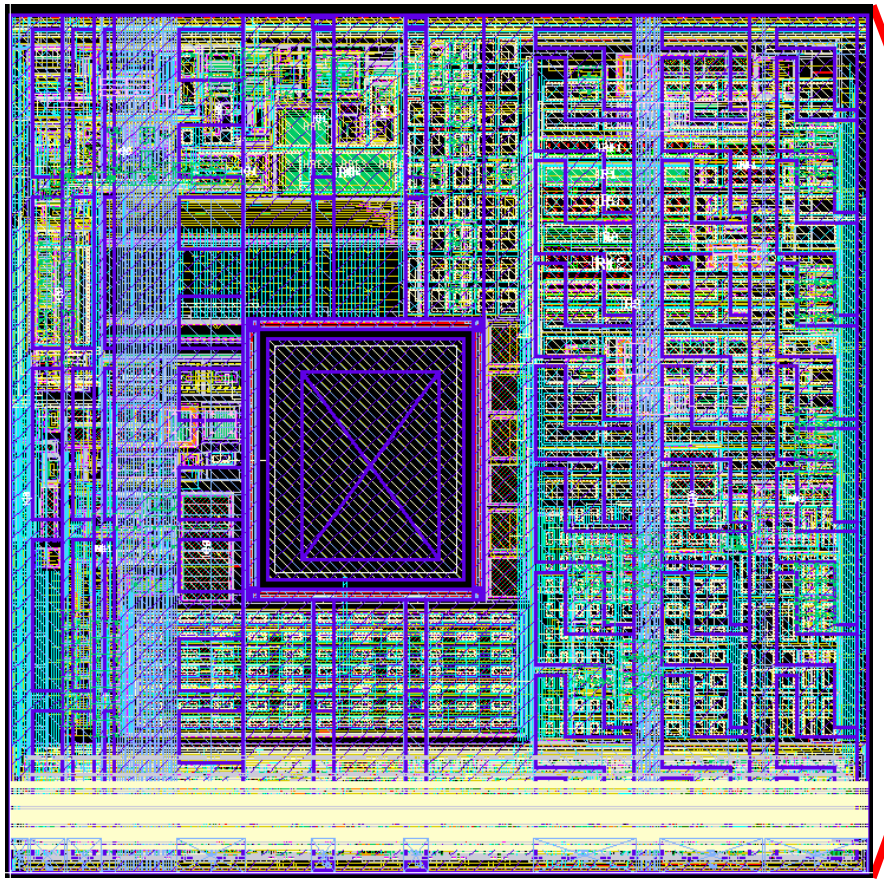


Fig 29: IDeF-X D²R$_2$ Pixel Layout

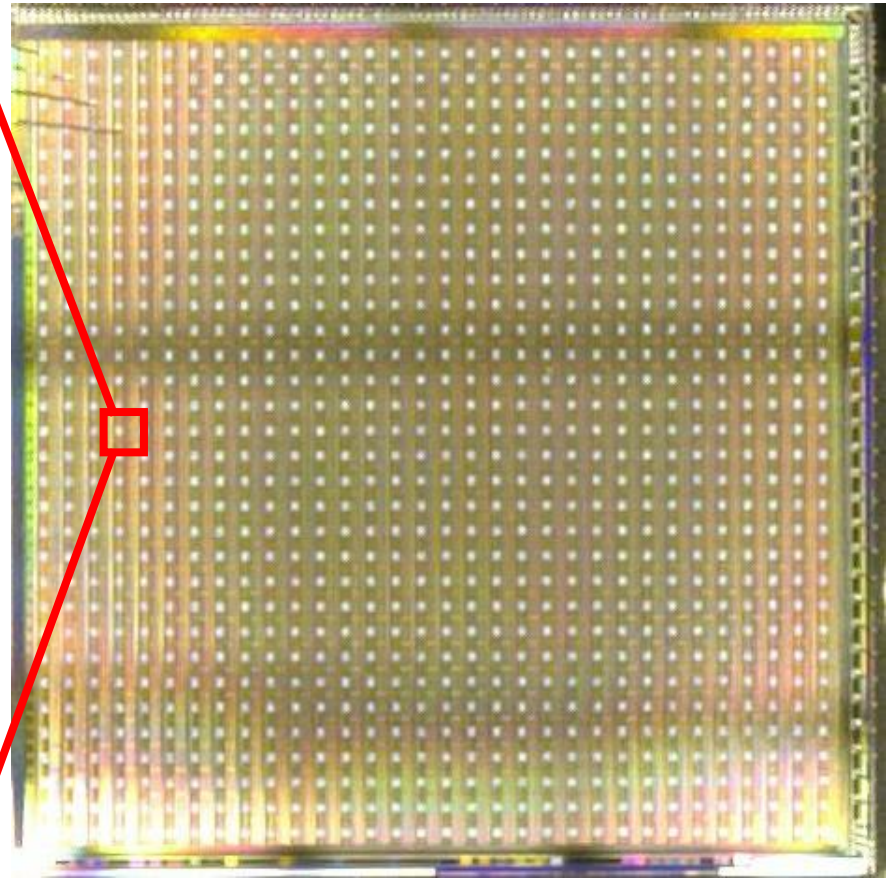


Fig 30: IDeF-X D²R$_2$ picture

A- D2R2 ASIC

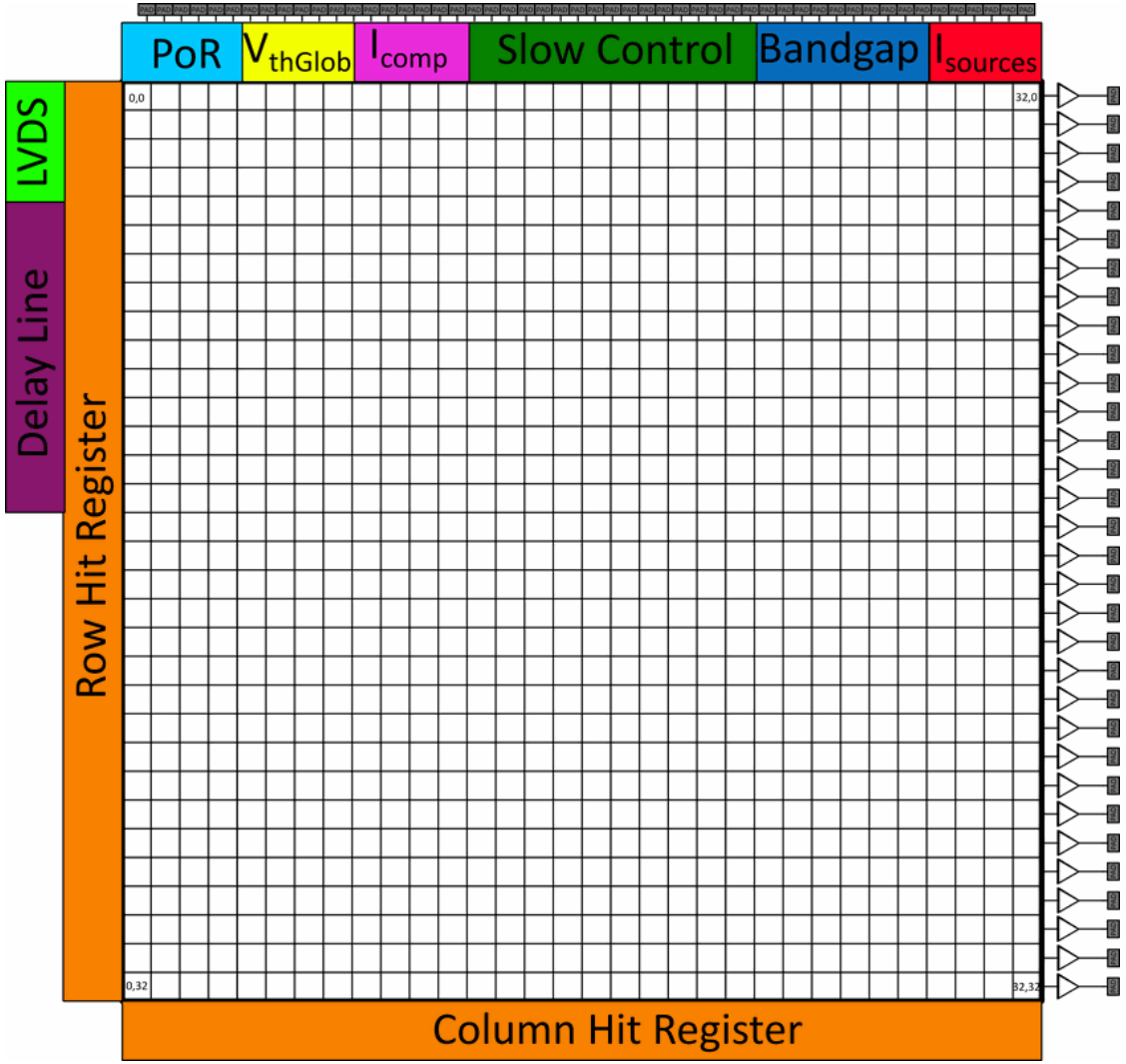
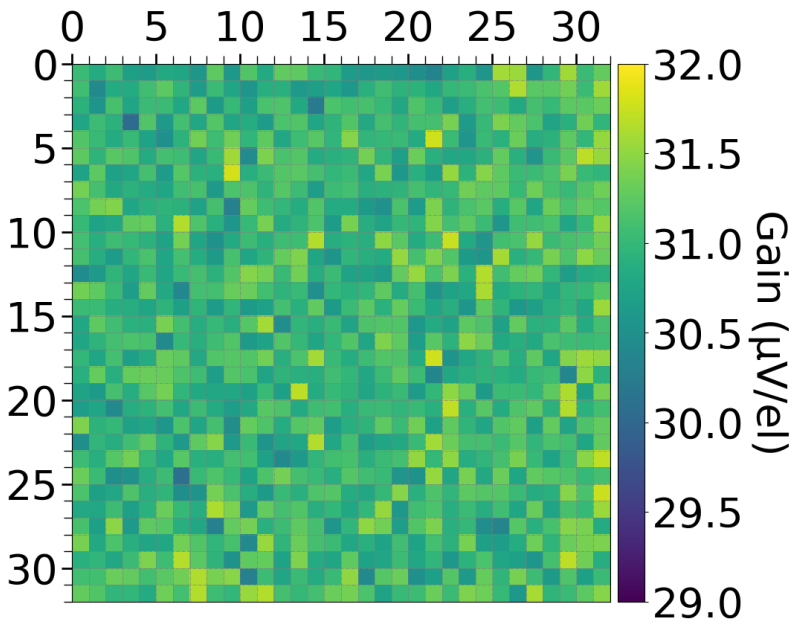


Fig 31: Readout Strategy

B- D2R2 ASIC results

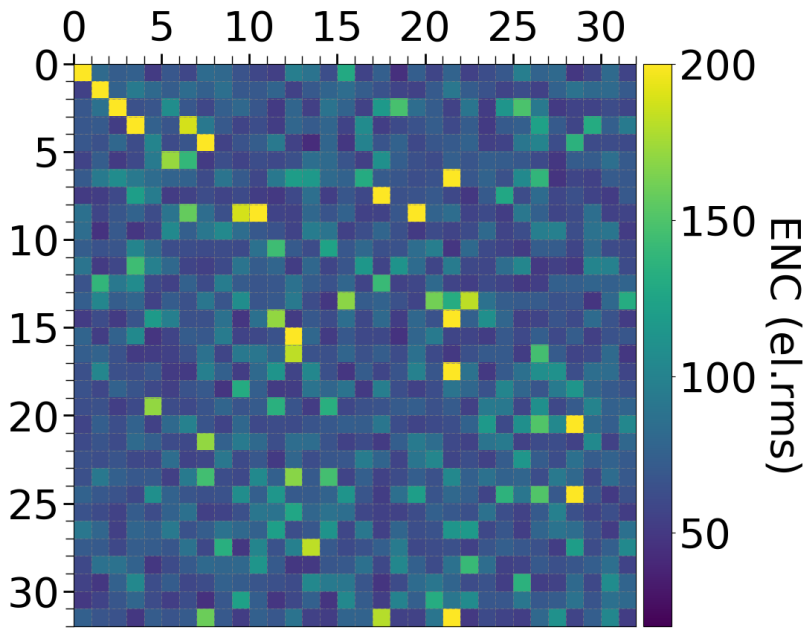
Fig 32: Gain Map



Mean value: 31 µV/el

Standard deviation: 271 nV/el

Fig 33: ENC Map



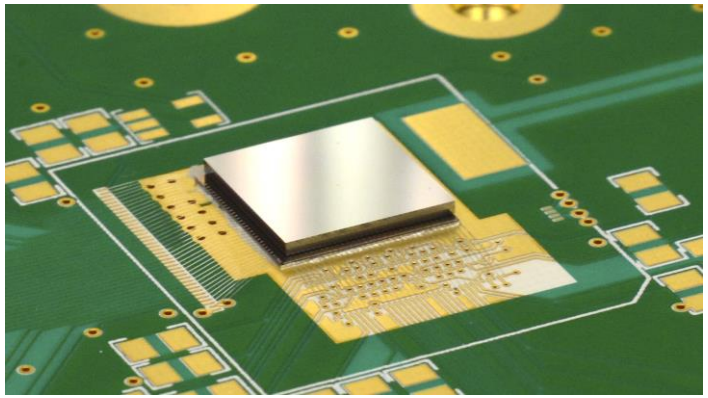
Mean value: 74 el.rms [12 expected]

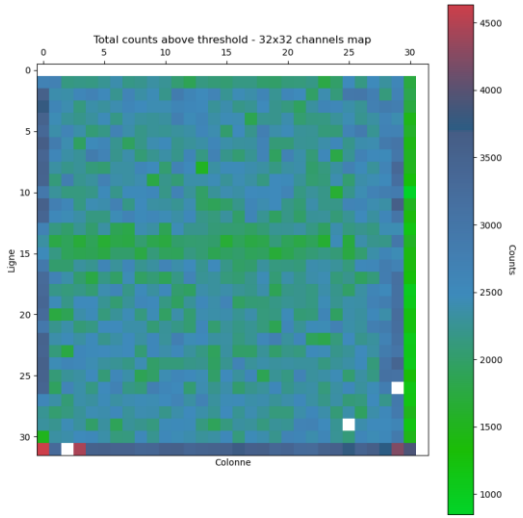
Minimum: 42 el.rms

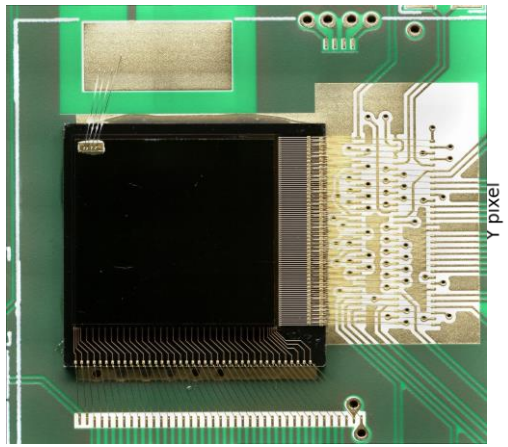
Standard deviation: 21 el.rms

[CSA + Internal shaper / All pixels]

C- Packaging and interconnexion







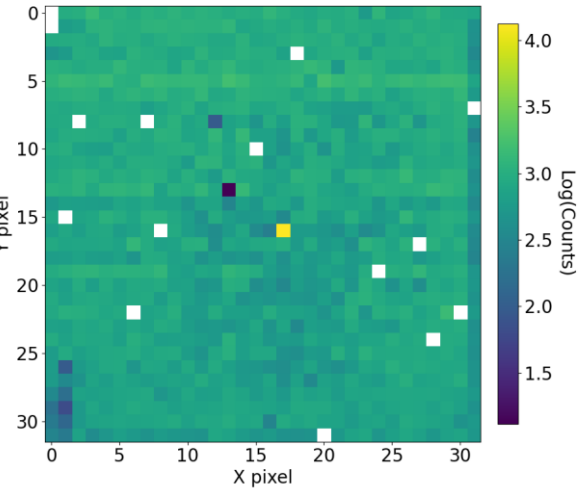


Fig 34: Hybrid made « inhouse », and count map.

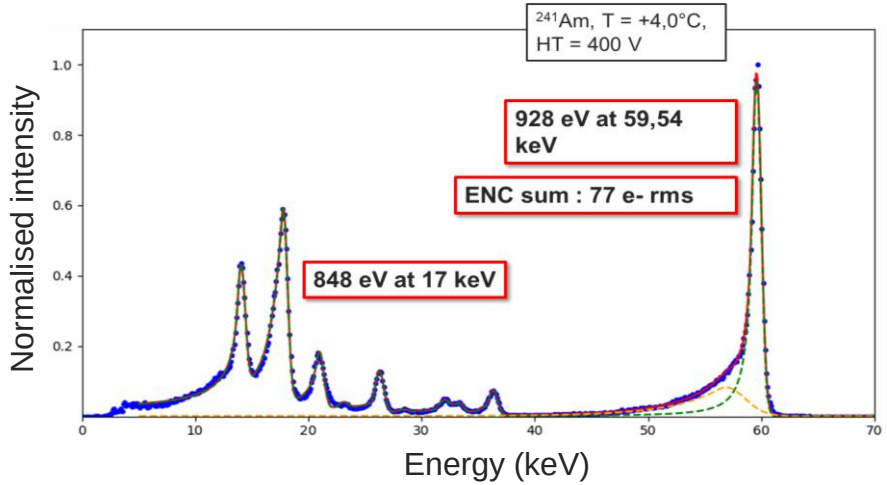


Fig 33: Hybrid made by Imagine-X Japan, hit map above threshold, and sum spectrum

- Noise with detector is similar than without (77 vs 74).
- Issue with excess of noise in the circuit (74 vs 14)
- Custom interconnects still needs improvement:
  - Not 100 % of full connection
  - Different gain seen in the pixels (not seen with IMAGIN-X hybrids)

C- ANAQIN ASIC results

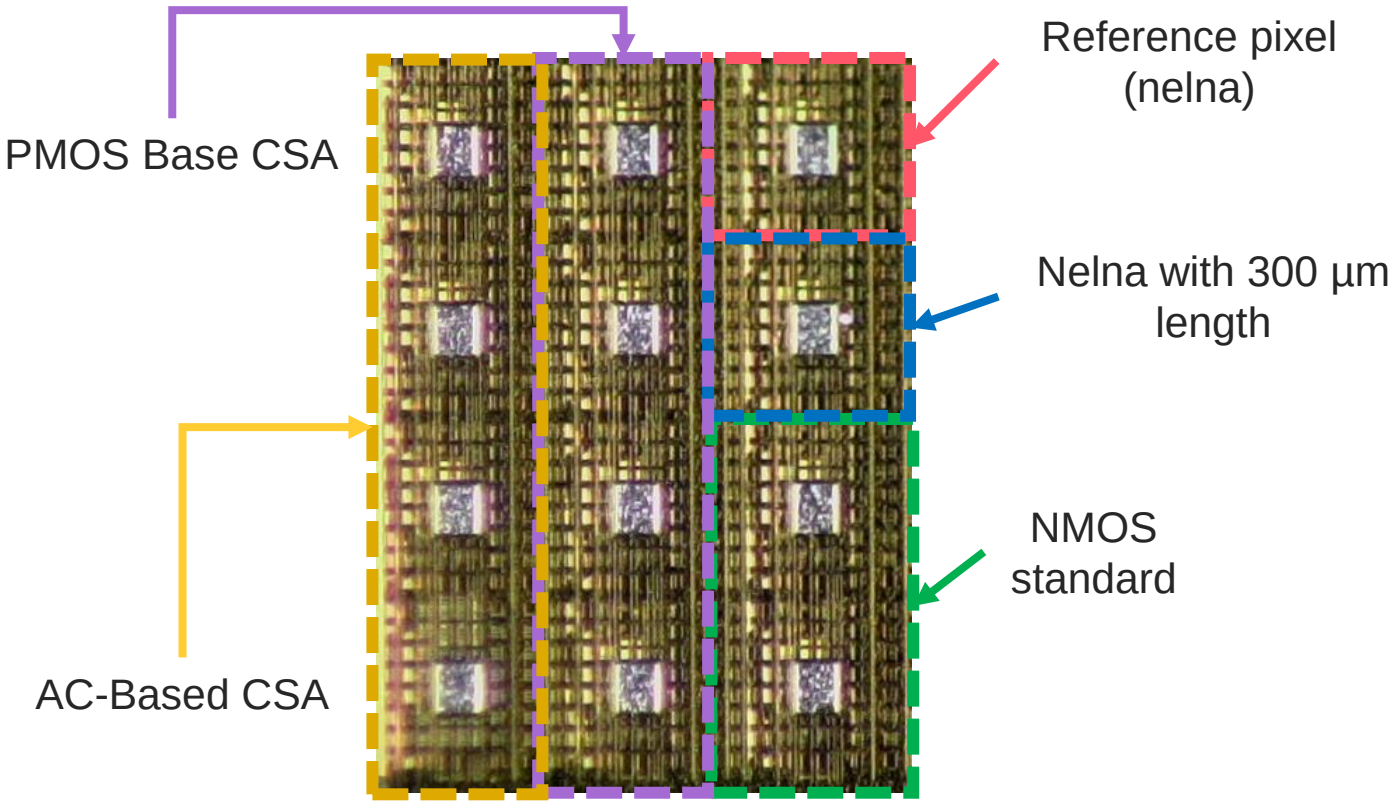
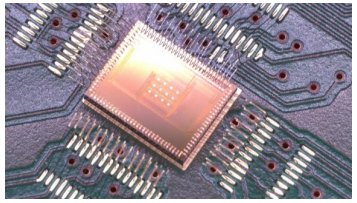
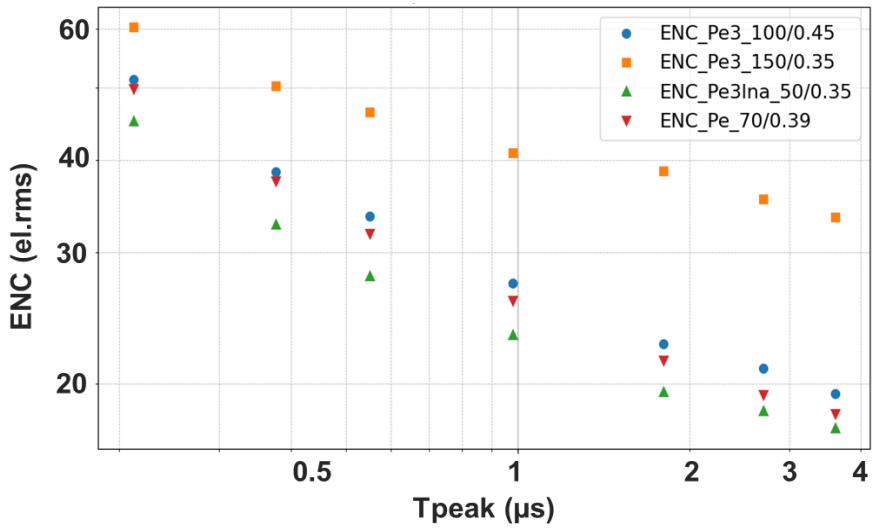


Fig 35: Picture of ANAQIN-X ASIC





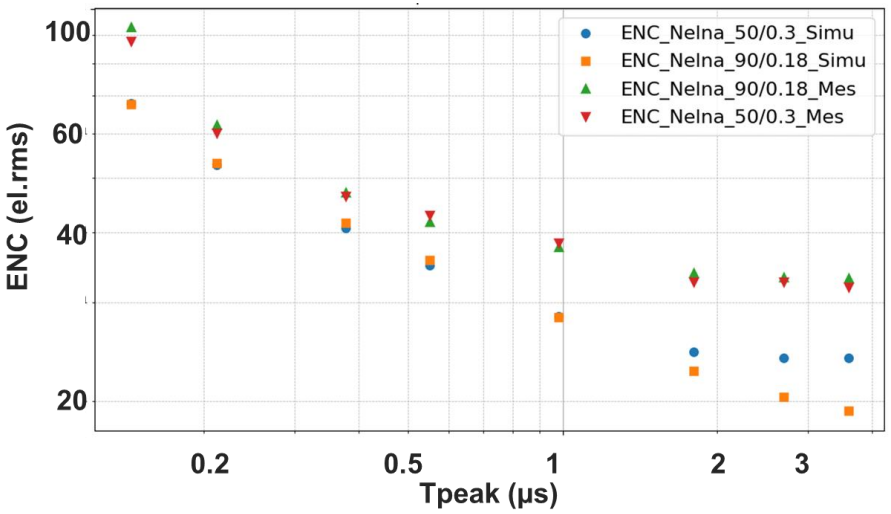


Fig 36: ENC versus peaking time for PMOS based CSA (top) and NMOS based CSA (bottom)

Conclusion

- I tried to show the different solutions we developped for reduction of:
  - Noise: CMOS amplifier, NSNS, semi-AC link
  - Interconnexion: packaging with custom WDoD
  - Space: Double stage CR-RC

- With ANAQIN-X we managed to find a pixel with a correct working point

- Future Matrix « CESAR » is planned to be taped out on july 2026
  - Pixel selected from ANAQIN-X measurements
  - Reduction of interfaces (136 pads to 64)
    - DACs for reference
    - Serialized mode for output
- In parallel, module is beeing built

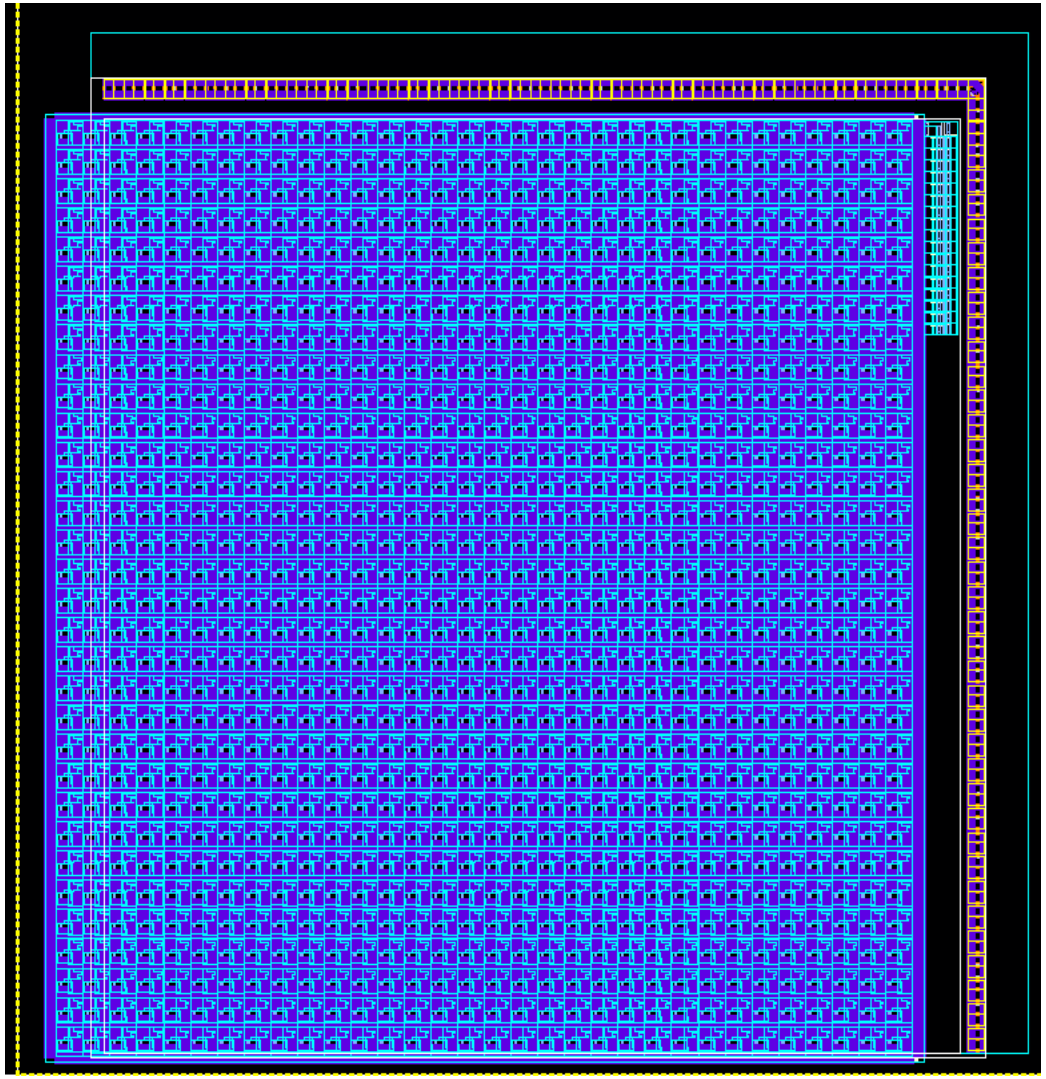
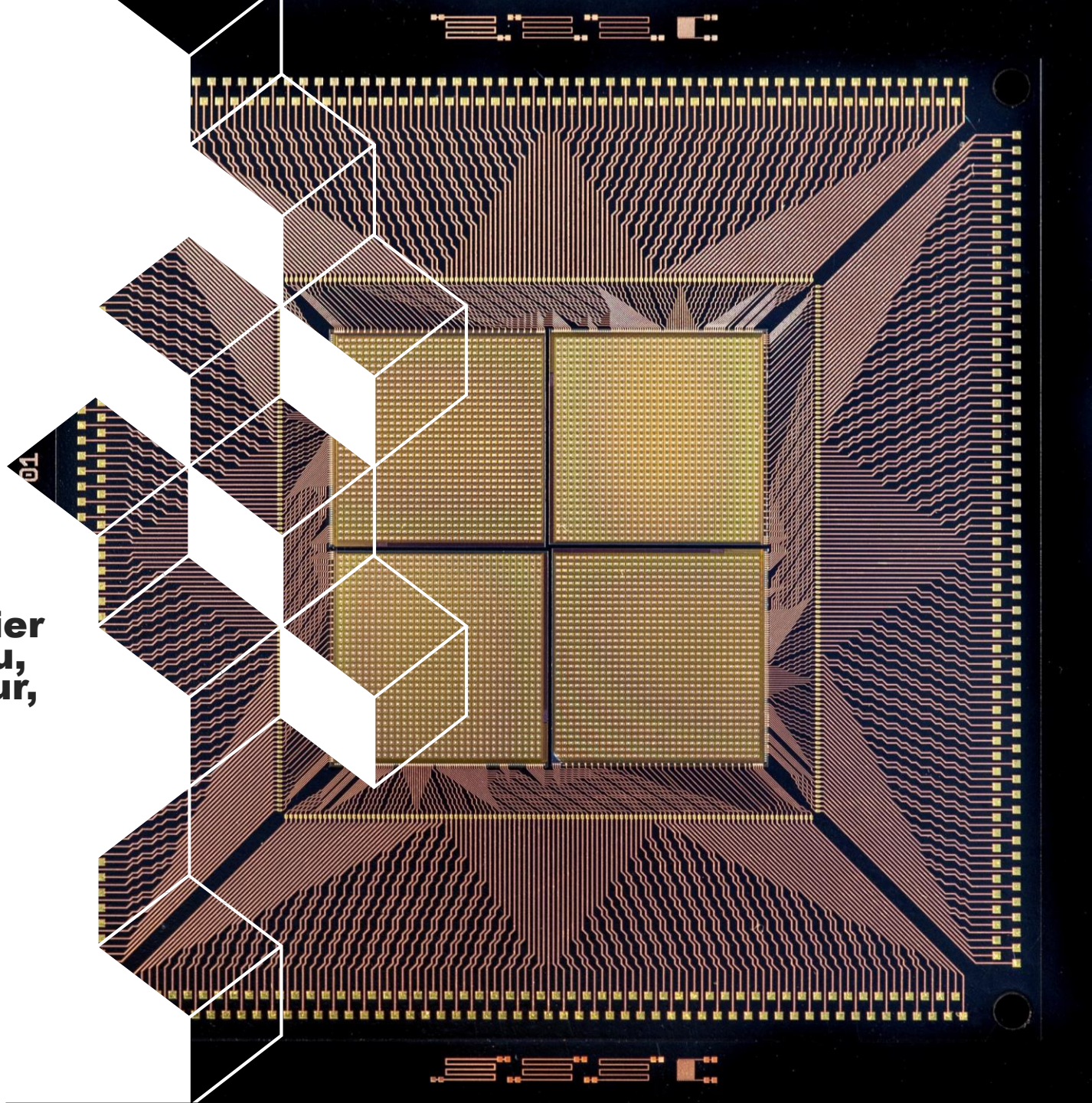


Fig 37: Layout of CESAR ASIC

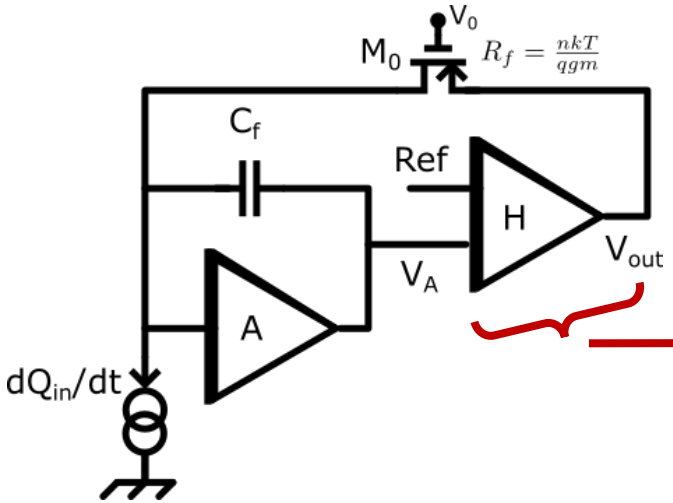
Thank You and thanks to the team

Xavier Coppolani, Pascal Couderc, Olivier Gevin, Olivier Limousin, Florent Bouyjou, Hugo Allaire, Diana Renaud, Marin Prieur, Aline Meuris, Fabrice Soufflet, Jean-Michel Guinet, Eric Tan, Noemie Belin, Jérémy Chauveau, Olivier Garel, Hervé Bervas, Denis Chesnais,...



Backups

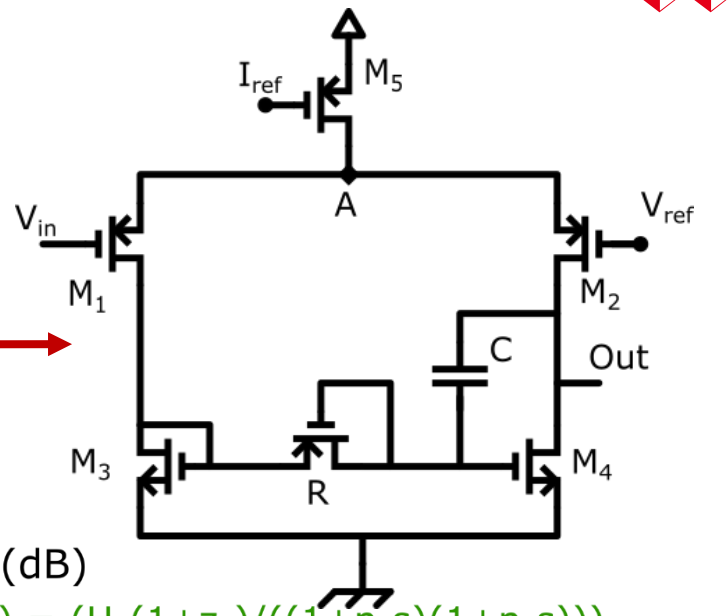
Oscillations with low pass NSNS

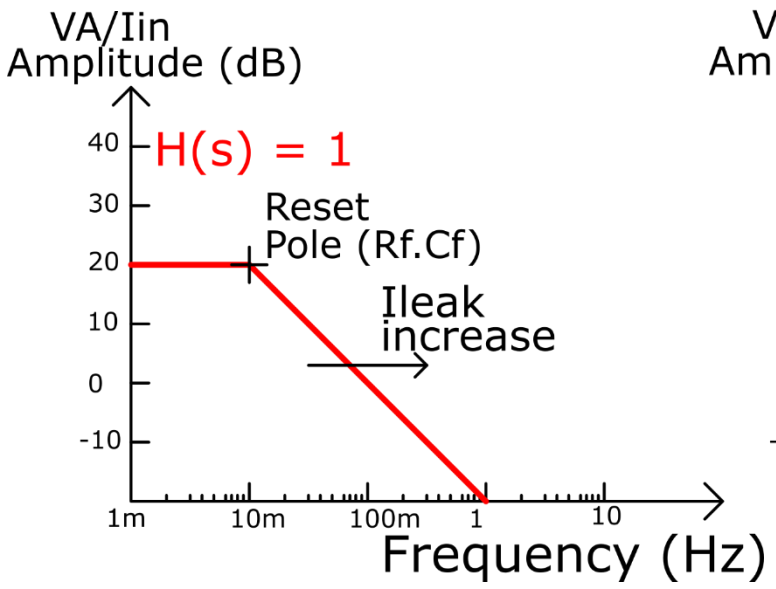


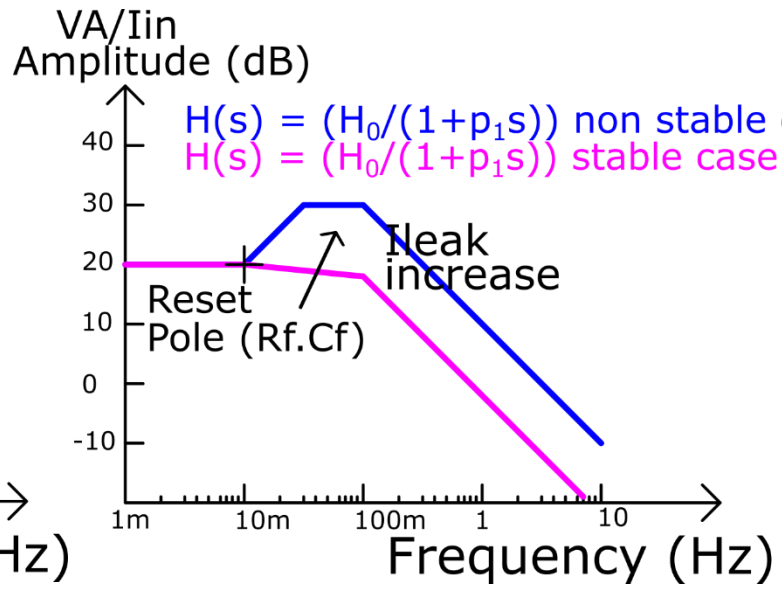
If Low pass:

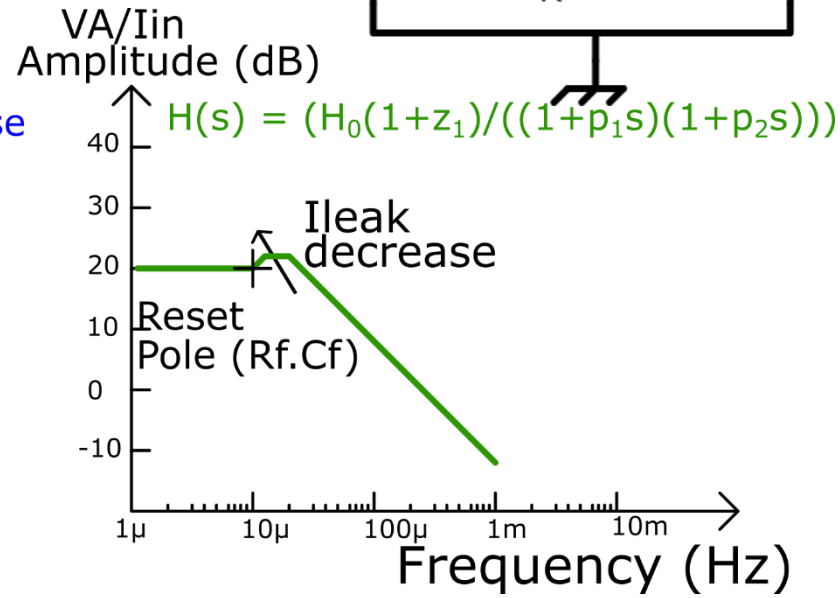
- $I_{leak} \uparrow \Leftrightarrow$ oscillation

Solution:







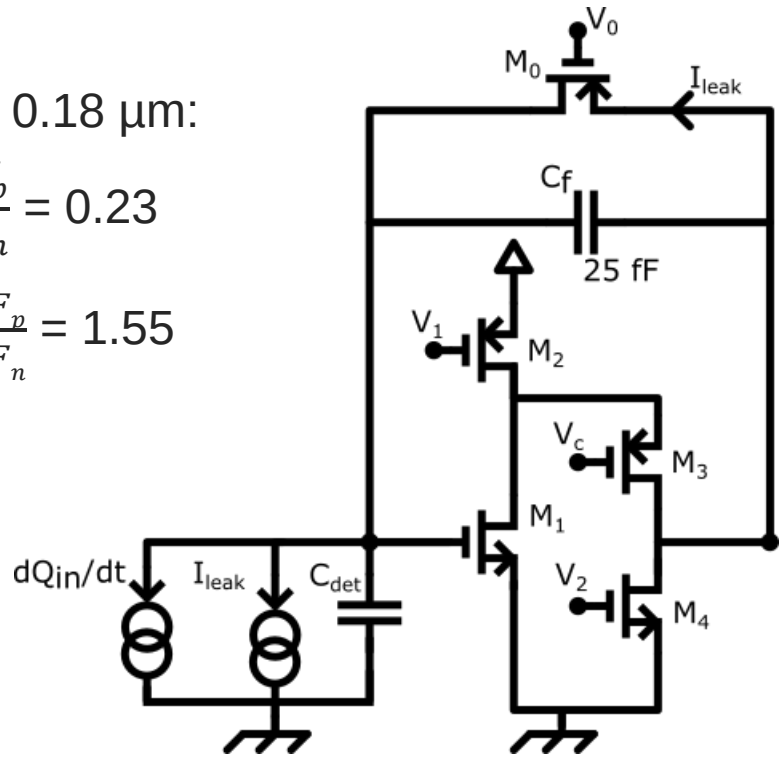


Simulation optimisation with XFAB018 and nelna

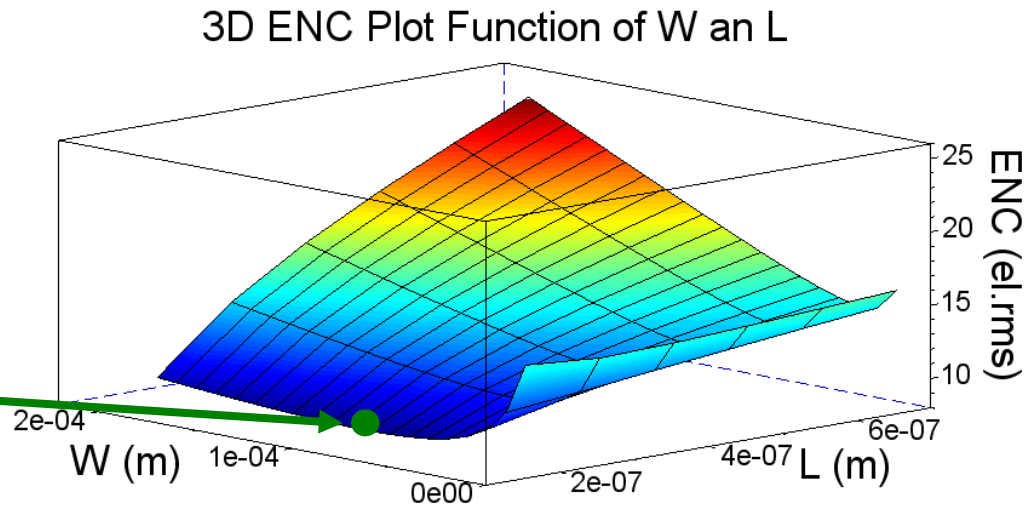
XFAB 0.18 µm:

$b = \frac{k'_p}{k'_n} = 0.23$

$c = \frac{KF_p}{KF_n} = 1.55$



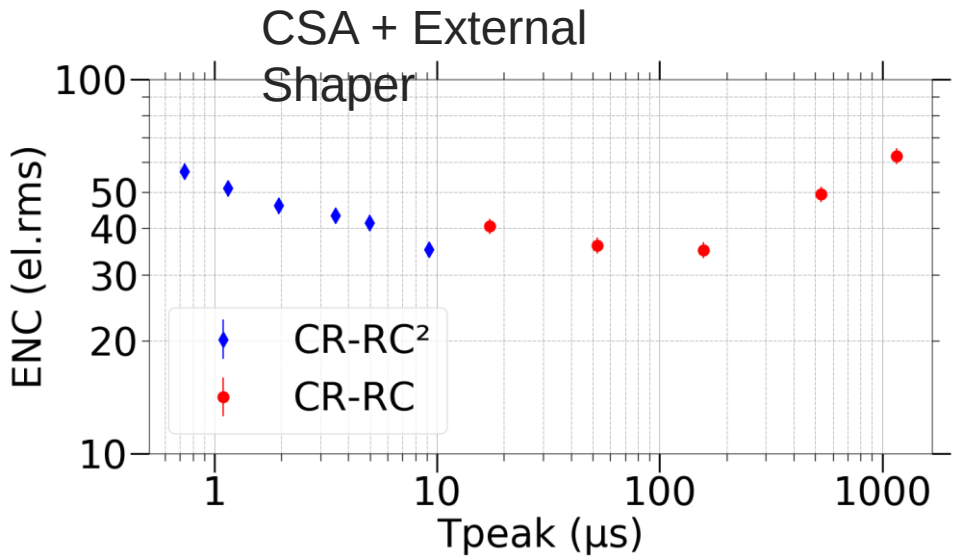
- G_{OL} = 8000 V/V
- G_{CL} = 6.2 µV/el
- T_{rise} = 50 ns
- W = 90 µm
- L = 180 nm

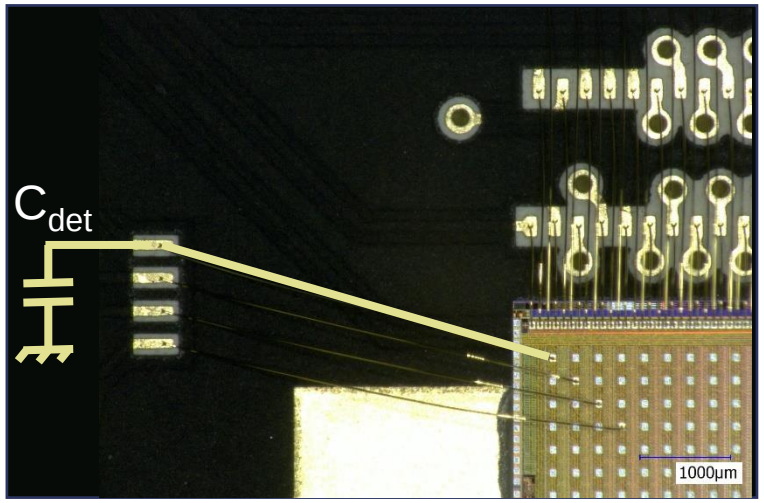


Noise	NMOS	PMOS	CMOS
Flicker	**0.38**	1	0.5
Thermal	1	1.44	**0.94**

- ENC_{Floor} = 14 el.rms with Ideal CR-RC filter

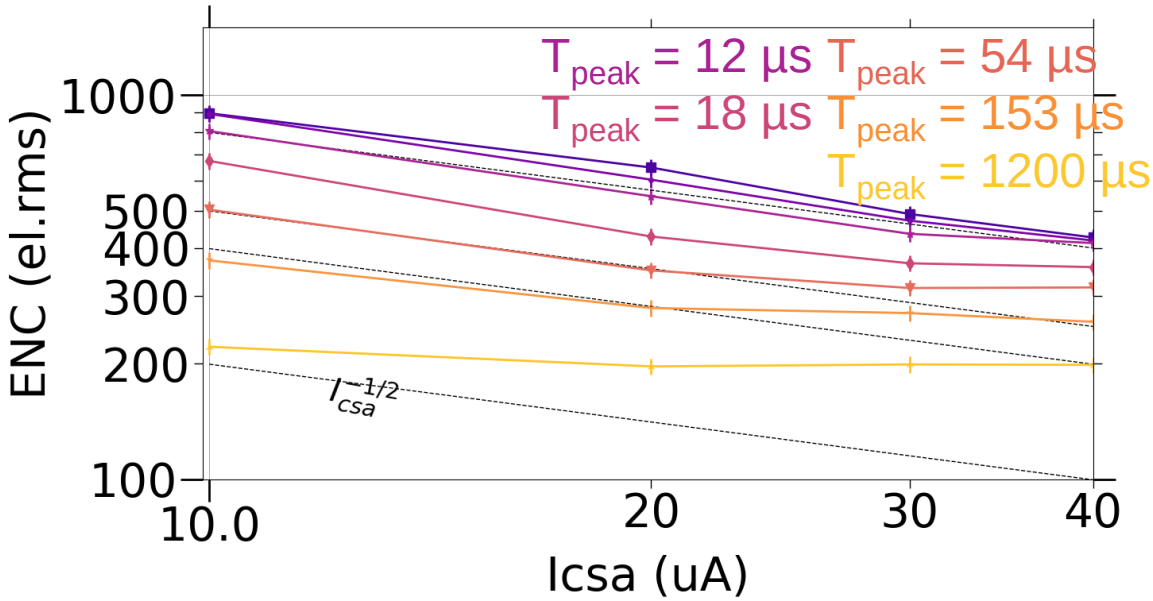
Measurement D2R2



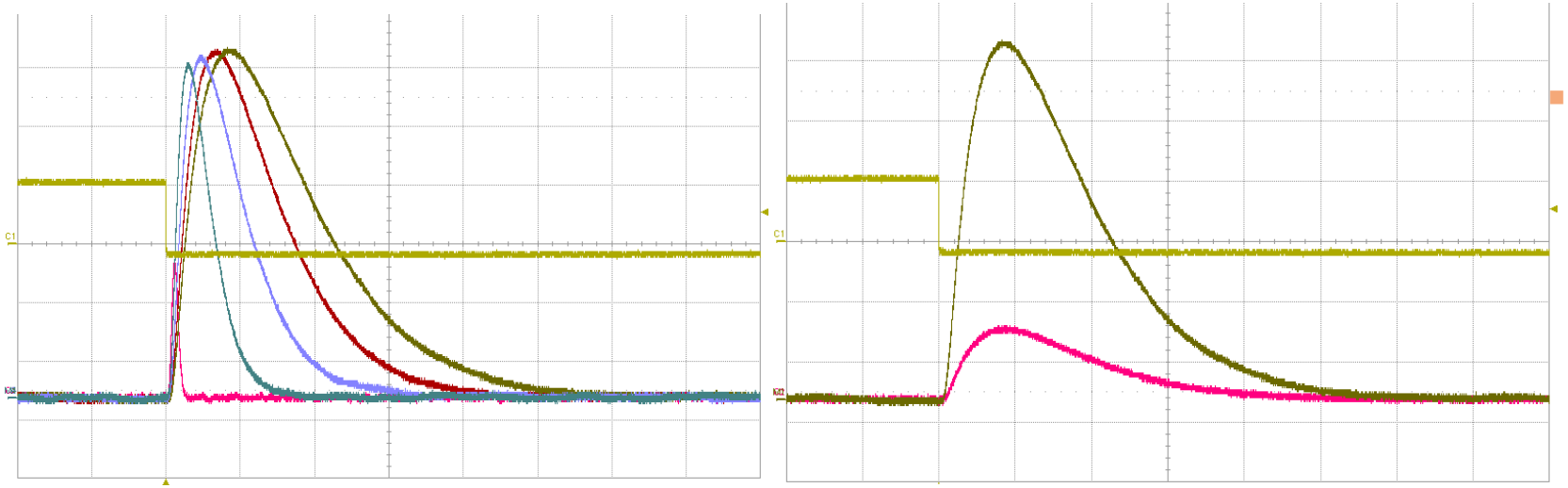


- « Flat » slope
- 1/f noise ?
- Vary with I_{csa}

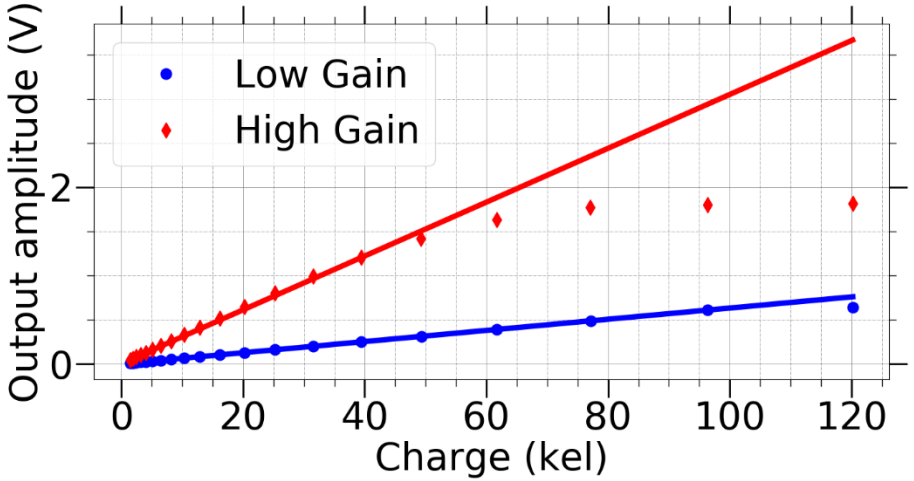
- Gain: 6.3 µV/el
- ENC_{floor}: 36 el.rms at T_{peak} = 9.5 µs [CSA + External filter] (14 el.rms expected)
- Variation with capacitance: 300 el/pF at T_{peak} = 4 µs

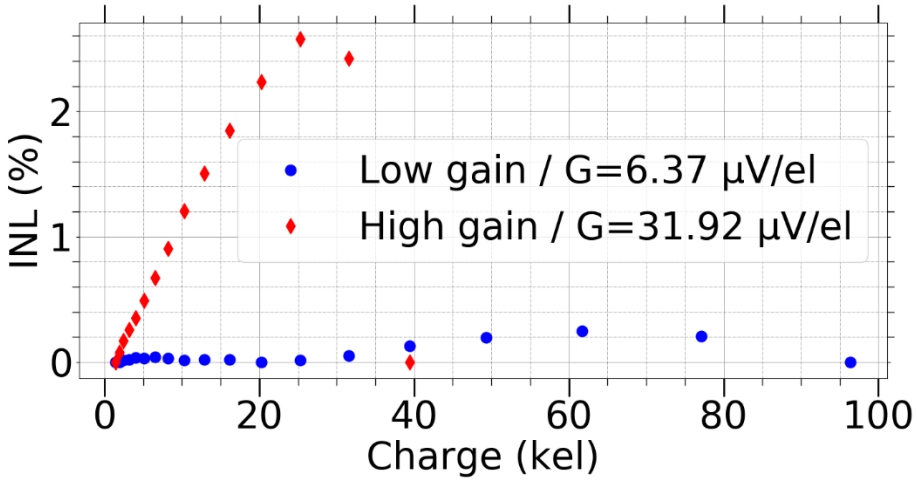


Measurement D2R2

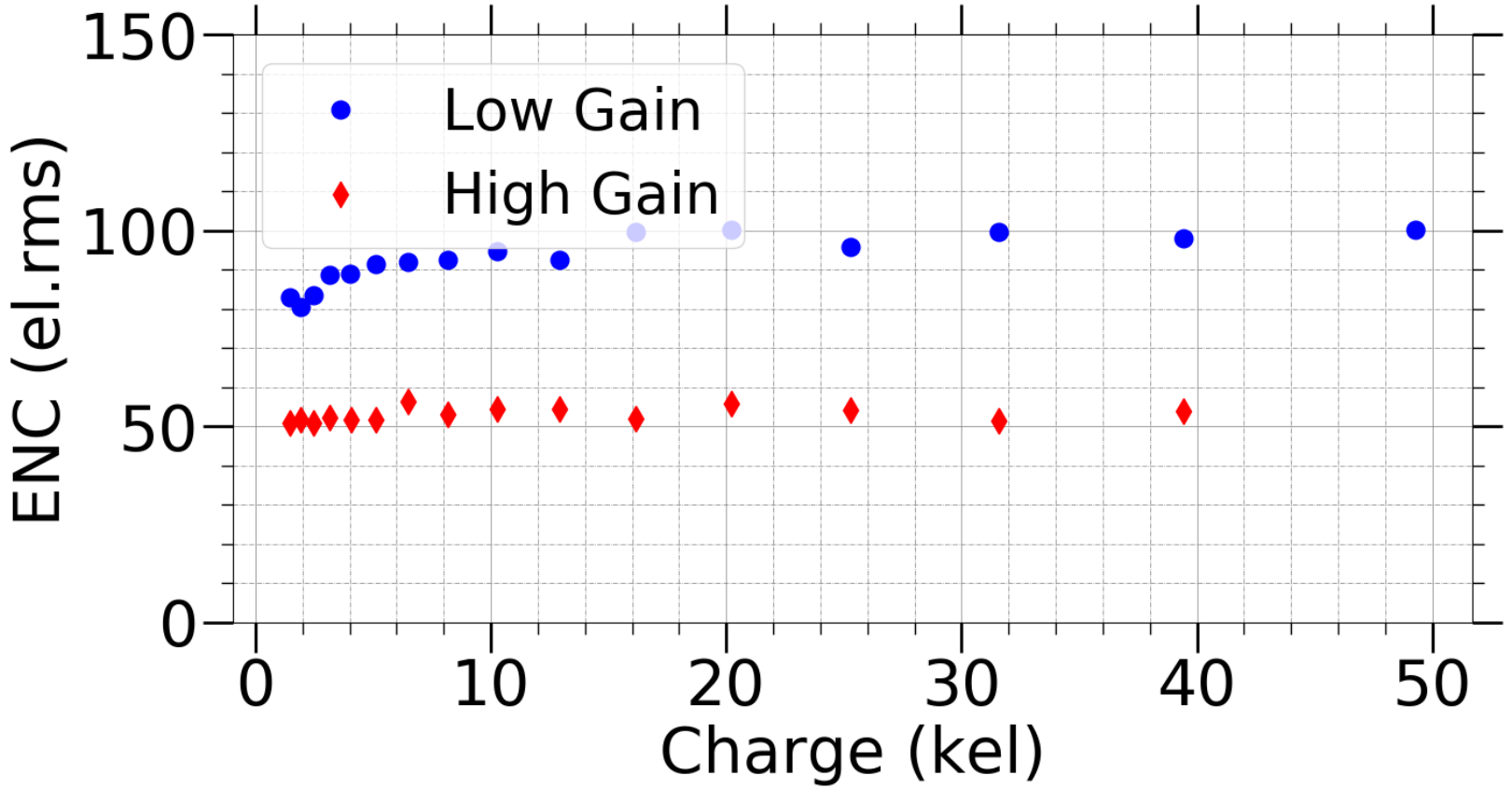


- Linearity
  - 2.6 % [For all range high gain]
  - 0.24 % [For 0-110 keV range high gain]



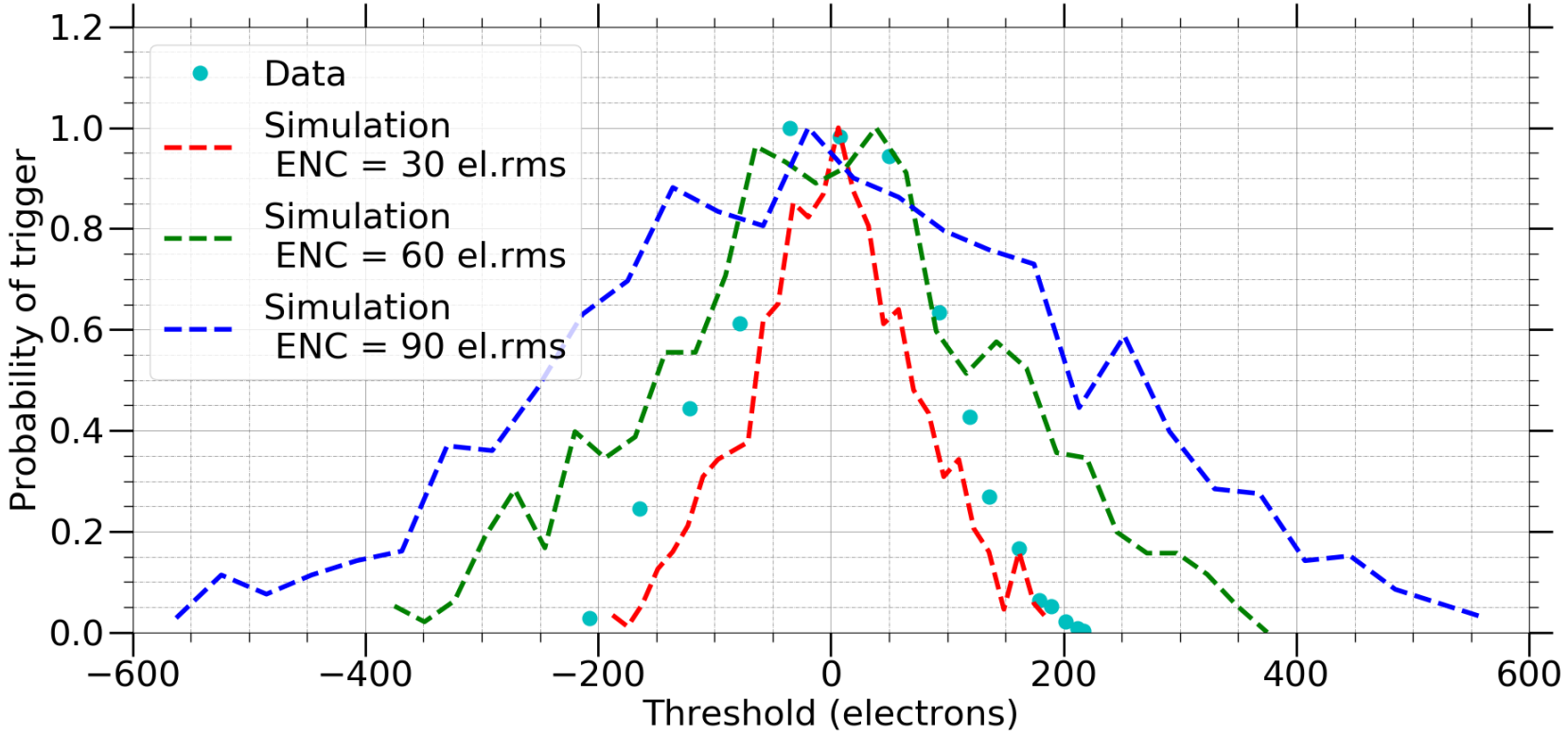


Measurement D2R2



Measurement D2R2

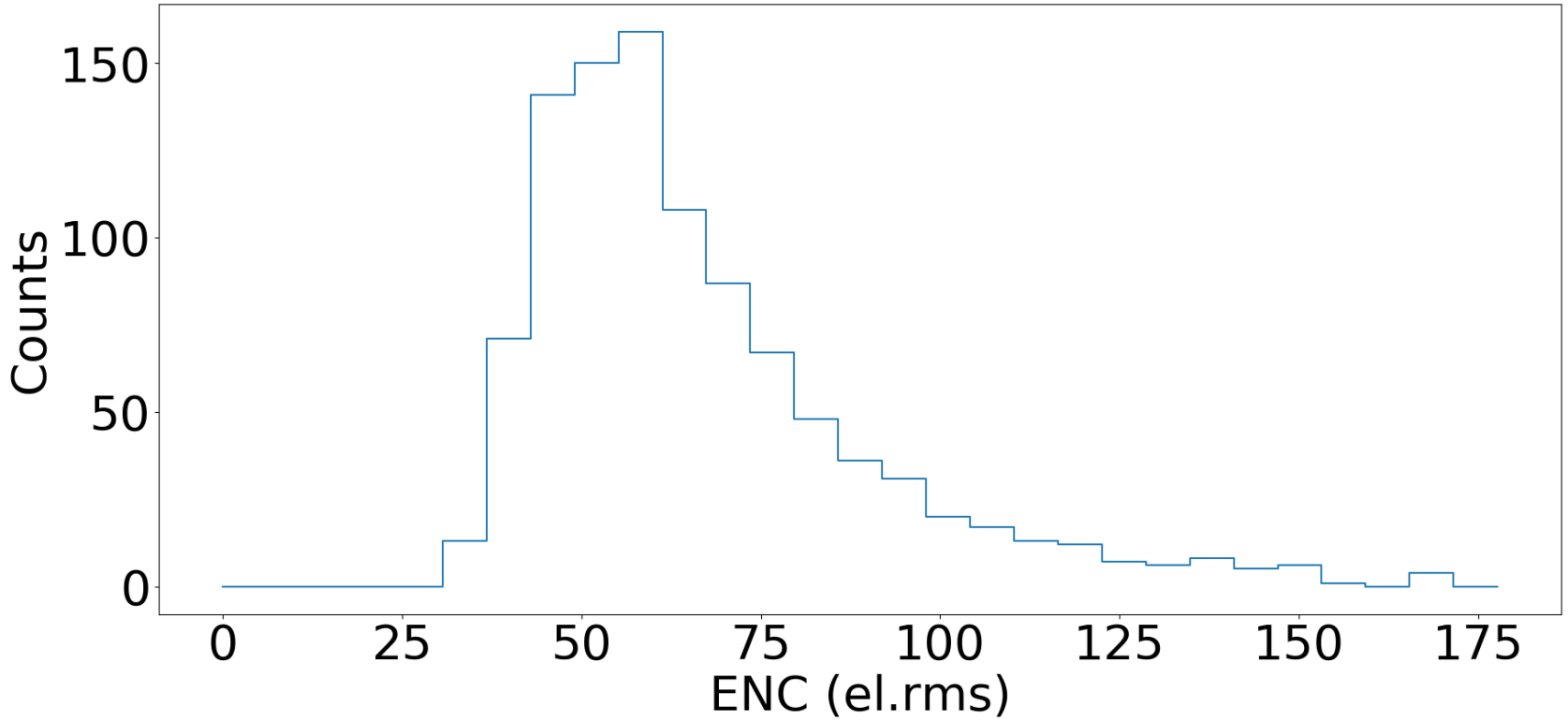
Discriminator



- Minimum threshold:
  - 1.5 keV
- Noise contribution From Discriminator:
  - < 30 el.rms

Measurement D2R2

Noise Distribution



Measurement D2R2

- Filter Function

$$H_{Csa}(s) = \frac{V_{out_{Csa}}}{Q_{in}} = \frac{\frac{s}{gm_1}}{1 + \frac{C_f}{gm_1}s}$$

$$H_{Stage_1}(s) = \frac{V_{out_{Stage_1}}}{V_{out_{Csa}}} = \frac{-\frac{N_1 gm_1}{gm_2}\left(1 + \frac{C_1 s}{N_1 gm_1}\right)}{1 + \frac{C_2 s}{gm_2}}$$

$$H_{Stage_2}(s) = \frac{V_{out_{Stage_2}}}{V_{out_{Stage_1}}} = \frac{-R_4 N_2 gm_2\left(1 + \frac{C_3 s}{N_2 gm_2}\right)}{(1 + R_4 C_4 s)(1 + R_c N_2 gm_2 + R_c C_3 s)}$$

$$N = N_1 \times N_2$$

$$C_1 = N_1 C_f$$

$$C_3 = N_2 C_2$$

$$C_3 = 3C_4$$

$$R_c = \frac{R_4}{3}$$

$$R_c \ll \frac{1}{N_2 gm_2}$$

$$H_{PZC_{TwoStages}}(s) = s \times \frac{R_4 N}{(1 + R_4 C_4 s)^2}$$

$$H_{PZC_{TwoStages}}(s) = \frac{\cancel{\frac{s}{gm_1}}}{1 + \cancel{\frac{C_f}{gm_1}}s} \times \frac{\frac{R_4 N_2 N_1 \cancel{gm_1} \cancel{gm_2}}{\cancel{gm_2}}\left(1 + \frac{C_1 s}{N_1 gm_1}\right)\left(1 + \cancel{\frac{C_3 s}{N_2 gm_2}}\right)}{\left(1 + \cancel{\frac{C_2 s}{gm_2}}\right)(1 + R_4 C_4 s)(1 + R_c \cancel{N_2 gm_2} + R_c C_3 s)}$$

Filter Area

$$S_1 = \frac{1}{\varepsilon}\left(\underbrace{C_f(1+N)}_{C_f \text{ and } C_1} + \underbrace{\frac{Nq}{3G_{tot}}}_{C_4}\right) + \underbrace{\frac{1}{\gamma}\left(\frac{4}{3}R_4\right)}_{R_4 \text{ and } R_c} + \underbrace{W_{reset}L_{reset}(1+N)}_{transistors}$$

$$S_2 = \frac{1}{\varepsilon}\left(\underbrace{C_f(1+N_1)}_{C_f \text{ and } C_1} + \underbrace{\frac{N_1 C_f}{Gain_{PZ}}\left(1 + \frac{N}{N_1}\right)}_{C_2 \text{ and } C_3} + \underbrace{\frac{Nq}{3Gain_{tot}}}_{C_4}\right) + \underbrace{\frac{1}{\gamma}\left(\frac{4}{3}R_4\right)}_{R_4 \text{ and } R_c} + \underbrace{W_{reset}L_{reset}\left(1 + N_1 + \frac{N}{N_1}\right)}_{transistors}$$

Measurement D2R2

- Why?:

Parallel noise:

$$ENC_{para}^2 = 2qI_{leak}T_{peak} + 4kTgm$$

WI: $gm_{WI} = \frac{qI_{leak}}{nkT}$

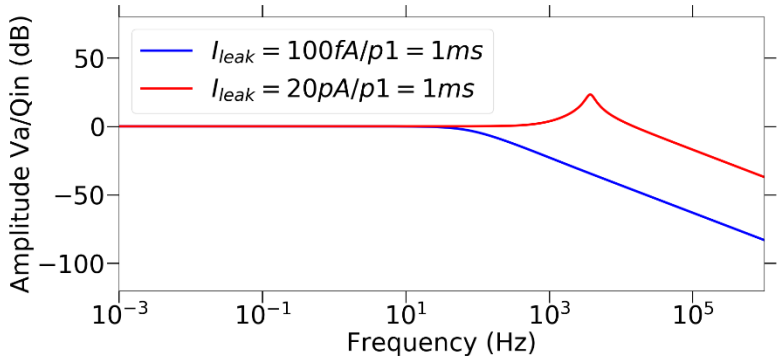
SI: $gm_{SI} = \sqrt{2k_n' I_{leak} \cdot \frac{W}{L}}$

- How?:

Low pass:

$$\frac{V_A}{Q_{in}} = \frac{R_f(1+p_1 s)}{H_0 + R_f C_f s + p_1 R_f C_f s^2}$$

Stability: $p_1 < \frac{0.25 R_f C_f}{H_0}$

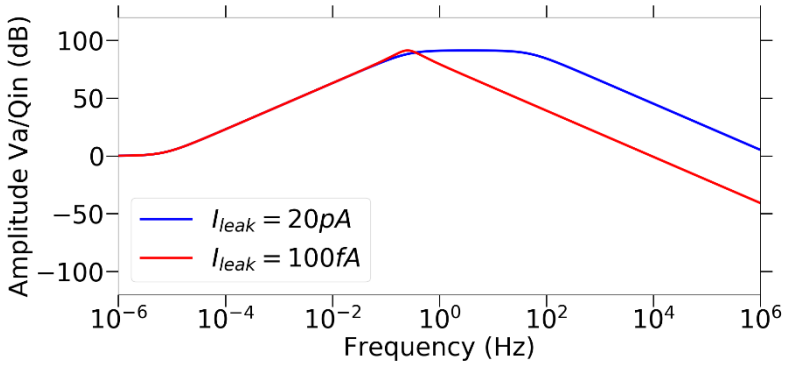


- How?:

3rd Order system:

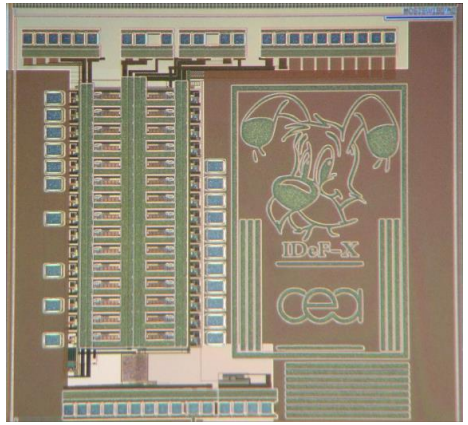
$$\frac{V_A}{Q_{in}} = \frac{G_f}{H_0} \frac{1 + (p_1+p_2)s + p_1 p_2 s^2}{1 + \left(z_1 + \frac{R_f C_f}{H_0}\right)s + \frac{R_f C_f}{H_0}(p_1+p_2)s^2 + \frac{R_f C_f}{H_0} p_1 p_2 s^3}$$

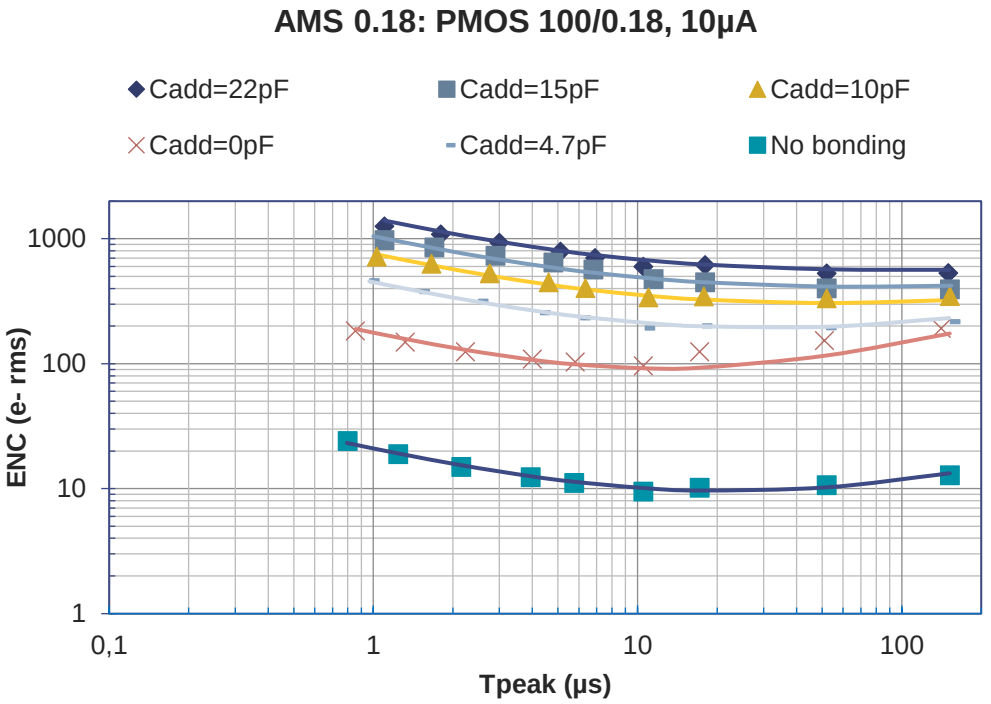
Stability:

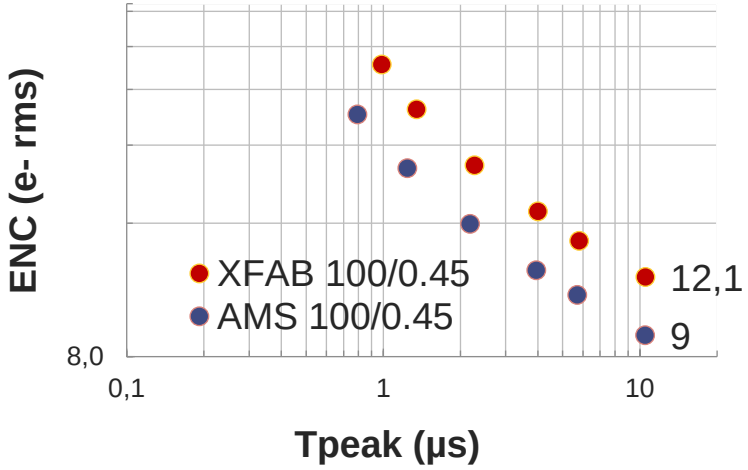


Technology validation

- For finding appropriate technology we have done several test matrices of CSA's in:
  - AMS 0,18 µm
    - Pmos
    - Nmos
  - XFAB 0,18 µm
    - Pmos
    - Nmos
    - Nmos « low noise »
    - Pmos 3,3V
    - Pmos « low noise »



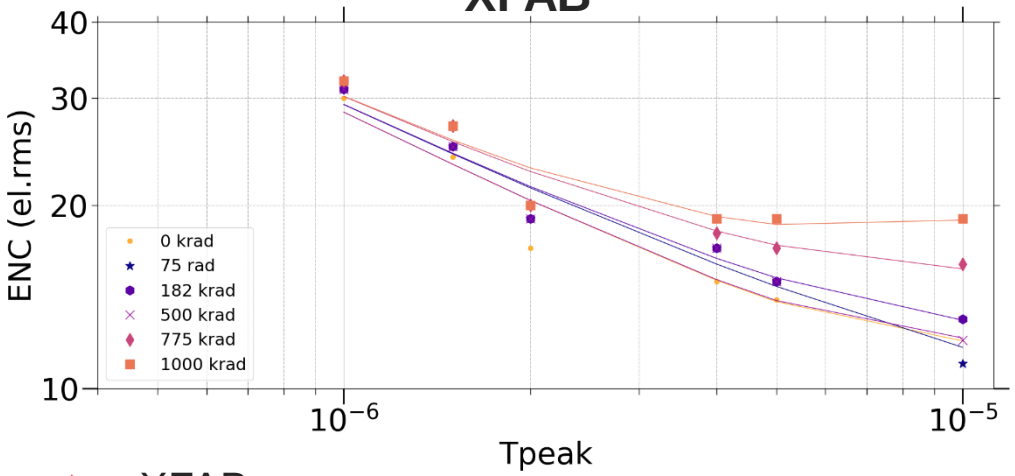


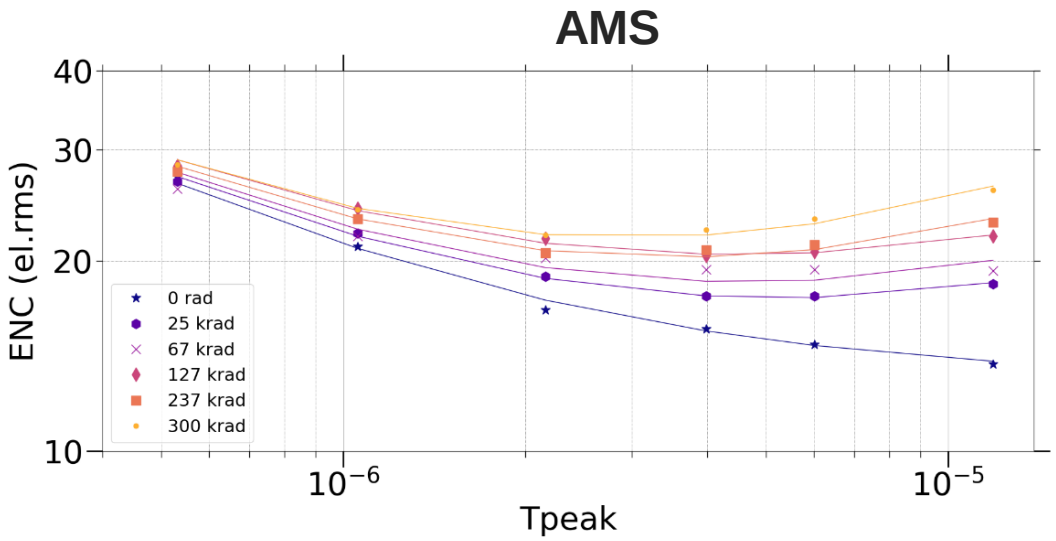


- Conclusion:
  - AMS 0,18 µm have shown better results
  - Both chip have been irradiated up to 1 Mrad and 300 krad (see next)
  - We unfortunately have been forced to stop ams 0.18 (OSRAM has reserved the foundry)

C- Technlogy validation

- Irradiation: With a ^{60}Co source





- XFAB:
  - We followed the previous development to characterize different types of transistor in a chip: ANAQIN