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U.S. DEPARTMENT OF ENERGY

Low-Noise Cryogenic Front-End ASICs for Noble Liquid Detectors

Prashansa Mukim (on behalf of the BNL Cold Electronics Team)

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Contributions and Acknowledgements

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- Grzegorz Deptuch
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BNL Physics Department:

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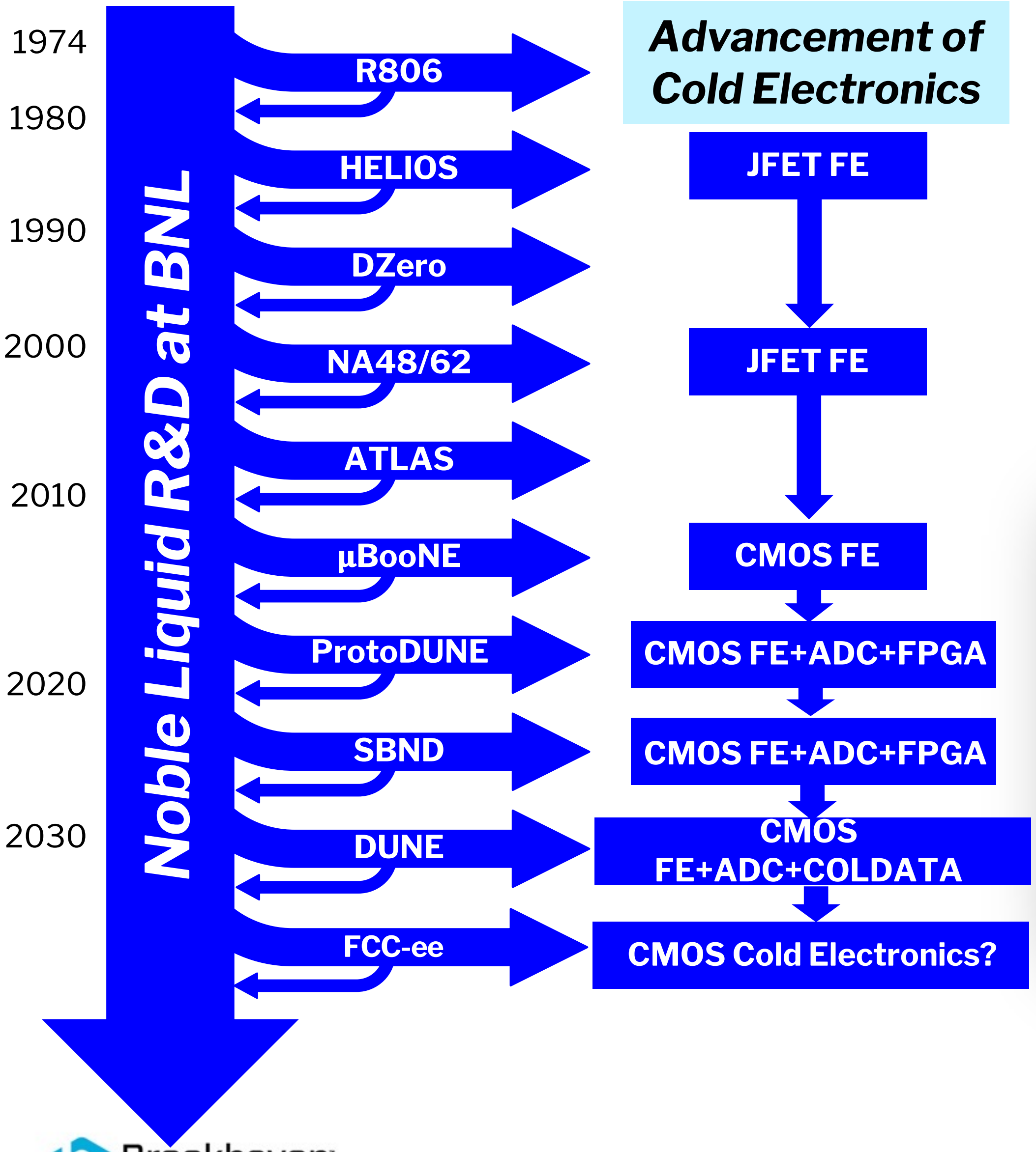
- Shanshan Gao (thanks for all the characterization results shared today!)
- Chao Zhang

Long History of Noble Liquid Detector R&D at BNL



Noble Liquid R&D at BNL

1974

1980

1990

2000

2010

2020

2030

R806

HELIOS

DZero

NA48/62

ATLAS

µBooNE

ProtoDUNE

SBND

DUNE

FCC-ee

Advancement of Cold Electronics

JFET FE

JFET FE

CMOS FE

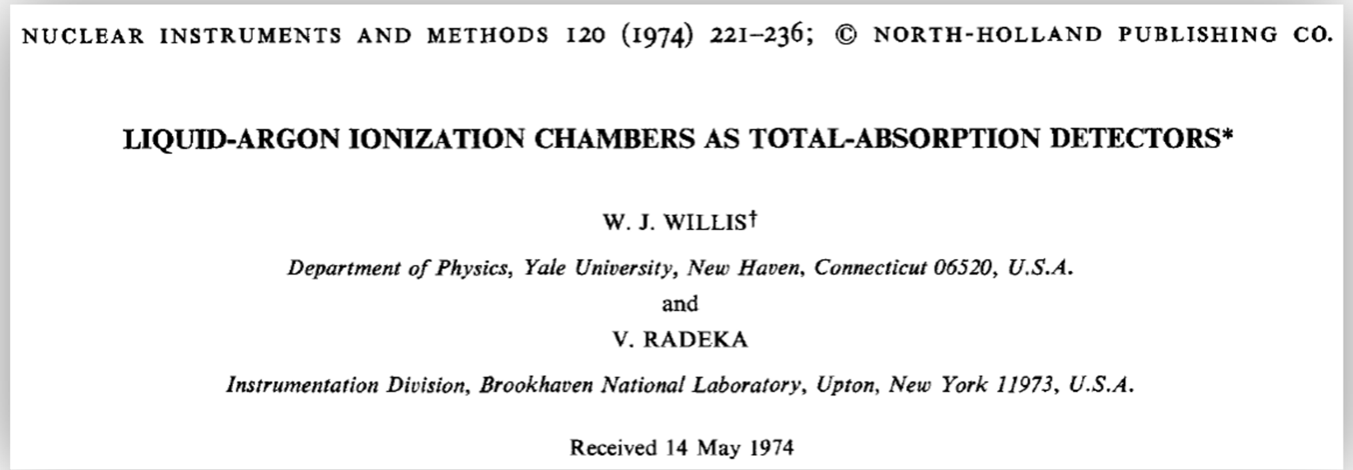
CMOS FE+ADC+FPGA

CMOS FE+ADC+FPGA

CMOS FE+ADC+COLDATA

CMOS Cold Electronics?

- BNL pioneered Liquid Argon based detector technology in 1974
- **Readout electronics** has always been an **integral** part of detector R&D effort for **precision measurement** with noble liquid detectors



NUCLEAR INSTRUMENTS AND METHODS 120 (1974) 221–236; © NORTH-HOLLAND PUBLISHING CO.

LIQUID-ARGON IONIZATION CHAMBERS AS TOTAL-ABSORPTION DETECTORS*

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and

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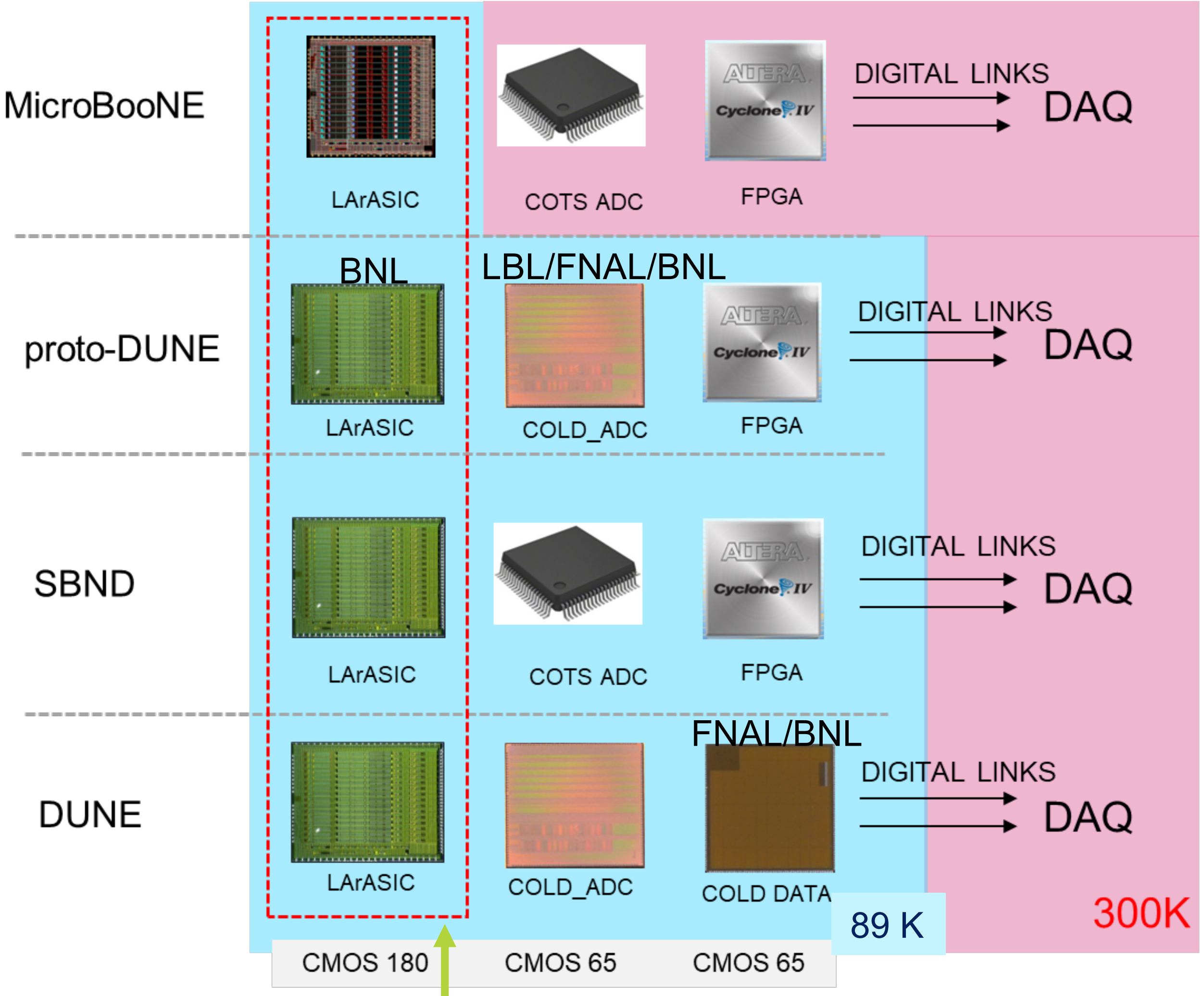
Received 14 May 1974

Status of BNL Cryogenic Front-end ASICs

About a decade of development



Peaking time programmable between 500 ns and 3 µs

3 ASICs vs. 1 ASIC solution:

- Initially two readout options were proposed:
  - 3 ASICs vs. 1 ASIC (idea of building 1 ASIC, combining FE/ADC/transmission brought in 2016 and included as parallel path of development)
- Evolutionary development MicroBooNE→ DUNE led to the 3 ASIC solution that:
  - Helped perfect the FE (through multiple iterations)
  - Allowed debugging (procedure for ADC calibration)
  - Allowed independent optimization of each chip
  - Disallowed analog – digital interfaces

To meet the demands of next generation experiments -> cryogenic front-end ASIC in a newer technology node - 65 nm

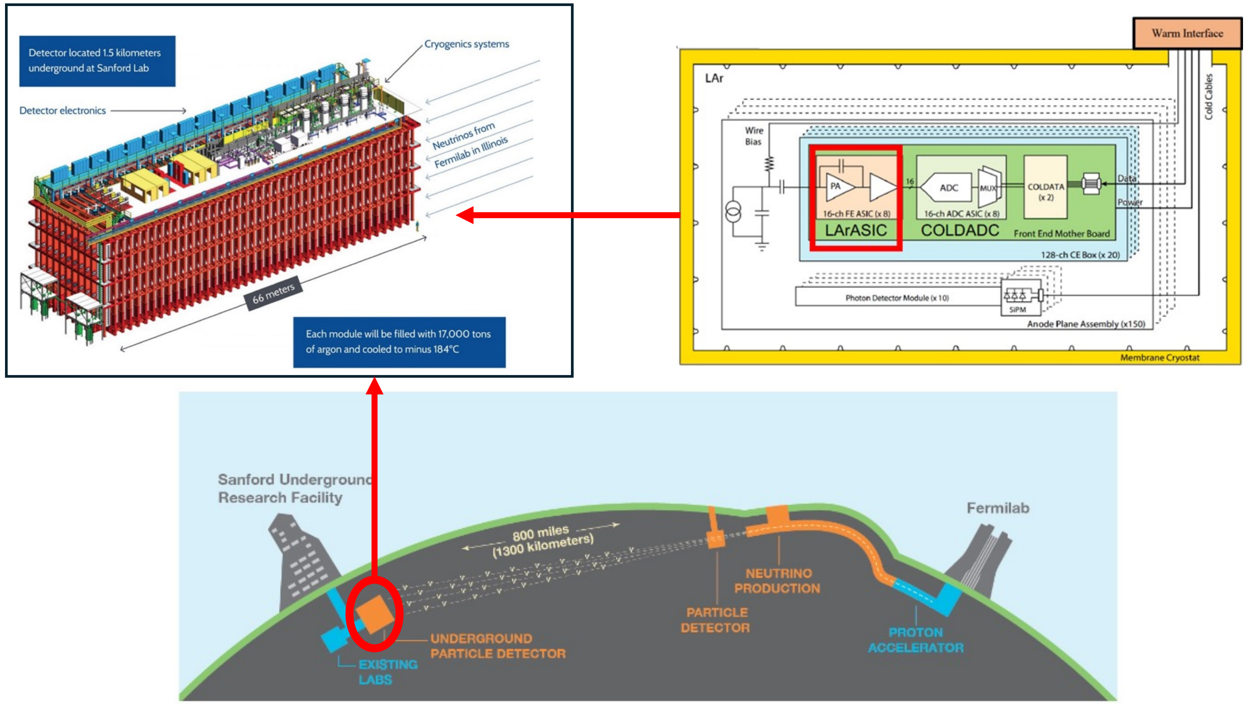
Currently in development: CHARMS250 (CHARge aMplifer + Shaper -> 65 nm cryogenic analog front-end ASIC with 250 ns shortest peaking time)

CHARMS10 with 10 ns shortest peaking time also planned for development

Targets for CHARMS - DUNE

Deep Underground Neutrino Experiment:

- Major scientific experiment for studying neutrino/antineutrino oscillations, detect neutrinos emerging from exploding stars, search for signs of proton decay
- DUNE far detector (FD) located 1.5 km underground in South Dakota will operate with an intense neutrino beam generated at Fermilab
- DUNE Phase-II FDs will utilize four 10kTon liquid argon time projection chambers (TPCs) to detect ionization charge and scintillation light generated when incident neutrinos interact with argon atoms



Usage	Temperature	Detector Capacitance	Shaping Time	Dynamic Range
FD 3/4 charge readout	89 K	150 pF – 200 pF	250 ns – 2 μs	10 bits
FD 3/4 light readout	89 K	few nF (SiPMs)	10 ns – 250 ns	12-13 bits

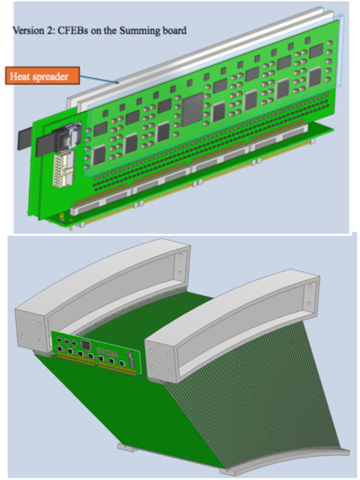
Targets for CHARMS - FCC-ee

Electron-Positron Future Circular Collider:

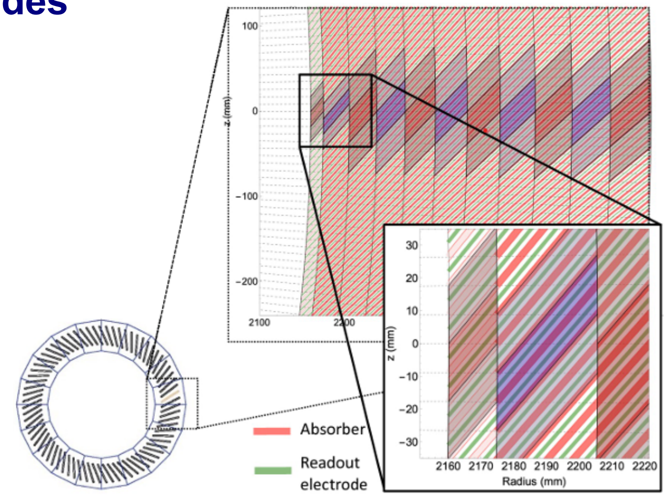
- Proposed to be constructed at CERN to serve as a general precision instrument for exploration of nature at the smallest scales
- Optimized to study with high precision the Z bosons, W pairs, Higgs bosons and top quark pairs
- **ALLEGRO (A Lepton coLlider Experiment with Granular calorimetry Read-Out)**, one of the proposed detectors, features a high granularity noble liquid electromagnetic calorimeter (ECAL) at its core

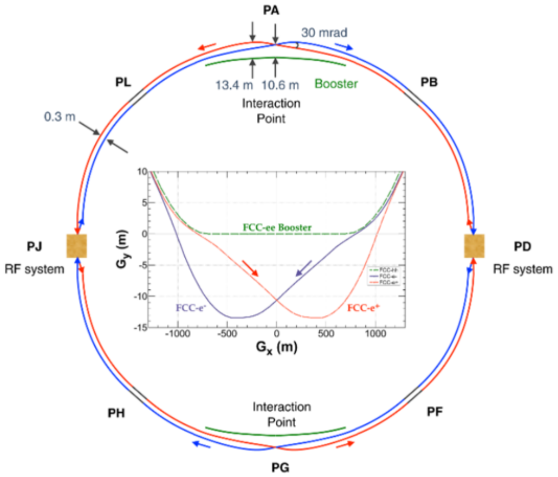
Usage	Temperature	Detector Capacitance	Shaping Time	Dynamic Range
Allegro	89 K	200 pF / 400 pF	200 ns	12 bits (4 fC – 10 pC)

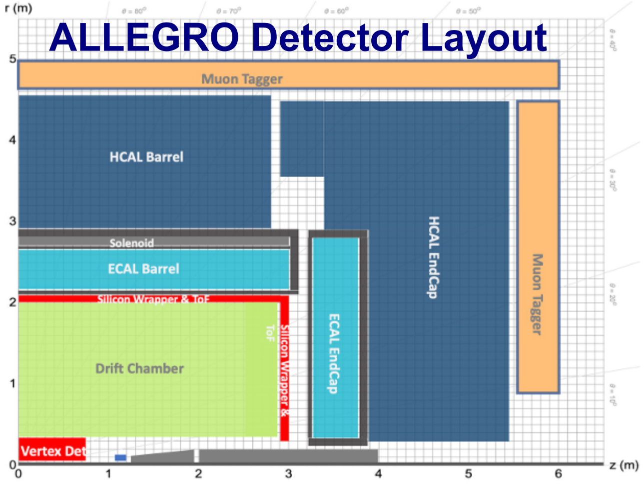
Cold Front-End Boards Integrated on PCB Electrodes



ALLEGRO Ecal Barrel Design







ALLEGRO Detector Layout

CHARMS250V1 specifications

Technology	65 nm CMOS: 1-poly, 9-metal
Supply voltage	1.8 V
Temperature range	77 K – 300 K (optimized for 89 K)
Number of channels	16
Maximum single-ended output swing	1.4 V peak to peak
Gain	4.7 mV/fC, 7.8 mV/fC, 14 mV/fC, 25 mV/fC
Full-scale input charge	300 fC, 180 fC, 100 fC, 56 fC
Baseline selection	200 mV (unipolar, collection mode), 900 mV (bipolar, induction mode)
Adaptive reset current	0.1 nA, 0.5 nA, 1 nA, 2 nA
Peaking time	250 ns, 500 ns, 1 μs, 2 μs
Output coupling	DC, AC
Output drive	Shaper, single-ended buffer, differential buffer
Integrated test capacitor	200 fF
Integrated pulse generator	10-bit DAC based
Configuration control	I^2C based for providing digital assistance (programmable gain, peaking time, baseline, RQI)

R & D ongoing on extending the full-scale input charge range to 10 pC (CHARMS250 V2A and V2B)

CHARMS10 (peaking time range 10-200 ns) also planned for development

- Key features and challenges
  - ***65 nm*** CMOS with ***thick oxide*** → To limit gate leakage current and ***parallel noise contribution***
  - ***Low*** power consumption (6-11 mW per channel) → support detector electrodes with ***fine segmentations***
  - ***Cryogenic*** operation with ***long lifetime of electronics*** → achieve optimum ***SNR***

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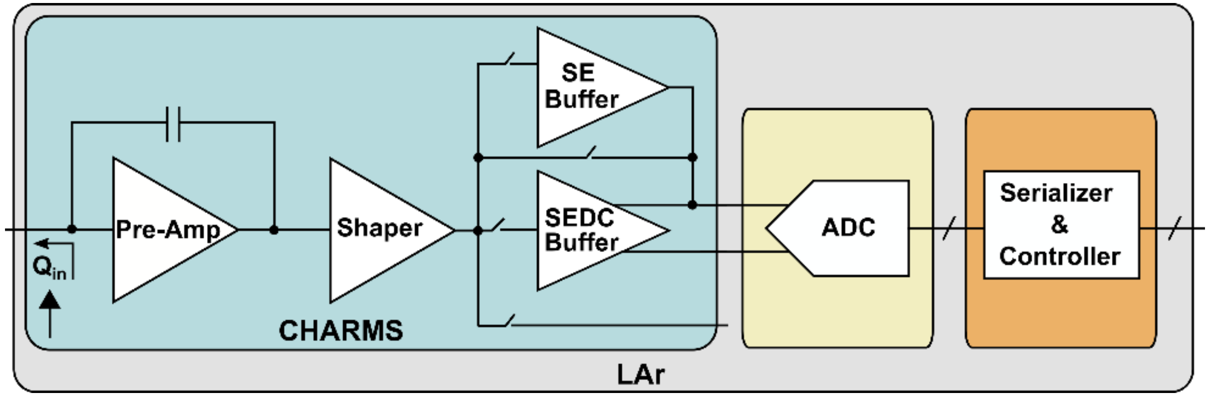
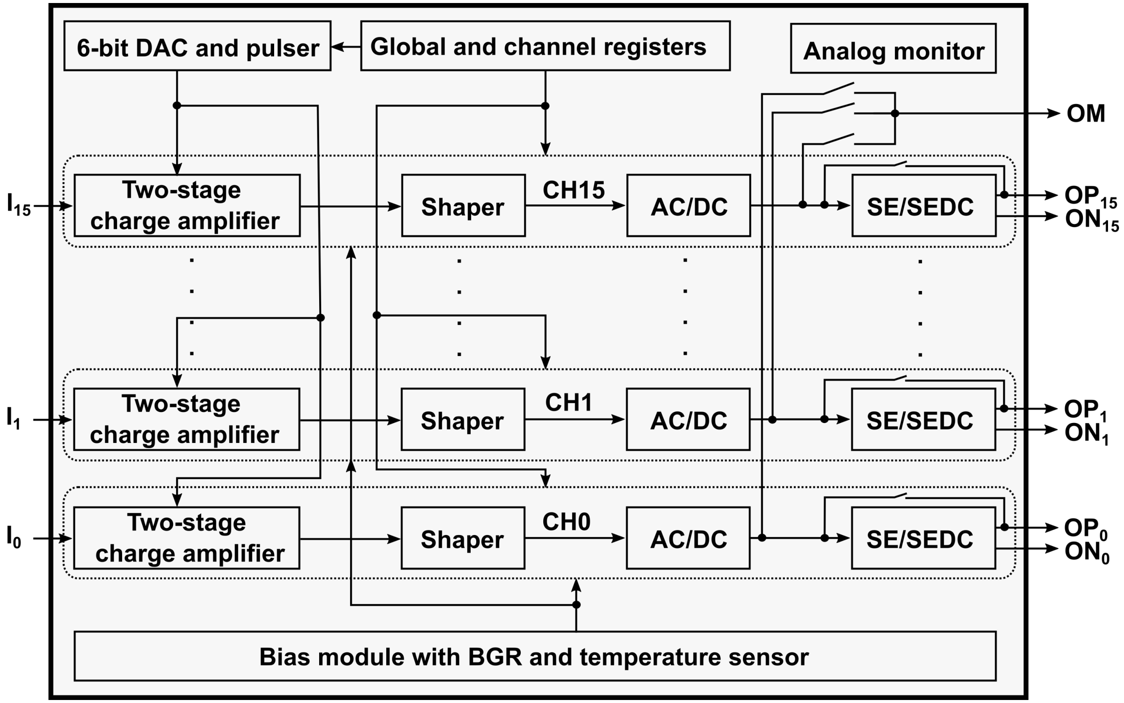
CHARMS250V1 Architecture and functionality

3-ASIC solution

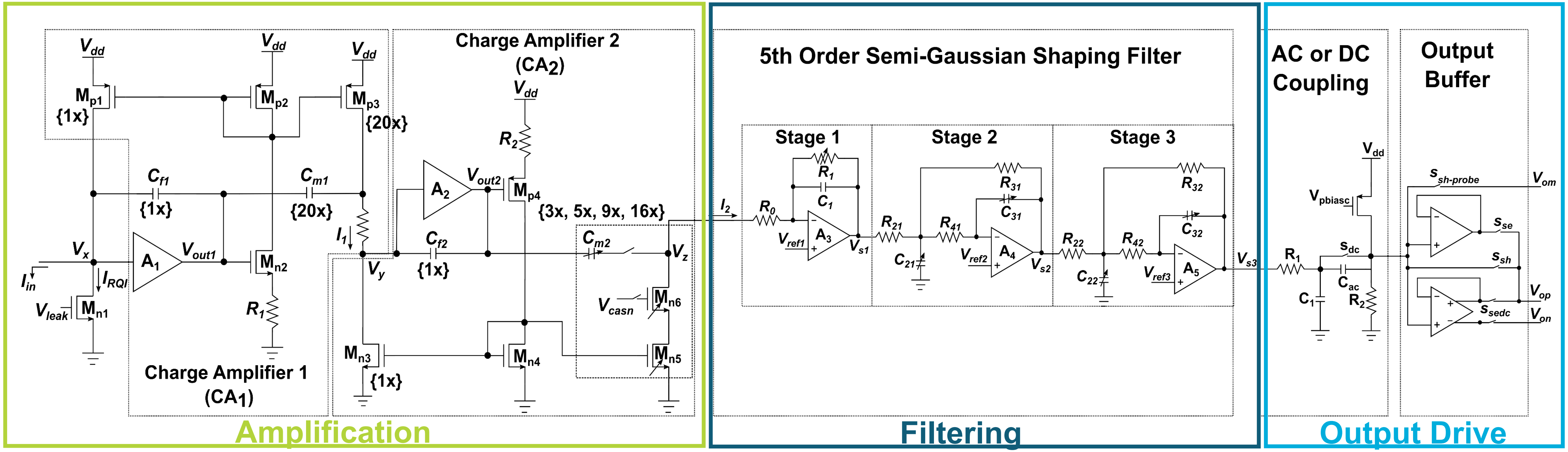


CHARMS250 Top-level block diagram

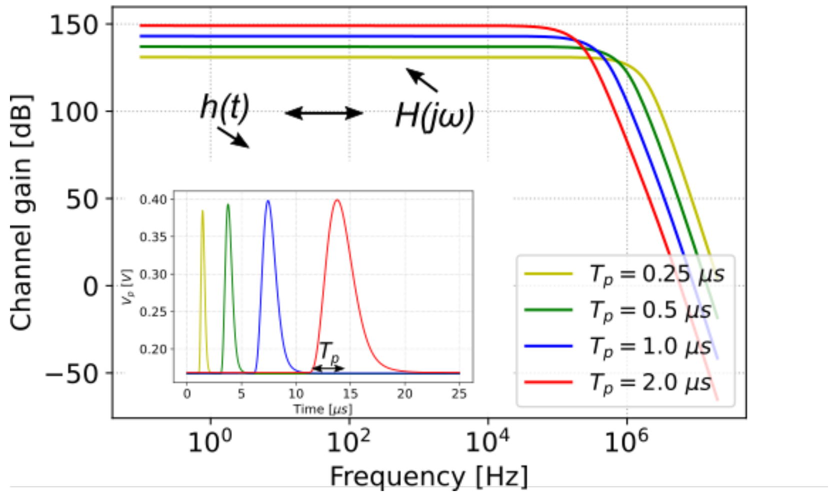


Front-end ASIC (CHARMS250) acts as an anti-aliasing filter

CHARMS250 Analog Channel Schematic and Impulse Response



Impulse Response ->



Peaking time (T_p)	Cut-of frequency (f_{3dB})	Sampling frequency ($f_s = 2/T_p$)	Gain change at f_s
0.25 µs	820 KHz	8 MHz	-79 dB
0.5 µs	411 KHz	4 MHz	-71 dB
1.0 µs	205 KHz	2 MHz	-68 dB
2.0 µs	102 KHz	1 MHz	-66 dB

Noise minimization strategy

$$ENC^2 = (C_d + C_{in})^2 \left(A_w v_n^2 \frac{1}{T_p} + A_f K_f \right) + A_p i_n^2 T_p$$

(Sum of white series noise, 1/f series noise and parallel noise components)

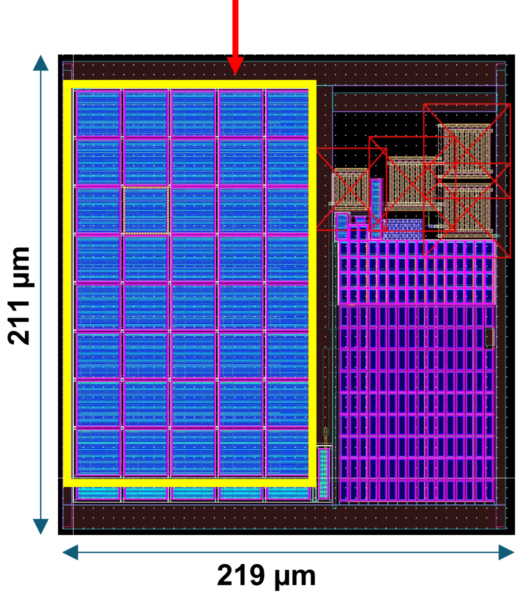
$$ENC_f^2 = K_f \frac{(C_d + C_g)^2}{C_g} N_f \Rightarrow C_g = C_d$$

$$ENC_w^2 = 4k_B T n \gamma \alpha_w \frac{(C_d + C_g)^2}{g_m(C_g)} N_f \Rightarrow C_g = \frac{1}{3} C_d$$

Input stage transistor sized to have C_g ~ 40 pF, optimal choice for minimizing noise with C_{det} ~ 150 pF with given power budget

	Minimum allowable transistor length	Input transistor length	Input transistor width
180 nm (LArASIC)	180 nm	270 nm	20 mm
65 nm (CHARMS250)	280 nm	400 nm	24 mm

Input transistor implemented with 30 copies of transistors of width of 20 µm and 40 fingers

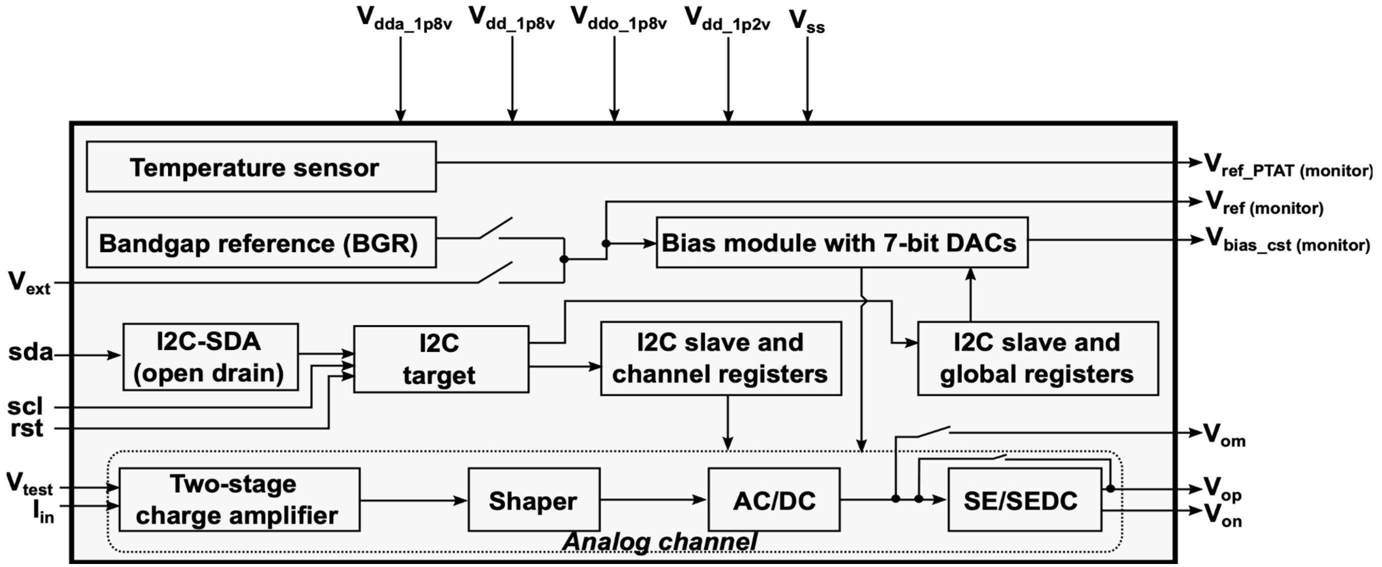


- **Input stage transistors for A_1 implemented using thick oxide (2.5 V) devices in 65 nm for CHARMS to limit leakage current and associated parallel noise**
- **Thin oxide device of the same dimensions has a gate leakage current of ≈ 20 nA, contributing almost 200 electrons to the ENC for 1 µs peaking time and triangular weighting function!**

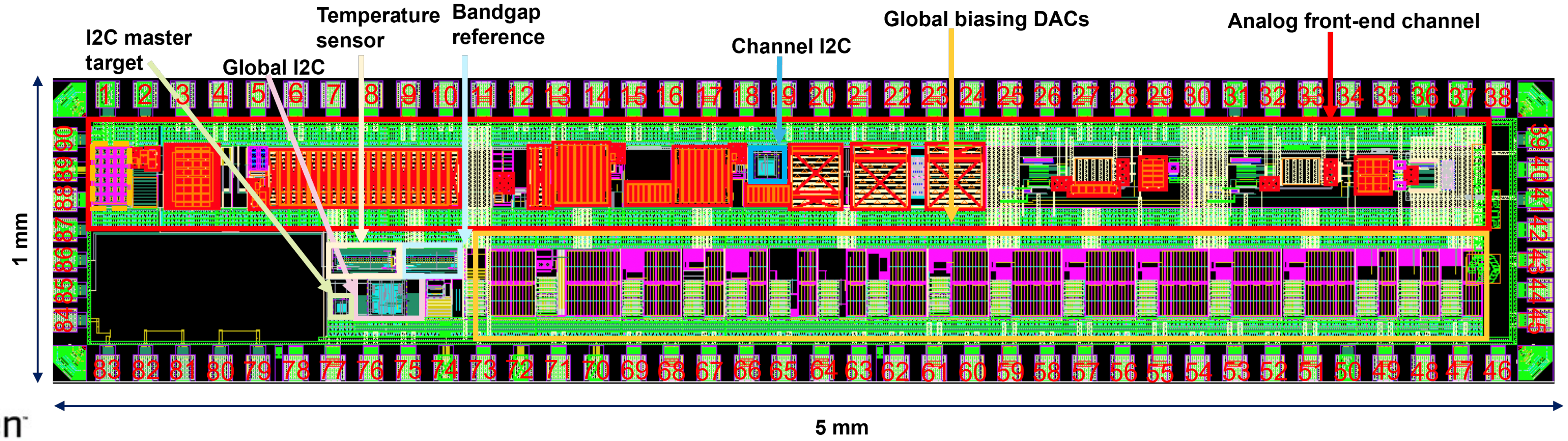
Ref: [1] Angelo Rivetti, Front-End Electronics for Radiation Sensors
[2] Veljko Radeka, Signal Processing for Particle Detectors

Single Channel Prototype: CHARMS250V1

CHARMS250V1 prototype block diagram

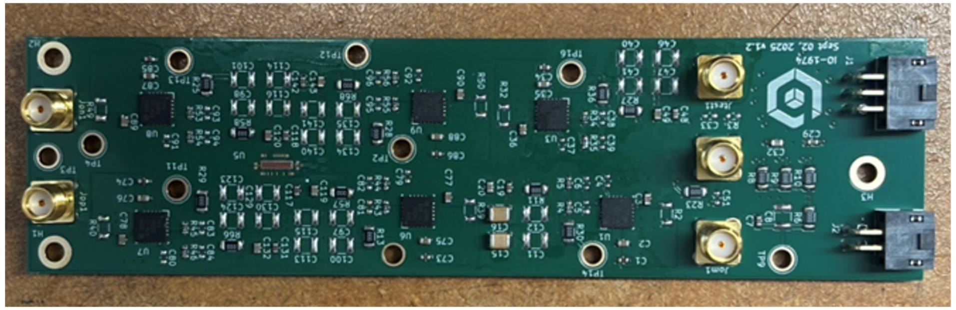


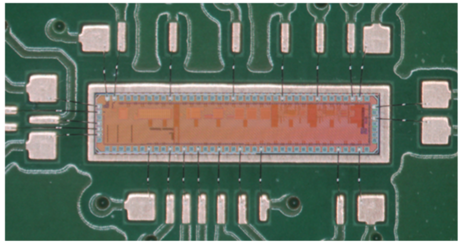
CHARMS250V1 prototype layout

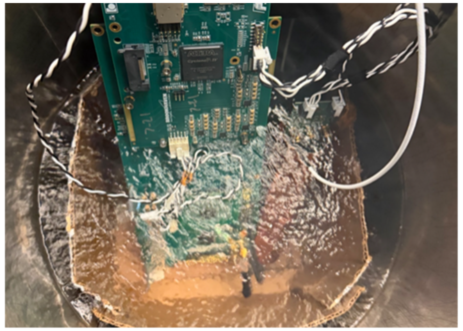


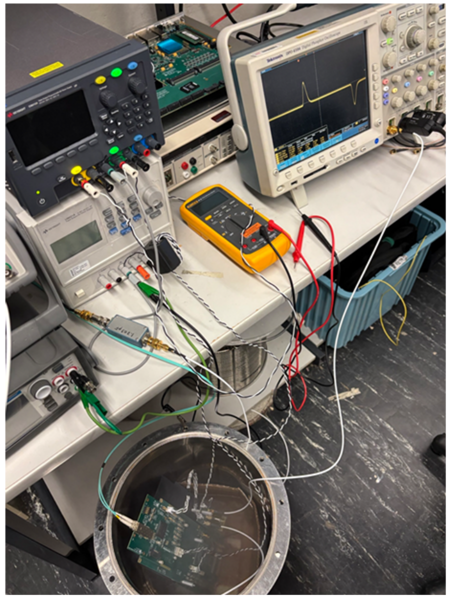
Submitted for fabrication in June 2025; received in October 2025.

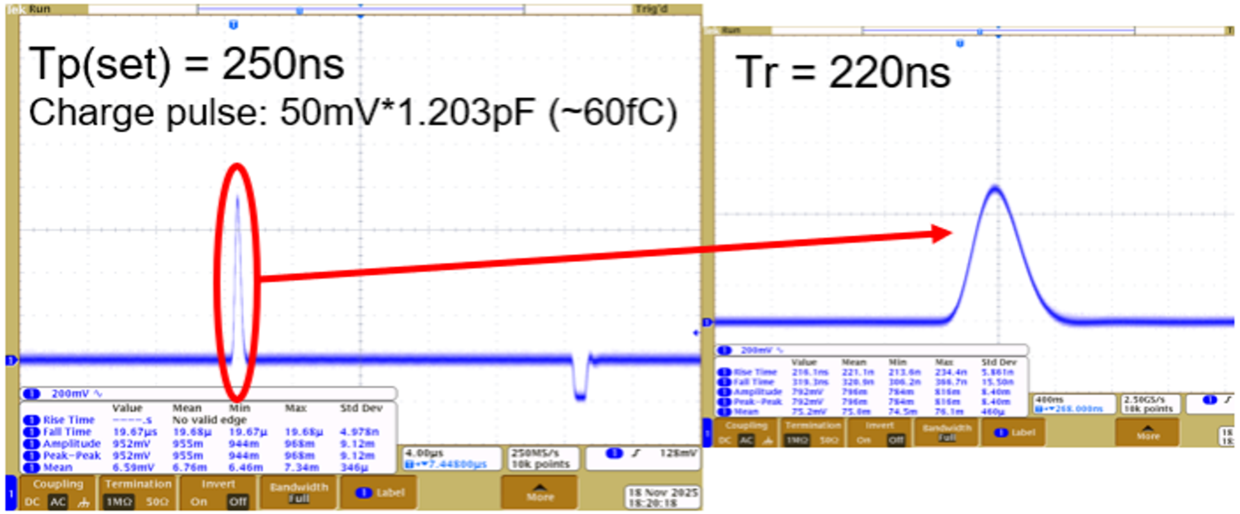
CHARMS250V1 Characterization Results











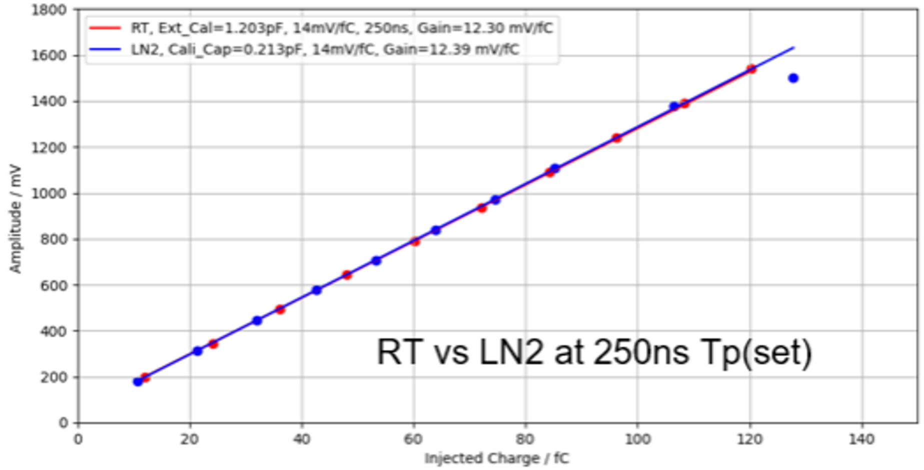
Tp(set) = 250ns

Charge pulse: 50mV*1.203pF (~60fC)

Tr = 220ns

	Value	Mean	Min	Max	Std Dev
Rise Time	-----.s	No valid edge			
Fall Time	19.67µs	19.68µ	19.67µ	19.68µ	4.978n
Amplitude	952mV	955m	944m	968m	9.12m
Peak-Peak	952mV	955m	944m	968m	9.12m
Mean	6.59mV	6.76m	6.46m	7.34m	346µ

	Value	Mean	Min	Max	Std Dev
Rise Time	216.1ns	221.1n	213.6n	234.4n	5.861n
Fall Time	319.3ns	320.9n	306.2n	366.7n	15.50n
Amplitude	792mV	796m	784m	816m	8.40m
Peak-Peak	792mV	796m	784m	816m	8.40m
Mean	75.2mV	75.0m	74.5m	76.1m	460µ



RT vs LN2 at 250ns Tp(set)

No significant gain change at LN2 compared to RT

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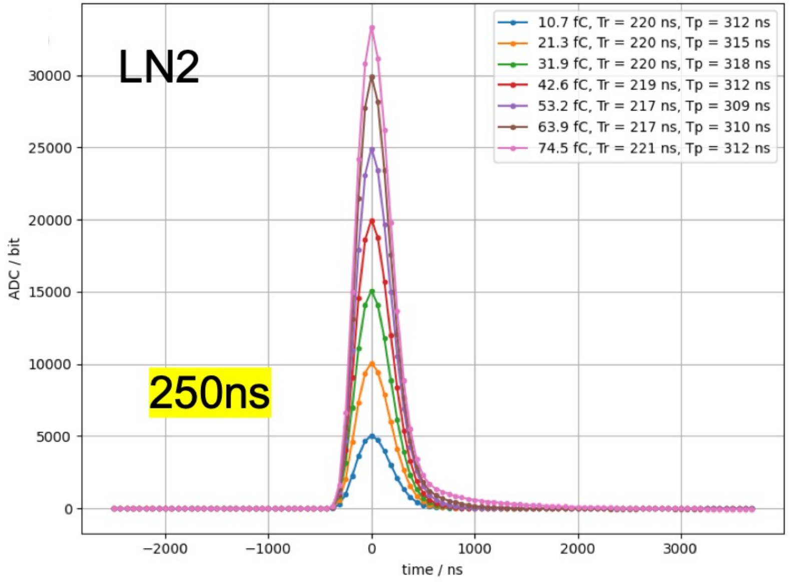
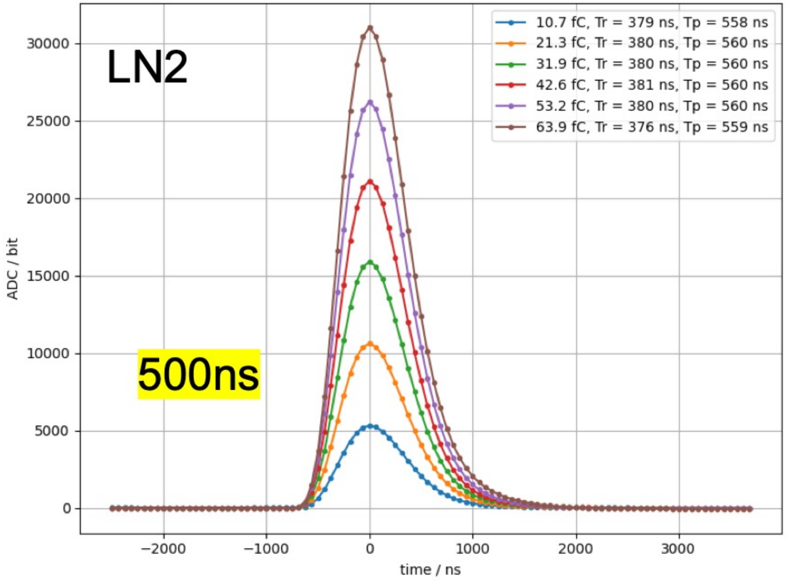
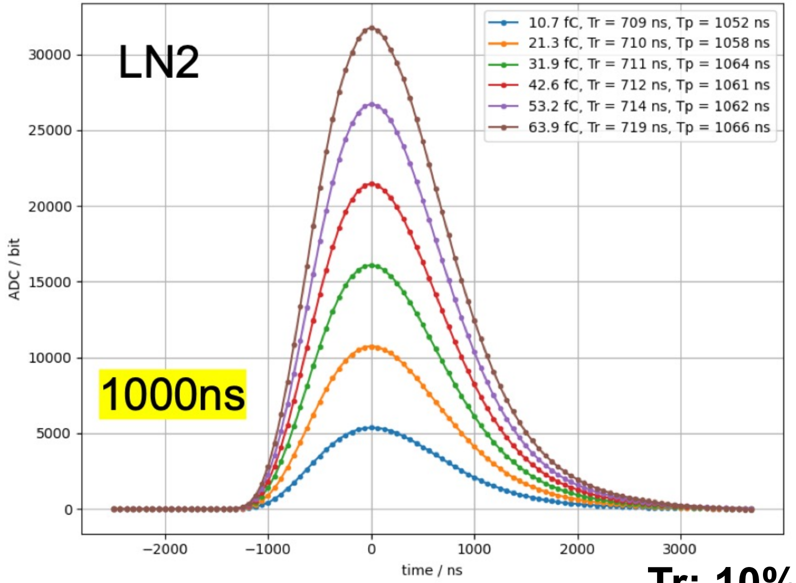
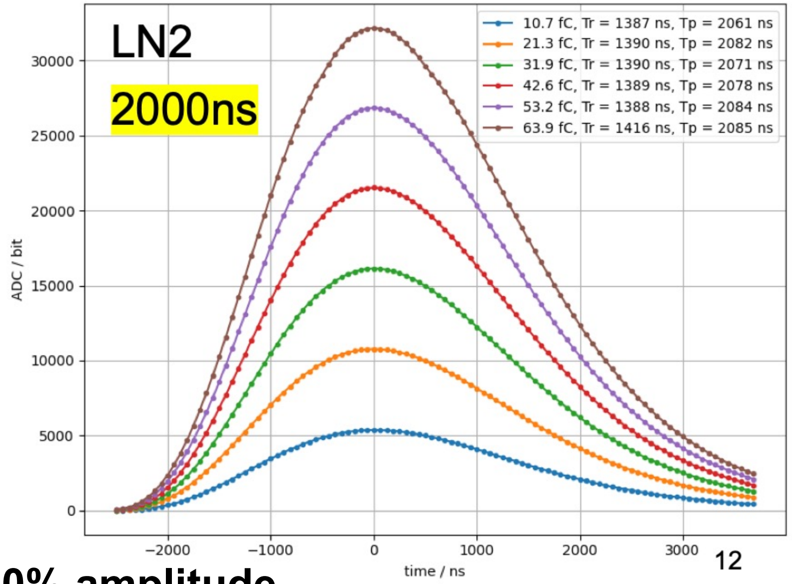
Detailed characterization results summarized in Shanshan's talk

Measured peaking times at LN2





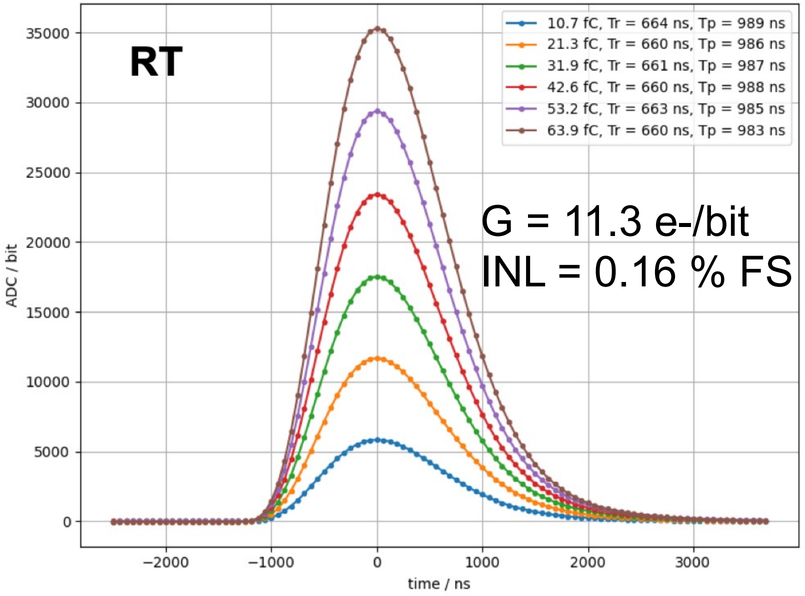




Tr: 10%-90% amplitude
Tp: 5% to peak amplitude

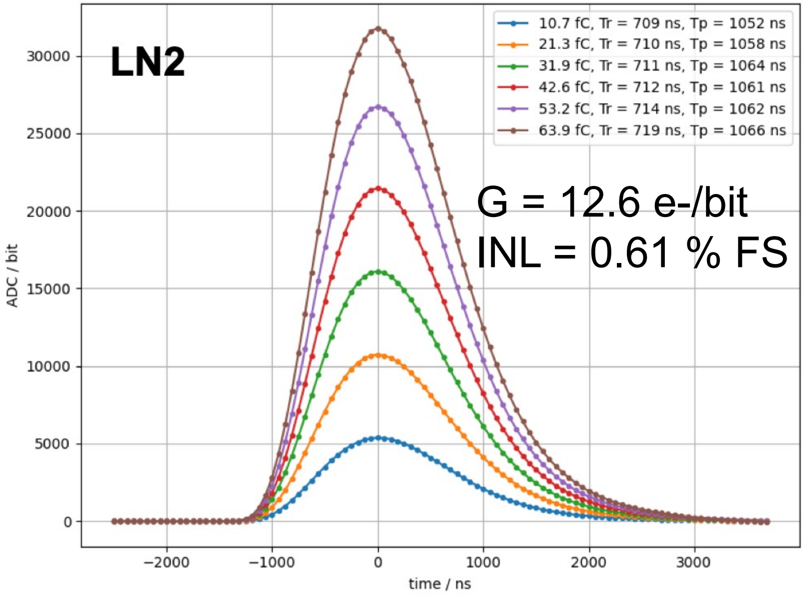
Pulse response comparison at RT and LN2

Gain: 14 mV/fC
Tp: 1 µs



RT

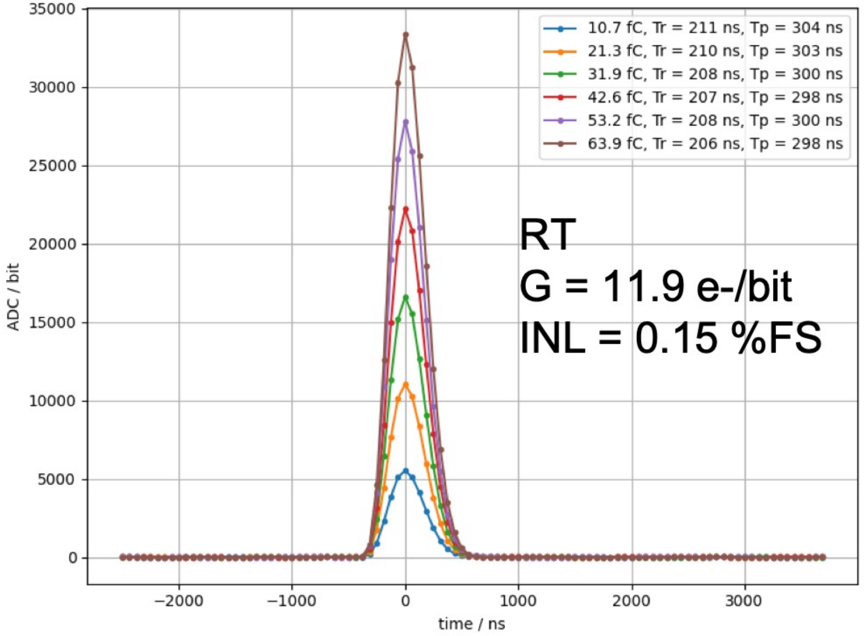
G = 11.3 e-/bit
INL = 0.16 % FS



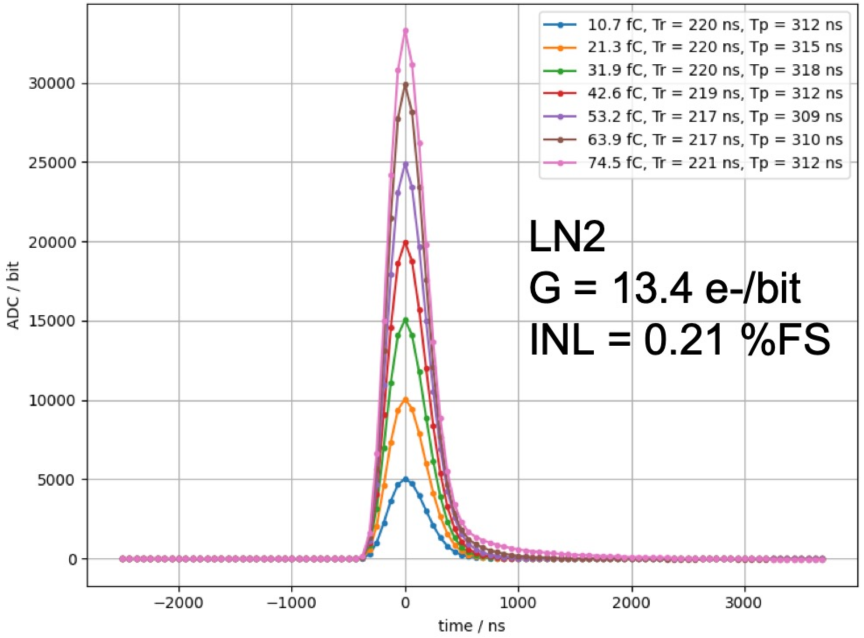
LN2

G = 12.6 e-/bit
INL = 0.61 % FS

Gain: 14 mV/fC
Tp: 250 ns

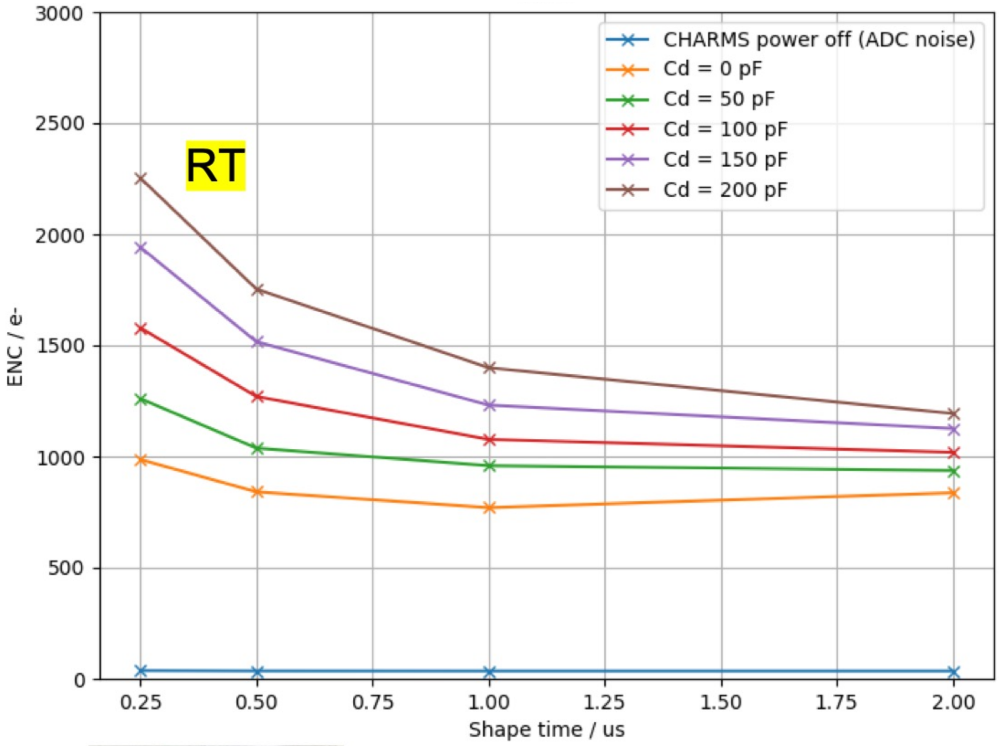


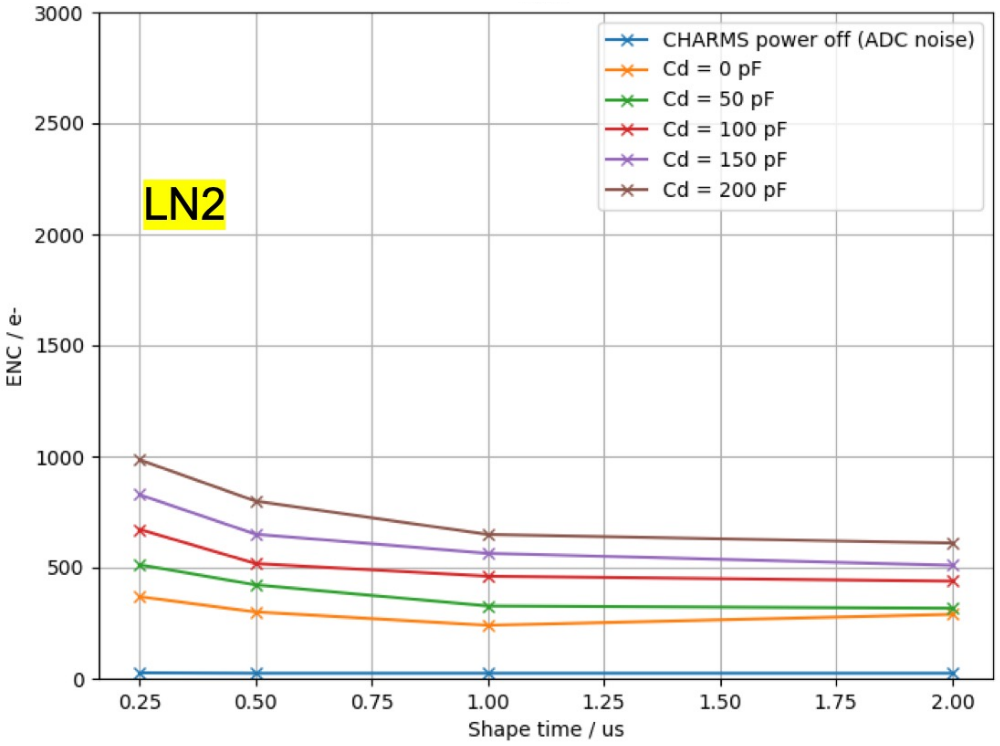
RT
G = 11.9 e-/bit
INL = 0.15 %FS

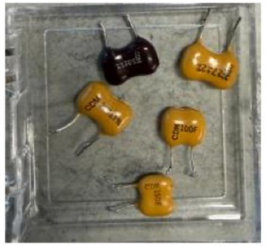


LN2
G = 13.4 e-/bit
INL = 0.21 %FS

Measured ENC at RT and LN2 (Gain: 14 mV/fC)







Mica caps as Cd

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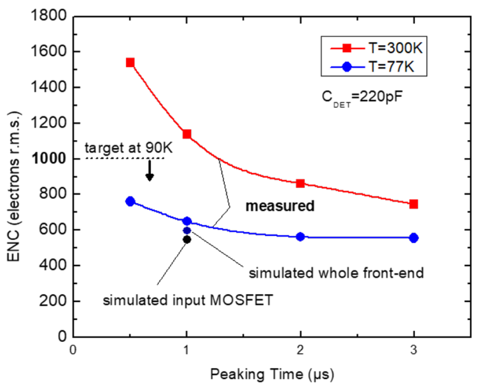
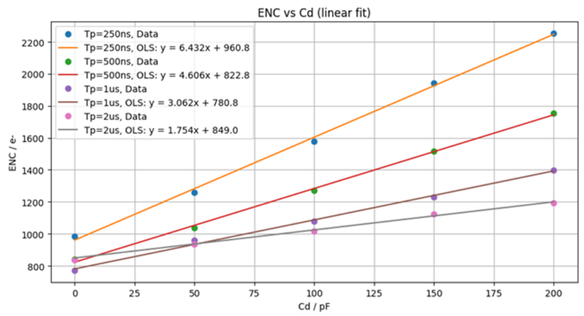
RT	14mV/fC			
Cd	250ns	500ns	1us	2us
ADC	36	35	34	34
0	986	841	770	836
50	1260	1037	958	936
100	1579	1270	1077	1019
150	1942	1516	1231	1125
200	2253	1753	1399	1193

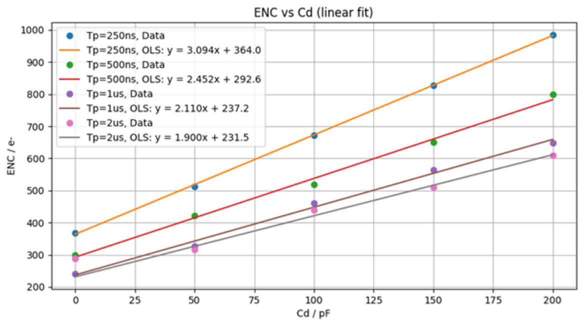
LN2	14mV/fC			
Cd	250ns	500ns	1us	2us
ADC	26	24	24	24
0	369	300	240	289
50	513	422	327	317
100	672	518	461	439
150	828	650	564	510
200	985	799	649	610

CHARMS250V1 Noise Projection and Test Summary



- Noise (ENC) in FE ASIC vs temperature and peaking time of the anti-aliasing filter
  - **White series noise** which is dominant at short peaking times **decreases** the most with temperature.
  - The remaining noise is dominated by 1/f noise, which is independent of the peaking time.





Peaking Time	**250ns**	500ns	1000ns	2000ns
RT	**6.4**	4.6	3.1	1.8
LN2	**3.1**	2.5	2.1	1.9

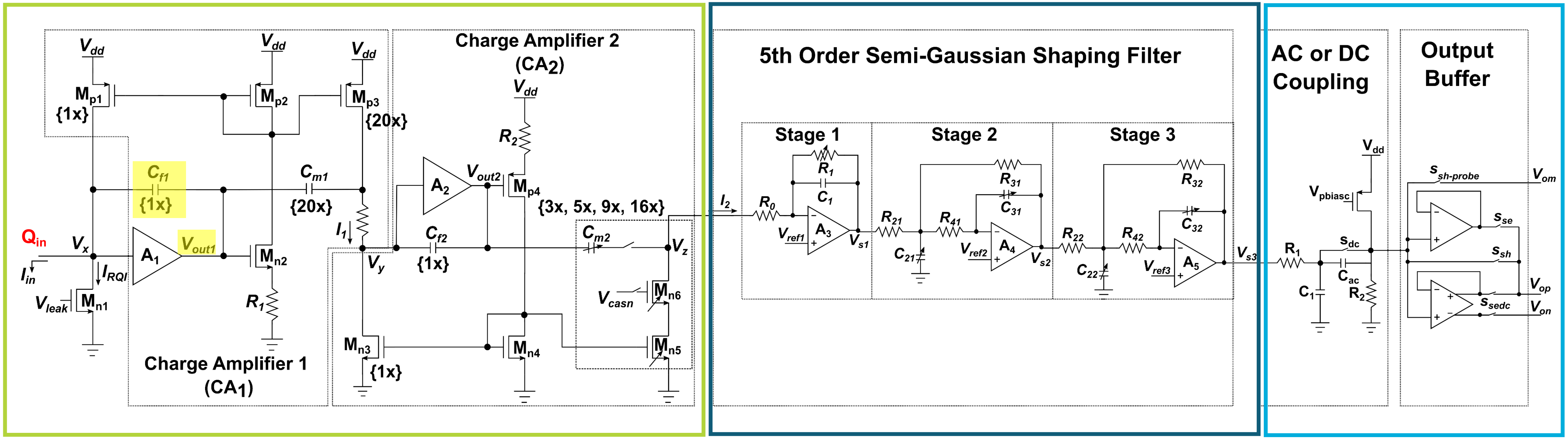
Noise Projection (e-/pF)

CHARMS250V1 meets most design expectations:

- **< 10 mW** per channel: preamplifier + shaper ~ 5.5 mW (from simulation) + other blocks (biasing, BGR, DAC etc.)
- Works at **77K** (-196 °C) – 300K
- **Excellent noise performance** at cold
- **Good peaking time and linearity** (some non-linearity in response seen for large charges at LN2; currently being debugged and understood)

Extending the dynamic range of CHARMS250 to 10 pC (CHARMS250V2A and CHARMS250V2B)

Updates needed for extending the dynamic range to 10 pC for ALLEGRO



Amplification

Filtering

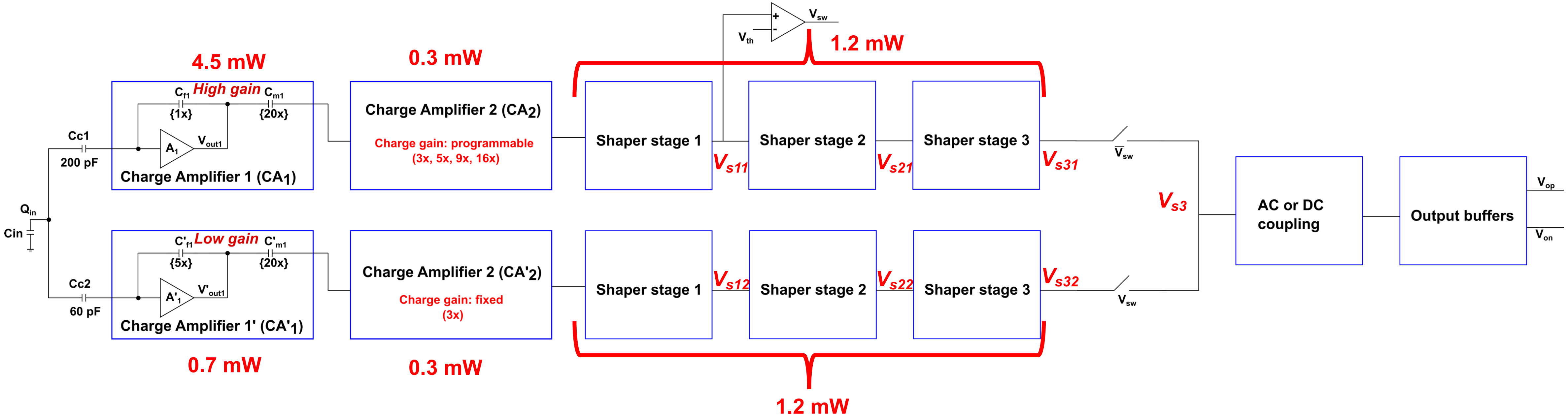
Output drive

- Current front-end designed to process charges up to 300 fC, CA_1 charge gain = 20, minimum CA_2 charge gain = 3
- C_{f1} ~ 1 pF, C_{f2} ~ 8 pF, So for 300 fC Q_{in}, V_{out1} swing is ~ (300 fC/1pF) = 300 mV and V_{out2} swing is ~ (300 x 20 fC/8 pF) = 750 mV
- For larger values of Q_{in}, V_{out1} starts to saturate → **We need to increase C_{f1} (by 30x for ~30x increase in input charge range)**
- **By simply increasing Cf1, front-end saturation up to 10 pC can be prevented, but noise increases by 10x or more**

CHARMS250V2A: Dual parallel gain paths

CHARMS250V2A (Dual parallel gain paths) architecture

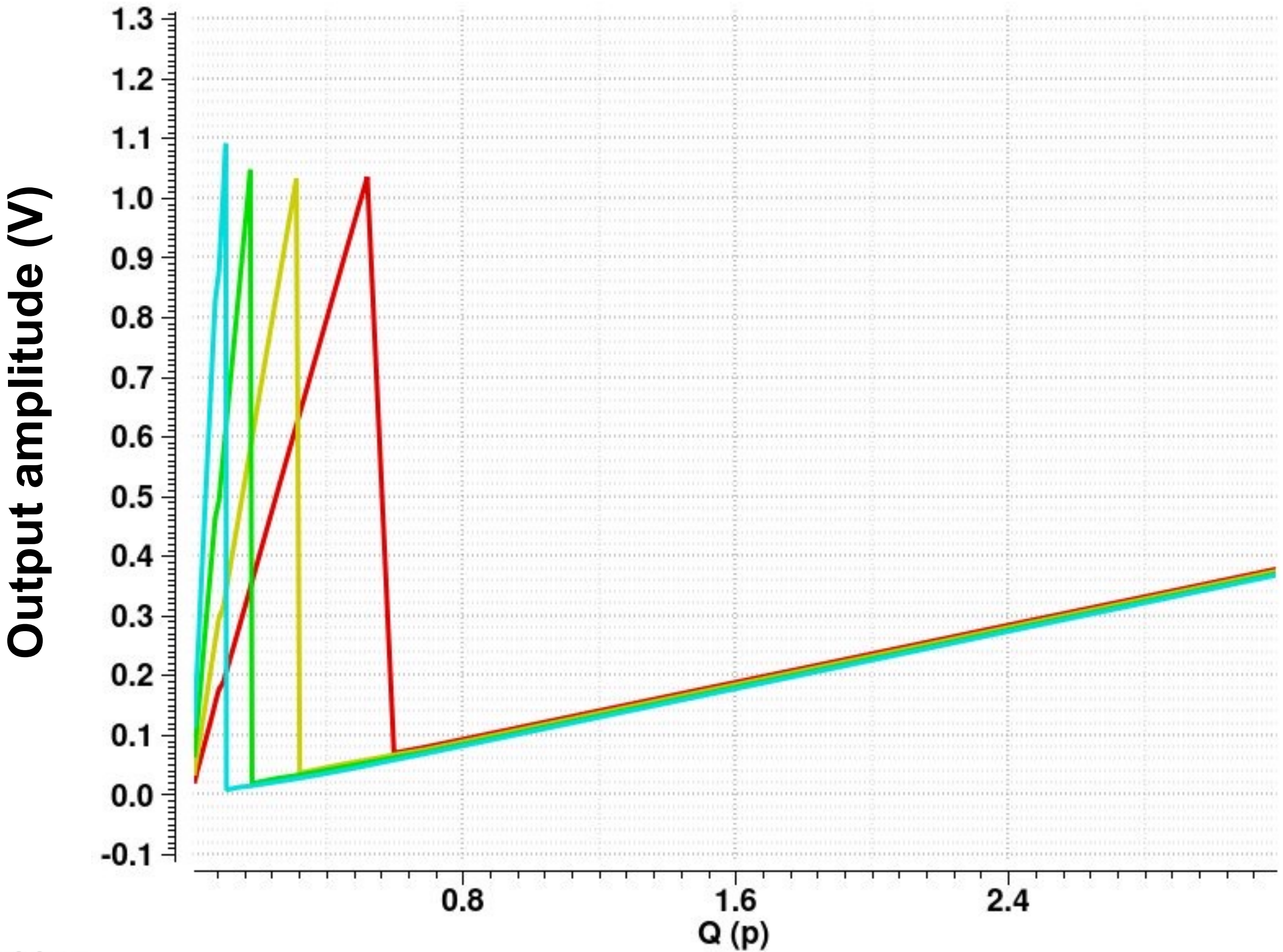
- **Two parallel gain and shaping filter paths, combined ac-dc coupling and output buffer**



- **High gain path optimized for low noise; low gain path (note lower power consumption) output has higher noise but allows high dynamic range**
- With Cin = 200 pF, Cc1 = 200 pF, Cc2 = 60 pF, charge coupled to the two paths:
  - Q1 = Qin* Cc1/(Cin + Cc1 + Cc2) = 0.43*Qin, Q2 = Qin * Cc2/(Cin + Cc1 + Cc2) = 0.13*Qin
- Possible to optimize noise further by tuning charge split ratio and CA1 gain

CHARMS250V2A transfer characteristics

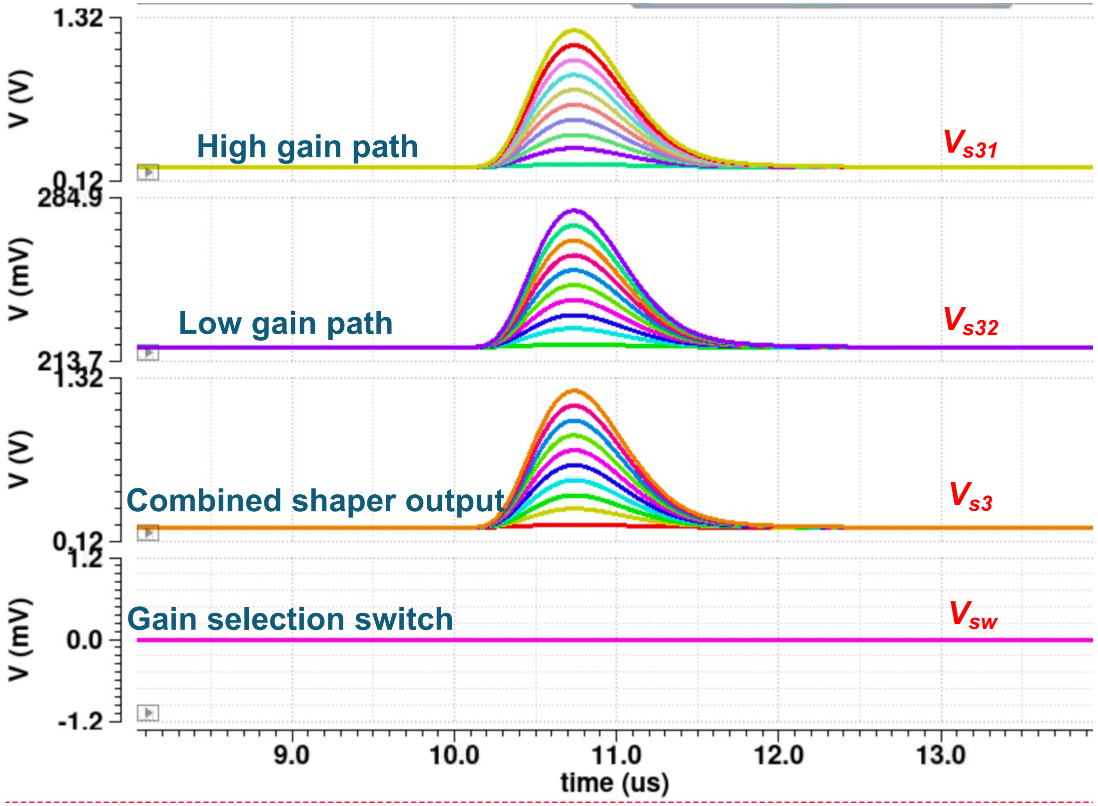
Input charge vs. output amplitude



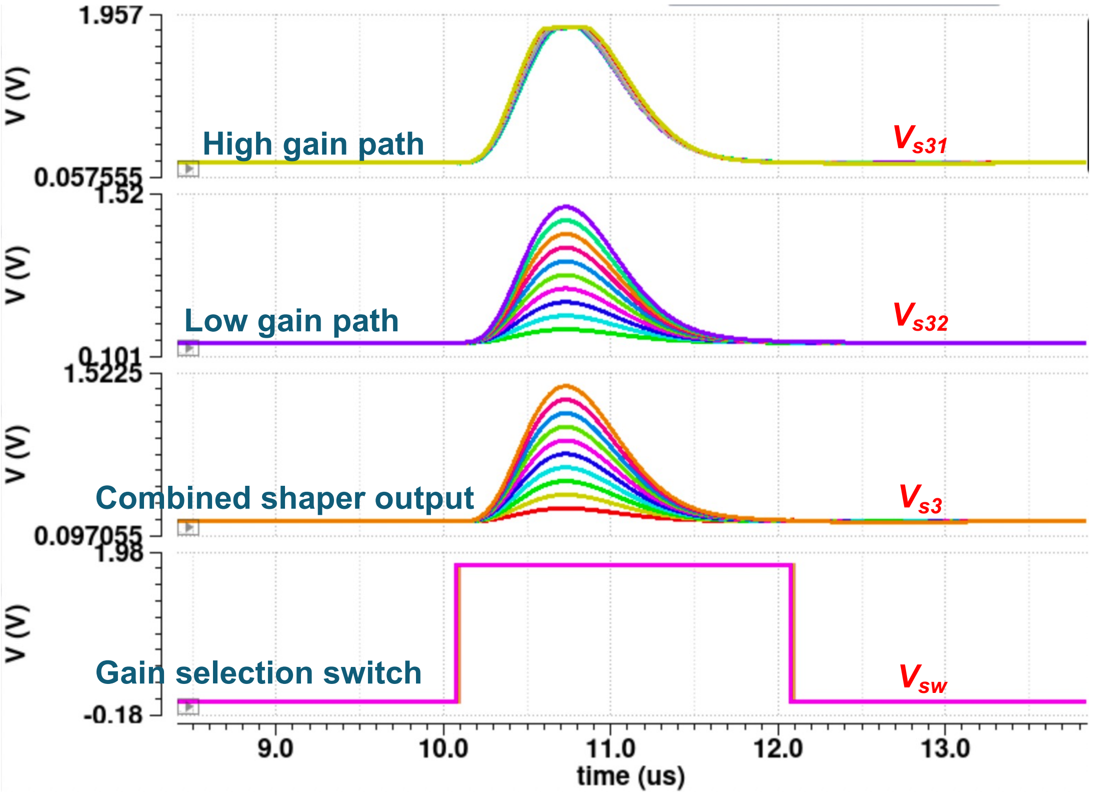
Gain setting index	Gain value	Charge range
1	11.3 mV/fC	125 fC
2	6.3 mV/fC	220 fC
3	3.3 mV/fC	430 fC
4	2 mV/fC	700 fC
5	0.12 mV/fC	11.6 pC

Transient response for CHARMS250V2A

Input charges from 10 fC – 500 fC, gain index: 4

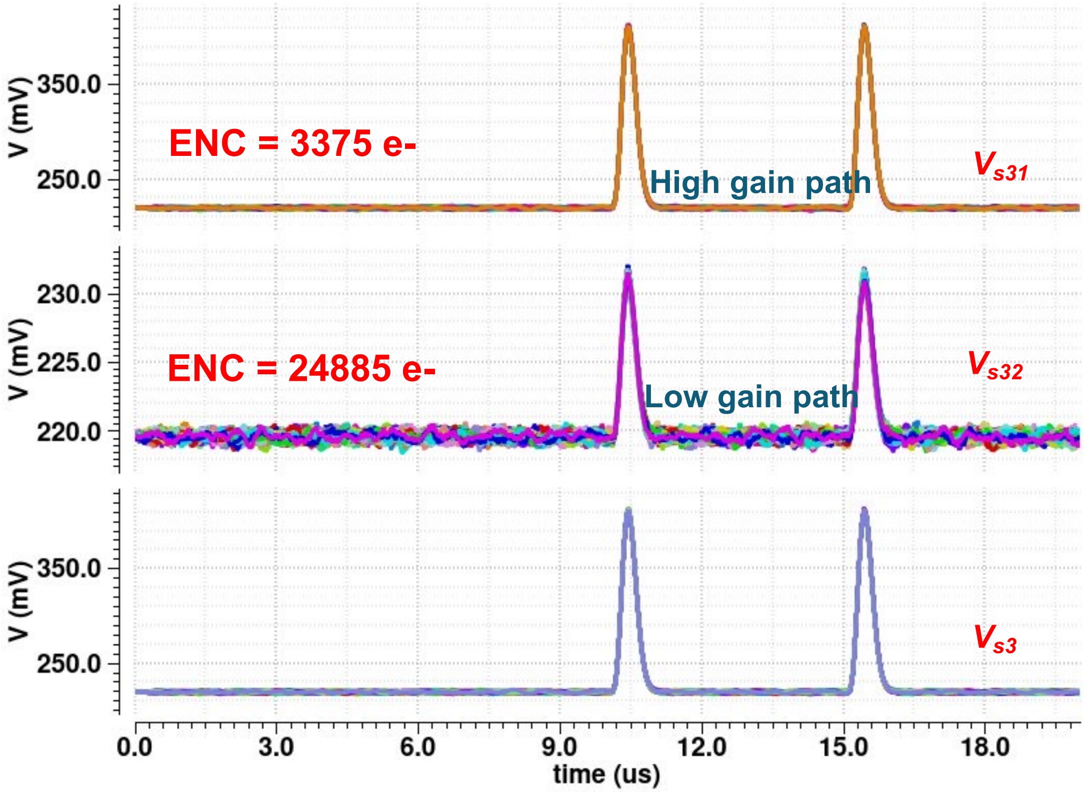


Input charges from 1 pC – 10 pC, gain index: 5

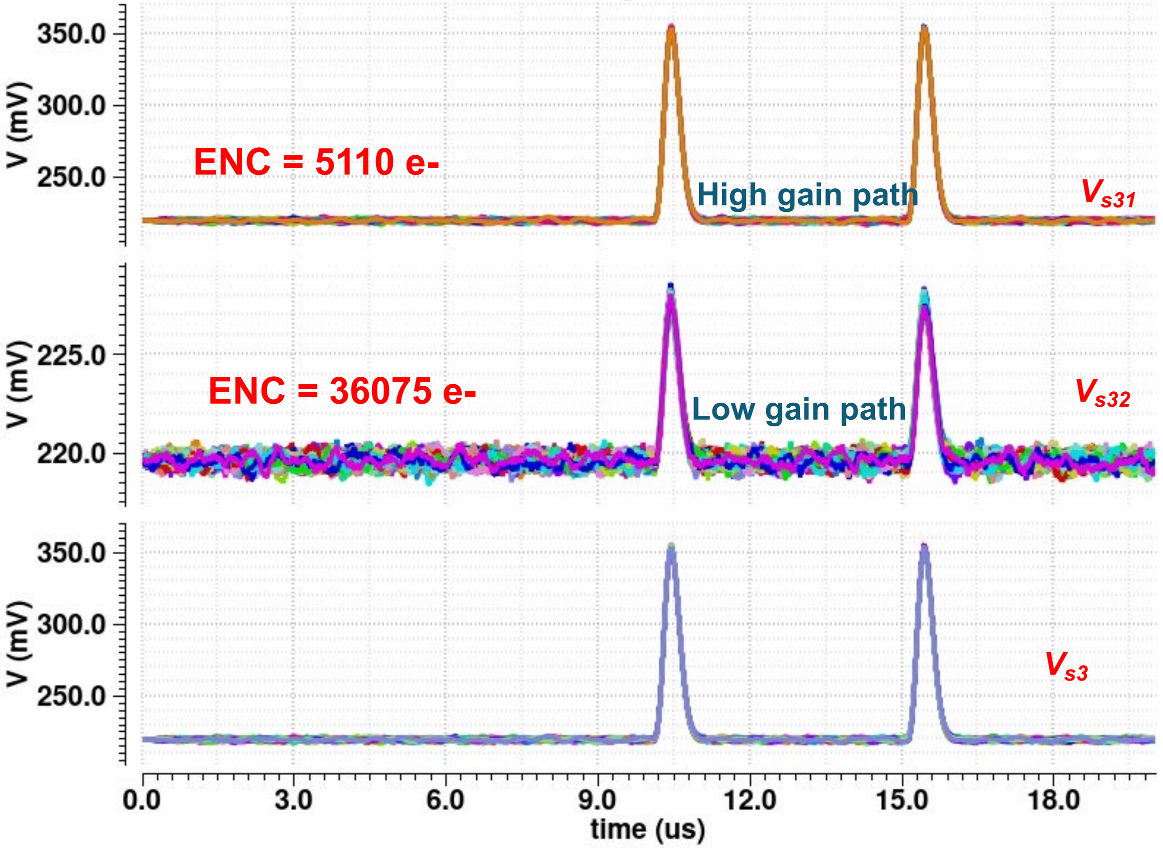


Noise for CHARMS250V2A, peaking time = 250 ns (RT)

C_{in} = 200 pF, Q_{in} = 100 fC



C_{in} = 400 pF, Q_{in} = 100 fC



Corresponding SNR for:

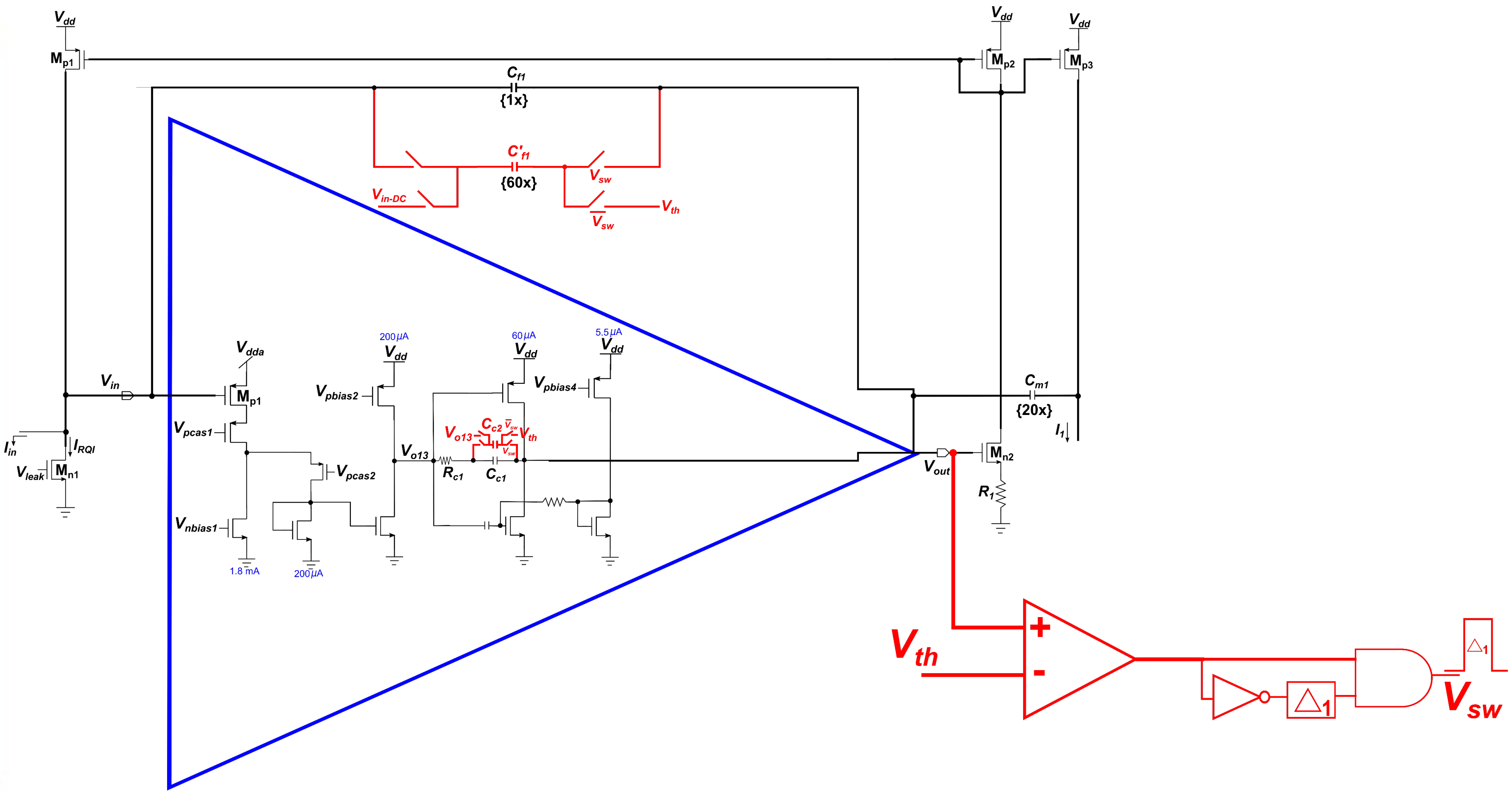
- MIP (4 fC): ~ 8
- Gain transition point (700 fC): ~176

Corresponding SNR for:

- MIP (4 fC): ~ 5
- Gain transition point (700 fC): ~121

CHARMS250V2B: Front-end with dynamic feedback capacitance switching

Dynamic feedback capacitance switching in CA1 for CHARMS250V2B

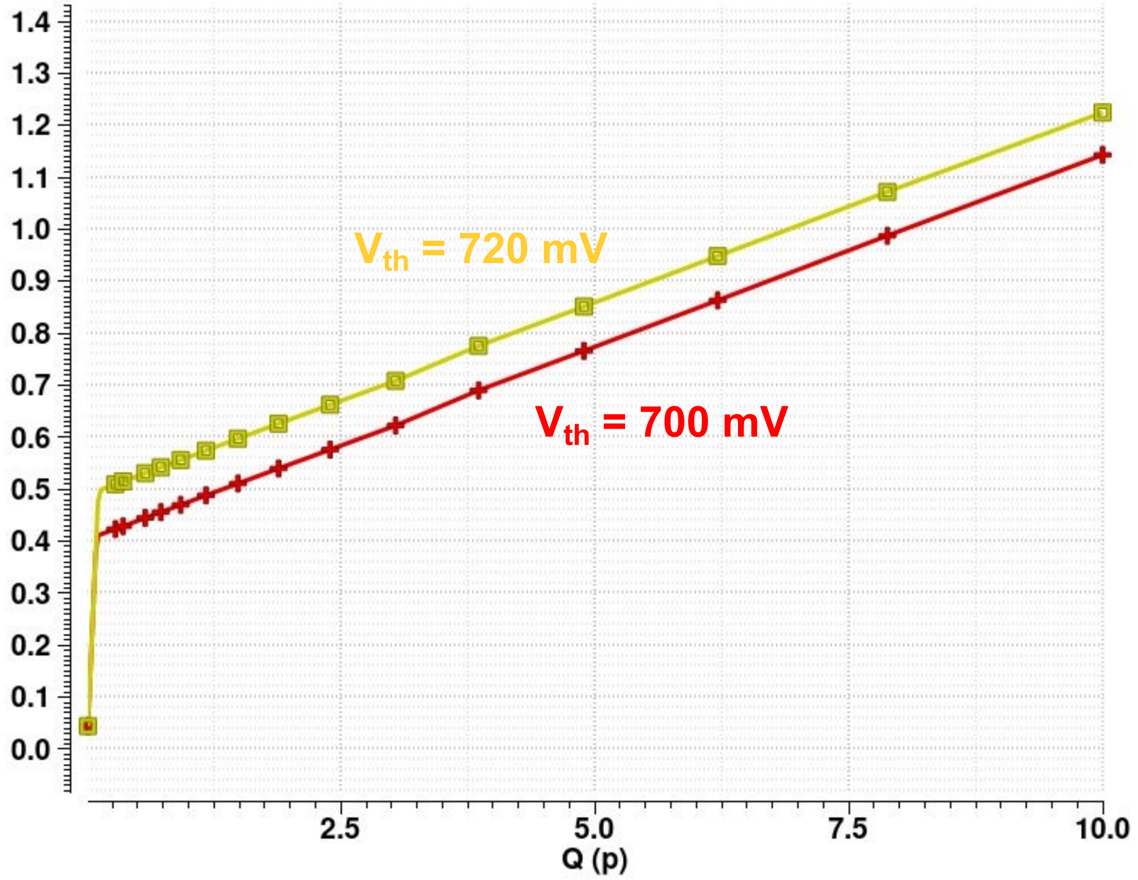


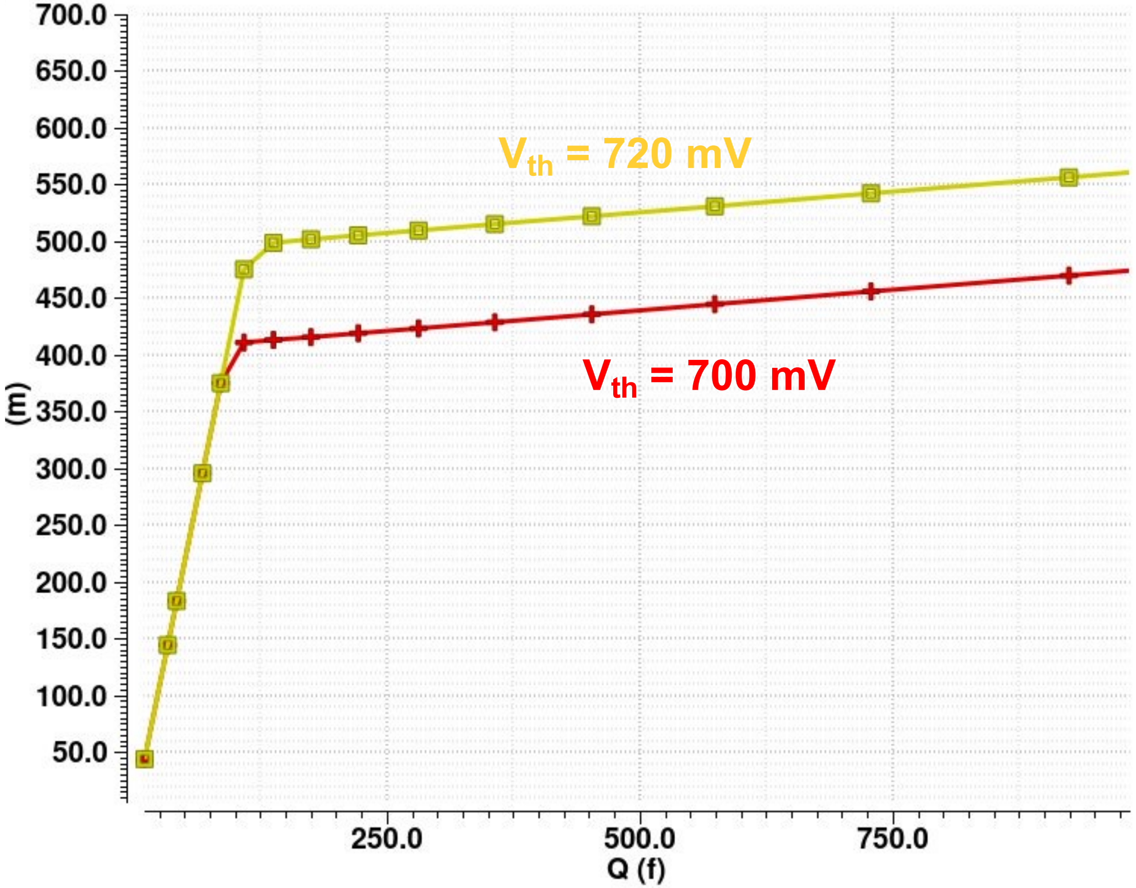
Circuitry in red added to original CHARMS250V1 CA1 circuit:

- Initially Cf1 in feedback path, C’f1 disconnected from feedback path and connected to references (equal to amplifier input/output DC potentials):
- If amplifier output (Vout1) crosses a threshold (Vth), Vsw goes high, and connects capacitor C’f1 to amplifier input and output.
- After some delay (∆1), Vsw goes low and C’f1 is disconnected from the feedback path.
- The compensation capacitor network follows a similar sequence (we need extra compensation capacitance with larger feedback capacitance to make the amplifier loop stable)

CHARMS250V2B transfer characteristics for charges up to 10 pC

Input charge vs. output amplitude

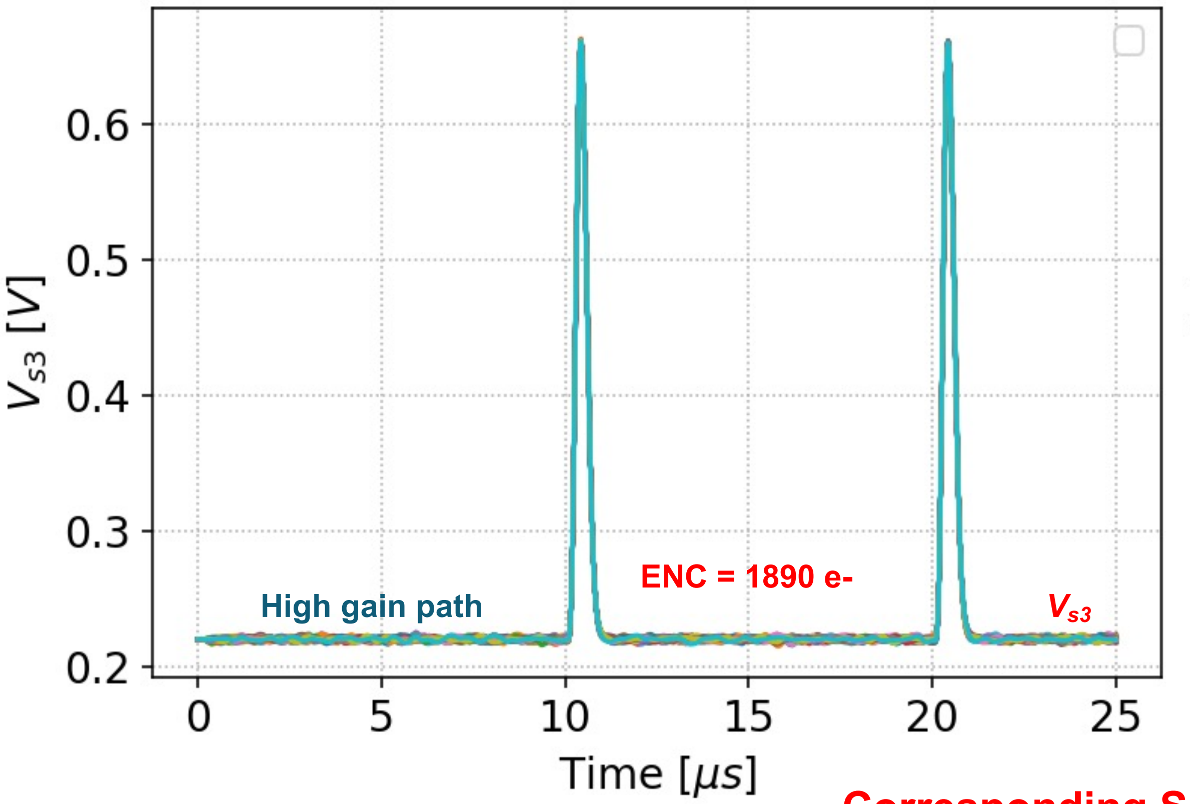




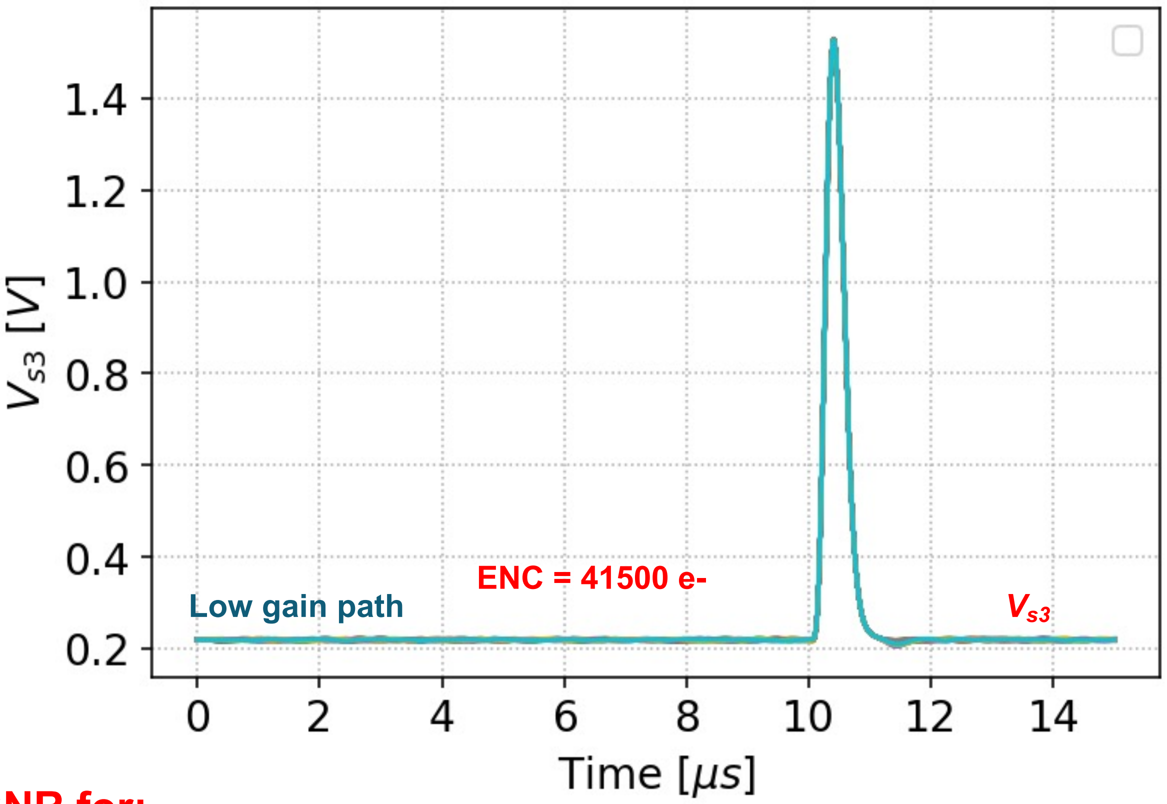
Brookhaven National Laboratory

Noise for CHARMS250V2B, peaking time = 250 ns (RT)

C_{in} = 200 pF, Q_{in} = 100 fC



C_{in} = 200 pF, Q_{in} = 5 pC



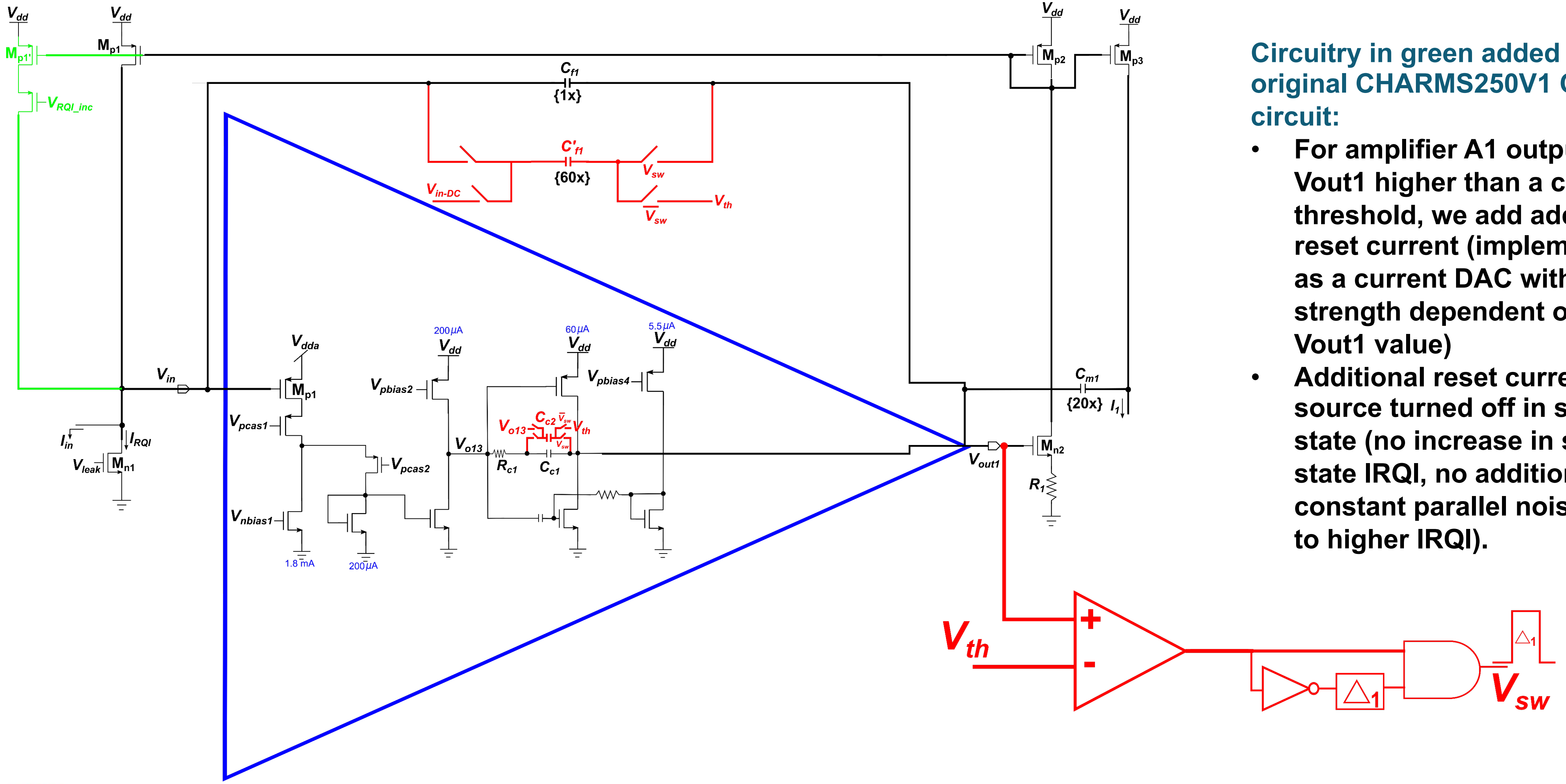
Corresponding SNR for:

- **MIP (4 fC): ~ 13**
- **Gain transition point (100 fC): 15**

Compared to CHARMS250V2A, CHARMS250V2B shows:

- ***Lower noise*** **on high gain path (greater charge coupling, higher overall gain)**
- ***Higher noise*** **on low gain path (larger 60x feedback capacitance to accommodate charges up to 10 pC in reduced voltage swing of ~ 1V)**

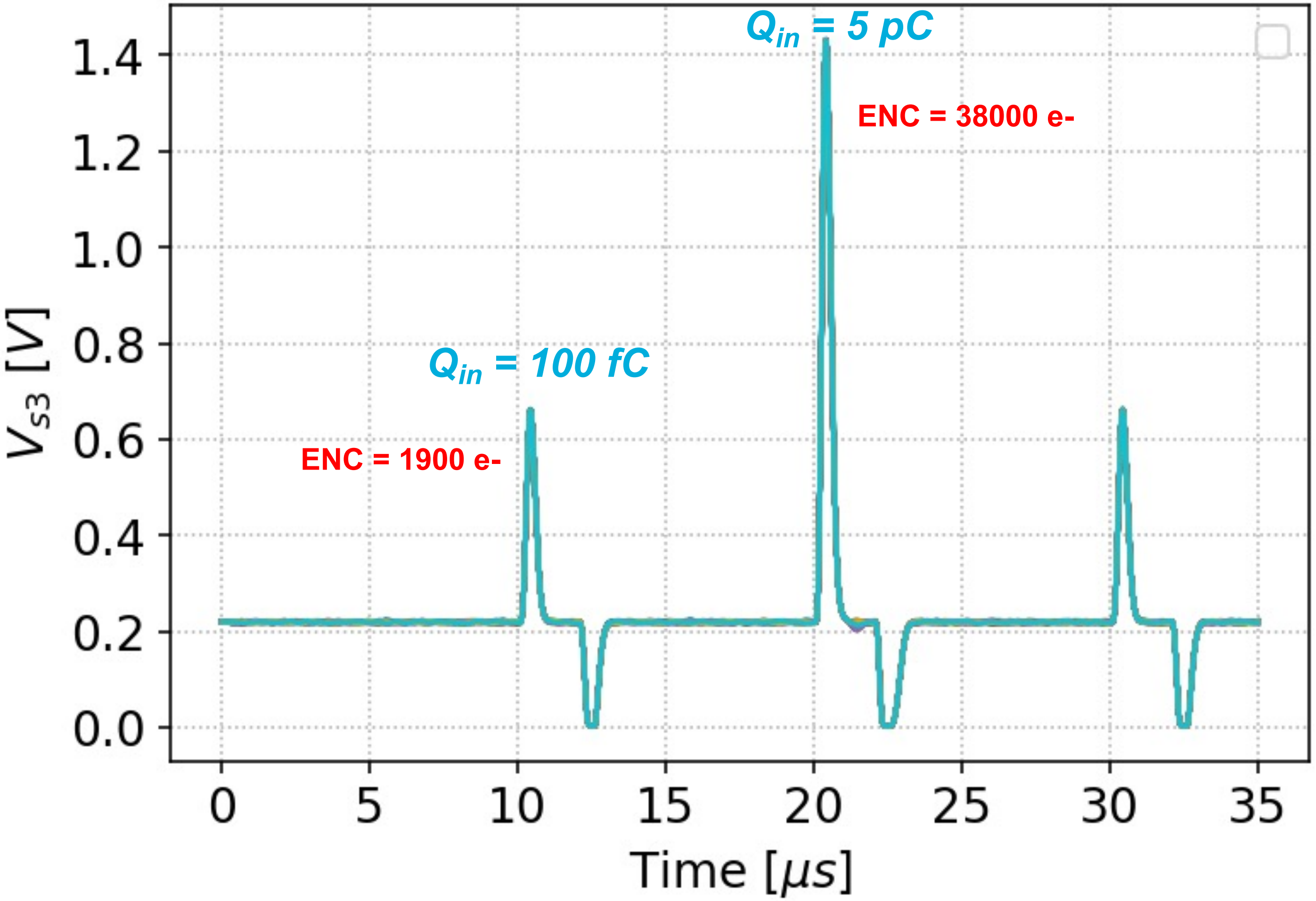
Solution for handling KHz event rates: dynamic I_{RQI} increase



Circuitry in green added to original CHARMS250V1 CA1 circuit:

- For amplifier A1 output Vout1 higher than a certain threshold, we add additional reset current (implemented as a current DAC with strength dependent on Vout1 value)
- Additional reset current source turned off in steady state (no increase in steady state IRQI, no addition of constant parallel noise due to higher IRQI).

CHARMS250V2B noise with dynamic reset current increase, peaking time = 250 ns, C_{in} = 200 pF (RT)



Noise practically unchanged, compared to the case with no dynamic reset current increase

Summary

- CHARMS family of low-noise cryogenic analog front-end ASICs in 65 nm being developed at BNL.
- CHARMS250V1 prototype fabricated and characterized at BNL; shows good noise performance down to 77 K.
- Two front-end architectures to extend the full-scale input charge range of CHARMS250V1 to 10 pC being developed:

	CHARMS250V2A	CHARMS250V2B
Architecture	Dual parallel gain paths	Dynamic feedback capacitance switching
# of inputs	2 (if coupling capacitor external)	1
# of outputs	2 (signal, enabled path)	1
ENC (Cin = 200 pF, T_p = 250 ns, room temperature)	High gain mode: 3.4k e-	High gain mode: 1.9k e-
	Low gain mode: 24k e-	Low gain mode: 40k e-
Power per channel (amplifier + shaping filter)	8.2 mW	6 mW

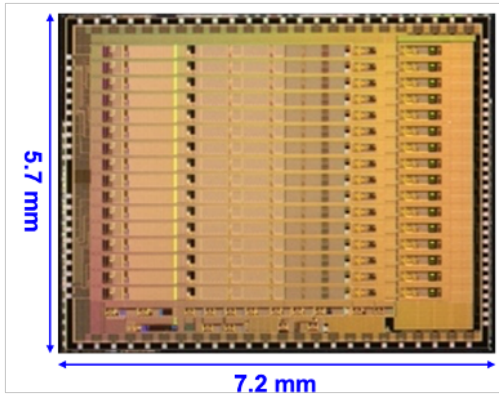
- Future work includes R&D for CHARMS10 with wide-dynamic range and shortest peaking time down to 10 ns.

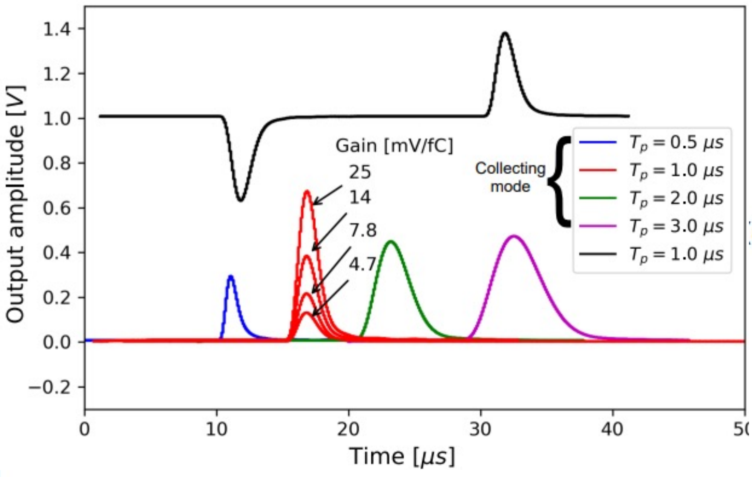
LArASIC, CHARMS Reference: P. Mukim *et al.*, "Cryogenic Front-End ASICs for Low-Noise Readout of Charge Signals," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 72, no. 4, pp. 1496-1509, April 2025, doi: 10.1109/TCSI.2024.3506828.

Backup Slides

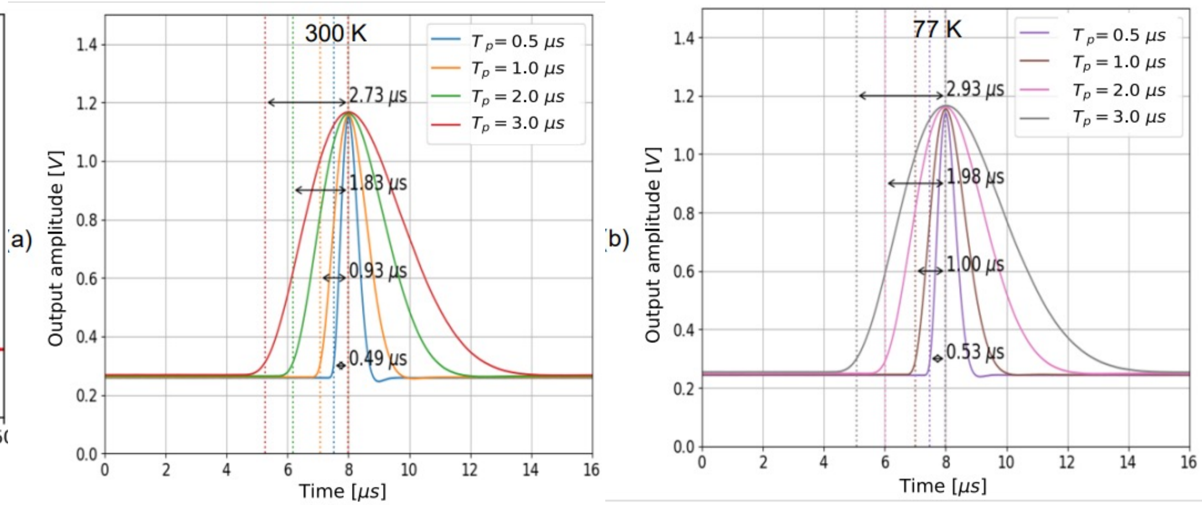
LArASIC summary

- LArASIC MPW met all the DUNE requirements
- 24,000 LArASIC chips being deployed in DUNE Phase-I Far Detectors (2 10kTon LAr Time Projection Chambers (TPCs))
- Final version (P5B) has improved input ESD protection compared to P5 -> Achieved ~97% yield at room temperature

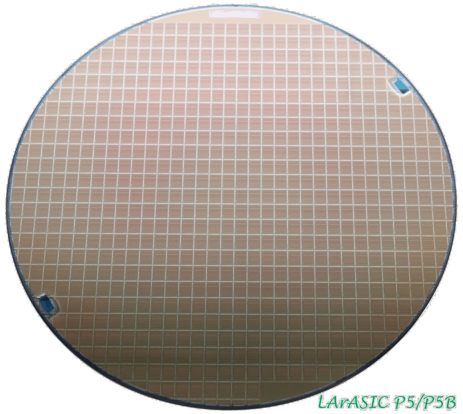




Oscilloscope outputs at 77 K



Measured peaking times

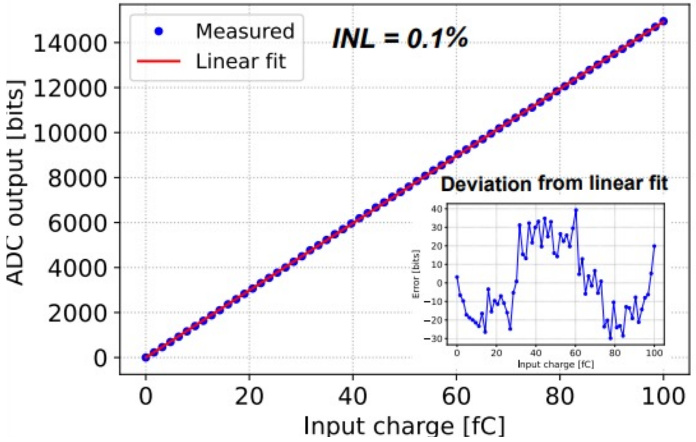


250 wafers LArASIC production run for DUNE 75k P5 and 75k P5B chips

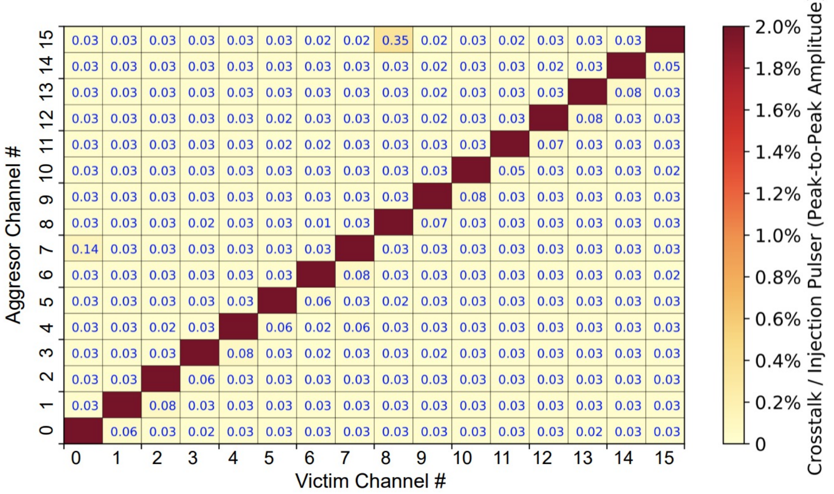
8” wafer with 610 LArASICs P5 and P5A(B) w. increased ESD protection

Very small deviations seen between RT and LNT in the measured peaking time and channel gain (< 2%)

LArASIC measurement results

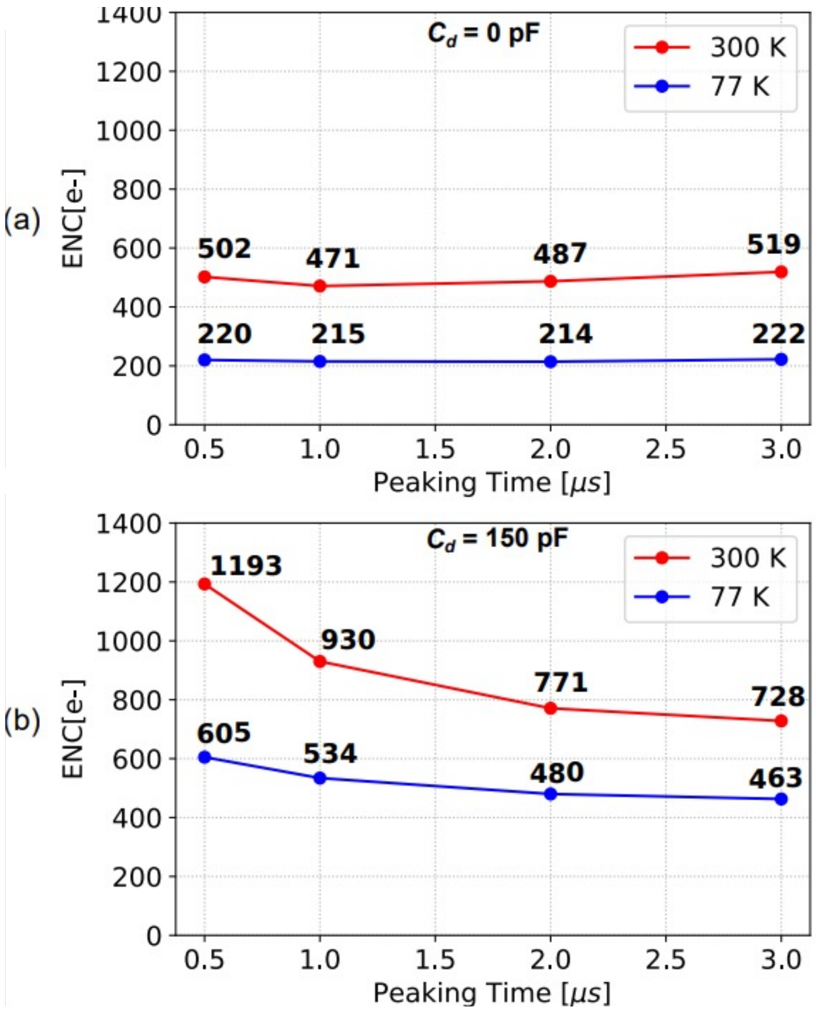


High linearity



Aggresor Channel #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
15	0.03	0.03	0.03	0.03	0.03	0.03	0.02	0.02	0.35	0.02	0.03	0.02	0.03	0.03	0.03	
14	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.02	0.03	0.03	0.02	0.03		0.05
13	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.02	0.03	0.03	0.03		0.08	0.03
12	0.03	0.03	0.03	0.03	0.03	0.02	0.03	0.03	0.03	0.02	0.03	0.03		0.08	0.03	0.03
11	0.03	0.03	0.03	0.03	0.03	0.02	0.02	0.03	0.03	0.03	0.03		0.07	0.03	0.03	0.03
10	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03		0.05	0.03	0.03	0.03	0.02
9	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03		0.08	0.03	0.03	0.03	0.03	0.03
8	0.03	0.03	0.03	0.02	0.03	0.03	0.01	0.03		0.07	0.03	0.03	0.03	0.03	0.03	0.03
7	0.14	0.03	0.03	0.03	0.03	0.03	0.03		0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03
6	0.03	0.03	0.03	0.03	0.03	0.03		0.08	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.02
5	0.03	0.03	0.03	0.03	0.03		0.06	0.03	0.02	0.03	0.03	0.03	0.03	0.03	0.03	0.03
4	0.03	0.03	0.02	0.03		0.06	0.02	0.06	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03
3	0.03	0.03	0.03		0.08	0.03	0.02	0.03	0.03	0.02	0.03	0.03	0.03	0.03	0.03	0.03
2	0.03	0.03		0.06	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03
1	0.03		0.08	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03
0		0.06	0.03	0.02	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.02	0.03	0.03

Low crosstalk (mean: 0.04%)



Low noise

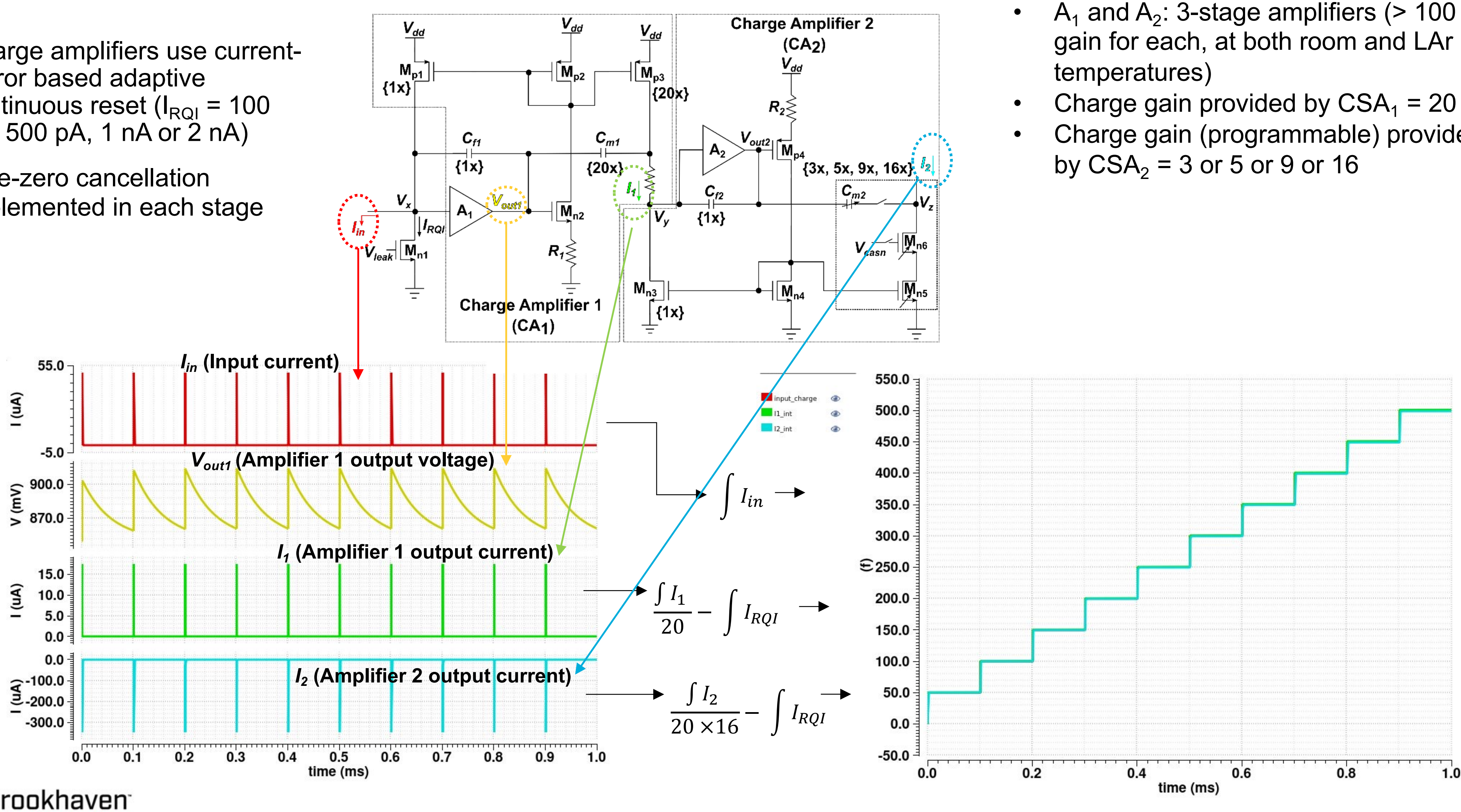
Temperature	Baseline	Power consumption (mW)		
		Buffers off	SE on	SEDC on
300 K	200 mV	5.6	9.0	10.7
77 K	200 mV	5.3	8.8	10.8
300 K	900 mV	5.8	9.5	10.6
77 K	900 mV	5.5	9.1	10.5

Power consumption

Charge amplifier design and transient response

- Charge amplifiers use current-mirror based adaptive continuous reset (I_{RQI} = 100 pA, 500 pA, 1 nA or 2 nA)
- Pole-zero cancellation implemented in each stage

- A_1 and A_2: 3-stage amplifiers (> 100 dB gain for each, at both room and LAr temperatures)
- Charge gain provided by CSA_1 = 20
- Charge gain (programmable) provided by CSA_2 = 3 or 5 or 9 or 16



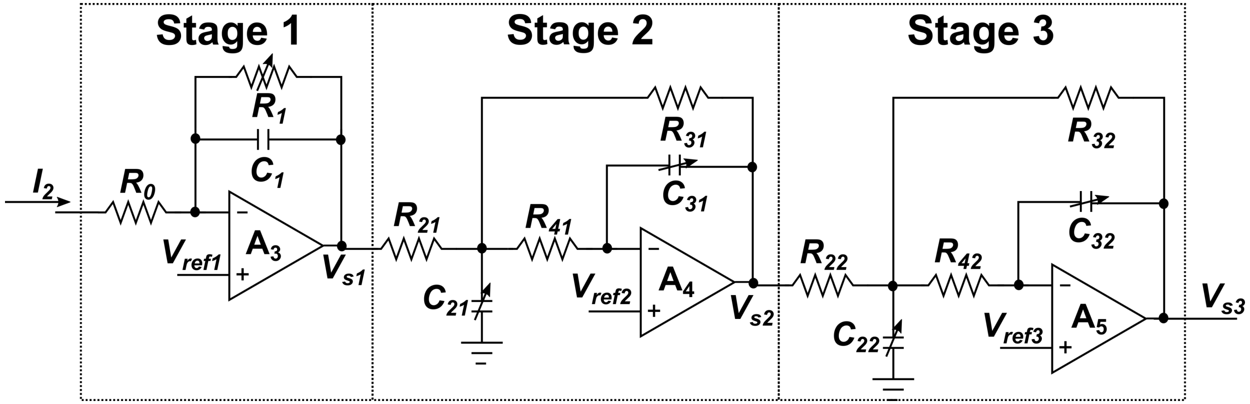
$$\int I_{in}$$

$$\frac{\int I_1}{20} - \int I_{RQI}$$

$$\frac{\int I_2}{20 \times 16} - \int I_{RQI}$$

Ref: G. De Geronimo et. al., Front-End ASIC for a GEM based Time Projection Chamber

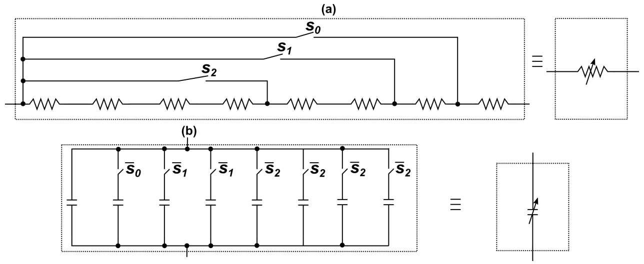
Shaping filter design



- Peaking time is programmable (0.25 μs – 2 μs)
- Lower series noise with longer shaping times
- Implemented shaper is a 5th order semi-gaussian filter with complex conjugate poles
- Semi-gaussian shaper has a faster return to baseline than a CR-RC^n shaping filter
- Faster tail lowers contribution of parallel noise
- Symmetric rising and falling edges also helpful for mitigating pile-up of events
- A_3, A_4, A_5 are two-stage miller compensated differential amplifiers
- V_{ref1}, V_{ref2}, V_{ref3} selected based on output baseline setting

Component values for CHARMS250

Resistor	Value (kΩ)	Capacitor	Value (pF)
R_0	0.3		
R_u (R_1)	7.5	C_1	11.9
R_{21}, R_{41}, R_{42}	18	C_u (C_{21})	5.9
R_{31}	60	C_u (C_{31})	1.39
R_{22}	36	C_u (C_{22})	5.5
R_{32}	39	C_u (C_{32})	1.13



$$V_{s1}(s) = -I_2(s)\frac{R_1}{(1+sC_1R_1)}$$

$$V_{s2}(s) = -V_{s1}(s)\frac{\frac{1}{R_{21}R_{41}C_{21}C_{31}}}{s^2 + s\left(\frac{1}{R_{21}C_{21}}+\frac{1}{R_{31}C_{31}}+\frac{1}{R_{41}C_{21}}\right)+\frac{1}{R_{31}R_{41}C_{21}C_{31}}}$$

$V_{s3}(s)$ is similar……

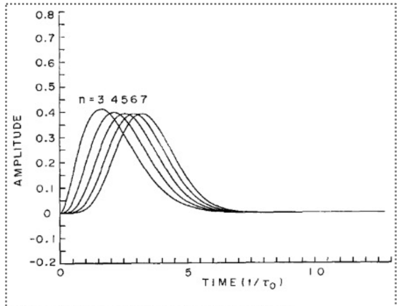
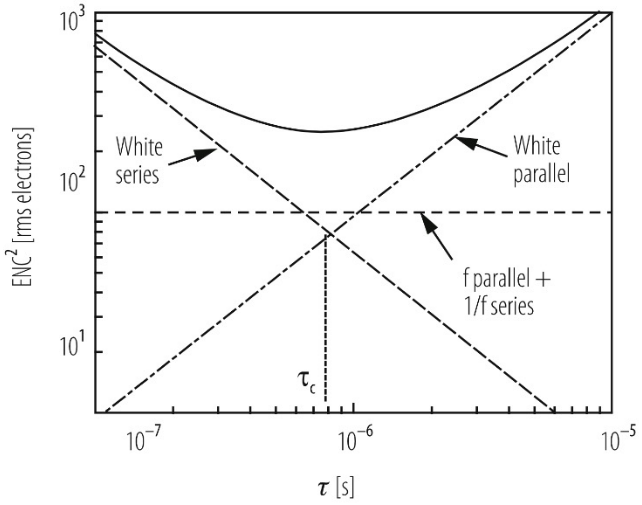


Fig. 3. Impulse responses of the Gaussian filters.

Ref: S. Ohkawa, M. Yoshizawa, K. Husimi, Direct synthesis of the Gaussian filter for nuclear pulse amplifiers.



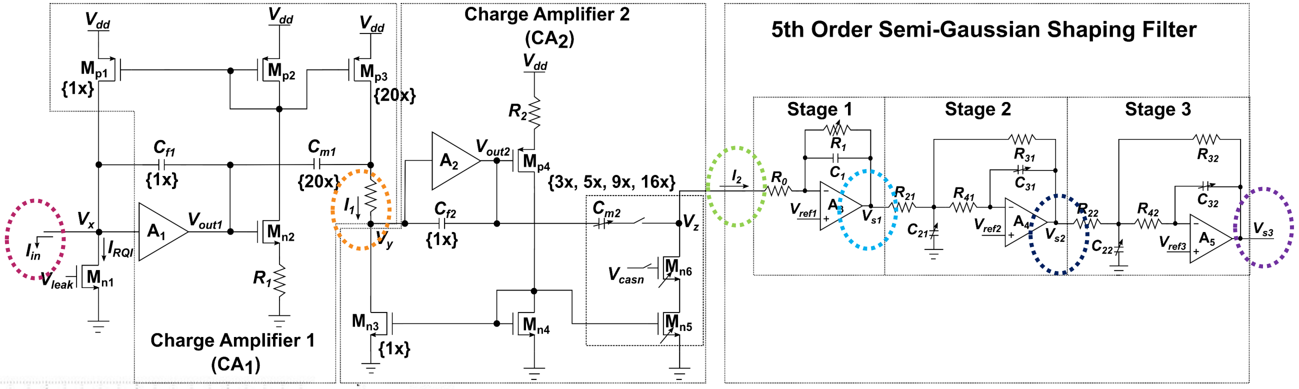
Ref: Veljko Radeka, Signal Processing for Particle Detectors

Analog chain simulated impulse response at LArT

I_{in} : Input current

I_1 : Amplifier 1 output current

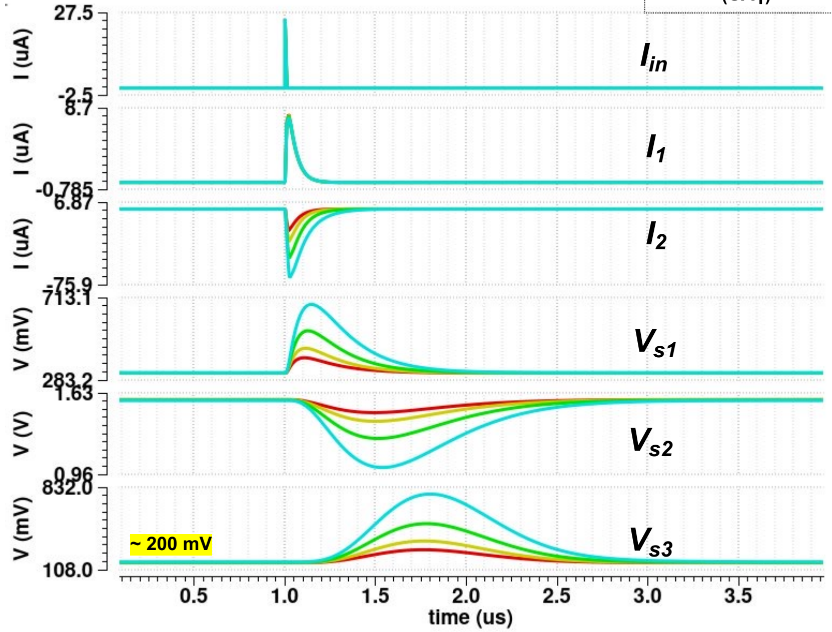
I_2 : Amplifier 2 output current



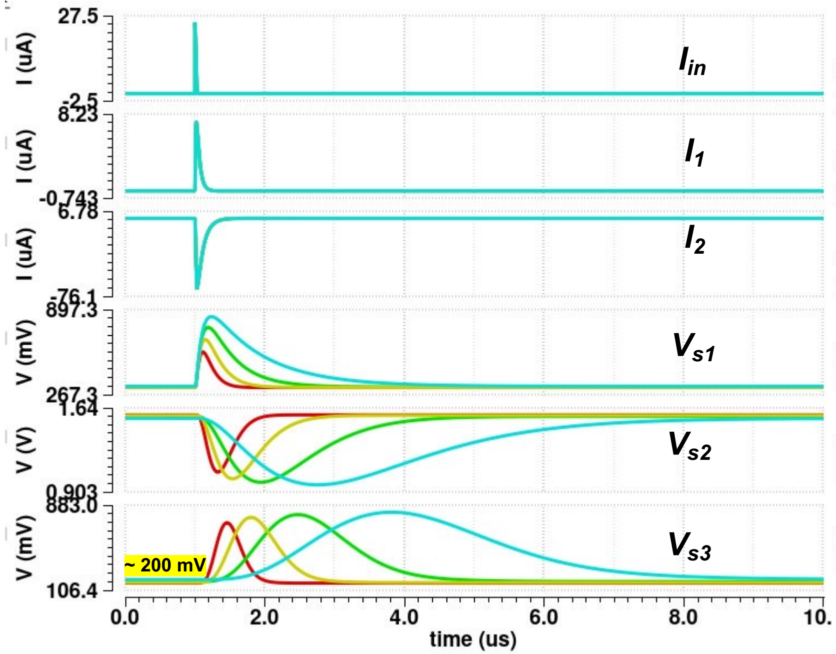
V_{s1} : Shaper stage 1 output voltage

V_{s2} : Shaper stage 2 output voltage

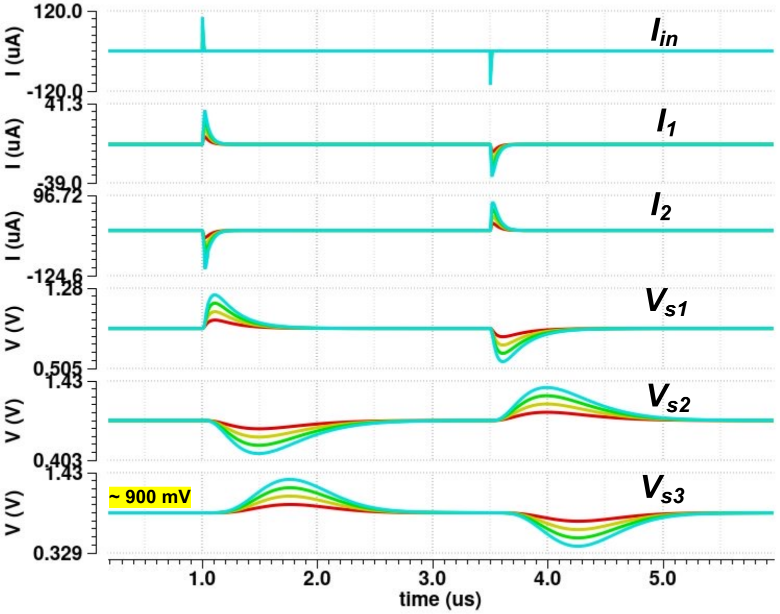
V_{s3} : Shaper stage 3 output voltage



Programmable gain (4.7 mV/fC, 7.8 mV/fC, 14 mV/fC, 25 mV/fC)

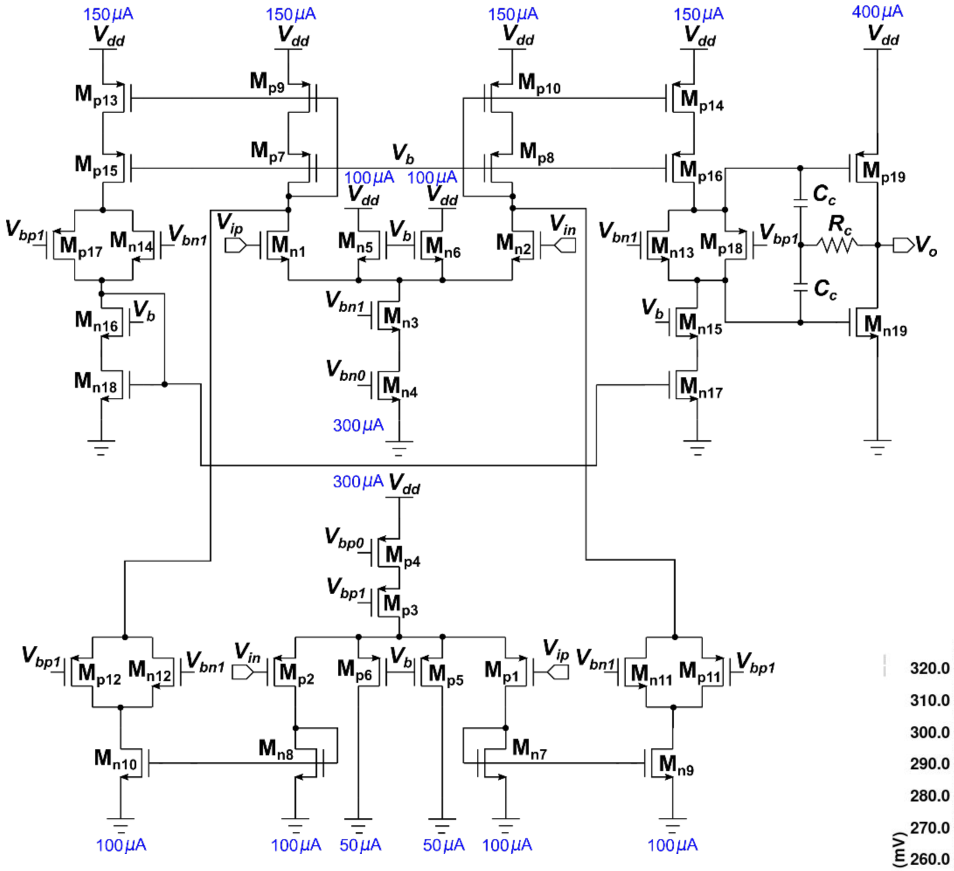


Programmable peaking time (0.25 µs, 0.5 µs, 1.0 µs, 2.0 µs)



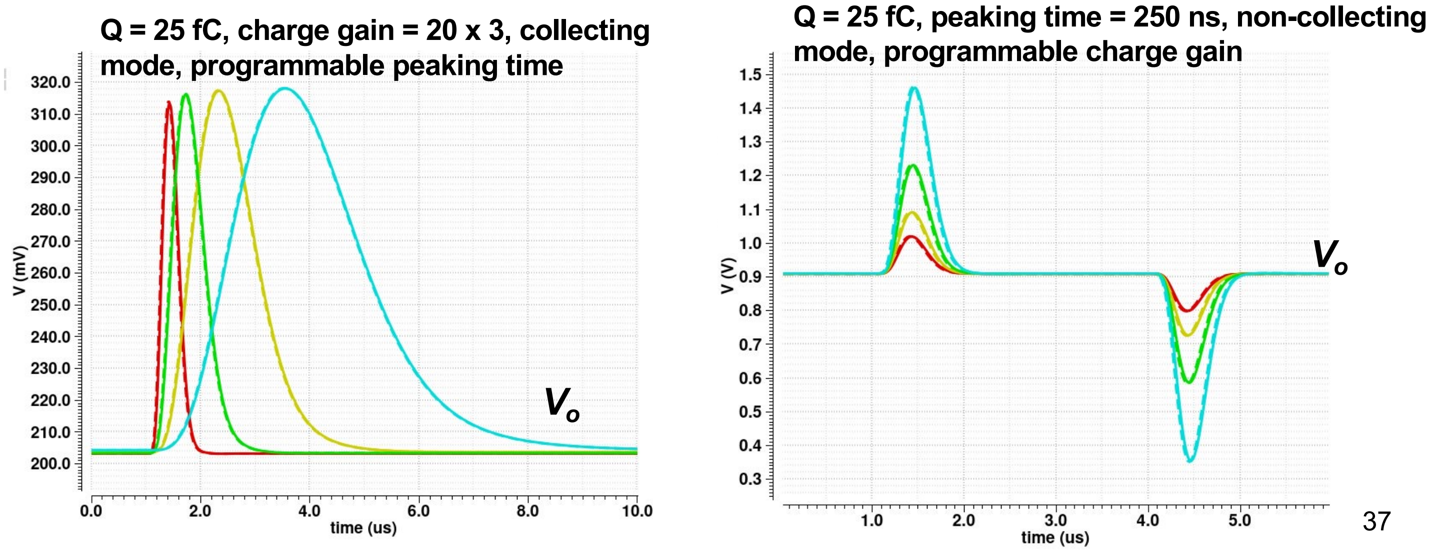
Non-collecting mode (Bipolar charges with magnitude 25 fC, 50 fC, 75 fC, 100 fC)

Output buffer design – single ended (SE) buffer



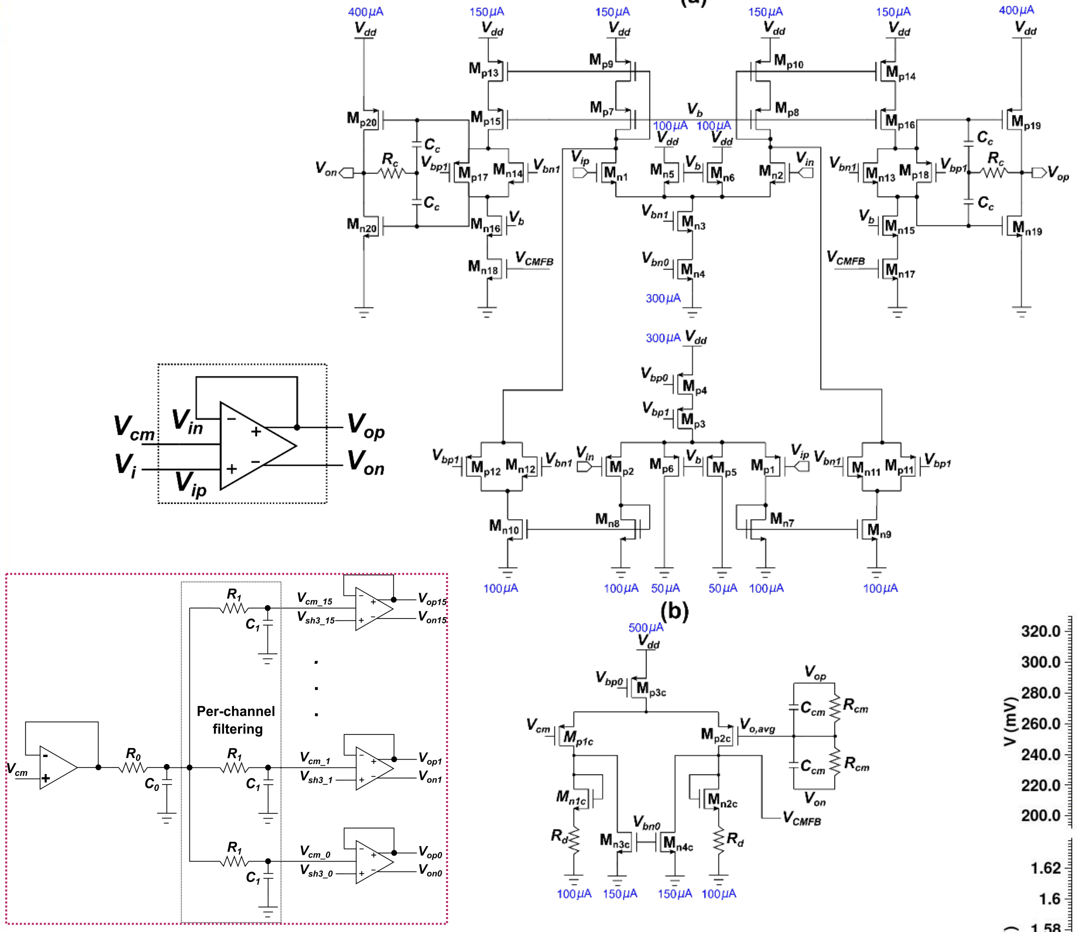
- Based on a folded-cascode current-mirror based operational transconductance amplifier
- Comprises of parallel NMOS and PMOS input pairs to support rail-to-rail operation
- Monticelli class-AB output stage used
- High open-loop DC gain (> 110 dB at LArT) ensures minimal introduction of distortions in the output signal
- Suitable to drive tens of pF of capacitance load (chip-to-chip trace)

SE Buffer impulse response with 100 pF load


Q = 25 fC, charge gain = 20 x 3, collecting mode, programmable peaking time

Q = 25 fC, peaking time = 250 ns, non-collecting mode, programmable charge gain

Output buffer design – single ended (SEDC) buffer


Main loop

(a)

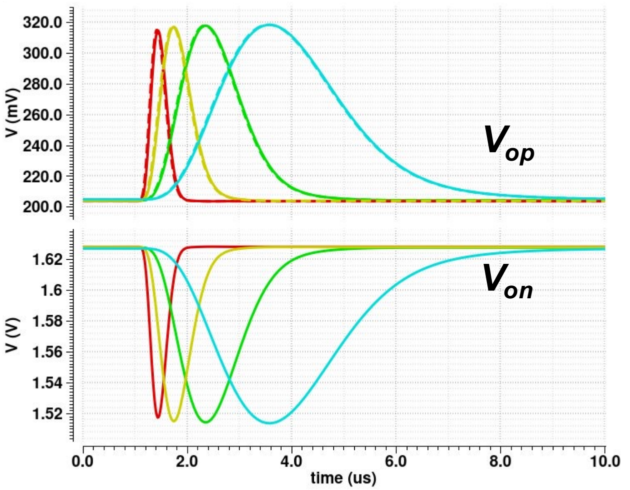
(b)

CMFB loop

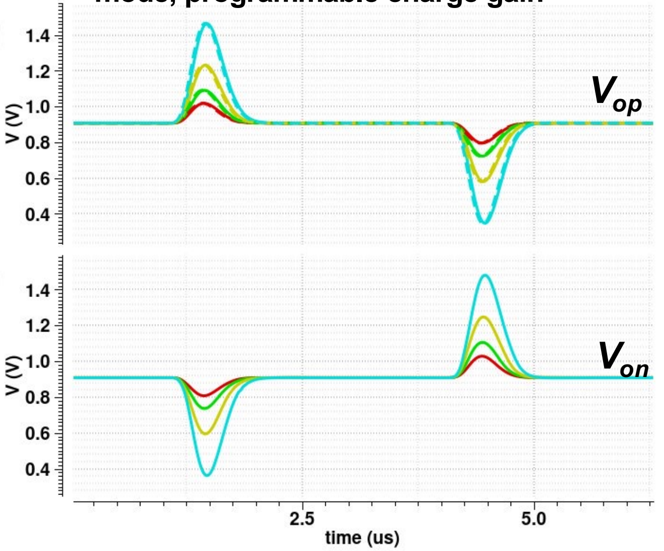
- Simpler, more compact and power-efficient compared to resistor or 3-operational amplifier based SEDC designs
- Circuit implementation similar to SE buffer, but core is fully-differential (inputs and outputs)
- Noise transferred from common-mode input signal (V_{cm}) to the output with 6 dB gain
- Global and local noise filtering implemented for V_{cm}
- Both common-mode and differential paths have high open loop DC voltage gains (> 110 dB) and comparable bandwidths (≈100 MHz) at LArT
- Helps with crosstalk cancellation

SEDC Buffer impulse response with 100 pF load

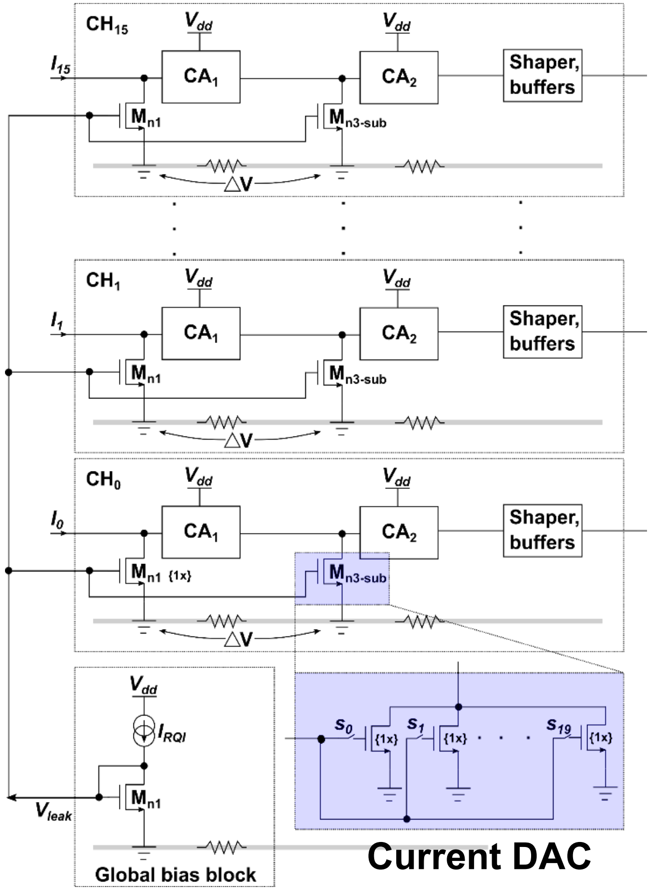
Q = 25 fC, charge gain = 20 x 3, collecting mode, programmable peaking time



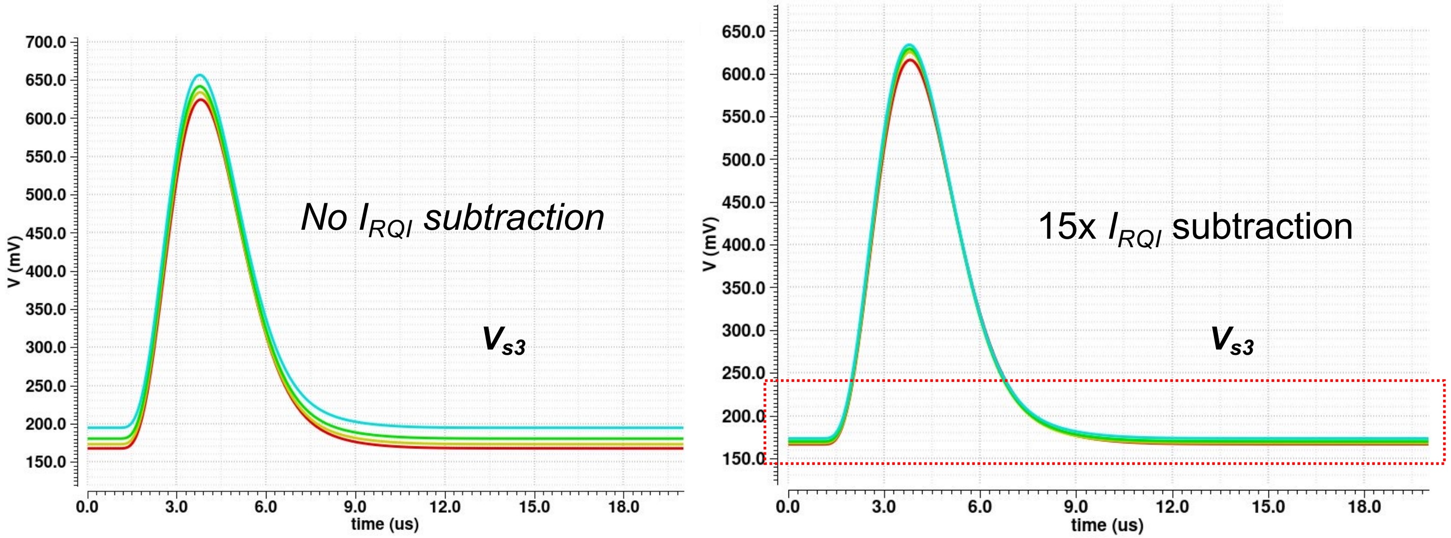
Q = 25 fC, peaking time = 250 ns, non-collecting mode, programmable charge gain



Programmable 5-bit RQI subtraction implemented in CHARMS250



Response with different values of I_{RQI}

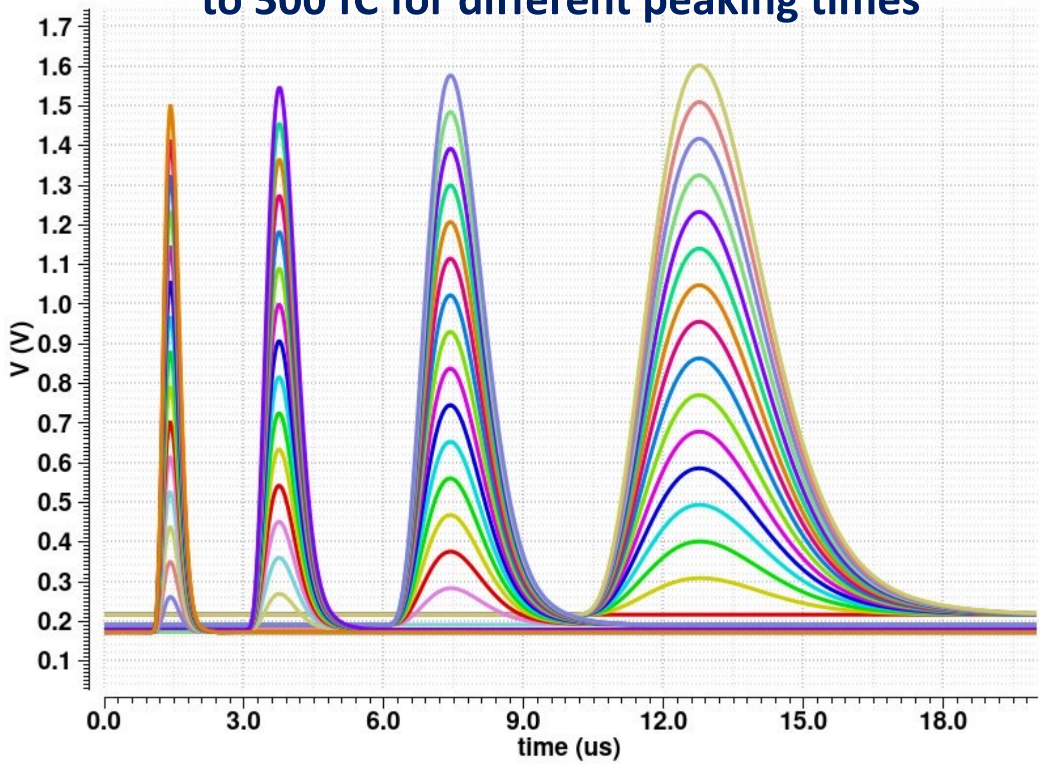


Baseline drift reduced

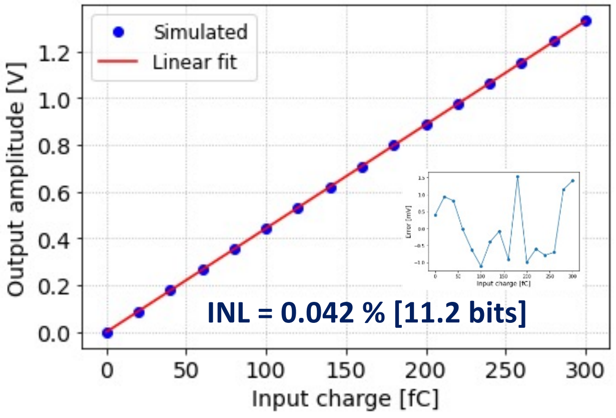
- Programmable I_{RQI} subtraction provides immunity against process mismatches and layout induced non-ideality
- For M_{n1} and $M_{n3\text{-sub}}$ operating in deep-subthreshold ($I_{RQI} \propto e^{(V_{gs}-V_{th})(q/\eta kT)}$), variance in at LNT almost 10x higher than at RT
- Previously, with fixed I_{RQI} subtraction, even few-millivolts of V_{gs} difference at M_{n1} and $M_{n3\text{-sub}}$ due to IR drop in ground rail was seen to cause subtraction to become > 20x and make the second stage reset mechanism non-operational

Simulated response for full-charge range and linearity

Shaping filter output (V_{s3}) for input charges up to 300 fC for different peaking times

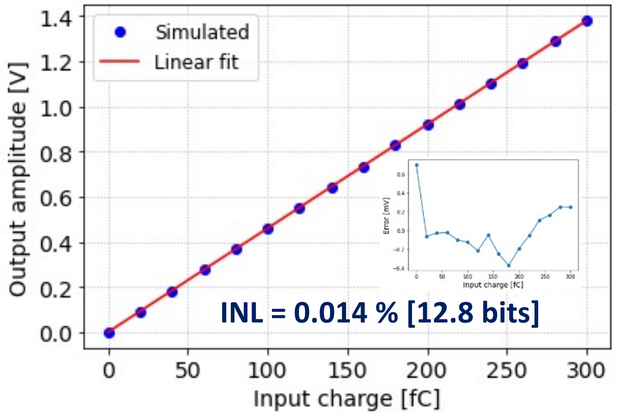


T_p = 0.25 µs



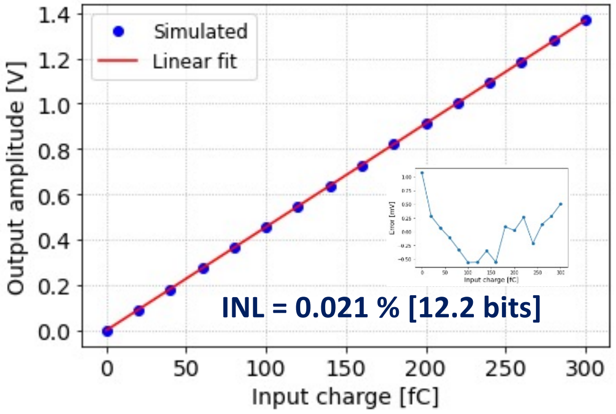
INL = 0.042 % [11.2 bits]

T_p = 1.0 µs



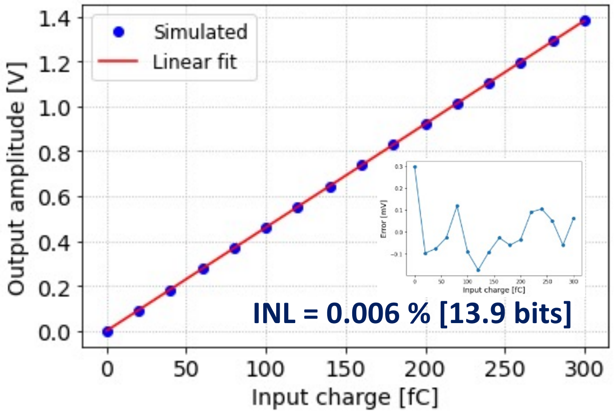
INL = 0.014 % [12.8 bits]

T_p = 0.5 µs



INL = 0.021 % [12.2 bits]

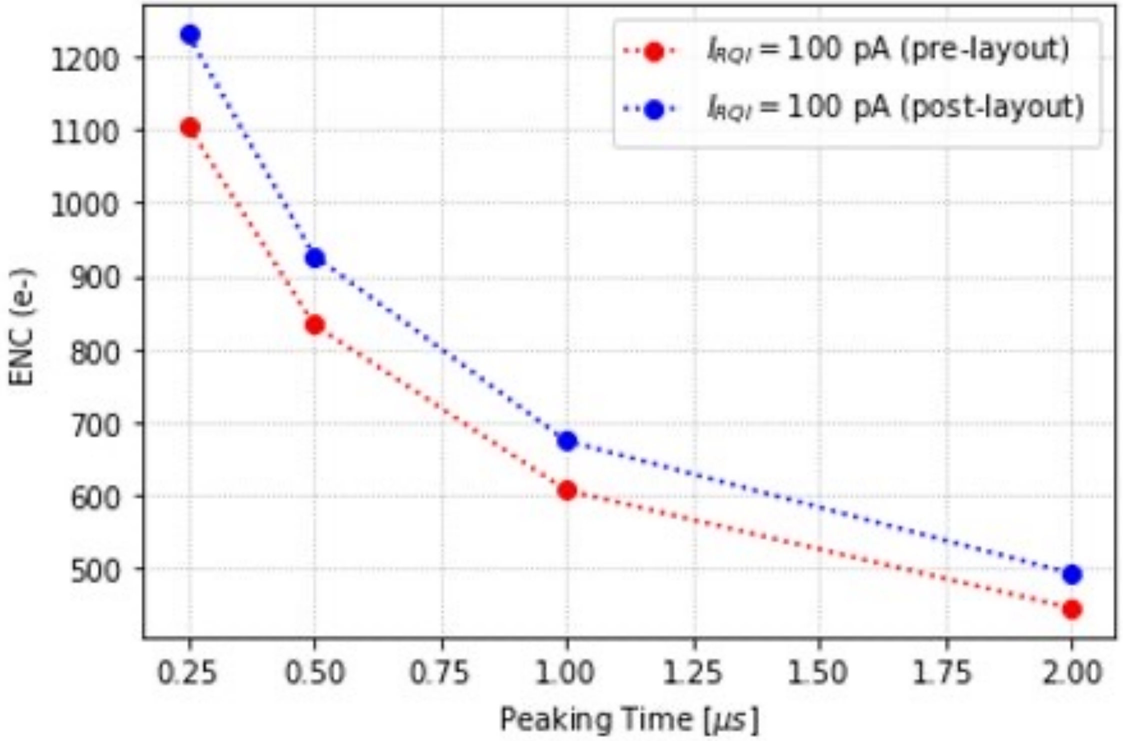
T_p = 2.0 µs



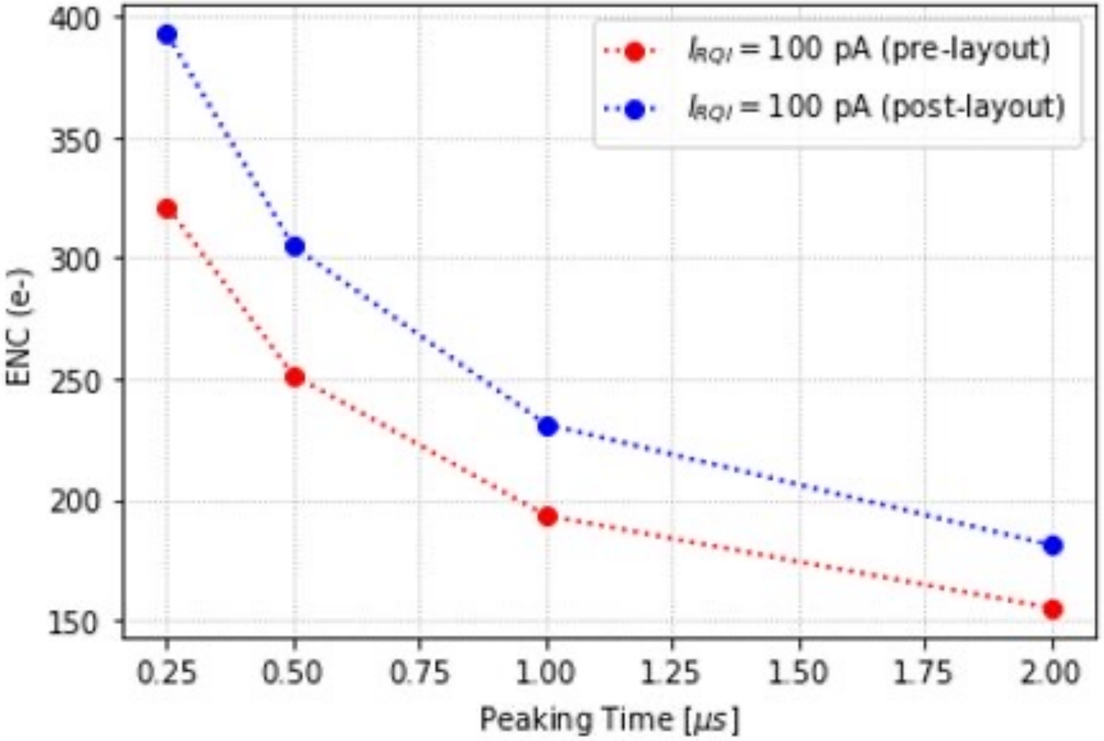
INL = 0.006 % [13.9 bits]

Noise (simulated) with C_d = 160 pF

Room temperature



Liquid argon temperature



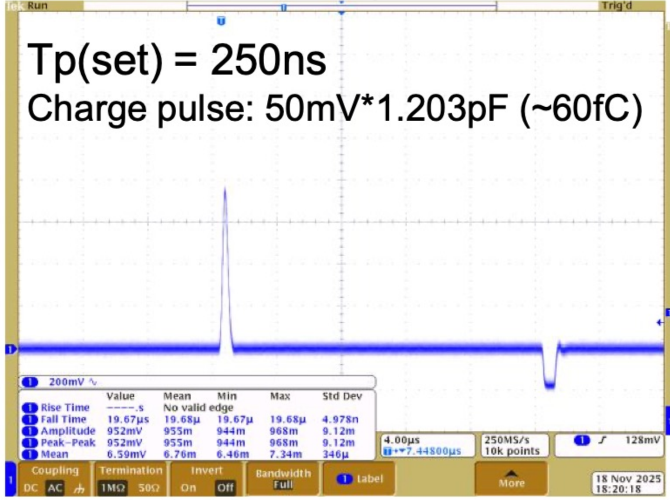
- 60-75% noise contribution is from the input transistor (thermal noise contribution dominates, flicker noise contribution is less than 5 %)
- These simulations may be too optimistic

Power Consumption & Preliminary Pulse response

	Single-ended output with single-ended buffer disabled			
	Voltage /mV	1Ohm /mV	current / mA	Power /mW
VDDO(R67)	1795	0	0	0.0
VDD1P1(R69)	1105	0.009	0.009	0.0
VDDA(R60)	1789	1.812	1.812	3.2
VDD(R61)	1797	3.204	3.204	5.8
total /mW			**5.025**	**9.0**

	Single-ended output with single-ended buffer enabled			
	Voltage /mV	1Ohm /mV	current / mA	Power /mW
VDDO(R67)	1792	0.785	0.785	1.4
VDD1P1(R69)	1105	0.009	0.009	0.0
VDDA(R60)	1789	1.812	1.812	3.2
VDD(R61)	1784	4.697	4.697	8.4
total			**7.303**	**13.0**

	Differential output with SEDC enabled			
	Voltage /mV	1Ohm /mV	current / mA	Power /mW
VDDO(R67)	1790	1.593	1.593	2.9
VDD1P1(R69)	1105	0.003	0.003	0.0
VDDA(R60)	1789	1.814	1.814	3.2
VDD(R61)	1784	4.974	4.974	8.9
total			**8.384**	**15.0**

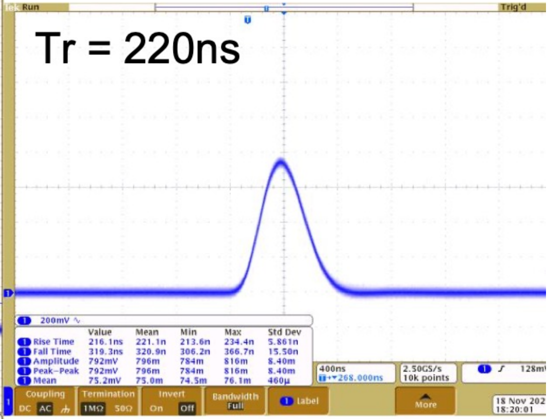


Tp(set) = 250ns

Charge pulse: 50mV*1.203pF (~60fC)

200mV

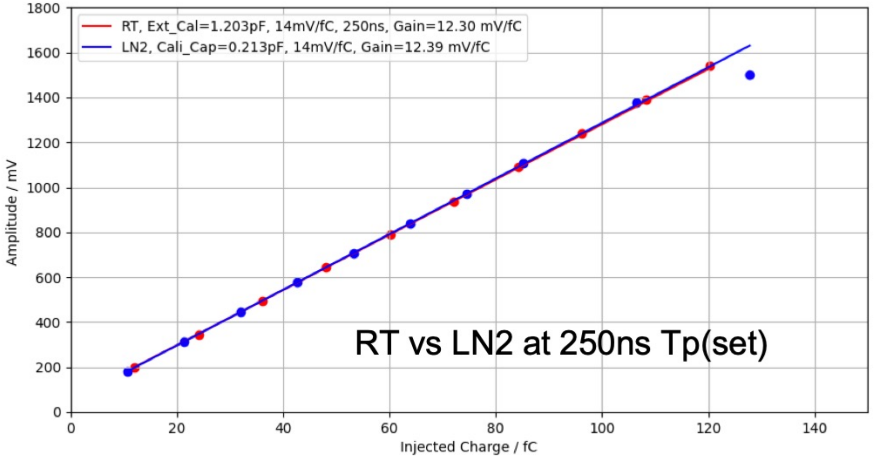
	Value	Mean	Min	Max	Std Dev
Rise Time	----.s	No valid edge			
Fall Time	19.67µs	19.68µ	19.67µ	19.68µ	4.978n
Amplitude	952mV	955m	944m	968m	9.12m
Peak–Peak	952mV	955m	944m	968m	9.12m
Mean	6.59mV	6.76m	6.46m	7.34m	346µ



Tr = 220ns

200mV

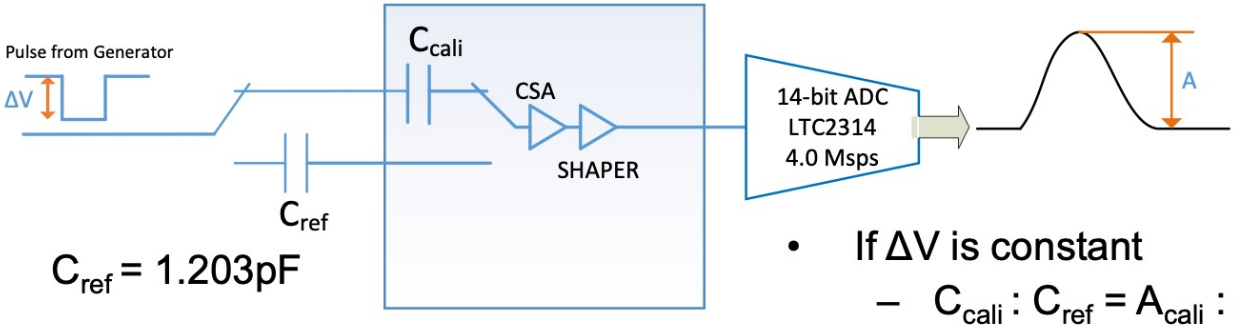
	Value	Mean	Min	Max	Std Dev
Rise Time	216.1ns	221.1n	213.6n	234.4n	5.861n
Fall Time	319.3ns	320.9n	306.2n	366.7n	15.50n
Amplitude	792mV	796m	784m	816m	8.40m
Peak–Peak	792mV	796m	784m	816m	8.40m
Mean	75.2mV	75.0m	74.5m	76.1m	460µ



RT vs LN2 at 250ns Tp(set)

Gain doesn't change significantly at both warm and cold

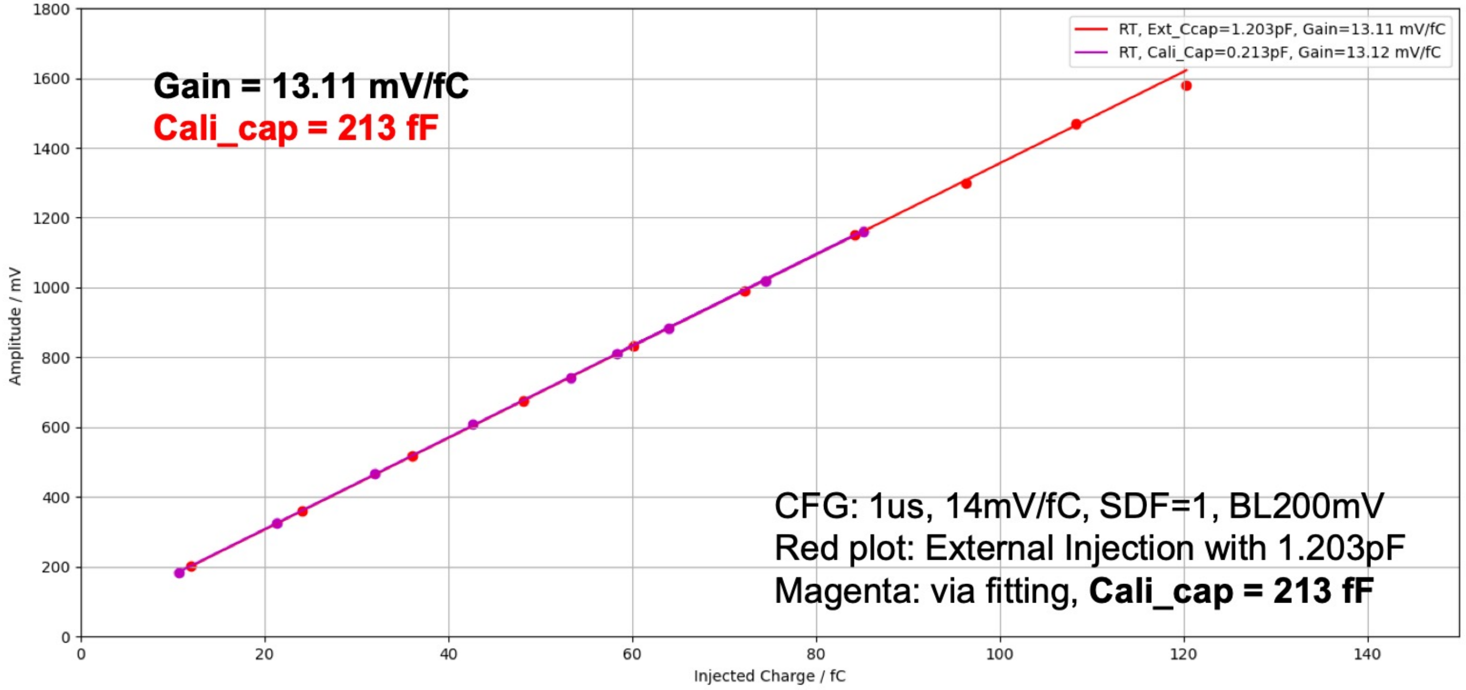
Embedded Calibration Capacitor measurement



C_{ref} = 1.203pF

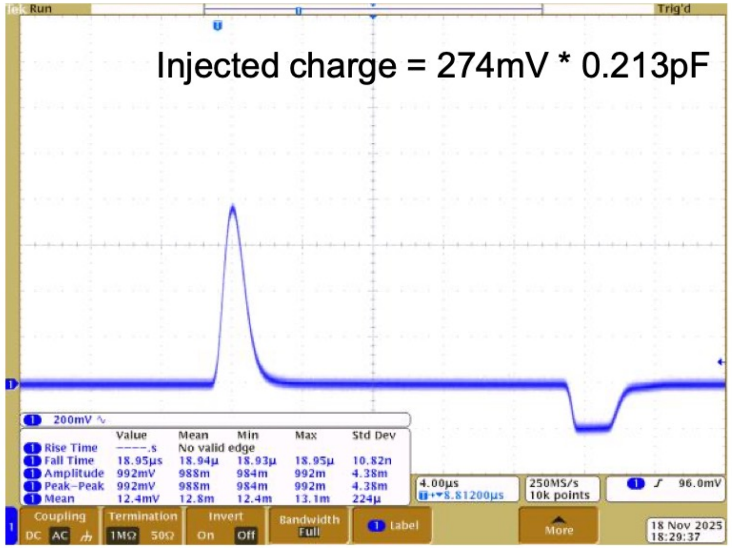
- If ΔV is constant
  - – $C_{cali} : C_{ref} = A_{cali} : A_{ref}$

C_{cali} is MIM (Metal-Insulator-Metal) capacitor, low temperature coefficient .



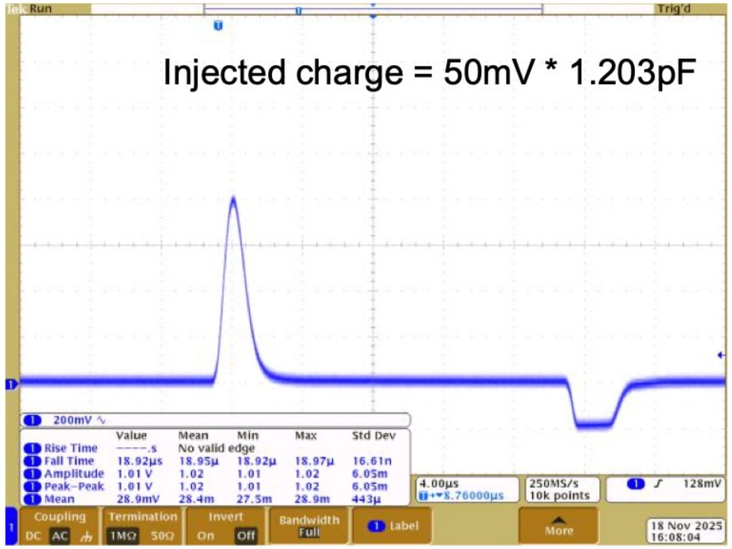
Gain = 13.11 mV/fC
Cali_cap = 213 fF

CFG: 1us, 14mV/fC, SDF=1, BL200mV
Red plot: External Injection with 1.203pF
Magenta: via fitting, **Cali_cap = 213 fF**



Injected charge = 274mV * 0.213pF

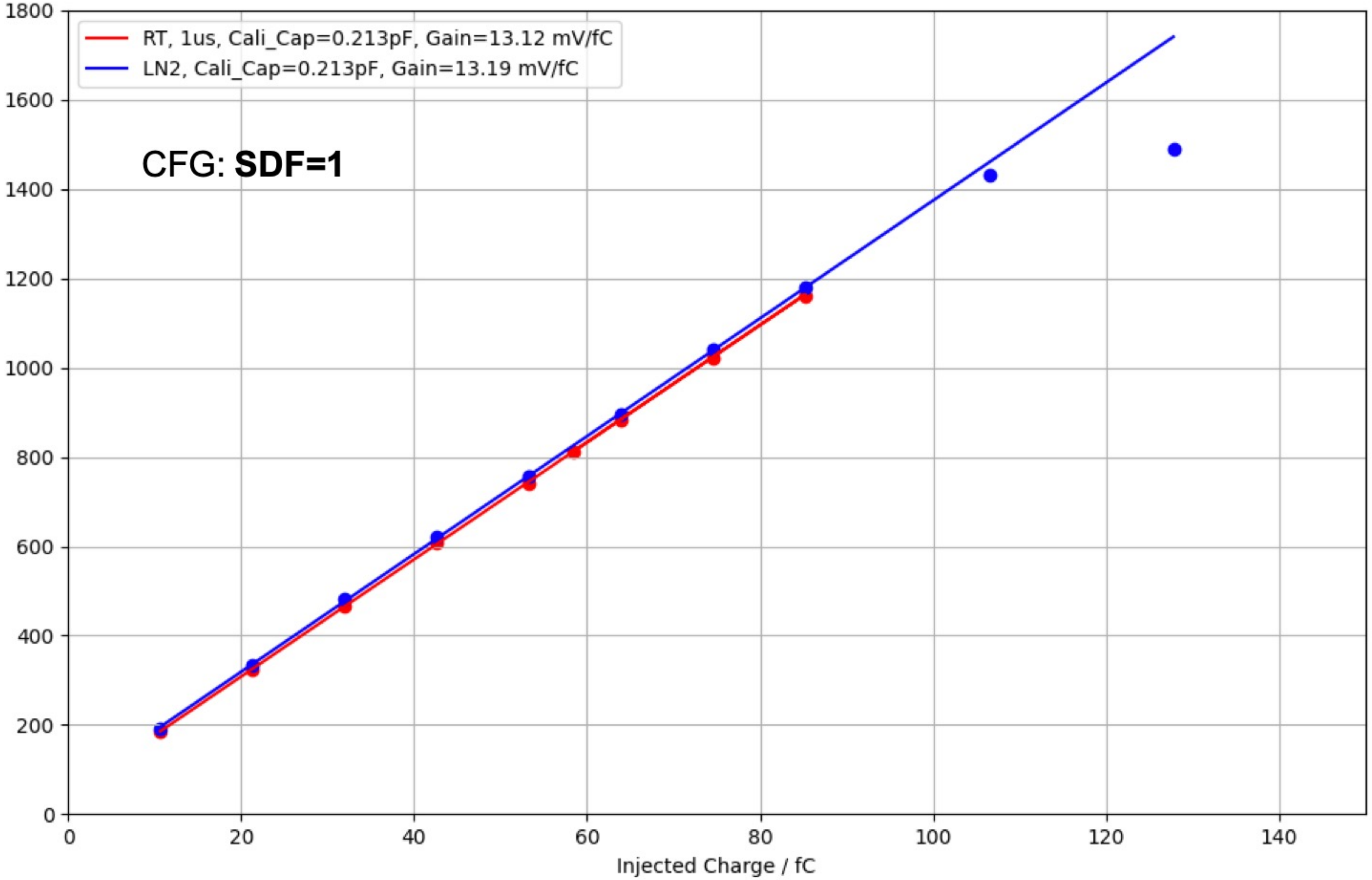
	Value	Mean	Min	Max	Std Dev
Rise Time	----.s	No valid edge			
Fall Time	18.95µs	18.94µ	18.93µ	18.95µ	10.82n
Amplitude	992mV	988m	984m	992m	4.38m
Peak-Peak	992mV	988m	984m	992m	4.38m
Mean	12.4mV	12.8m	12.4m	13.1m	224µ



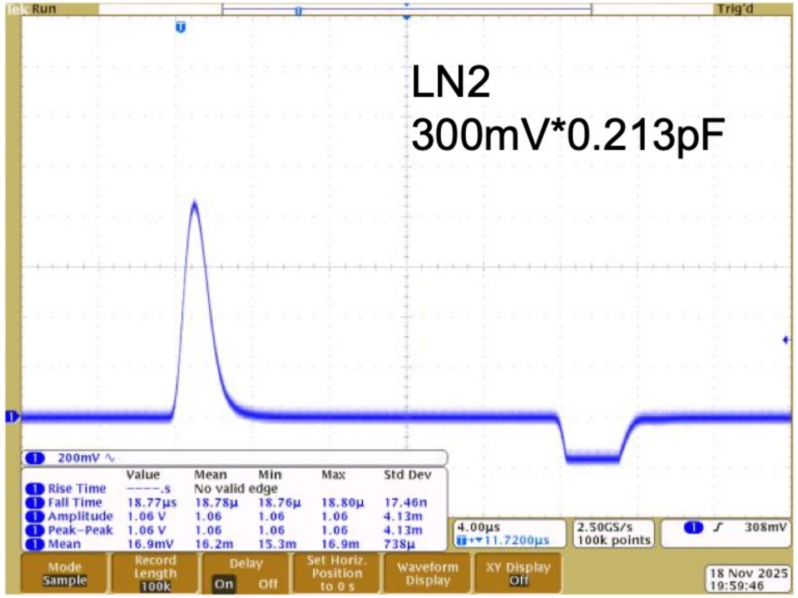
Injected charge = 50mV * 1.203pF

	Value	Mean	Min	Max	Std Dev
Rise Time	----.s	No valid edge			
Fall Time	18.92µs	18.95µ	18.92µ	18.97µ	16.61n
Amplitude	1.01 V	1.02	1.01	1.02	6.05m
Peak-Peak	1.01 V	1.02	1.01	1.02	6.05m
Mean	28.9mV	28.4m	27.5m	28.9m	443µ

Gain at RT and LN2 (1 µs peaking time)



CFG: **SDF=1**

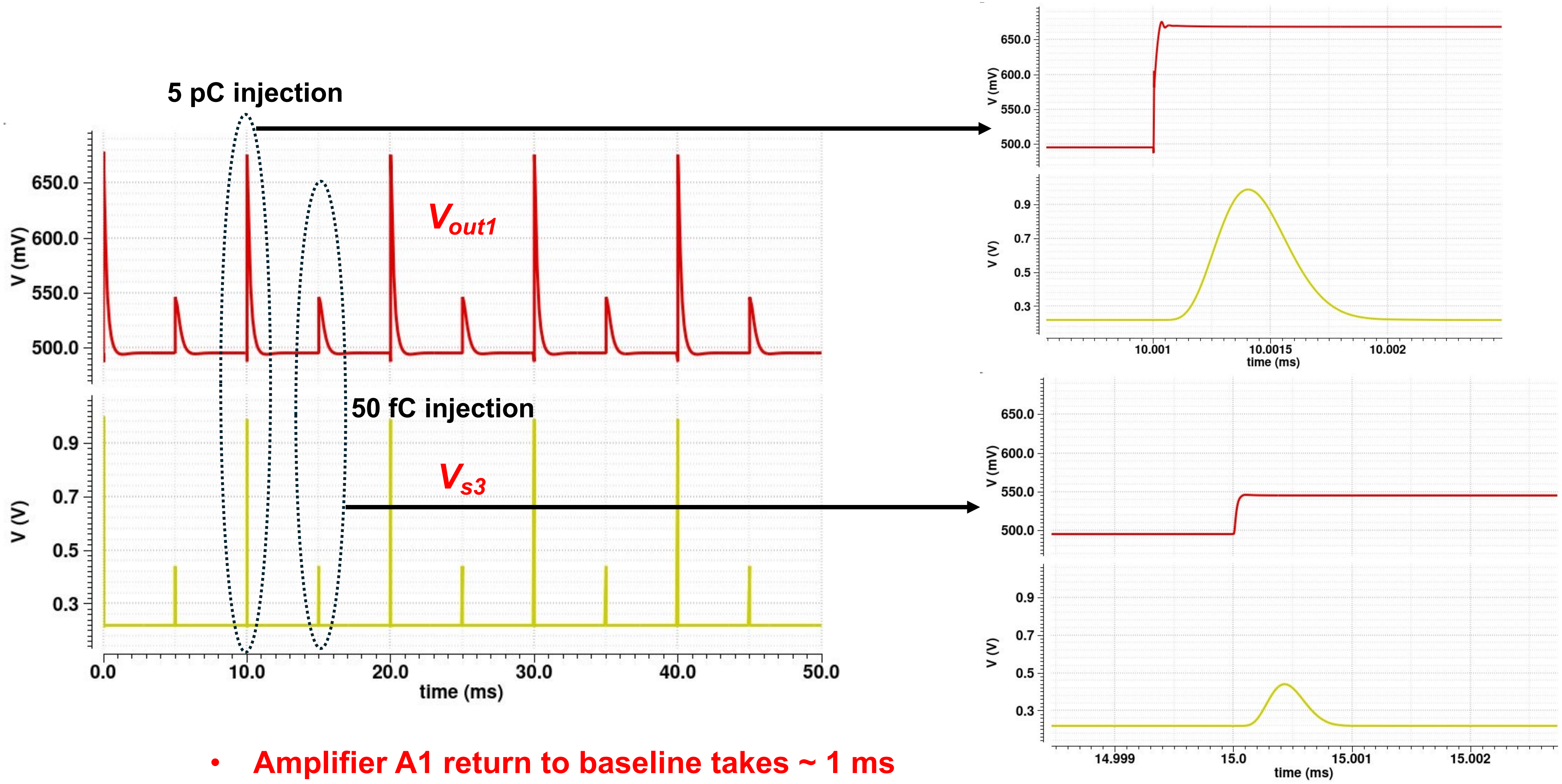


```
             Value      Mean          Min      Max      Std Dev
Rise Time    ----.s     No valid edge
Fall Time    18.77µs    18.78µ        18.76µ   18.80µ   17.46n
Amplitude    1.06 V     1.06          1.06     1.06     4.13m
Peak-Peak    1.06 V     1.06          1.06     1.06     4.13m
Mean         16.9mV     16.2m         15.3m    16.9m    738µ
```

LN2
300mV*0.213pF

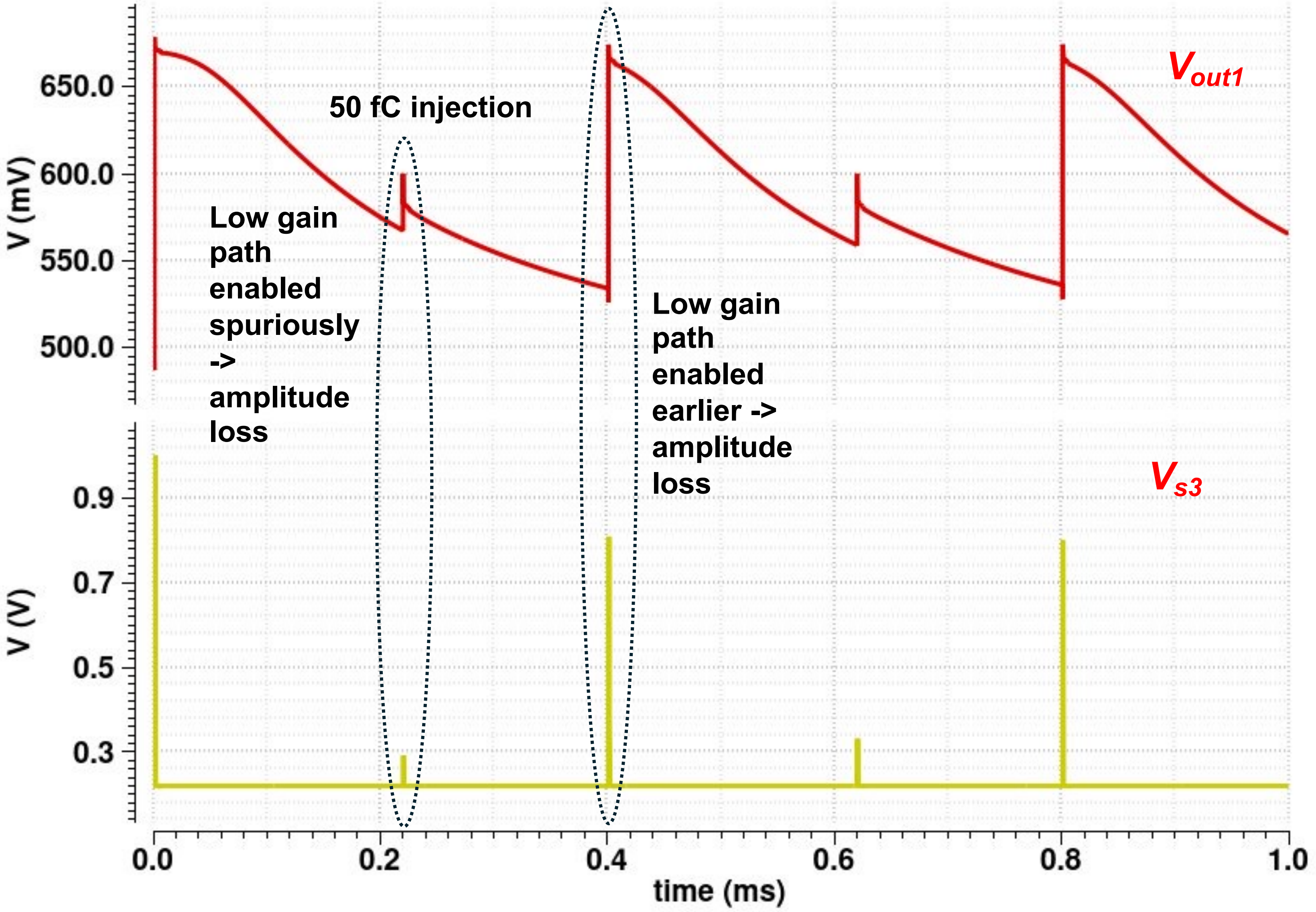
No significant gain change at LN2 compared to RT

CHARMS250V2B response for 200 Hz event rate



- **Amplifier A1 return to baseline takes ~ 1 ms**
- **For slow event rates, both CHARMS250V2A and CHARMS250V2B have the correct gain path enabled**

CHARMS250V2B response for 5 KHz event rate



5 pC injection

50 fC injection

Low gain path enabled spuriously -> amplitude loss

Low gain path enabled earlier -> amplitude loss

- However, for event rates in the range 1-100 KHz, slow return to baseline for amplifier A1, can have low gain path be enabled incorrectly
- We need a way to return to baseline faster, without adding noise